General Description

The MAX20326 is a dual-channel, precision, open-drain, communication-line accelerator. It provides the acceleration from a low-to-high transition necessary to allow faster data transfer in a highly capacitive, multidrop node system.

The MAX20326 is optimized for the I²C bus, as well as 1-Wire® bus, where a high-speed, open-drain operation is often required with a highly capacitive load.

This device is available in a 4-pin 0.5mm pitch 1.25mm x 1.25mm flip-chip QFN package and operates over the -40°C to +85°C extended temperature range.

Applications

- I²C
- MDIO
- 1-Wire Bus

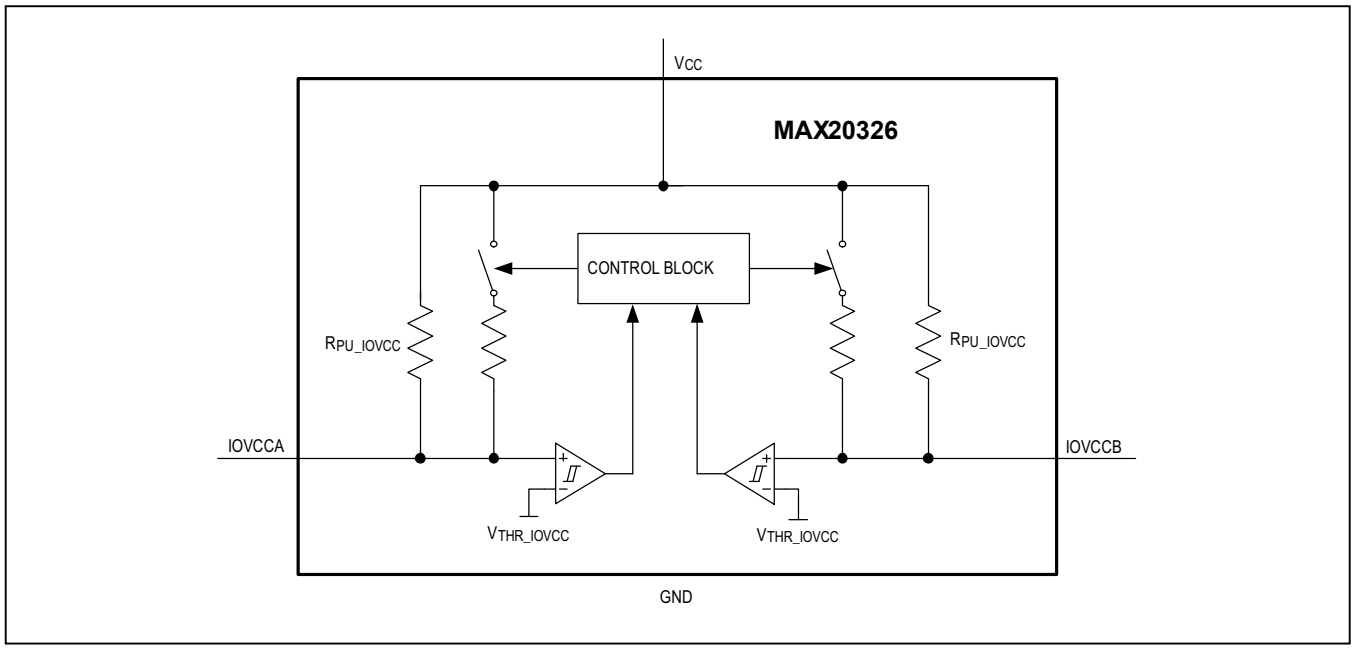
1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Reliable Communication
  - Wide Operating Input Voltage: +1.4V to +5.5V
  - Precision Accelerator Trigger Threshold: 0.5V ±50mV
  - Fast Charge Up to 1000pF Load
  - Low EMI: Controlled Acceleration Slope
- Space Saving
  - 4-Pin (0.5mm Pitch 1.25mm x 1.25mm Flip-Chip QFN)
  - Integrated Precision Pullup

***Ordering Information* appears at end of data sheet.**

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{CC} .....-0.5V to +6V
IOVCCA, IOVCCB .....-0.5V to V_{CC} + 0.5V
Continuous Current Into Any Terminal .....±100mA
Continuous Power Dissipation (T_A = +70°C)
FC QFN (derate 5.15mW/ºC above +70°C).....412mW

Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

4 FC QFN

PACKAGE CODE	F41A1F+1
Outline Number	21-100188
Land Pattern Number	90-100054
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	194°C/W
Junction to Case (θ_{JC})	84°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 1.4V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 1.8V, T_A = +25°C) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY OPERATION						
Operating Voltage	V_{CC}		1.4		5.5	V
Supply Current	I_{Q_VCC}	V_{IOVCCA} = V_{IOVCCB} = V_{CC}, V_{CC} ≤ 1.8V		11	18	µA
		V_{IOVCCA} = V_{IOVCCB} = V_{CC}, V_{CC} ≤ 5.5V			45	
Supply Shutdown Threshold	V_{TH_VCC}	V_{CC} rising		0.7	1.1	V
Supply Shutdown Threshold Hysteresis	$V_{TH\_HY\_VCC}$			40		mV
I/O LOGIC LEVELS						
Resistive Static Pullup	R_{PU_IOVCC}		1.98	2.2	2.42	kΩ
IOVCC_ Accelerator Rising Trigger Threshold	V_{THR_IOVCC}		0.45	0.5	0.55	V
IOVCC_ Accelerator Falling Threshold Hysteresis	V_{THH_IOVCC}			19		mV
Minimum IOVCC_ Low Pulse Duration	t_{LOW_REARM}		125			ns
ACCELERATOR						
Accelerator Pulse Duration	t_{ACC_ON}	V_{CC} ≥ 1.6V	120		200	ns
		V_{CC} ≥ 1.4V	120		250	
Accelerator Static Source Impedance (Note 3)	R_{ACC_STAT}	R_{LOAD} = 25Ω, accelerator driven with internal clock waveform		22		Ω
CAPACITANCE						
IOVCC_ Capacitance	C_{IOVCC}			13		pF
ESD PROTECTION						
Human Body Model		All pins		±2		kV

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design.

Note 2: After V_{CC} reaches V_{TH_VCC}, at least 3ms is needed in order to guarantee all min/max values.

Note 3: The impedance exhibited by the accelerator when driving a capacitive load varies and transiently differs from the static one.

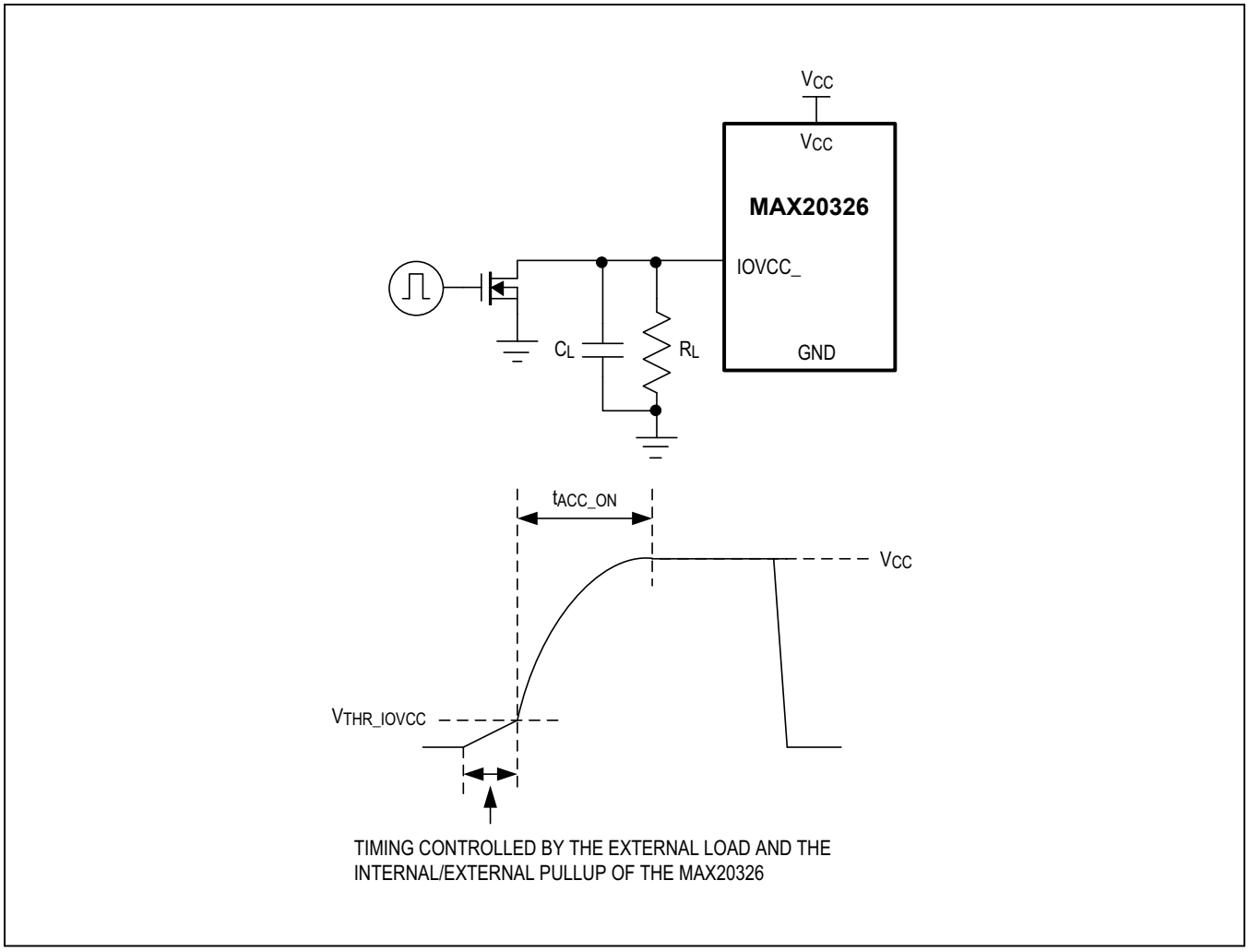
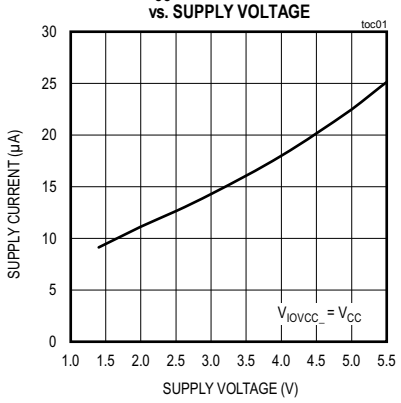


Figure 1. Timing Diagram

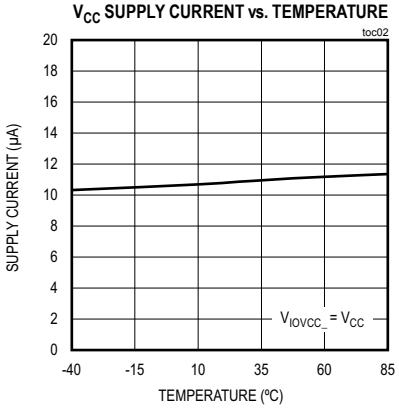
Typical Operating Characteristics

(V_{CC} = 1.8V, T_A = +25°C, unless otherwise noted.)

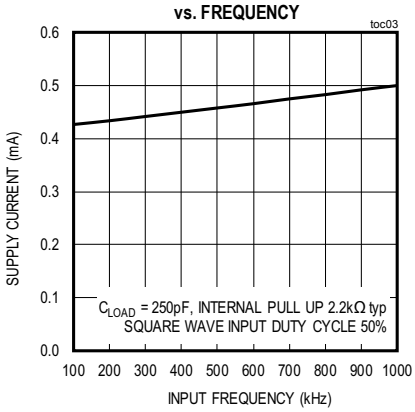
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



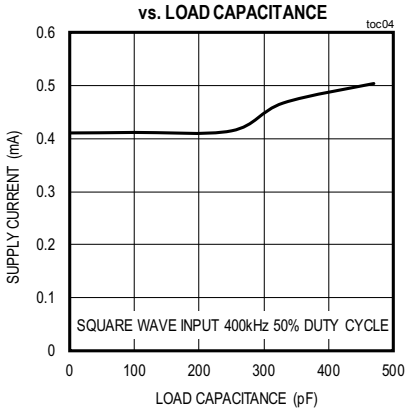
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



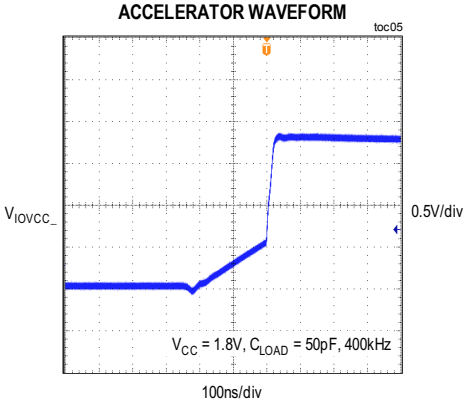
DYNAMIC SUPPLY CURRENT vs. FREQUENCY



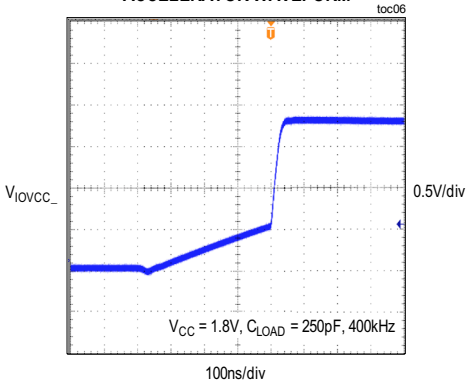
DYNAMIC SUPPLY CURRENT vs. LOAD CAPACITANCE



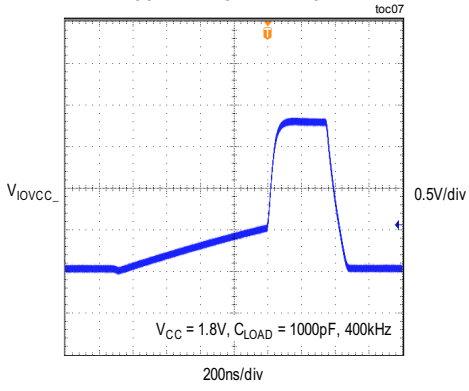
ACCELERATOR WAVEFORM



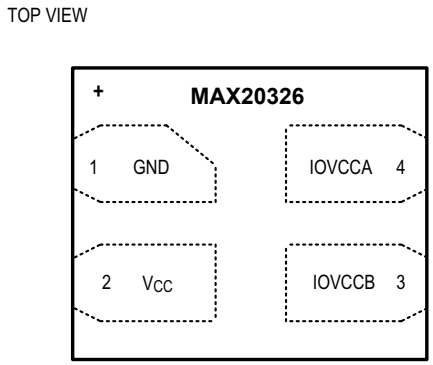
ACCELERATOR WAVEFORM



ACCELERATOR WAVEFORM



Pin Configuration



FLIP CHIP QF
(0.5mm PITCH 1.25mm x 1.25mm)

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	V_{CC}	V_{CC} Supply Input. Bypass V_{CC} with a ceramic capacitor 0.1µF or greater as close as possible to the device.
3	IOVCCB	Input/Output Channel B. Reference to V_{CC}.
4	IOVCCA	Input/Output Channel A. Reference to V_{CC}.

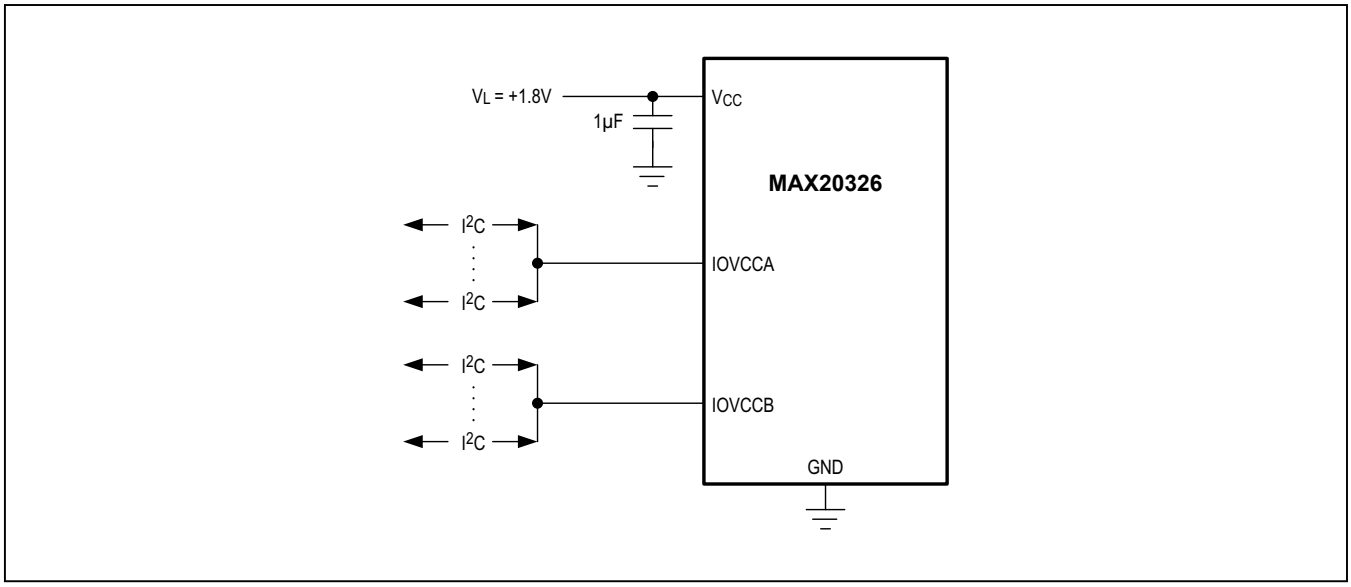
Detailed Description

The MAX20326 is a precision input/output accelerator. The MAX20326 provides the precision pullup resistance to the IOVCC_ line. When the IOVCC_ transitions from logic-low to logic-high, the slope-adjusted accelerator kicks in to optimize the turn-on time to cope with various load capacitance. The device is optimized for an open-drain and high-speed operation, such as I2C bus, MDIO bus, or 1-wire bus. The device features a precision ±10% accurate internal pullup on each IOVCC_ line.

High-Speed Operation

The MAX20326 assists the system with meeting the requirements of high-speed, open-drain operation. The maximum data rate is at least 1MHz for open-drain operation, with the total bus capacitance up to 1000pF. The maximum operating frequency is limited by the load capacitance, the internal/external pullup used on the IOVCC_ line, accelerator pulse duration, and the minimum IOVCC_ low-pulse duration.

Typical Application Circuit



Ordering Information

PART	INTERNAL PULLUP	TOP MARK	TEMP RANGE	PIN-PACKAGE
MAX20326EFS+T	2.2kΩ	AA	-40ºC TO +85ºC	4 FC QFN

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS