

# Power Line Communication with ModelGauge Fuel Gauge and Charger

**MAX20357**

## General Description

The MAX20357 is a Power Line Communication (PLC) slave with ModelGauge m5 EZ fuel gauge and charger. The MAX20357 and MAX20355 provide a complete system solution for charging and data transfer between a charging case and battery powered device over a single contact.

The PLC interface is capable of 100kpbs throughput while simultaneously providing 200mA of charging/system current per channel. A 4Mbaud half-duplex data only UART mode provides an easy and fast method for firmware updates, debugging interface, and factory modes.

The charger on slave device MAX20357 controls the output of the 3.3W buck-boost converter in the MAX20355 with dynamic voltage scaling (DVS).

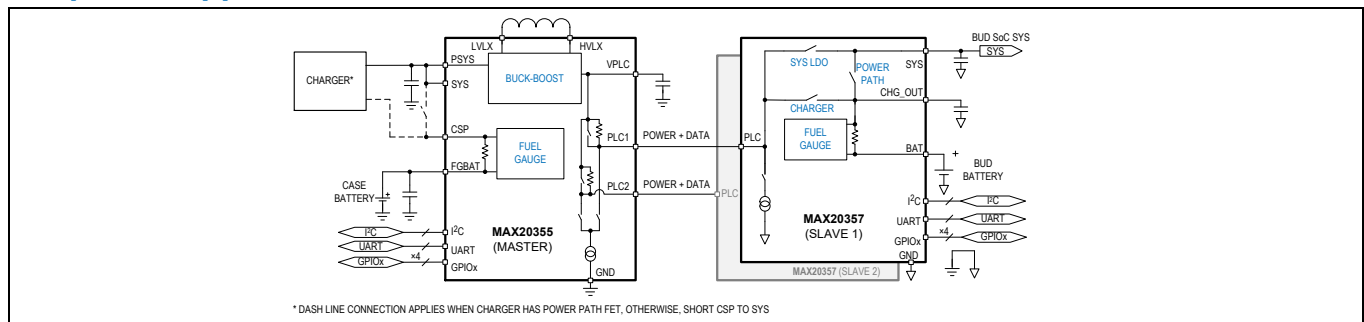
The MAX20357 integrates an ultra-low power fuel-gauge which implements the Maxim ModelGauge™ m5 algorithm. The IC monitors a single-cell battery pack and supports internal current sensing.

Additional features include comprehensive master device insertion and removal notifications, moisture detection, overcurrent protection, and 8kV contact rated ESD protection on the PLC output.

## Applications

- True Wireless Stereo Headphones
- Augmented Reality Glasses
- Wearable Devices

## Simplified Application Circuit



ModelGauge is a trademark of Maxim Integrated Products, Inc.

## Benefits and Features

- Power Line Communication (PLC) Interface
  - 100kpbs System Throughput
  - 167.7kpbs Bit Rate
  - 200mA Dual-Slave and 400mA Mono-Slave Output Charging Current
  - Automatic Earbud Insertion/Removal Detection
  - 4Mbaud, Half-Duplex, Data Only UART Mode
  - PLC Controllable GPIOs, Reset and Shipping Mode
- High-Efficiency Autonomous Charging System
  - 90% End-to-End Charging Efficiency from Master to Slave Battery
  - 400mA Integrated Linear Charger
  - Optimized Charging Efficiency by Automatic DVS Negotiation between Master and Slave
- Robust PLC Output Protection Features
  - Highly Flexible Moisture Detection Block
  - Input Current Limiting
  - 8kV Contact ESD Protection
- Small Solution Size
  - Low External Component Count
  - 2.69mm x 2.69mm 36-bump, 0.4mm pitch WLP Package

[Ordering information](#) appears at end of data sheet.

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### Absolute Maximum Ratings

|  |                |  |                 |
|--|----------------|--|-----------------|
| VDIG to GND.....   | -0.3V to +2V   | BAT to CHG_OUT (SYS power path) sense resistor current limit (10% utilization).....  | 350mA           |
| PLC, CHG_OUT, SYS, BAT, THM, UART_TX, UART_RX to GND.....  | -0.3V to +6V   | BAT to CHG_OUT (SYS power path) sense resistor current limit (Peak pulsed current, 250ms maximum pulse width, 10% maximum duty cycle, 1% utilization)..... | 450mA           |
| SDA, SCL, INT, EN, GPIO1, GPIO2, GPIO3, GPIO4 to GND - 0.3V to +6V                               |                | Any other pin (Continuous Current).....  | 20mA            |
| ALRT to GND.....   | -0.3V to +17V  | Continuous Power Dissipation (Multilayer Board) (T <sub>A</sub> = +70°C, derate 21.87mW/°C above +70°C.).....  | 1.75W           |
| CTB to GND.....  | -0.3V to +6V   | Operating Temperature Range.....   | -40°C to +85°C  |
| CTB to BAT.....  | +0.3V          | Junction Temperature.....  | +150°C          |
| GDIG to GND.....   | -0.3V to +0.3V | Storage Temperature Range.....   | -40°C to +150°C |
| PLC (Continuous Current).....  | 550mA          | Soldering Temperature (Reflow).....  | +260°C          |
| CHG_OUT (Continuous Current).....  | 450mA          |  |                 |
| BAT to CHG_OUT (SYS power path) sense resistor current limit (100%, Continuous utilization)..... | 250mA          |  |                 |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Information

#### WLP

|  |                           |
|--|---------------------------|
| Package Code                                 | W362J2+1                  |
| Outline Number                               | <a href="#">21-100525</a> |
| <b>Thermal Resistance, Four Layer Board:</b> |                           |
| Junction-to-Ambient (θ <sub>JA</sub> )       | 45.72°C/W                 |

### Electrical Characteristics

(T<sub>A</sub> = -40°C to +85°C, V<sub>BAT</sub> = 3.7V, C<sub>DIG</sub> = 1µF, C<sub>SYS</sub> = 1µF, C<sub>BAT</sub> = 1µF. All capacitance listed are effective values.)

| PARAMETER                               | SYMBOL                | CONDITIONS  | MIN | TYP | MAX | UNITS |
|---|-----------------------|---|-----|-----|-----|-------|
| <b>GLOBAL POWER SUPPLIES (PLC, BAT)</b> |                       |   |     |     |     |       |
| PLC Supply Current                      | I <sub>PLC</sub>      | Master found, Charger and SYS LDO enabled, I <sub>CHG</sub> = I <sub>SYS</sub> = 0mA, fuel gauge disabled, PLC communication not active |     | 380 | 650 | µA    |
| PLC Valid Supply Voltage                | V <sub>PLC_DET</sub>  |   |     | 3   |     | V     |
| PLC Detection Debounce Time             | t <sub>PLC_DEB</sub>  |   |     | 19  |     | ms    |
| BAT Input Start-Up Voltage              | V <sub>BAT_STUP</sub> |   | 2.9 |     |     | V     |
| BAT Input Voltage Range                 | V <sub>BAT_RNG</sub>  |   | 2.8 |     | 5.5 | V     |
| BAT Supply Current                      | I <sub>BAT1</sub>     | Master detection state, V <sub>BAT</sub> = 3.7V, Fuel Gauge disabled  |     | 2.8 | 30  | µA    |
|   | I <sub>BAT2</sub>     | Master found, V <sub>BAT</sub> = 4.2V, device in PLC IDLE State, averaged, Fuel Gauge disabled  |     | 11  | 40  |       |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER                               | SYMBOL                        | CONDITIONS                                       |                                  | MIN  | TYP  | MAX   | UNITS |
|---|-------------------------------|--|----------------------------------|------|------|-------|-------|
|   | I <sub>BAT3</sub>             | EN = 0, V <sub>BAT</sub> = 3.7V, device disabled | (OFF state)                      |      | 0.6  | 2     |       |
|   | I <sub>BAT4</sub>             | EN = 0, V <sub>BAT</sub> = 3.7V, device disabled | SEAL mode (SYSUVLO or SEAL mode) |      | 165  |       | nA    |
| <b>INTERNAL SUPPLIES, UVLO</b>          |                               |  |                                  |      |      |       |       |
| Internal V <sub>DIG</sub> Regulator     | V <sub>DIG</sub>              |  |                                  | 1.71 | 1.80 | 1.89  | V     |
| V <sub>DIG</sub> UVLO Threshold         | V <sub>DIG_UVLOR</sub>        | V <sub>DIG</sub> rising                          |                                  | 1.61 |      | 1.715 | V     |
|   | V <sub>DIG_UVLOF</sub>        | V <sub>DIG</sub> falling                         |                                  | 1.51 |      | 1.61  |       |
|   | V <sub>DIG_UVLO_H</sub>       |  |                                  |      | 100  |       | mV    |
| Internal V <sub>CCINT</sub> LDO         | V <sub>CCINT_LDO</sub>        | V <sub>PLC</sub> present                         |                                  |      | 2.8  |       | V     |
| V <sub>CCINT</sub> UVLO (POR) Threshold | V <sub>CCINT_UVLO_R</sub>     | Supply rising                                    |                                  | 2.25 | 2.47 | 2.72  | V     |
|   | V <sub>CCINT_UVLO_F</sub>     | Supply falling                                   |                                  | 2.2  | 2.42 | 2.67  |       |
|   | V <sub>CCINT_UVLO_H</sub>     |  |                                  |      | 50   |       | mV    |
| V <sub>OTP_OK</sub> UVLO Threshold      | V <sub>OTP_OK_UVL_OF</sub>    | Supply falling                                   |                                  | 2.6  | 2.75 | 2.9   | V     |
|   | V <sub>OTP_OK_UVL_OH</sub>    |  |                                  |      | 50   |       | mV    |
| V <sub>CCINT</sub> FG UVLO Threshold    | V <sub>CCINT_FGUV_LR</sub>    | Supply rising                                    |                                  | 2.47 | 2.55 | 2.63  | V     |
|   | V <sub>CCINT_FGUV_LF</sub>    | Supply falling                                   |                                  | 2.42 | 2.50 | 2.58  |       |
|   | V <sub>CCINT_FGUV_LH</sub>    |  |                                  |      | 50   |       | mV    |
| Battery Presence, FG BATUVLO Threshold  | V <sub>BP_FG_UVLO_R</sub>     | PLC valid present                                |                                  | 2.48 | 2.55 | 2.6   | V     |
|   | V <sub>BP_FG_UVLO_F</sub>     | PLC valid present                                |                                  | 2.45 | 2.5  | 2.55  |       |
|   | V <sub>BP_FG_UVLO_H</sub>     | PLC valid present                                |                                  |      | 50   |       | mV    |
| BAT Pulldown Resistance                 | RPD <sub>BAT</sub>            | BattPullDown = 0b1                               |                                  |      | 3    |       | kΩ    |
| SYS UVLO Threshold                      | V <sub>SYS_UVLO1F</sub>       | SYSUVLOThSel = 0b00                              | V <sub>SYS</sub> falling         | 2.60 | 2.70 | 2.80  | V     |
|   | V <sub>SYS_UVLO2F</sub>       | SYSUVLOThSel = 0b01                              | V <sub>SYS</sub> falling         | 2.80 | 2.90 | 3.00  |       |
|   | V <sub>SYS_UVLO3F</sub>       | SYSUVLOThSel = 0b10                              | V <sub>SYS</sub> falling         | 2.90 | 3.00 | 3.10  |       |
|   | V <sub>SYS_UVLO4F</sub>       | SYSUVLOThSel = 0b11                              | V <sub>SYS</sub> falling         | 3.10 | 3.20 | 3.30  |       |
|   | V <sub>SYS_UVLO_H</sub><br>YS |  |                                  |      | 50   |       | mV    |
| <b>POWER LINE COMMUNICATION (PLC)</b>   |                               |  |                                  |      |      |       |       |
| Data Throughput                         | TP <sub>DAT</sub>             | Maximum output current                           |                                  |      | >100 |       | kbps  |



(T<sub>A</sub> = -40°C to +85°C, V<sub>BAT</sub> = 3.7V, C<sub>DIG</sub> = 1μF, C<sub>SYS</sub> = 1μF, C<sub>BAT</sub> = 1μF. All capacitance listed are effective values.)

| PARAMETER                                     | SYMBOL                   | CONDITIONS  | MIN              | TYP                        | MAX                        | UNITS |                           |
|---|--------------------------|---|------------------|----------------------------|----------------------------|-------|---------------------------|
| <b>UART SWITCH</b>                            |                          |   |                  |                            |                            |       |                           |
| Analog Signal Range                           | V <sub>UART_RNG</sub>    |   | 0                |                            | V <sub>BAT</sub>           | V     |                           |
| On-Resistance                                 | R <sub>ONUART</sub>      |   |                  | 9                          | 15                         | Ω     |                           |
| On-Resistance Flatness                        | R <sub>FLATUART</sub>    |   |                  | 0.1                        | 0.3                        | Ω     |                           |
| Off-Leakage Current                           | I <sub>LUART(OFF)</sub>  |   |                  |                            | 1                          | μA    |                           |
| On-Leakage Current                            | I <sub>LUART(ON)</sub>   | V <sub>UART</sub> = 0V, V <sub>BAT</sub> = 3.7V                           |                  |                            | 1                          | μA    |                           |
|   |                          | V <sub>UART</sub> = 5.5V, V <sub>BAT</sub> = 5.5V                         |                  |                            | 10                         |       |                           |
| <b>UART TIMING</b>                            |                          |   |                  |                            |                            |       |                           |
| Enter UART Delay Time                         | t <sub>UART_DELAY</sub>  | From V <sub>PLC</sub> < 2.9V to UART Done                                 |                  | 20.2                       |                            | ms    |                           |
| Exit UART Idle Time                           | t <sub>UART_IDLE</sub>   | From UART idle to UART switch open  |                  | 0.5                        |                            | s     |                           |
| Exit UART Switch Open Time                    | t <sub>SW_OPN</sub>      | From UART switch open to UART exit  |                  | 0.6                        |                            | s     |                           |
| <b>WATCHDOG TIMING</b>                        |                          |   |                  |                            |                            |       |                           |
| Watchdog Timeout                              | t <sub>WD_TO</sub>       | wd_eoc_sel = 0b00   |                  | 4                          |                            | s     |                           |
|   |                          | wd_eoc_sel = 0b01   |                  | 8                          |                            |       |                           |
|   |                          | wd_eoc_sel = 0b10   |                  | 16                         |                            |       |                           |
|   |                          | wd_eoc_sel = 0b11   |                  | 32                         |                            |       |                           |
| <b>BATTERY CHARGER (PLC TO BAT)</b>           |                          |   |                  |                            |                            |       |                           |
| PLC to BAT Charge Current Reduction Threshold | V <sub>PLC_BAT_LIM</sub> | Measured as V <sub>PLC</sub> - V <sub>BAT</sub> , V <sub>BAT</sub> = 4.0V | PLC_DROP = 0b000 |                            | 50                         | mV    |                           |
|   |                          |   | PLC_DROP = 0b001 |                            | 75                         |       |                           |
|   |                          |   | PLC_DROP = 0b010 |                            | 100                        |       |                           |
|   |                          |   | PLC_DROP = 0b011 |                            | 125                        |       |                           |
|   |                          |   | PLC_DROP = 0b100 |                            | 150                        |       |                           |
|   |                          |   | PLC_DROP = 0b101 |                            | 175                        |       |                           |
|   |                          |   | PLC_DROP = 0b110 |                            | 200                        |       |                           |
|   |                          | Measured as V <sub>PLC</sub> - V <sub>BAT</sub> , V <sub>BAT</sub> = 4.0V | PLC_DROP = 0b111 |                            | 225                        |       |                           |
| Precharge Current                             | I <sub>PCHG</sub>        | IPChg = 0b00  |                  | 0.047 × I <sub>FCHG2</sub> |                            | mA    |                           |
|   |                          | IPChg = 0b01  |                  | 0.070 × I <sub>FCHG2</sub> | 0.094 × I <sub>FCHG2</sub> |       | 0.12 × I <sub>FCHG2</sub> |
|   |                          | IPChg = 0b10  |                  | 0.20 × I <sub>FCHG2</sub>  |                            |       |                           |
|   |                          | IPChg = 0b11  |                  | 0.30 × I <sub>FCHG2</sub>  |                            |       |                           |
| Precharge Threshold                           | V <sub>BAT_PCHG</sub>    | V <sub>BAT</sub> rising   | VPChg = 0b000    |                            | 2.7                        | V     |                           |
|   |                          |   | VPChg = 0b001    |                            | 2.8                        |       |                           |

(T<sub>A</sub> = -40°C to +85°C, V<sub>BAT</sub> = 3.7V, C<sub>DIG</sub> = 1μF, C<sub>SYS</sub> = 1μF, C<sub>BAT</sub> = 1μF. All capacitance listed are effective values.)

| PARAMETER                        | SYMBOL                    | CONDITIONS              | MIN                  | TYP  | MAX | UNITS |
|----------------------------------|---------------------------|-------------------------|----------------------|------|-----|-------|
|                                  |                           | VPChg = 0b010           |                      | 2.9  |     |       |
|                                  |                           | VPChg = 0b011           |                      | 3.0  |     |       |
|                                  |                           | VPChg = 0b100           |                      | 3.1  |     |       |
|                                  |                           | VPChg = 0b101           |                      | 3.2  |     |       |
|                                  |                           | VPChg = 0b110           |                      | 3.3  |     |       |
|                                  |                           | VPChg = 0b111           |                      | 3.4  |     |       |
| Precharge Threshold Hysteresis   | V <sub>BAT_PCHG_H</sub>   |                         |                      | 120  |     | mV    |
| Step Charge Threshold            | V <sub>BAT_STPCHG</sub>   | V <sub>BAT</sub> rising | ChgStepRise = 0b0000 | 3.80 |     | V     |
|                                  |                           |                         | ChgStepRise = 0b0001 | 3.85 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0010 | 3.90 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0011 | 3.95 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0100 | 4.00 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0101 | 4.05 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0110 | 4.10 |     |       |
|                                  |                           |                         | ChgStepRise = 0b0111 | 4.15 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1000 | 4.20 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1001 | 4.25 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1010 | 4.30 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1011 | 4.35 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1100 | 4.40 |     |       |
|                                  |                           |                         | ChgStepRise = 0b1101 | 4.45 |     |       |
| ChgStepRise = 0b1110             | 4.50                      |                         |                      |      |     |       |
| ChgStepRise = 0b1111             | 4.55                      |                         |                      |      |     |       |
| Step Charge Threshold Hysteresis | V <sub>BAT_STPCHG_H</sub> | ChgStepHyst = 0b000     |                      | 100  |     | mV    |
|                                  |                           | ChgStepHyst = 0b001     |                      | 200  |     |       |
|                                  |                           | ChgStepHyst = 0b010     |                      | 300  |     |       |
|                                  |                           | ChgStepHyst = 0b011     |                      | 400  |     |       |
|                                  |                           | ChgStepHyst = 0b100     |                      | 500  |     |       |
|                                  |                           | ChgStepHyst = 0b101     |                      | 600  |     |       |
|                                  |                           | ChgStepHyst = 0b110     |                      | 600  |     |       |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER                  | SYMBOL                 | CONDITIONS                                    | MIN             | TYP                           | MAX    | UNITS |
|----------------------------|------------------------|---|-----------------|-------------------------------|--------|-------|
|                            |                        | ChgStepHyst = 0b111                           |                 | 600                           |        |       |
| Fast-Charge Current Zone 1 | I <sub>FCHG1</sub>     | CC1IFChg = 0b0000000 to 0b0111100             |                 | 5 to 65<br>step 1             |        | mA    |
|                            |                        | CC1IFChg = 0b0111101 to 0b1001111             |                 | 70 to<br>160 step<br>5        |        |       |
|                            |                        | CC1IFChg = 0b1010000 to 0b1010011             |                 | 170 to<br>200 step<br>10      |        |       |
|                            |                        | CC1IFChg = 0b1010100 to 0b1111111             |                 | 200                           |        |       |
| Fast-Charge Current Zone 2 | I <sub>FCHG2</sub>     | CC2IFChg = 0b0000000 to 0b0111100             |                 | 5 to 65<br>step 1             |        | mA    |
| Fast-Charge Current Zone 2 | I <sub>FCHG2</sub>     | CC2IFChg = 0b0111101 to 0b1001111             |                 | 70 to<br>160 step<br>5        |        | mA    |
|                            |                        | CC2IFChg = 0b1010000 to 0b1010011             |                 | 170 to<br>200 step<br>10      |        |       |
|                            |                        | CC2IFChg = 0b1010100 to 0b1111111             |                 | 200                           |        |       |
| Battery-Regulation Voltage | V <sub>BATREG</sub>    | BatReg = 0b001111 to 0b110111                 |                 | 4.05 to<br>4.6 step<br>10m    |        | V     |
|                            |                        | BatReg = 0b111000 to 0b111111                 |                 | 4.6                           |        |       |
| Battery-Regulation Voltage | V <sub>BATREG</sub>    | BatReg = 0b001111, $T_A = 25^{\circ}\text{C}$ | 4.1958          | 4.200                         | 4.2042 | V     |
|                            |                        | BatReg = 0b001111                             | 4.179           | 4.200                         | 4.221  |       |
| Battery Recharge Threshold | V <sub>BAT_RECHG</sub> | Charger recharge threshold to BatReg          | BatReChg = 0b00 |                               | -50    | mV    |
|                            |                        |   | BatReChg = 0b01 |                               | -100   |       |
|                            |                        |   | BatReChg = 0b10 |                               | -150   |       |
|                            |                        |   | BatReChg = 0b11 |                               | -200   |       |
| Precharge Timer            | t <sub>PCHG</sub>      | PChgTmr = 0b00                                |                 | 30                            |        | min   |
|                            |                        | PChgTmr = 0b01                                |                 | 60                            |        |       |
|                            |                        | PChgTmr = 0b10                                |                 | 120                           |        |       |
|                            |                        | PChgTmr = 0b11                                |                 | 240                           |        |       |
| Fast Charge CC1 Timer      | t <sub>FCHG1</sub>     | CC1FChgTmr = 0b00                             |                 | 30                            |        | min   |
|                            |                        | CC1FChgTmr = 0b01                             |                 | 60                            |        |       |
|                            |                        | CC1FChgTmr = 0b10                             |                 | 120                           |        |       |
|                            |                        | CC1FChgTmr = 0b11                             |                 | 240                           |        |       |
| Charger Safety Timer       | t <sub>CHG</sub>       | ChgTmr = 0b00                                 |                 | 75                            |        | min   |
| Charger Safety Timer       | t <sub>CHG</sub>       | ChgTmr = 0b01                                 |                 | 150                           |        | min   |
|                            |                        | ChgTmr = 0b10                                 |                 | 300                           |        |       |
|                            |                        | ChgTmr = 0b11                                 |                 | 600                           |        |       |
| Charge Done Qualification  | I <sub>CHG_DONE</sub>  | IChgDone = 0b00                               |                 | 0.023 ×<br>I <sub>FCHG2</sub> |        | mA    |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER   | SYMBOL                     | CONDITIONS   |                                   | MIN                             | TYP                             | MAX                            | UNITS                     |
|---|----------------------------|--|-----------------------------------|---------------------------------|---------------------------------|--------------------------------|---------------------------|
|   |                            | IChgDone = 0b01  |                                   |                                 | $0.051 \times I_{\text{FCHG2}}$ |                                |                           |
|   |                            | IChgDone = 0b10  |                                   | $0.091 \times I_{\text{FCHG2}}$ | $0.10 \times I_{\text{FCHG2}}$  | $0.11 \times I_{\text{FCHG2}}$ |                           |
|   |                            | IChgDone = 0b11  |                                   |                                 | $0.20 \times I_{\text{FCHG2}}$  |                                |                           |
| Maximum Maintain Charge Time                            | $t_{\text{MTCHG}}$         | MtChgTmr = 0b00  |                                   |                                 | 0                               |                                | min                       |
|   |                            | MtChgTmr = 0b01  |                                   |                                 | 15                              |                                |                           |
|   |                            | MtChgTmr = 0b10  |                                   |                                 | 30                              |                                |                           |
|   |                            | MtChgTmr = 0b11  |                                   |                                 | 60                              |                                |                           |
| Timer Accuracy  | $t_{\text{CHG\_ACC}}$      |  |                                   | -10                             |                                 | +10                            | %                         |
| Fast-Charge Timer Extend Current Threshold              | $I_{\text{FCHG\_TEXT}}$    | See <a href="#">Figure 14</a>  |                                   |                                 | 50                              |                                | %<br>$I_{\text{FCHG1,2}}$ |
| Fast-Charge Timer Suspend Current Threshold             | $I_{\text{FCHG\_TSUS}}$    | See <a href="#">Figure 14</a>  |                                   |                                 | 20                              |                                | %<br>$I_{\text{FCHG1,2}}$ |
| Battery Regulation Voltage Reduction Due to Temperature | $V_{\text{BAT\_REG\_JTA}}$ | ChgCool/Room/WarmBatReg = 0b00   |                                   |                                 | $V_{\text{BAT\_REG}} - 0.15$    |                                | V                         |
|   |                            | ChgCool/Room/WarmBatReg = 0b01   |                                   |                                 | $V_{\text{BAT\_REG}} - 0.1$     |                                |                           |
|   |                            | ChgCool/Room/WarmBatReg = 0b10   |                                   |                                 | $V_{\text{BAT\_REG}} - 0.05$    |                                |                           |
|   |                            | ChgCool/Room/WarmBatReg = 0b11   |                                   |                                 | $V_{\text{BAT\_REG}}$           |                                |                           |
| Fast-Charge Current Reduction Due to Temperature        | $I_{\text{FCHG\_JTA}}$     | CCxIFChg = CC1IFChg or CC2IFChg based on Step Charge comparator status | ChgCool/Room/WarmCCxIFChg = 0b000 |                                 | 20                              |                                | %<br>$I_{\text{FCHG1,2}}$ |
|   |                            |  | ChgCool/Room/WarmCCxIFChg = 0b001 |                                 | 30                              |                                |                           |
|   |                            |  | ChgCool/Room/WarmCCxIFChg = 0b010 |                                 | 40                              |                                |                           |
|   |                            | CCxIFChg = CC1IFChg or CC2IFChg based on Step Charge comparator status | ChgCool/Room/WarmCCxIFChg = 0b011 |                                 | 50                              |                                |                           |
|   |                            |  | ChgCool/Room/WarmCCxIFChg = 0b100 |                                 | 60                              |                                |                           |
|   |                            |  | ChgCool/Room/WarmCCxIFChg = 0b101 |                                 | 70                              |                                |                           |
|   |                            |  | ChgCool/Room/WarmCCxIFChg = 0b110 |                                 | 80                              |                                |                           |

(T<sub>A</sub> = -40°C to +85°C, V<sub>BAT</sub> = 3.7V, C<sub>DIG</sub> = 1μF, C<sub>SYS</sub> = 1μF, C<sub>BAT</sub> = 1μF. All capacitance listed are effective values.)

| PARAMETER                              | SYMBOL                   | CONDITIONS                                      |                                     | MIN                      | TYP | MAX   | UNITS |
|--|--------------------------|---|-------------------------------------|--------------------------|-----|-------|-------|
|  |                          |   | ChgCool/Room/WarmCCxIFChg = 0b111   |                          | 100 |       |       |
| Reverse Protection Threshold           | V <sub>CHG_REV_TH</sub>  | V <sub>BAT</sub> raising over V <sub>PLC</sub>  | V <sub>BAT</sub> - V <sub>PLC</sub> |                          | 25  |       | mV    |
|  | V <sub>CHG_REV_HYS</sub> | V <sub>BAT</sub> raising over V <sub>PLC</sub>  | V <sub>BAT</sub> - V <sub>PLC</sub> |                          | 50  |       |       |
| <b>LDO (PLC TO SYS)</b>                |                          |   |                                     |                          |     |       |       |
| PLC to SYS Current Reduction Threshold | V <sub>PLC_SYS_LIM</sub> | Measured as V <sub>PLC</sub> - V <sub>SYS</sub> | PLC_DROP = 0b000<br>SysMin = 0b0000 |                          | 50  |       | mV    |
|  |                          |   | PLC_DROP = 0b001<br>SysMin = 0b0000 |                          | 75  |       |       |
|  |                          |   | PLC_DROP = 0b010<br>SysMin = 0b0000 |                          | 100 |       |       |
|  |                          |   | PLC_DROP = 0b011<br>SysMin = 0b0000 |                          | 125 |       |       |
|  |                          | Measured as V <sub>PLC</sub> - V <sub>SYS</sub> | PLC_DROP = 0b100<br>SysMin = 0b0000 |                          | 150 |       |       |
|  |                          |   | PLC_DROP = 0b101<br>SysMin = 0b0000 |                          | 175 |       |       |
|  |                          |   | PLC_DROP = 0b110<br>SysMin = 0b0000 |                          | 200 |       |       |
|  |                          |   | PLC_DROP = 0b111<br>SysMin = 0b0000 |                          | 225 |       |       |
| LDO Output Current Limit               | I <sub>LDO_LIM</sub>     |   |                                     | 3.125 to 200, step 3.125 |     | mA    |       |
| Minimum SYS Voltage                    | V <sub>SYS_MIN</sub>     | V <sub>BAT</sub> = 2.8V                         | SysMin = 0b0000                     | 2.97                     | 3.0 | 3.03  | V     |
|  |                          |   | SysMin = 0b0001                     |                          | 3.1 |       |       |
|  |                          |   | SysMin = 0b0010                     |                          | 3.2 |       |       |
|  |                          |   | SysMin = 0b0011                     |                          | 3.3 |       |       |
|  |                          |   | SysMin = 0b0100                     | 3.366                    | 3.4 | 3.434 |       |
|  |                          |   | SysMin = 0101                       |                          | 3.5 |       |       |
|  |                          |   | SysMin = 0b0110                     |                          | 3.6 |       |       |
|  |                          |   | SysMin = 0b0111                     |                          | 3.7 |       |       |
|  |                          |   | SysMin = 0b1000                     |                          | 3.8 |       |       |
|  |                          |   | SysMin = 0b1001                     |                          | 3.9 |       |       |
|  |                          |   | SysMin = 0b1010                     |                          | 4.0 |       |       |
| SysMin = 0b1011                        |                          | 4.1   |                                     |                          |     |       |       |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER                               | SYMBOL                       | CONDITIONS   |                                   | MIN   | TYP                       | MAX   | UNITS               |
|---|------------------------------|--|-----------------------------------|-------|---------------------------|-------|---------------------|
|   |                              |  | SysMin = 0b1100                   |       | 4.2                       |       |                     |
|   |                              |  | SysMin = 0b1101                   |       | 4.3                       |       |                     |
|   |                              |  | SysMin = 0b1110                   |       | 4.4                       |       |                     |
|   |                              |  | SysMin = 0b1111                   |       | 4.5                       |       |                     |
| SYS Regulation Voltage                  | $V_{\text{SYS\_REG}}$        | $V_{\text{BAT}} = 3\text{V}$   | SysMin = 0b0000                   |       | $V_{\text{BAT}}$          |       | V                   |
| Reverse Protection Threshold            | $V_{\text{LDO\_REV\_TH}}$    | $V_{\text{SYS}}$ raising over $V_{\text{PLC}}$   | $V_{\text{SYS}} - V_{\text{PLC}}$ |       | 25                        |       | mV                  |
| Reverse Protection Threshold Hysteresis | $V_{\text{LDO\_REV\_HY\_S}}$ | $V_{\text{SYS}} - V_{\text{PLC}}$  |                                   |       | 50                        |       | mV                  |
| <b>POWER PATH (BAT TO SYS)</b>          |                              |  |                                   |       |                           |       |                     |
| BAT to SYS On Resistance                | $R_{\text{PP}}$              | $V_{\text{BAT}} = 4.35\text{V}$ , $I_{\text{SYS}} = 200\text{mA}$ , SYS LDO disabled   |                                   |       | 200                       | 290   | m $\Omega$          |
| BAT to SYS On Threshold                 | $V_{\text{BAT\_SYS\_ON}}$    | LDO enabled, $V_{\text{BAT}} = 4.35\text{V}$ , $V_{\text{PLC}} = 3.5\text{V}$ , $I_{\text{SYS}} = 10\text{mA}$ , measured as $V_{\text{BAT}} - V_{\text{SYS}}$ | PP_drp = 0b000                    | 14    | 25                        | 36    | mV                  |
|   |                              |  | PP_drp = 0b001                    | 25    | 37.5                      | 50    |                     |
|   |                              | LDO enabled, $V_{\text{BAT}} = 4.35\text{V}$ , $V_{\text{PLC}} = 3.5\text{V}$ , $I_{\text{SYS}} = 10\text{mA}$ , measured as $V_{\text{BAT}} - V_{\text{SYS}}$ | PP_drp = 0b010                    | 37.5  | 50                        | 62.5  |                     |
|   |                              | LDO enabled, $V_{\text{BAT}} = 4.35\text{V}$ , $V_{\text{PLC}} = 3.5\text{V}$ , $I_{\text{SYS}} = 10\text{mA}$ , measured as $V_{\text{BAT}} - V_{\text{SYS}}$ | PP_drp = 0b011                    | 50    | 62.5                      | 75    |                     |
|   |                              |  | PP_drp = 0b100                    | 62    | 75                        | 88    |                     |
|   |                              |  | PP_drp = 0b101                    | 74.5  | 87.5                      | 100.5 |                     |
|   |                              |  | PP_drp = 0b110                    | 86.5  | 100                       | 113.5 |                     |
| PP_drp = 0b111                          | 98.5                         | 112.5  | 126.5                             |       |                           |       |                     |
| <b>PLC INPUT CURRENT LIMITER</b>        |                              |  |                                   |       |                           |       |                     |
| Total PLC Current Limit                 | $I_{\text{PLC\_LIM}}$        | $I_{\text{chg\_x2}} = 0$   |                                   |       | 3.333 to 203.3 step 3.125 |       | mA                  |
|   |                              | $I_{\text{chg\_x2}} = 1$   |                                   |       | 6.666 to 406.6 step 6.25  |       |                     |
| <b>THERMISTOR MONITOR</b>               |                              |  |                                   |       |                           |       |                     |
| THM Hot Threshold                       | $V_{\text{THM\_HOT1}}$       | $V_{\text{THM}}$ falling ( $70^{\circ}\text{C}$ )  |                                   | 16.36 | 18.36                     | 20.36 | % $V_{\text{VDIG}}$ |
|   | $V_{\text{THM\_HOT2}}$       | $V_{\text{THM}}$ falling ( $65^{\circ}\text{C}$ )  |                                   | 18.70 | 20.70                     | 22.70 |                     |
|   | $V_{\text{THM\_HOT3}}$       | $V_{\text{THM}}$ falling ( $60^{\circ}\text{C}$ )  |                                   | 21.44 | 23.44                     | 25.44 |                     |
|   | $V_{\text{THM\_HOT4}}$       | $V_{\text{THM}}$ falling ( $55^{\circ}\text{C}$ )  |                                   | 24.17 | 26.17                     | 28.17 |                     |
|   | $V_{\text{THM\_HOT5}}$       | $V_{\text{THM}}$ falling ( $50^{\circ}\text{C}$ )  |                                   | 27.30 | 29.30                     | 31.30 |                     |
|   | $V_{\text{THM\_HOT6}}$       | $V_{\text{THM}}$ falling ( $45^{\circ}\text{C}$ )  |                                   | 30.81 | 32.81                     | 34.81 |                     |
|   | $V_{\text{THM\_HOT7}}$       | $V_{\text{THM}}$ falling ( $40^{\circ}\text{C}$ )  |                                   | 34.72 | 36.72                     | 38.72 |                     |

(T<sub>A</sub> = -40°C to +85°C, V<sub>BAT</sub> = 3.7V, C<sub>DIG</sub> = 1μF, C<sub>SYS</sub> = 1μF, C<sub>BAT</sub> = 1μF. All capacitance listed are effective values.)

| PARAMETER                   | SYMBOL                   | CONDITIONS                      |                        | MIN   | TYP   | MAX   | UNITS              |
|-----------------------------|--------------------------|---------------------------------|------------------------|-------|-------|-------|--------------------|
|                             | V <sub>THM_HOT8</sub>    | V <sub>THM</sub> falling (35°C) |                        | 39.02 | 41.02 | 43.02 |                    |
| THM Warm Threshold          | V <sub>THM_WARM1</sub>   | V <sub>THM</sub> falling (55°C) |                        | 24.17 | 26.17 | 28.17 | %V <sub>VDIG</sub> |
|                             | V <sub>THM_WARM2</sub>   | V <sub>THM</sub> falling (50°C) |                        | 27.30 | 29.30 | 31.30 |                    |
|                             | V <sub>THM_WARM3</sub>   | V <sub>THM</sub> falling (45°C) |                        | 30.81 | 32.81 | 34.81 |                    |
|                             | V <sub>THM_WARM4</sub>   | V <sub>THM</sub> falling (40°C) |                        | 34.72 | 36.72 | 38.72 |                    |
|                             | V <sub>THM_WARM5</sub>   | V <sub>THM</sub> falling (35°C) |                        | 39.02 | 41.02 | 43.02 |                    |
|                             | V <sub>THM_WARM6</sub>   | V <sub>THM</sub> falling (30°C) |                        | 43.31 | 45.31 | 47.31 |                    |
|                             | V <sub>THM_WARM7</sub>   | V <sub>THM</sub> falling (25°C) |                        | 48.00 | 50.00 | 52.00 |                    |
|                             | V <sub>THM_WARM8</sub>   | V <sub>THM</sub> falling (20°C) |                        | 52.69 | 54.69 | 56.69 |                    |
| THM Cool Threshold          | V <sub>THM_COOL1</sub>   | V <sub>THM</sub> rising (25°C)  |                        | 48.00 | 50.00 | 52.00 | %V <sub>VDIG</sub> |
|                             | V <sub>THM_COOL2</sub>   | V <sub>THM</sub> rising (20°C)  |                        | 52.69 | 54.69 | 56.69 |                    |
|                             | V <sub>THM_COOL3</sub>   | V <sub>THM</sub> rising (15°C)  |                        | 57.77 | 59.77 | 61.77 |                    |
|                             | V <sub>THM_COOL4</sub>   | V <sub>THM</sub> rising (10°C)  |                        | 62.45 | 64.45 | 66.45 |                    |
|                             | V <sub>THM_COOL5</sub>   | V <sub>THM</sub> rising (25°C)  |                        | 67.14 | 69.14 | 71.14 |                    |
|                             | V <sub>THM_COOL6</sub>   | V <sub>THM</sub> rising (20°C)  |                        | 71.83 | 73.83 | 75.83 |                    |
|                             | V <sub>THM_COOL7</sub>   | V <sub>THM</sub> rising (15°C)  |                        | 76.13 | 78.13 | 80.13 |                    |
|                             | V <sub>THM_COOL8</sub>   | V <sub>THM</sub> rising (10°C)  |                        | 80.03 | 82.03 | 84.03 |                    |
| THM Cold Threshold          | V <sub>THM_COLD1</sub>   | V <sub>THM</sub> rising (15°C)  |                        | 57.77 | 59.77 | 61.77 | %V <sub>VDIG</sub> |
|                             | V <sub>THM_COLD2</sub>   | V <sub>THM</sub> rising (10°C)  |                        | 62.45 | 64.45 | 66.45 |                    |
|                             | V <sub>THM_COLD3</sub>   | V <sub>THM</sub> rising (5°C)   |                        | 67.14 | 69.14 | 71.14 |                    |
|                             | V <sub>THM_COLD4</sub>   | V <sub>THM</sub> rising (0°C)   |                        | 71.83 | 73.83 | 75.83 |                    |
|                             | V <sub>THM_COLD5</sub>   | V <sub>THM</sub> rising (-5°C)  |                        | 76.13 | 78.13 | 80.13 |                    |
|                             | V <sub>THM_COLD6</sub>   | V <sub>THM</sub> rising (-10°C) |                        | 80.03 | 82.03 | 84.03 |                    |
|                             | V <sub>THM_COLD7</sub>   | V <sub>THM</sub> rising (-15°C) |                        | 83.16 | 85.16 | 87.16 |                    |
|                             | V <sub>THM_COLD8</sub>   | V <sub>THM</sub> rising (-20°C) |                        | 86.28 | 88.28 | 90.28 |                    |
| THM Disable Threshold       | V <sub>THM_DIS</sub>     | V <sub>THM</sub> rising         |                        | 91.75 | 93.75 | 95.75 | %V <sub>VDIG</sub> |
| THM Threshold Hysteresis    | V <sub>THM_H</sub>       |                                 |                        |       | 60    |       | mV                 |
| THM Input Leakage           | I <sub>THM_LK</sub>      | V <sub>THM</sub> = 0V to 5.5V   | TPU switch open        | -1    |       | +1    | μA                 |
| <b>MOISTURE DETECTION</b>   |                          |                                 |                        |       |       |       |                    |
| Impedance Measurement Range | R <sub>MOIST_RANGE</sub> |                                 |                        | 6     |       | 1400  | kΩ                 |
| Current Source Accuracy     | I <sub>ID_ACC</sub>      | PLC = 1.5V                      | I <sub>ID</sub> = 1μA  | -29.5 |       | +5.5  | %                  |
|                             |                          |                                 | I <sub>ID</sub> = 4μA  | -10.5 |       | +4.5  |                    |
|                             |                          |                                 | I <sub>ID</sub> = 16μA | -6.4  |       | +4.9  |                    |
|                             |                          |                                 | I <sub>ID</sub> = 64μA | -5.4  |       | +5.0  |                    |
| Current Source              | I <sub>ID</sub>          |                                 |                        |       | 1     |       | μA                 |
|                             |                          |                                 |                        |       | 4     |       |                    |
|                             |                          |                                 |                        |       | 16    |       |                    |
|                             |                          |                                 |                        |       | 64    |       |                    |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER                                      | SYMBOL                 | CONDITIONS   | MIN                             | TYP    | MAX | UNITS         |
|--|------------------------|--|---------------------------------|--------|-----|---------------|
| ADC Resolution                                 | ADC_RES                |  |                                 | 8      |     | bit           |
| ADC Voltage Step                               | ADC_STEP               |  |                                 | 5.9    |     | mV            |
| ADC Full-Scale Error                           | ADC_ERR                |  | -2                              |        | +2  | %             |
| ADC Noise Filtering                            | ADC_NOISE              |  |                                 | 45     |     | $\mu\text{s}$ |
| ADC Full Scale                                 | ADC_SCALE              |  |                                 | 1.5    |     | V             |
| <b>PLC COMMUNICATION DETECTION THRESHOLDS</b>  |                        |  |                                 |        |     |               |
| PLC Detection Threshold                        | $V_{\text{TH\_PLC}}$   | PLCThrSel = 0b00   |                                 | 75     |     | mV            |
|  |                        | PLCThrSel = 0b01   |                                 | 90     |     |               |
|  |                        | PLCThrSel = 0b10   |                                 | 105    |     |               |
|  |                        | PLCThrSel = 0b11   |                                 | 120    |     |               |
| <b>PLC COMMUNICATION TIME UNIT</b>             |                        |  |                                 |        |     |               |
| PLC Communication Time Unit                    | $TU_{\text{PLC}}$      |  |                                 | 6      |     | $\mu\text{s}$ |
| <b>PLC COMMUNICATION CURRENT SINK</b>          |                        |  |                                 |        |     |               |
| Current Sink Accuracy                          | $I_{\text{SINK\_ACC}}$ |  | -10                             |        | +10 | %             |
| Current Sink                                   | $I_{\text{SINK}}$      | PLC = 4V   | PLCSnkSel = 0b00, lchg_x2 = 0b0 |        | 50  | mA            |
|  |                        |  | PLCSnkSel = 0b01, lchg_x2 = 0b0 |        | 70  |               |
|  |                        |  | PLCSnkSel = 0b10, lchg_x2 = 0b0 |        | 90  |               |
|  |                        |  | PLCSnkSel = 0b11, lchg_x2 = 0b0 |        | 110 |               |
|  |                        |  | PLCSnkSel = 0b00, lchg_x2 = 0b1 |        | 100 |               |
|  |                        |  | PLCSnkSel = 0b01, lchg_x2 = 0b1 |        | 140 |               |
|  |                        |  | PLCSnkSel = 0b10, lchg_x2 = 0b1 |        | 180 |               |
|  |                        |  | PLCSnkSel = 0b11, lchg_x2 = 0b1 |        | 220 |               |
| <b>FUEL GAUGE POWER SUPPLY</b>                 |                        |  |                                 |        |     |               |
| Shutdown Supply Current                        | $I_{\text{DD0}}$       |  |                                 | 0.5    |     | $\mu\text{A}$ |
| Hibernate Supply Current                       | $I_{\text{DD1}}$       | Average current  |                                 | 5.1    |     | $\mu\text{A}$ |
| Active Supply Current                          | $I_{\text{DD2}}$       | Average current not including thermistor measurement current |                                 | 15     |     | $\mu\text{A}$ |
| <b>FUEL GAUGE ANALOG-TO-DIGITAL CONVERSION</b> |                        |  |                                 |        |     |               |
| BATT Measurement Error                         | $V_{\text{GERR}}$      | $T_A = +25^{\circ}\text{C}$                                  | -7.5                            |        | 7.5 | mV            |
|  |                        | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$      | -20                             |        | 20  |               |
| BATT Measurement Resolution                    | $V_{\text{LSB}}$       |  |                                 | 78.125 |     | $\mu\text{V}$ |
| BATT Measurement Range                         | $V_{\text{FS}}$        |  | 2.8                             |        | 4.9 | V             |



( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER   | SYMBOL                    | CONDITIONS   | MIN  | TYP                           | MAX  | UNITS              |
|---|---------------------------|--|------|-------------------------------|------|--------------------|
| <b>FUEL GAUGE LEAKAGE</b>   | $R_{\text{SNS}}$          | $T_A = +25^{\circ}\text{C}$  |      | 30                            |      | m $\Omega$         |
| Current Measurement Offset Error  | $I_{\text{OERR}}$         | Long term average without load current   |      | $\pm 1$                       |      | mA                 |
| Current Measurement Resolution  | $I_{\text{LSB}}$          |  |      | 39.0625                       |      | $\mu\text{A}$      |
| Current Measurement Gain Error  | $I_{\text{GERR}}$         | (Note 1)   |      | $\pm 2.5$                     |      | % of Reading       |
| Current Measurement Error   | $I_{\text{ERR}}$          | $T_A \leq +50^{\circ}\text{C}$ , 0.125A and 0.25A (Note 1)                     | -3   |                               | +3   | % of Reading       |
| Internal Temperature Measurement Error  | $T_{\text{IGERR}}$        | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$                        |      | $\pm 1$                       |      | $^{\circ}\text{C}$ |
| Internal Temperature Measurement Resolution                                   | $T_{\text{ILSB}}$         |  |      | 0.00391                       |      | $^{\circ}\text{C}$ |
| <b>FUEL GAUGE INPUT/OUTPUT</b>  |                           |  |      |                               |      |                    |
| THM Pullup Resistance (Internal)  | $R_{\text{TH10}}$         | Config.R100 = 0  | 9.6  | 16                            | 22.4 | k $\Omega$         |
|   | $R_{\text{TH100}}$        | Config.R100 = 1  | 96   | 160                           | 224  |                    |
| Output Drive Low, ALRT, SDA   | $V_{\text{OL}}$           | $I_{\text{OL}} = 4\text{mA}$ , $V_{\text{BAT}} = 2.3\text{V}$                  |      |                               | 0.4  | V                  |
| Input Logic-High, ALRT, SCL, SDA  | $V_{\text{IH}}$           |  | 1.5  |                               |      | V                  |
| Input Logic-Low, ALRT, SCL, SDA   | $V_{\text{IL}}$           |  |      |                               | 0.5  | V                  |
| Battery-Detach Detection Threshold  | $V_{\text{DET}}$          | Measured as a fraction of $V_{\text{BAT}}$ on TH rising                        | 91.0 | 96.2                          | 99.0 | %                  |
| Battery-Detach Detection Threshold Hysteresis                                 | $V_{\text{DET-HYS}}$      | Measured as a fraction of $V_{\text{BAT}}$ on TH falling                       |      | 1                             |      | %                  |
| Battery-Detach Comparator Delay   | $t_{\text{TOFF}}$         | TH step from 70% to 100% of $V_{\text{BAT}}$ (ALRTP = 0, ENAIN = 1, FTHRM = 1) |      |                               | 100  | $\mu\text{s}$      |
| <b>FUEL GAUGE LEAKAGE</b>   |                           |  |      |                               |      |                    |
| Leakage Current, ALRT   | $I_{\text{LEAK}}$         | $V_{\text{ALRT}} < 15\text{V}$   | -1   |                               | +1   | $\mu\text{A}$      |
| Leakage Current, THM  | $I_{\text{LEAK\_TH}}$     |  | -1   |                               | +1   | $\mu\text{A}$      |
| <b>FUEL GAUGE TIMING</b>  |                           |  |      |                               |      |                    |
| Time-Base Accuracy  | $t_{\text{ERR}}$          | $T_A = +25^{\circ}\text{C}$  | -1   |                               | 1    | %                  |
|   |                           | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$                        | -5   |                               | 5    | %                  |
| THM Precharge Time  | $t_{\text{PRE}}$          |  | 8.48 |                               |      | ms                 |
| <b>DIGITAL SIGNALS (SDA, SCL, nINT, EN, GPIO1, GPIO2, GPIO3, GPIO4, ALRT)</b> |                           |  |      |                               |      |                    |
| Input Logic-High  | $V_{\text{IO\_IH}}$       |  | 1.4  |                               |      | V                  |
| Input Logic-Low   | $V_{\text{IO\_IL}}$       |  |      |                               | 0.4  | V                  |
| Input Logic-High GPIO CMOS  | $V_{\text{IO\_IH\_CMOS}}$ | (Note 2)   |      | $0.7 \times V_{\text{CCINT}}$ |      | V                  |
| Input Logic-Low GPIO CMOS   | $V_{\text{IO\_IL\_CMOS}}$ | (Note 2)   |      | $0.3 \times V_{\text{CCINT}}$ |      | V                  |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{BAT} = 3.7\text{V}$ ,  $C_{DIG} = 1\mu\text{F}$ ,  $C_{SYS} = 1\mu\text{F}$ ,  $C_{BAT} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER  | SYMBOL              | CONDITIONS  | MIN                 | TYP | MAX | UNITS              |
|--|---------------------|---|---------------------|-----|-----|--------------------|
| GPIO Input Pullup/Pulldown Resistor                        | $R_{in\_GPIO}$      | Input resistor presence I <sup>2</sup> C controlled, as Pullup, it is tied to $V_{CCINT}$ |                     | 175 |     | k $\Omega$         |
| Input Leakage Current                                      | $I_{LK\_I}$         | SCL and EN  | -1                  |     | +1  | $\mu\text{A}$      |
| Output Logic-High Leakage Current (Open Drain Only)        | $I_{LK\_O}$         | SDA, nINT, GPIO1, GPIO2, GPIO3, GPIO4, ALRT   |                     |     | 1   | $\mu\text{A}$      |
| Output Logic-Low   | $V_{IO\_OL}$        | $I_{SINK} = 20\text{mA}$  |                     |     | 0.4 | V                  |
| <b>I<sup>2</sup>C TIMING (SDA, SCL)</b>                    |                     |   |                     |     |     |                    |
| SCL Clock Frequency  | $f_{SCL}$           | (Note 3)  | 0                   |     | 400 | kHz                |
| Bus Free Time Between a STOP and START Condition           | $t_{BUF}$           |   | 1.3                 |     |     | $\mu\text{s}$      |
| Hold Time (Repeated) START Condition                       | $t_{HD:STA}$        | (Note 4)  | 0.6                 |     |     | $\mu\text{s}$      |
| Low Period of SCL Clock                                    | $t_{LOW}$           |   | 1.3                 |     |     | $\mu\text{s}$      |
| High Period of SCL Clock                                   | $t_{HIGH}$          |   | 0.6                 |     |     | $\mu\text{s}$      |
| Setup Time for a Repeated START Condition                  | $t_{SU:STA}$        |   | 0.6                 |     |     | $\mu\text{s}$      |
| Data Hold Time   | $t_{HD:DAT}$        | (Note 5, Note 6)  | 0                   |     | 0.9 | $\mu\text{s}$      |
| Data Setup Time  | $t_{SU:DAT}$        | (Note 5)  | 100                 |     |     | ns                 |
| Setup Time for STOP Condition                              | $t_{SU:STO}$        |   | 0.6                 |     |     | $\mu\text{s}$      |
| Spike Pulse Width Suppressed by Input Filter               | $t_{SP}$            | (Note 7)  |                     |     | 50  | ns                 |
| <b>ESD PROTECTION (PLC, ALL OTHER PINS)</b>                |                     |   |                     |     |     |                    |
| ESD Protection Rating                                      |                     | PLC   | Contact discharge   |     | 8   | kV                 |
|  |                     | All other pins  | HBM                 |     | 2   |                    |
| <b>THERMAL PROTECTION &amp; THERMAL CURRENT LIMITATION</b> |                     |   |                     |     |     |                    |
| Overtemperature Threshold                                  | $T_{SHDN\_PLC}$     | Valid PLC present   | ChgThrmLim = 0b0000 |     | 40  | $^{\circ}\text{C}$ |
|  |                     | Valid PLC present   | ChgThrmLim = 0b0001 |     | 45  |                    |
|  |                     |   | ChgThrmLim = 0b0010 |     | 50  |                    |
|  |                     | Valid PLC present   | ChgThrmLim = 0b0011 |     | 55  |                    |
|  |                     | Valid PLC present   | ChgThrmLim = 0b0100 |     | 60  |                    |
|  |                     |   | ChgThrmLim = 0b0101 |     | 65  |                    |
| Valid PLC present  | ChgThrmLim = 0b0110 |   | 70                  |     |     |                    |

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 3.7\text{V}$ ,  $C_{\text{DIG}} = 1\mu\text{F}$ ,  $C_{\text{SYS}} = 1\mu\text{F}$ ,  $C_{\text{BAT}} = 1\mu\text{F}$ . All capacitance listed are effective values.)

| PARAMETER                            | SYMBOL                  | CONDITIONS        | MIN                 | TYP                        | MAX | UNITS              |
|--------------------------------------|-------------------------|-------------------|---------------------|----------------------------|-----|--------------------|
|                                      |                         | Valid PLC present | ChgThrmLim = 0b0111 |                            | 75  |                    |
|                                      |                         |                   | ChgThrmLim = 0b1000 |                            | 80  |                    |
|                                      |                         | Valid PLC present | ChgThrmLim = 0b1001 |                            | 85  |                    |
|                                      |                         | Valid PLC present | ChgThrmLim = 0b1010 |                            | 90  |                    |
|                                      |                         |                   | ChgThrmLim = 0b1011 |                            | 95  |                    |
|                                      |                         | Valid PLC present | ChgThrmLim = 0b1100 |                            | 100 |                    |
|                                      |                         | Valid PLC present | ChgThrmLim = 0b1101 |                            | 105 |                    |
|                                      |                         |                   | ChgThrmLim = 0b1110 |                            | 110 |                    |
| Valid PLC present                    | ChgThrmLim = 0b1111     |                   | 115                 |                            |     |                    |
| Overtemperature Threshold Hysteresis | $T_{\text{SHDN\_PLCH}}$ | Valid PLC present |                     | 3                          |     | $^{\circ}\text{C}$ |
| Current Thermal Limitation           | $T_{\text{LIM}}$        | Valid PLC present |                     | $T_{\text{SHDN\_PLC}} - 3$ |     | $^{\circ}\text{C}$ |
| Overtemperature Threshold            | $T_{\text{SHDN}}$       |                   |                     | 130                        |     | $^{\circ}\text{C}$ |
| Overtemperature Threshold Hysteresis | $T_{\text{SHDN}}$       |                   |                     | 18                         |     | $^{\circ}\text{C}$ |

**Note 1:** GBD and not production tested.

**Note 2:**  $V_{\text{CCINT}}$  is an internal supply generated from either BAT or PLC. Its voltage is determined by the following:  
If  $V_{\text{PLC}} > V_{\text{PLC\_DET}}$  (3V typ),  $V_{\text{CCINT}} = \text{MAX}(V_{\text{BAT}}, V_{\text{PLC}})$ . Under all other conditions,  $V_{\text{CCINT}} = V_{\text{BAT}}$ .

**Note 3:** Timing must be fast enough to prevent the IC from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.

**Note 4:**  $f_{\text{SCL}}$  must meet the minimum clock low time plus the rise/fall times.

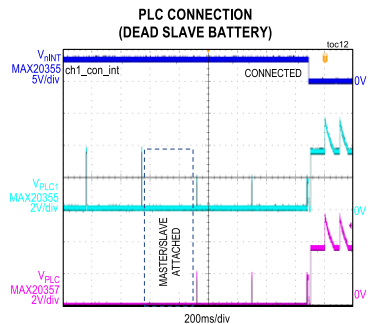
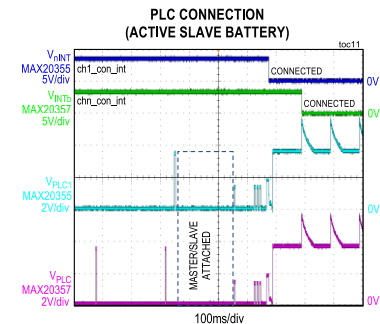
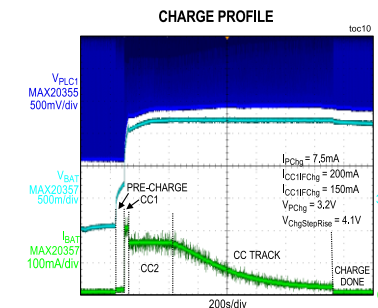
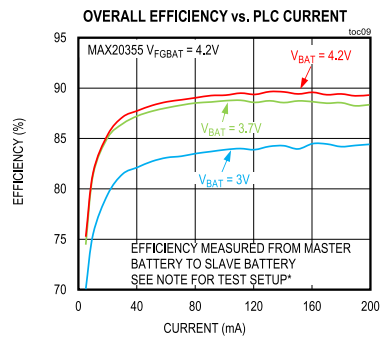
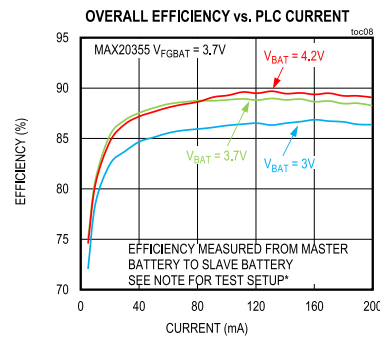
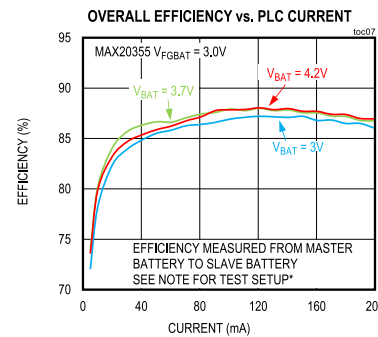
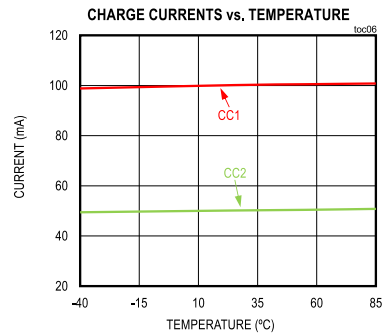
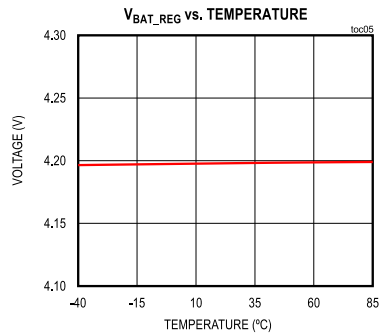
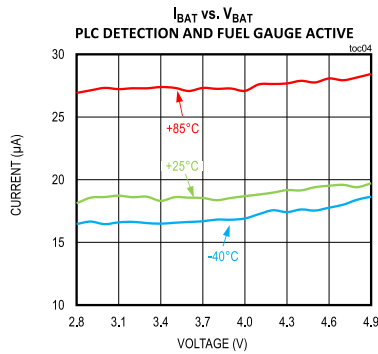
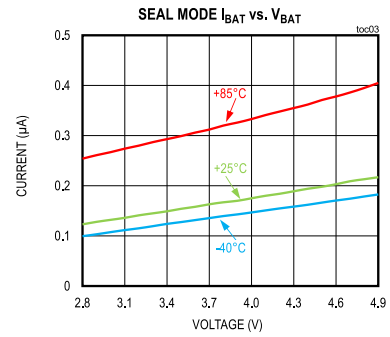
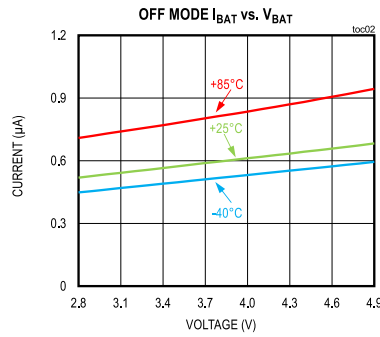
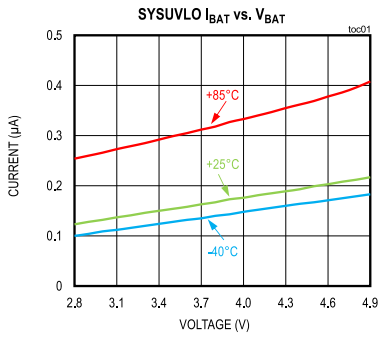
**Note 5:** The maximum  $t_{\text{HD\_DAT}}$  has only to be met if the device does not stretch the low period ( $t_{\text{LOW}}$ ) of the SCL signal.

**Note 6:** This device internally provides a hold time of at least 100ns for the SDA signal (refer to the minimum  $V_{\text{IH}}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

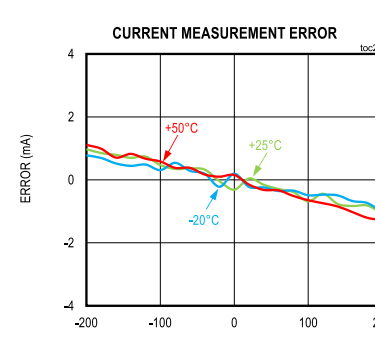
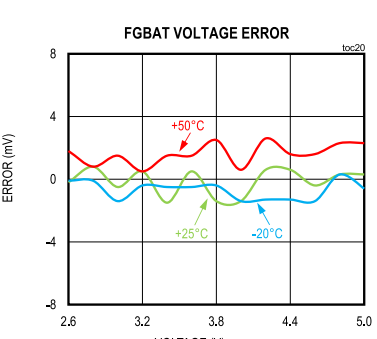
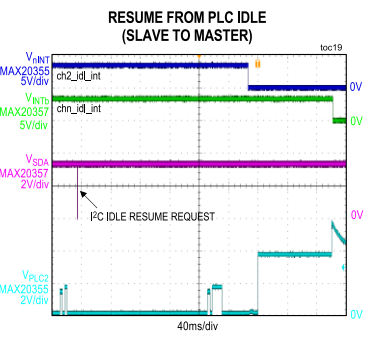
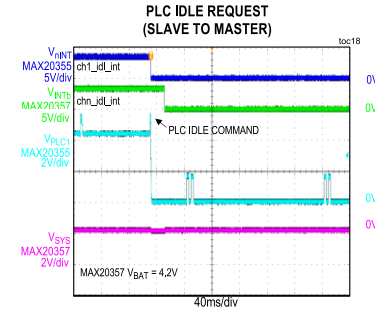
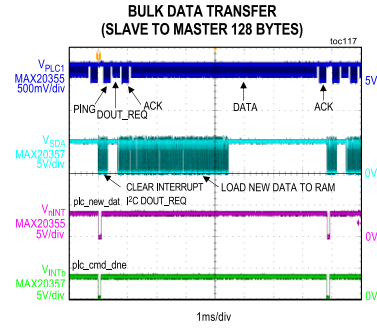
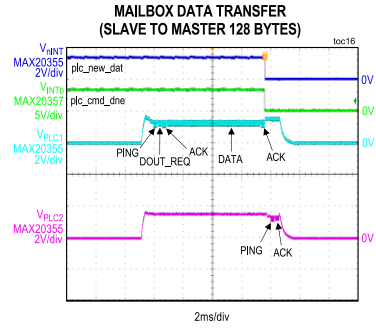
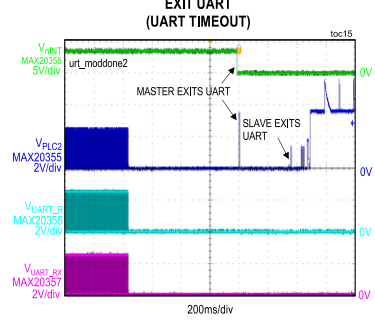
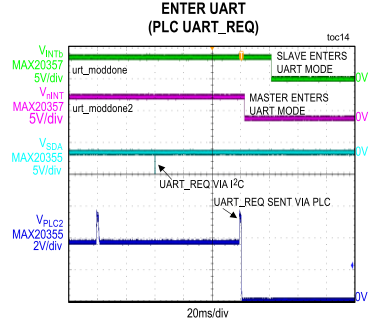
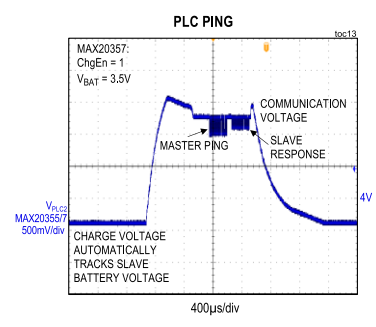
**Note 7:** Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

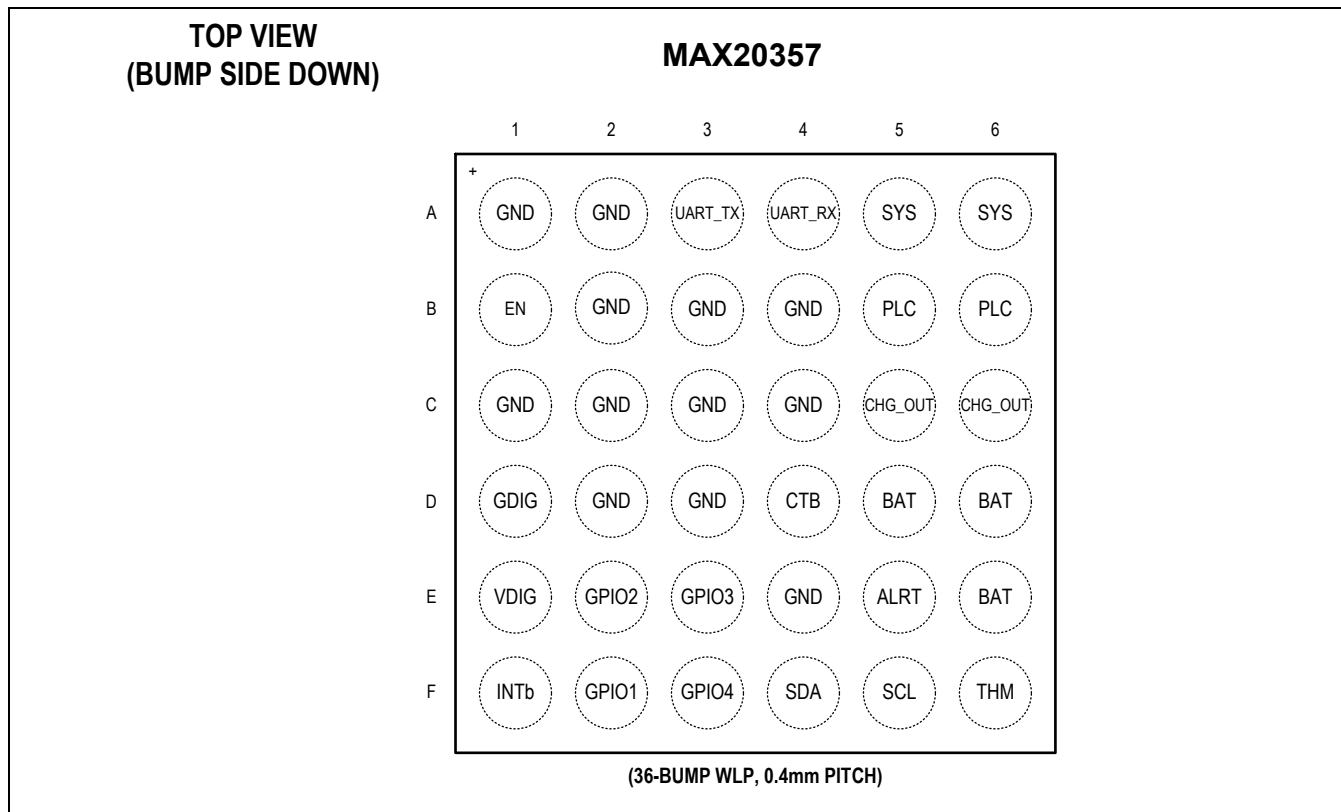


# Power Line Communication with ModelGauge Fuel Gauge and Charger



\* Efficiency test setup: Test on PLC1  
 MAX20355: pl2\_chn\_ena = 0 disable PLC2  
 MAX20357: PLC\_DROP = 100mV, PLC\_HREF = 125mV, PLC\_HLD = 62.5mV, VPChg = 2.7V, BatReg = 4.5V

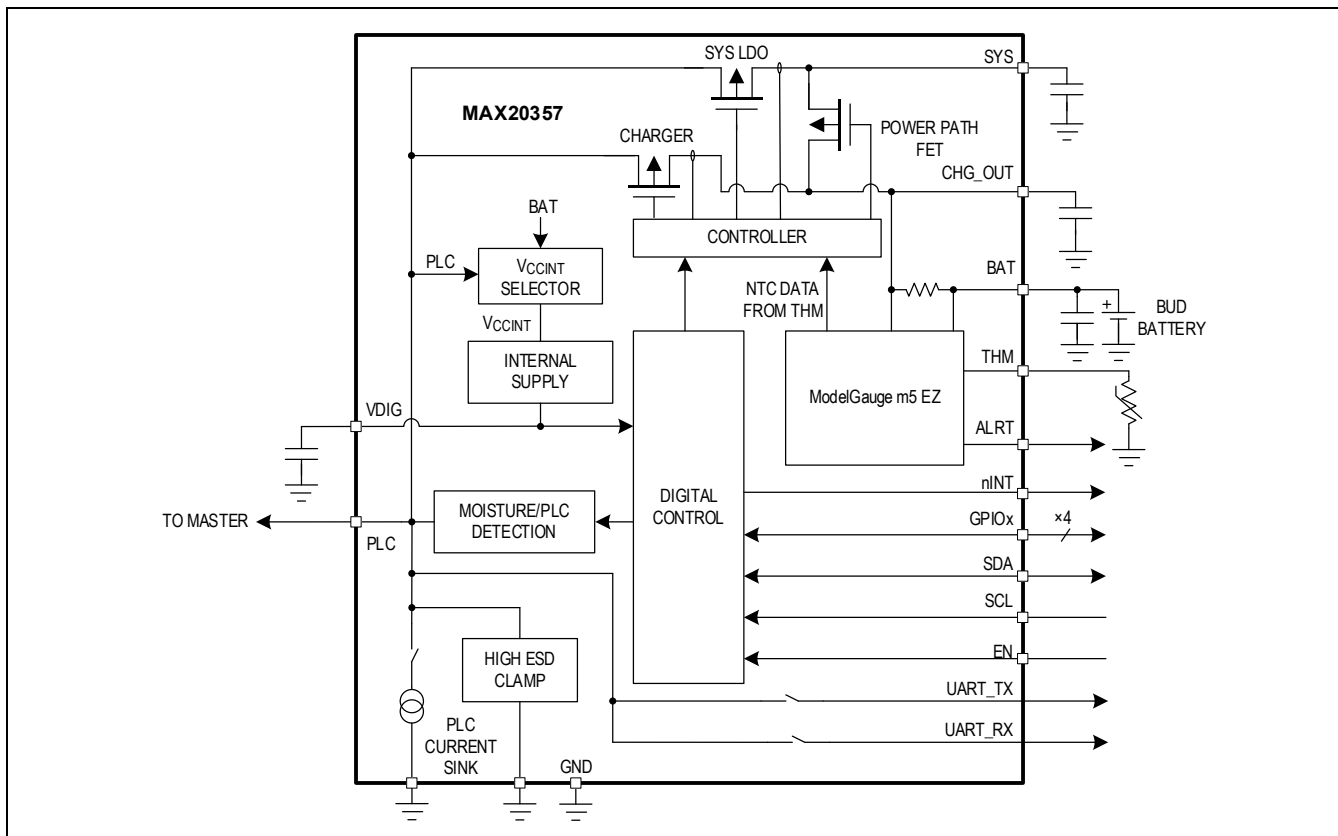
### Pin Configuration



## Pin Descriptions

| PIN  | NAME    | FUNCTION  |
|--|---------|---|
| A1, A2, B2, B3, B4, C1, C2, C3, C4, D2, D3, E4 | GND     | Ground  |
| A3   | UART_TX | Half-Duplex UART_TX   |
| A4   | UART_RX | Half-Duplex UART_RX   |
| A5, A6   | SYS     | System Power Connection Monitored by the Fuel Gauge. Bypass to ground with 1 $\mu$ F capacitor.   |
| B1   | EN      | Active High Enable Input. Drive EN low to place the device in low power shutdown mode. EN pin functionality can be disabled through I <sup>2</sup> C. |
| B5, B6   | PLC     | Power Line Communication Slave Connection. Power input. Data input or output. Connect to master PLC1/2.   |
| C5, C6   | CHG_OUT | Charger Output. Direct path input. Internally shorted to FG_BAT through fuel gauge sense resistor. Bypass to ground with 1 $\mu$ F capacitor.         |
| D1   | GDIG    | Digital Ground. Short to GND.   |
| D4   | CTB     | Connect to BAT  |
| D5, D6, E6                                     | BAT     | Fuel Gauge Connection to Battery. Connect to positive terminal of Li-ion battery.   |
| E1   | VDIG    | Internal 1.8V Supply. Bypass with 1 $\mu$ F capacitor to GND.   |
| E2   | GPIO2   | Programmable GPIO2. May be configured as a digital input or open drain output.  |
| E3   | GPIO3   | Programmable GPIO3. May be configured as a digital input or open drain output.  |
| E5   | ALRT    | Alert Output. The ALRT pin is open-drain active-low output which indicates fuel gauge alerts. Connect it to GND if not used.                          |
| F1   | INTb    | Open-Drain Active-Low Interrupt Output  |
| F2   | GPIO1   | Programmable GPIO1. May be configured as a digital input or open drain output.  |
| F3   | GPIO4   | Programmable GPIO4. May be configured as a digital input or open drain output.  |
| F4   | SDA     | I <sup>2</sup> C Serial Data  |
| F5   | SCL     | I <sup>2</sup> C Serial Clock   |
| F6   | THM     | Thermistor Input. Connect thermistor between THM and GND.   |

## Functional Diagram



## Detailed Description

The MAX20355, together with the MAX20357, form an integrated Power Line Communication (PLC) and automated charging system. These devices provide a complete system solution for efficient charging and data transfer between a charging case and wireless earbuds over a single contact.

The MAX20355 and MAX20357 feature data transfers while simultaneously delivering 200mA of charge/system current per output. Both devices support a 166.7kbps bit rate while charging. With a 166.7kbps bit rate, the PLC protocol can achieve up to 130kbps of throughput using the bulk data transfer feature. Additionally, a 4Mbaud half-duplex data-only UART mode provides an easy and fast method for firmware updates, debug interface, and factory modes. Finally, dedicated hardware PLC commands allow both devices to control GPIOs and enter various power modes, such as ultra-low current ship mode, through the PLC link.



The MAX20355 integrates a completely autonomous charging system that utilizes a 3.3W buck-boost with dynamic voltage scaling (DVS) to provide an optimized charge voltage to the earbuds. An integrated digital state machine automatically manages the dynamic voltage adjustment based on the earbud battery voltage to minimize earbud power dissipation and maximize charging efficiency.

Additional features include comprehensive earbud insertion and removal notifications, even in dead case or bud battery scenarios, and moisture detection on the PLC outputs to prevent contact corrosion. The PLC pins are protected from overcurrent events by an integrated current limiting circuit and ESD events by integrated 8kV contact-rated ESD protection structures.

### Power Line Communication (PLC)

The MAX20355/MAX20357 PLC interface offers a means by which charging, and exchange of data can occur simultaneously on a single wire connection. The interface can accommodate 100kbps of throughput and can do so while delivering up to 200mA of current per channel in dual slave mode and up to 400mA in mono slave mode. The MAX20355 has an integrated current sink and resistor  $R_{TX}$  as shown in [Figure 1](#). During communication, the MAX20355 utilizes the pulses generated by the PLC current sink over resistor  $R_{TX}$  to create PLC pulses on the PLC line. The MAX20355 uses PLC pulses to transfer information to the MAX20357. At the same time, the charging function is not affected. The MAX20357 uses a similar approach to create PLC pulses and transfer information over the PLC line. When there is no ongoing PLC communication,  $R_{TX}$  is shorted by a bypass switch to achieve higher overall power transfer efficiency.

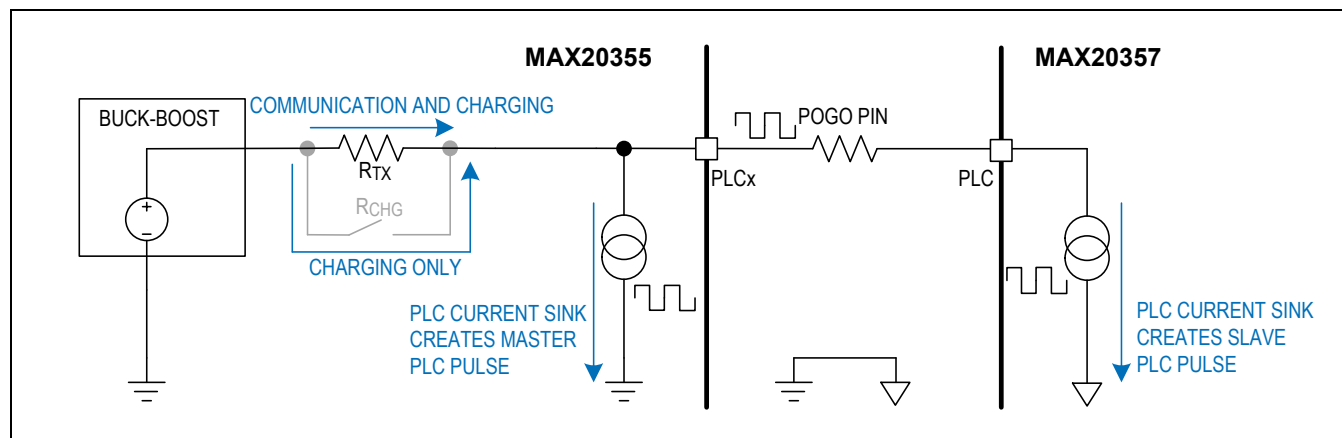


Figure 1. Simplified Scheme of Power Line Communication (PLC)

The PLC interface balances between robustness and throughput. Synchronization mechanisms and checksums offer robust data transfer, but this is also balanced against protocol overhead. With a 166.67kbps bit rate, this careful balance allows a low error rate while achieving throughput up to 130kbps in bulk data transfer mode. To overcome limitations on throughput due to the I<sup>2</sup>C interface, the MAX20355/MAX20357 integrates two 128-byte FIFOs. This allows the system to keep I<sup>2</sup>C overhead low utilizing bulk writes. The MAX20355 also features a 4Mbaud, data-only, half-duplex UART passthrough mode. This mode uses a simple switch that connects UART ports from master to slave for firmware updates, factory mode, and debug mode over a single PLC line.

The following sections describe the PLC PING (PLC command/mailbox data transfer), FIFO (bulk data transfer), and UART interface in detail.

### PLC PING

The PLC interface between master and slave follows a master-initiated scheme. There are two data transfer types—PING and bulk data transfer. PINGs begin with a transfer from master to slave to send data across the interface, request data from the slave, offer the slave a chance to make requests, and sometimes issue commands to the slave. [Figure 2](#) shows the basic structure of the master to slave PING packet. Master initiates the transmission with a preamble which synchronizes the link and then transmits data. The slave responds in the same manner within a response timeout period. PLC PINGs are automatically generated and transmitted through the PLC line every telemetry period.

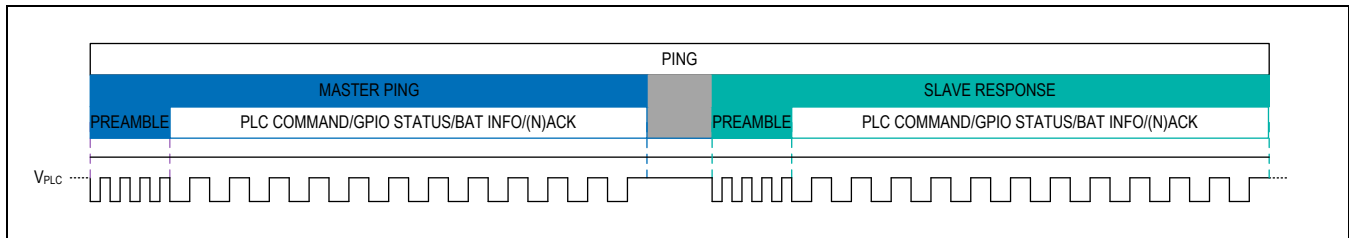


Figure 2. Periodic PING

### LISTEN Command and Continuously Updated Information

Each PLC PING contains one PLC command. Most PLC commands are initiated by an I<sup>2</sup>C write from the system. However, the MAX20355 features automatic LISTEN command, which is sent periodically independent of input from the I<sup>2</sup>C interface. When there is no customer PLC command issued through I<sup>2</sup>C, LISTEN command is automatically sent through the PING, the slave has the option to send its command back to the master using its command field. In response to the master's PING, the slave sends the appropriate data based on the contents of the master PING. The contents of the command and data fields are filled according to the requirements of the command sent from the master. The periodic PING offers the following features:

1. Send master PLC command from master to slave ([Table 1](#)).
2. Give slave an opportunity to send slave PLC commands to master ([Table 2](#)).
3. Transmit GPIO status between master and slave.
4. Exchange master/slave battery information: master battery voltage, slave battery voltage, slave SoC, and slave charging status.
5. Automatic PLC voltage adjustment to track slave battery voltage and minimize power consumption. Details are described in the [Charger Battery Voltage Tracking Loop](#) section.
6. Automatic disconnection detection. Master detects slave is disconnected if there is no proper slave response for master PING.

The exchanged GPIO status and battery information between master and slave are ready to read from the master and slave local registers.

### Master Commands

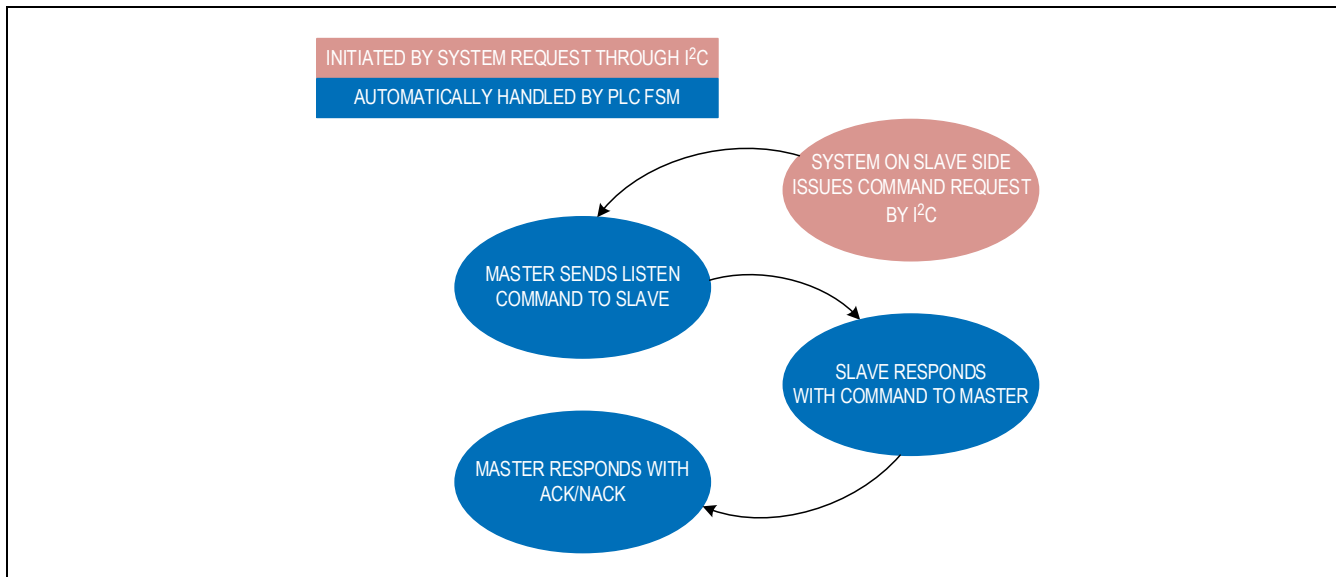
In addition to the LISTEN command, which is handled automatically, the master can execute other commands manually as well. Master's command field determines what type of transaction occurs on the PLC interface. Commands over the PLC interface are requested by I<sup>2</sup>C. [Table 1](#) describes the various commands master can send and what data and statuses are exchanged. Note that many commands can be sent from master to slave or from slave to master. However, it is only in response to a LISTEN command where the slave may send its commands. Master commands are initiated by writing to the `plc_command1/2` and triggered by `plc_run_trg1/2` through master I<sup>2</sup>C. In the command argument register `plc_cmd_arg1/2`, details on how the command is processed are available for the user to specify.

**Table 1. Master Commands**

| MASTER COMMANDS | plc_command1/2 | plc_cmd_arg1/2                       |   |
|-----------------|----------------|--------------------------------------|---|
| LISTEN          | N/A            | N/A                                  |   |
| SET_GPIO        | 0x3            | New slave GPIO setting               |   |
| DOUT_REQ        | 0x5            | Number of bytes (up to 128 bytes)    |   |
| UART_REQ        | 0x6            | slave_uart_sw[1:0]                   |   |
| SYST_REQ        | 0x0            | 0x00                                 | SEAL request. Puts slave in SEAL mode.  |
|                 |                | 0x01                                 | Soft reset request. Resets slave's registers.                                   |
|                 |                | 0x02                                 | Hard reset request. Cycle the power on the slave's SYS node.                    |
|                 |                | 0x03                                 | Fuel gauge reset request. Resets fuel gauge block.                              |
|                 |                | 0x04                                 | FIFO request. Puts system into bulk data transfer mode.                         |
|                 |                | 0x05                                 | Free request. Stop bulk data transfer and free the data line.                   |
|                 |                | 0x06                                 | IDLE mode request. Sends system into PLC IDLE mode.                             |
|                 |                | 0x07                                 | Hard + Soft reset request. Reset all registers, FSM and cycle the power at SYS. |
|                 |                | {0x3F, slave_uart_tx, slave_uart_rx} | UBOOT request. Hard resets slave and puts slave in UART mode.                   |

**Slave Commands**

The slave can also issue commands to the master. The slave similarly issues the commands based on I<sup>2</sup>C input, but it must wait for a master LISTEN command before the command can be sent back to the master. Once the LISTEN command is received, the slave then sends its command using the COMMAND field. *Figure 3* shows the method by which the slave can send a command. Slave commands are initiated with a write to plc\_command and triggered by plc\_run\_trg through master I<sup>2</sup>C. In the command argument register plc\_cmd\_arg, details on how to process the PLC commands are available for the user to specify.



*Figure 3. Sending Commands from the Slave*

**Table 2. Slave Commands**

| SLAVE COMMAND* | plc_command | plc_cmd_arg (DATA)                |   |
|----------------|-------------|-----------------------------------|---|
| SET_GPIO       | 0x3         | New master GPIO setting           |   |
| DOUT_REQ       | 0x5         | Number of bytes (up to 128 bytes) |   |
| UART_REQ       | 0x6         | master_uart_sw[3:0]               |   |
| SYST_REQ       | 0x0         | 0x01                              | Soft reset request. Resets master's registers.                    |
|                |             | 0x03                              | Fuel gauge reset request. Resets master's fuel gauge block.       |
|                |             | 0x04                              | FIFO request. Puts master and slave into bulk data transfer mode. |
|                |             | 0x05                              | Free request. Stop bulk data transfer and free the data line.     |
|                |             | 0x06                              | Idle mode request. Sends master into idle mode.                   |

\*Always sent in response to the "LISTEN" command from the master shown in [Table 1](#).

**Mailbox Data Transfer (DOUT\_REQ)**

**From Master to Slave**

Mailbox data transfers are used to exchange one data packet, up to 128 bytes, from master to slave. A mailbox data transfer begins with a data out request (DOUT\_REQ) master command. Fill the data packet into the master RAM, write the number of bytes to be transferred in the command argument field `plc_cmd_arg1/2`, then trigger the DOUT\_REQ command. If slave responds ACK to DOUT\_REQ command, data in RAM is transferred to slave automatically. After slave successfully receives data, `plc_new_dat` interrupt is asserted and `RAM_is_full` is set to 1. Once `RAM_is_full` is set to 1, slave RAM is protected from PLC and it sends NACK to master's DOUT\_REQ command until `RAM_is_full` is write cleared. Make sure to read data in RAM before clearing `RAM_is_full` to avoid data loss. Note that although both PLC devices have two integrated 128-byte RAMs, only one RAM is used in mailbox data transfer. [Figure 4](#) shows the flow of data during a master to slave write.

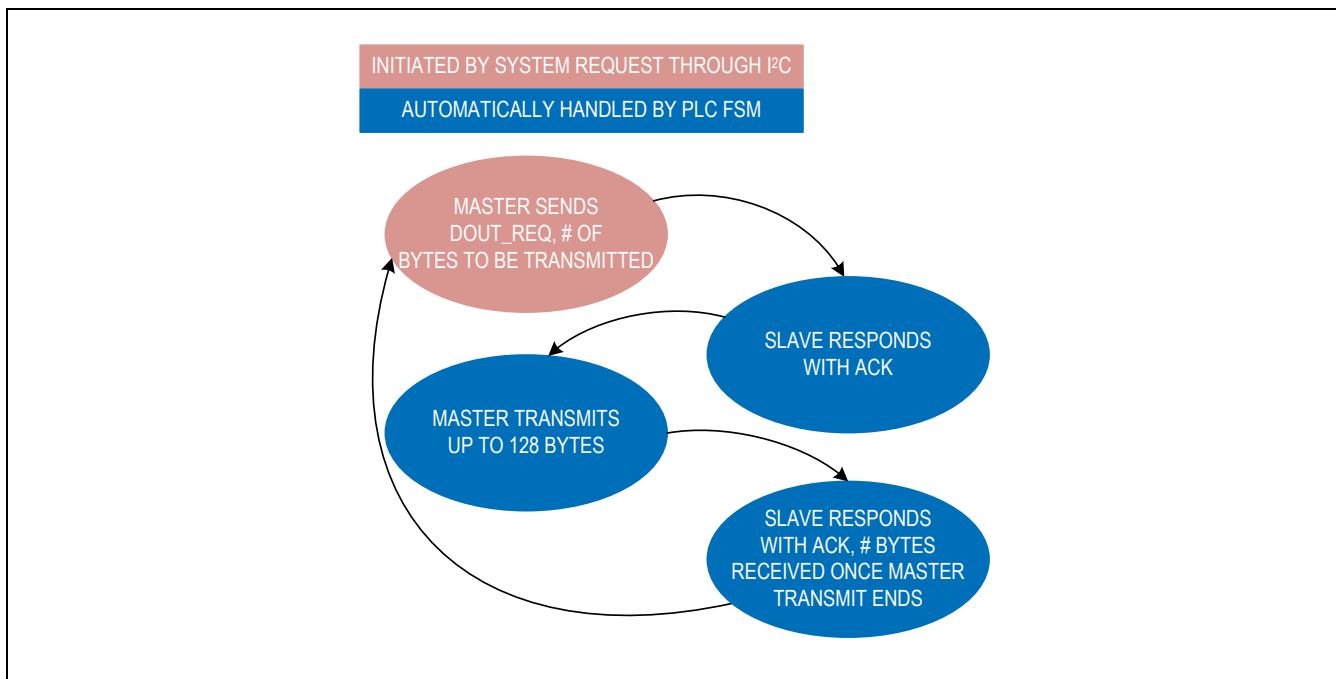


Figure 4. Master to Slave Mailbox Data Transfer

### From Slave to Master

A similar scheme is used to send a packet of data, up to 128 bytes, from slave to master. A mailbox data transfer begins with a data out request (DOUT\_REQ) slave command. Write the number of bytes to be transferred in the command argument field `plc_cmd_arg`. Fill the data packet into the slave RAM, write the number of bytes to be transferred in the command argument field `plc_cmd_arg`, then trigger the DOUT\_REQ command. Since the system follows master initiated scheme, the slave triggers the DOUT\_REQ command when it receives the master Listen command. After the master receives DOUT\_REQ and responds to ACK, data in RAM is transferred to the slave automatically. After master successfully receives data, `plc_new_dat` interrupt is asserted and `RAM_is_full` is set to 1. Once `RAM_is_full` is set to 1, master RAM is protected from PLC, and it sends NACK to slave's DOUT\_REQ command until `RAM_is_full` is write cleared. Make sure to read data in RAM before clearing `RAM_is_full` to avoid data loss. Note that although both PLC devices have two integrated 128-byte RAMs, only one RAM is used in mailbox data transfer. [Figure 5](#) shows the flow of data during a slave to master write.

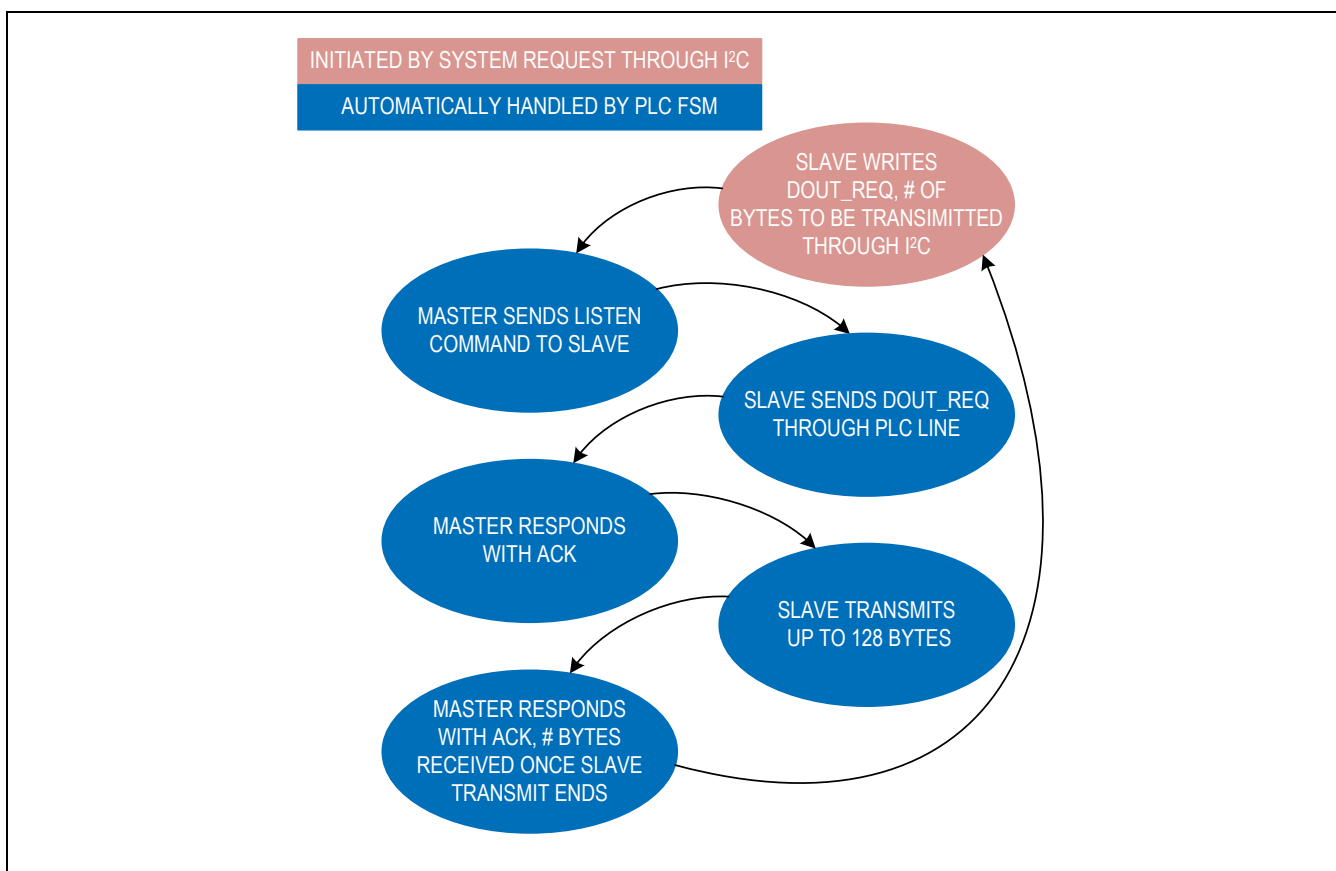


Figure 5. Slave to Master Mailbox Data Transfer

### Bulk Data Transfer (FIFO)

To minimize the impact of I<sup>2</sup>C protocol overhead on the achievable throughput, the MAX20355 and MAX20357 integrate two 128-byte RAMs for bulk data transfer. The bulk data transfer scheme is shown in [Figure 6](#). The I<sup>2</sup>C bus connects first to the RAM\_1 to load data with I<sup>2</sup>C bulk writes at data rates up to 400kbps. Once the DOUT\_REQ command is triggered, the I<sup>2</sup>C bus and PLC line are swapped, I<sup>2</sup>C bus from RAM\_1 to RAM\_2 and PLC from RAM\_2 to RAM\_1. While RAM\_1 is being emptied by the PLC engine, the next set of data can be loaded by I<sup>2</sup>C bulk write again into the RAM\_2. An interrupt is sent to the system after RAM\_1 is completely emptied. Repeat the same process to swap the I<sup>2</sup>C bus and PLC back and forth to load and transmit data simultaneously. Similar implementation on receiving side swaps I<sup>2</sup>C bus and PLC back and forth to receive and read data to receiver's microcontroller. Dual-RAM architecture reduces I<sup>2</sup>C protocol overhead and enhances achievable throughput. Packets of any size up to 128 bytes can be sent by this method.

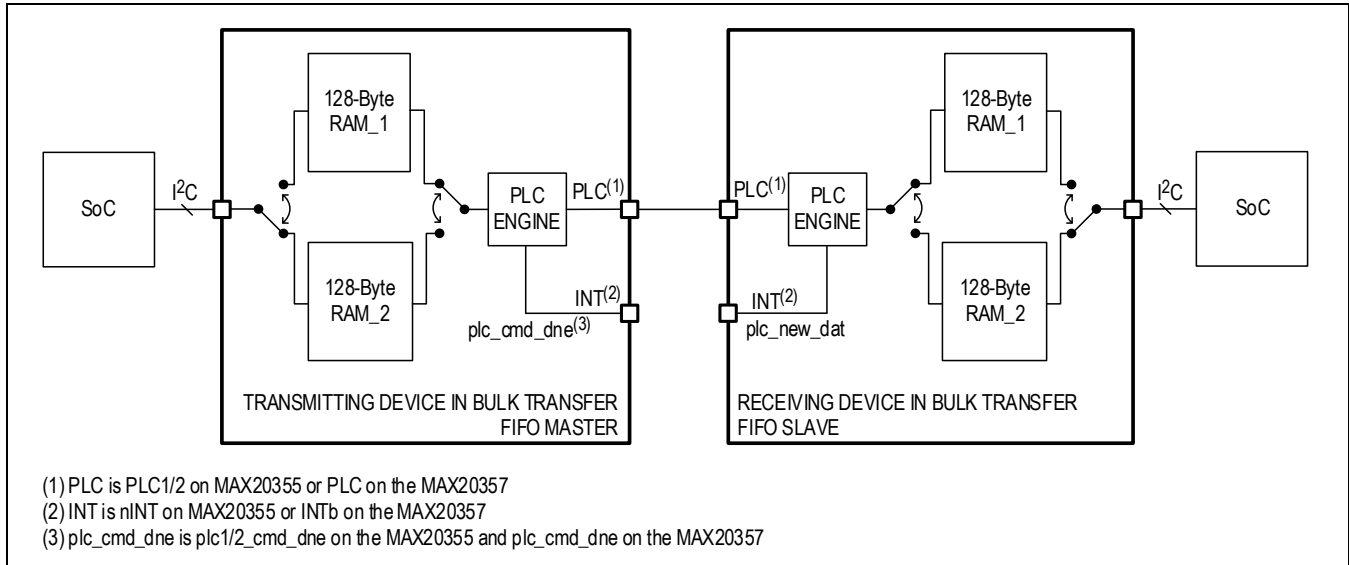


Figure 6. Bulk Data Transfer Implementation

### From Master to Slave

Bulk data transfers from master to slave begin with a system request (SYST\_REQ) master command. In the command argument of SYST\_REQ, the master needs to send a FIFO request. Once receiving an ACK from the slave, PLC voltage is pulled up to communication voltage and the PLC line is locked for bulk data transfer. Before triggering the data transfer, the data packet needs to be filled into the master RAM through I<sup>2</sup>C. Similar to mailbox data transfer, write the number of bytes to be transferred to plc\_cmd\_trg1/2, then trigger the DOUT\_REQ command and wait for plc1/2\_cmd\_dne interrupt. Repeat DOUT\_REQ and wait for plc1/2\_cmd\_dne to interrupt multiple times as needed. After all data packets are transferred, issue a FREE request from the master side to unlock the line and return to normal PLC mode. Note that master bulk data transfer is designed to transfer data only from master to slave. [Figure 7](#) shows the flow of data during a master to slave write.

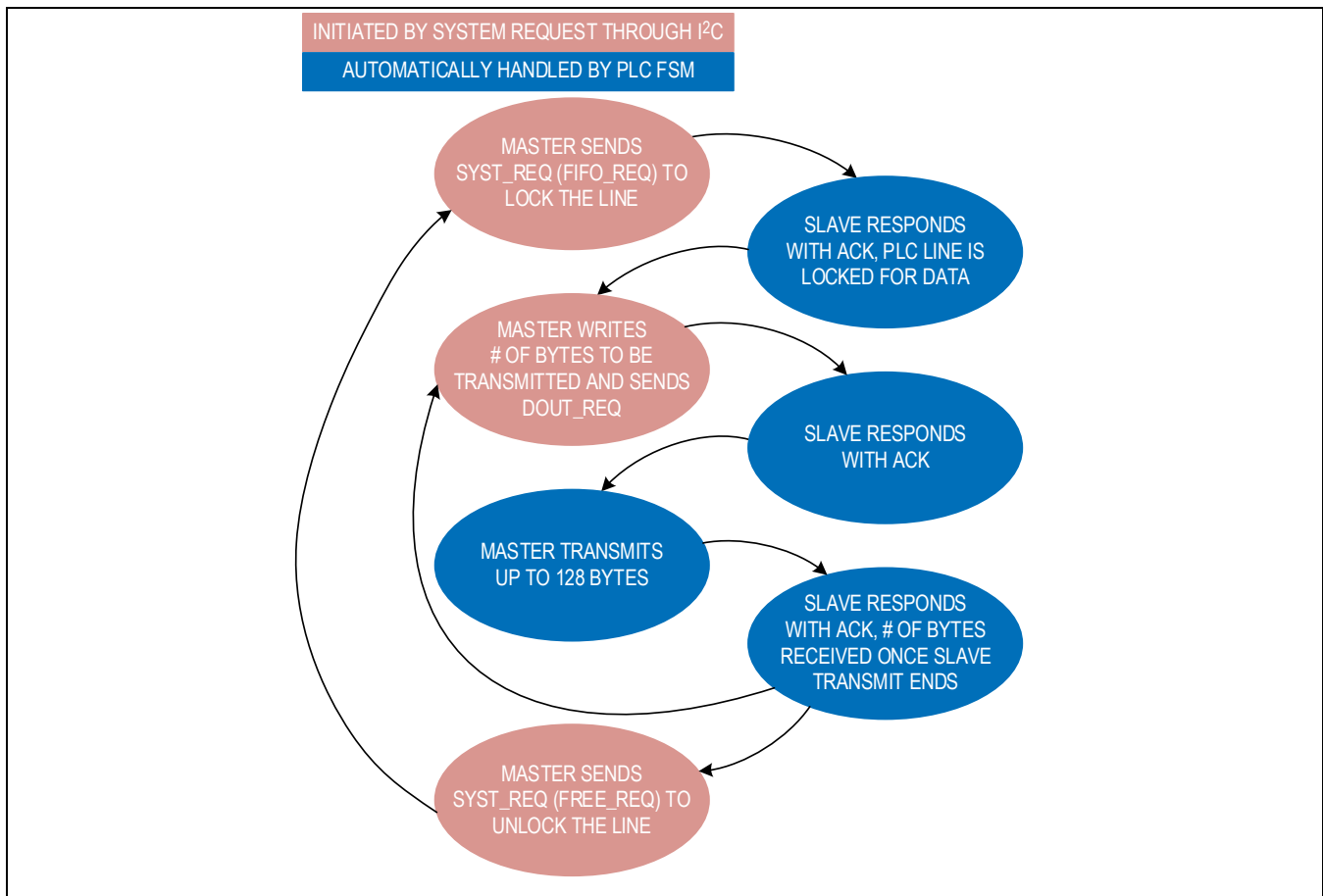


Figure 7. Master to Slave Bulk Data Transfer

#### From Slave to Master

Bulk data transfers from slave to master begin with a system request (SYST\_REQ) slave command. In the command argument of SYST\_REQ, the slave needs to write a FIFO request. The slave waits until the master's LISTEN command to send out a FIFO request through the PLC line. Once receiving an ACK from the master, the master locks the PLC line and enters bulk data transfer mode. Before triggering the data transfer, the data packet needs to be filled into the slave RAM. Similar to mailbox data transfer, write the number of bytes to be transferred to `plc_cmd_arg`, then trigger the DOUT\_REQ command and wait for `plc_cmd_dne` interrupt. Repeat DOUT\_REQ and wait for `plc_cmd_dne` to interrupt multiple times as needed. After all data packets are transferred, issue a FREE request from the slave side to unlock the line and return to normal PLC mode. Note that slave bulk data transfer is designed to transfer data only from slave to master. [Figure 8](#) shows the flow of data during a slave to master write.

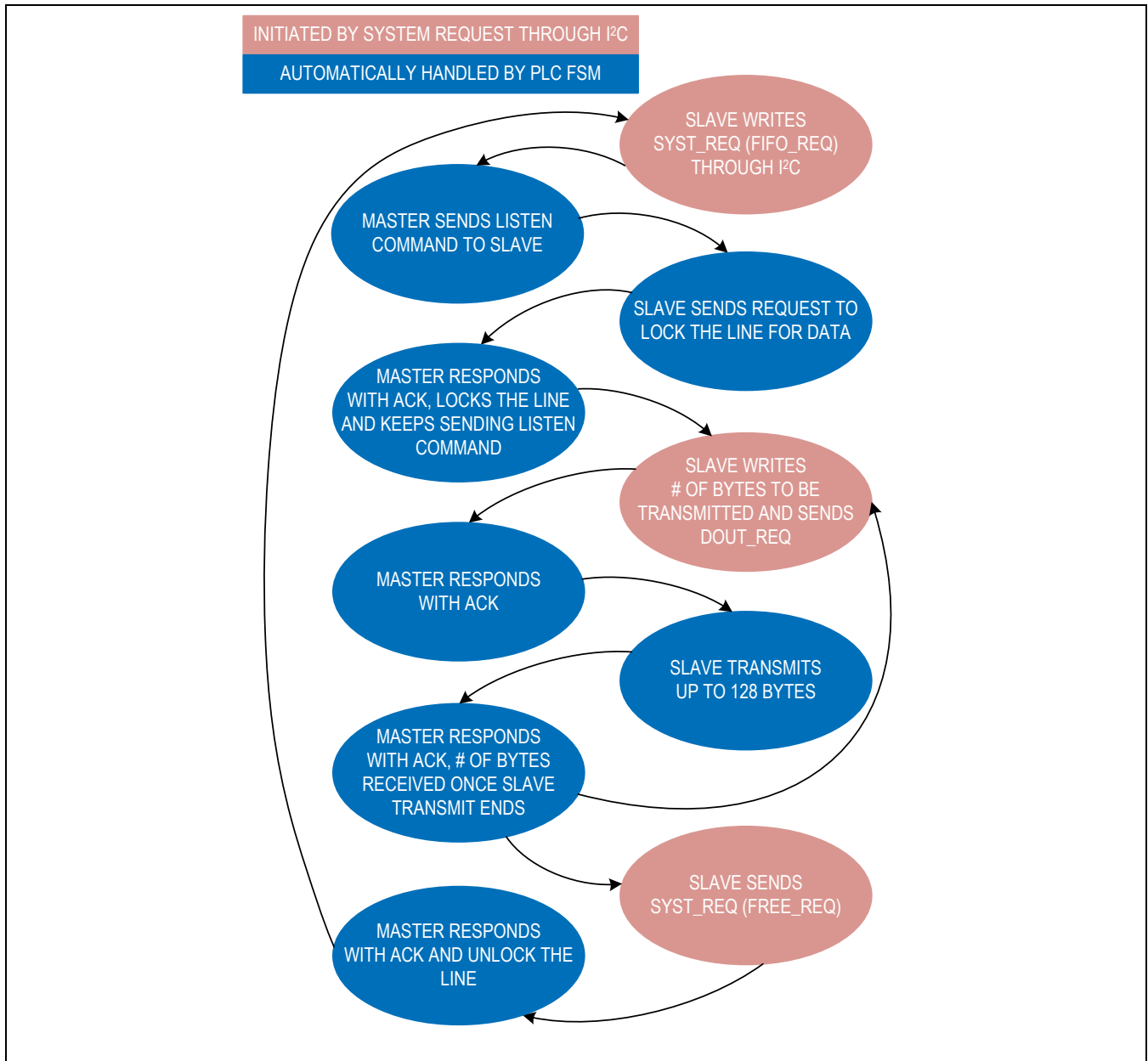


Figure 8. Slave to Master Bulk Data Transfer

### Half-Duplex UART Passthrough Interface

The MAX20355 and MAX20357 feature a 4Mbaud, data-only, half-duplex UART passthrough mode. This mode is a simple switch that connects either the TX or RX for firmware updates, factory mode, and debug mode over the single PLC line. A UART command can be sent through the PLC interface to send either device into UART mode in a particular configuration. Internal switches allow the user to separate UART TX and UART RX. The configuration can be seen in [Figure 9](#). The user can use the I<sup>2</sup>C command to switch roles from TX to RX or vice versa on master and slave. The slave provides one additional feature to detect incoming data automatically through its UART\_RX pin. In this mode, once the slave enters UART mode, it closes its UART\_TX switch by default. Once it detects a rising/falling edge on its UART\_RX pin from the slave microcontroller, it toggles the switch from UART\_TX to UART\_RX automatically. After the data transfer is completed in receiving direction, switch toggles back from UART\_RX to UART\_TX automatically after a programmable blanking time. This feature allows the user to send and receive data through UART when the slave I<sup>2</sup>C is not available.



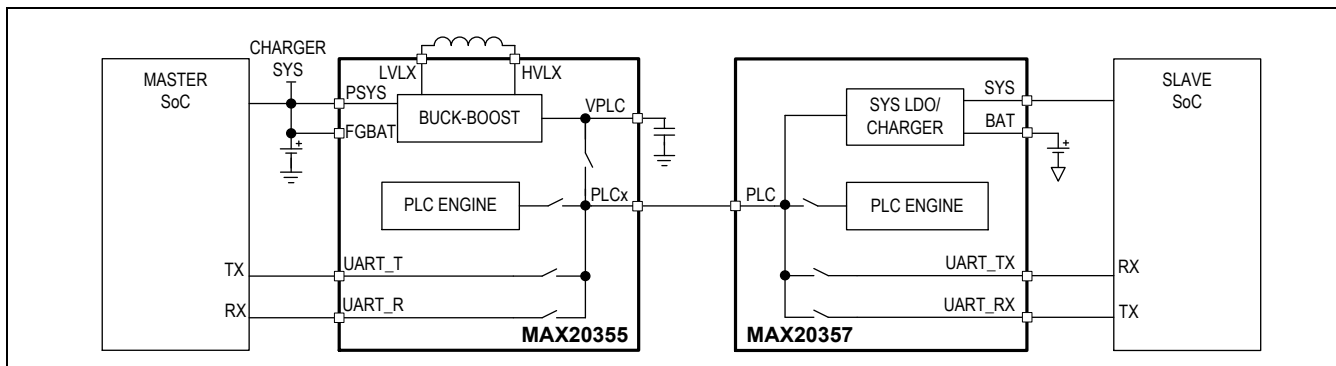


Figure 9. UART Interface

### From Master to Slave

The master can put the slave into UART mode by using the UART\_REQ master command. The direction of UART communication is set in the command argument. Corresponding master and slave switches are closed once the UART command is successfully triggered. The switch settings are shown in [Table 3](#). If the user wants to control UART switches manually in UART mode, all the master/slave UART switch settings can be changed through I2C.

**Table 3. UART Switch Settings in Master PLC Command Argument**

| slave_uart_sw[1:0] | MASTER UART_T | MASTER UART_R | SLAVE UART_TX | SLAVE UART_RX |
|--------------------|---------------|---------------|---------------|---------------|
| 0b00               | x             | x             | x             | x             |
| 0b01               | x             | √             | x             | √             |
| 0b10               | √             | x             | √             | x             |
| 0b11               | √             | √             | √             | √             |

“√” represents the switch is ON and “x” represents the switch is OFF

### From Slave to Master

The slave can put the master into UART mode by using the UART\_REQ slave command. Corresponding master switches are closed once the UART command is successfully triggered. The switch settings are shown in [Table 4](#). No slave switch is closed after UART\_REQ. The slave UART\_TX and UART\_RX switches need to be closed through the slave I2C write. If the user wants to control UART switches manually in UART mode, all the master/slave UART switch settings can be changed through the master/slave I2C.

**Table 4. UART Switch Settings in Slave PLC Command Argument**

| master_uart_sw[3:0] | MASTER PLC2 UART_T | MASTER PLC2 UART_R | MASTER PLC1 UART_T | MASTER PLC1 UART_R |
|---------------------|--------------------|--------------------|--------------------|--------------------|
| 0b0000              | x                  | x                  | x                  | x                  |
| 0b0001              | x                  | x                  | x                  | √                  |
| 0b0010              | x                  | x                  | √                  | x                  |
| 0b0011              | x                  | x                  | √                  | √                  |
| 0b0100              | x                  | √                  | x                  | x                  |
| 0b1000              | √                  | x                  | x                  | x                  |
| 0b1100              | √                  | √                  | x                  | x                  |

“√” represents the switch is ON and “x” represents the switch is OFF

### Exit UART Mode

There are two ways to quit UART mode: 1. Master/slave can quit UART mode by disabling UART mode and disconnecting the UART switch through the master/slave I2C; 2. Use master and slave UART timeout counter and wait for UART timeout interrupt. Enable timeout counter through tmo\_tmr\_ena1/2 on master and tmo\_tmr\_ena on slave before entering UART mode. Once the TX/RX line is idle for 0.5s, the slave turns off its UART switch, disconnect UART\_TX or UART\_RX from the PLC line and start a counter to count for 0.6s. After a 0.6s delay, the slave exits UART mode, connects the PLC line to the PLC engine, and returns to the PLC detection mode. Meanwhile, once the line is idle for 0.75s, the master turns off

its UART switch, disconnects UART\_T or UART\_R from the PLC line, connects to the PLC engine, and returns to the PLC detection mode. Note that once the slave disconnects its UART switch at time point 0.5s, it enters an automatic UART exit process and this process is irreversible. It is not allowed to send data from master through UART after time point 0.5s. If data resumes from the master between time point 0.5s and 0.75s, the master UART timeout counter is cleared, and it holds the master in UART mode for another 0.75s. This causes an issue because the slave exits UART mode at time point 1.1s and starts to send PLC detection pulse immediately. If master is still in UART mode after slave exits UART mode, slave's PLC detection pulse may hold master in UART mode.

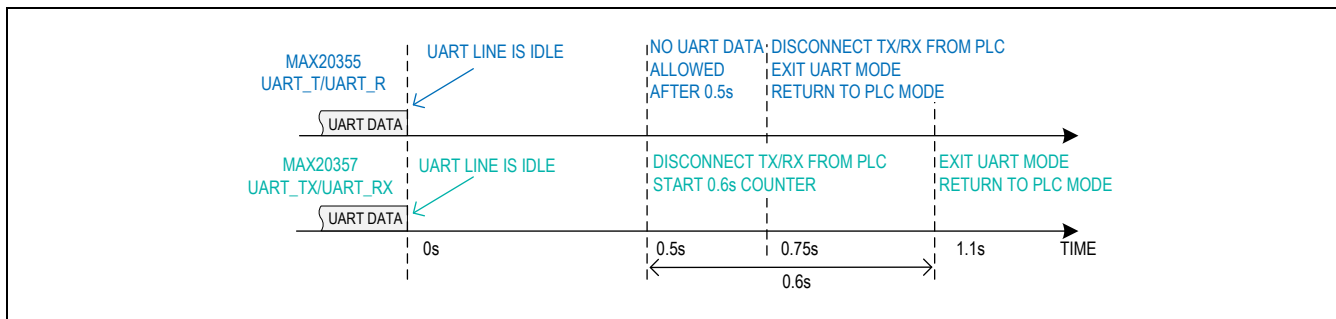


Figure 10. UART Automatic Exit Through UART Timeout

### Autonomous Optimized Battery Charging

The MAX20355 interacts with MAX20357 to create an autonomous, closed-loop battery voltage tracking charging system. This system utilizes a dynamic voltage scaling (DVS) buck-boost on the MAX20355 in conjunction with an ultra-low dropout charger (ULDO) on the MAX20357. The PLC interface closes the loop allowing the buck-boost to adjust its output voltage to accommodate the minimum required headroom on the charger. This method allows for excellent 90% efficient energy transfer from the case battery to the earbud battery without the need to place bulky inductors on the tiny form factor ear buds. The excellent efficiency and extremely low heat generation of this charging system offer an increase in the number of charging cycles that can be supported by the case battery as well as the option to increase the rate of charge and deliver faster recharge times to the end customer.

### Charger Battery Voltage Tracking Loop

Figure 11 shows the structure of the automatic charger battery voltage tracking algorithm. The charger battery voltage tracking algorithm is accomplished with data exchanges initiated by the master and responded to by the slave(s). Once the connection is built between master and slave(s), the master connects the buck-boost regulator to the PLC line and holds PLC voltage to `bb_vlt_def` (3.5V by default) for 100ms. Then pull PLC line to communication voltage (5.5V by default) and starts to PING. The communication voltage is programmable through `bb_vlt_tran`. Slave responds with ACK packet after master sends the first LISTEN command during PING. Slave's ACK packet contains information including slave GPIO status, battery information, charging status, and PLC voltage up/down request. Master adjusts buck-boost output based on the PLC voltage up/down request received from slave(s).

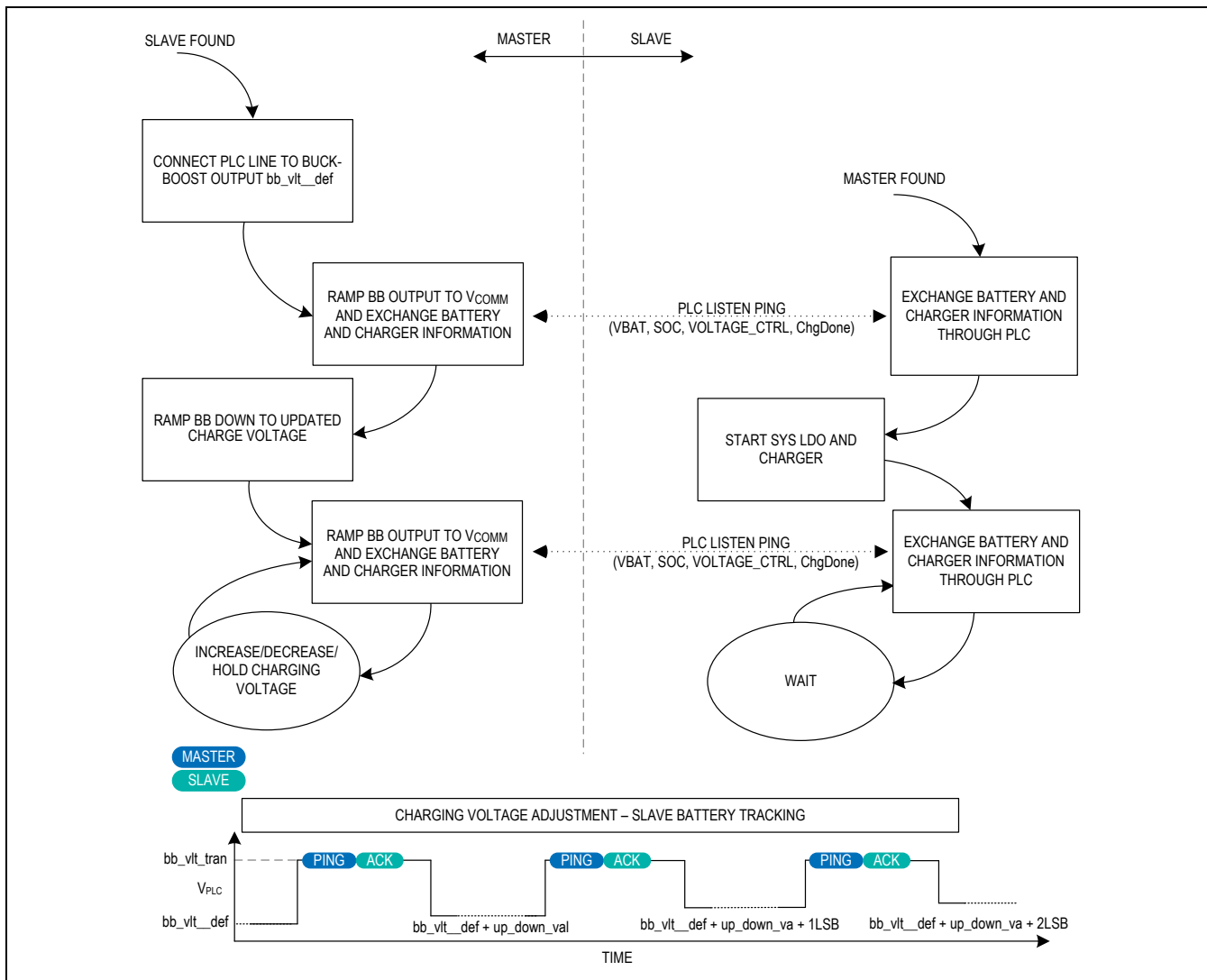


Figure 11. Polling Structure of Automatic Charging Algorithm

Slave compares battery voltage with PLC line voltage. If the PLC input voltage is above the programmed upper threshold (PLC voltage is in decrease zone), the slave sends a “decrease” signal during PING. Similarly, if PLC voltage is below the lower limit (increase zone) or within the limit (hold zone), it sends an “increase” or “hold” signal accordingly. The voltage thresholds are fully programmable through the parameters shown in [Figure 12](#). The minimum step of voltage adjustment is programmable through I<sup>2</sup>C register bits  $up\_down\_val$ .

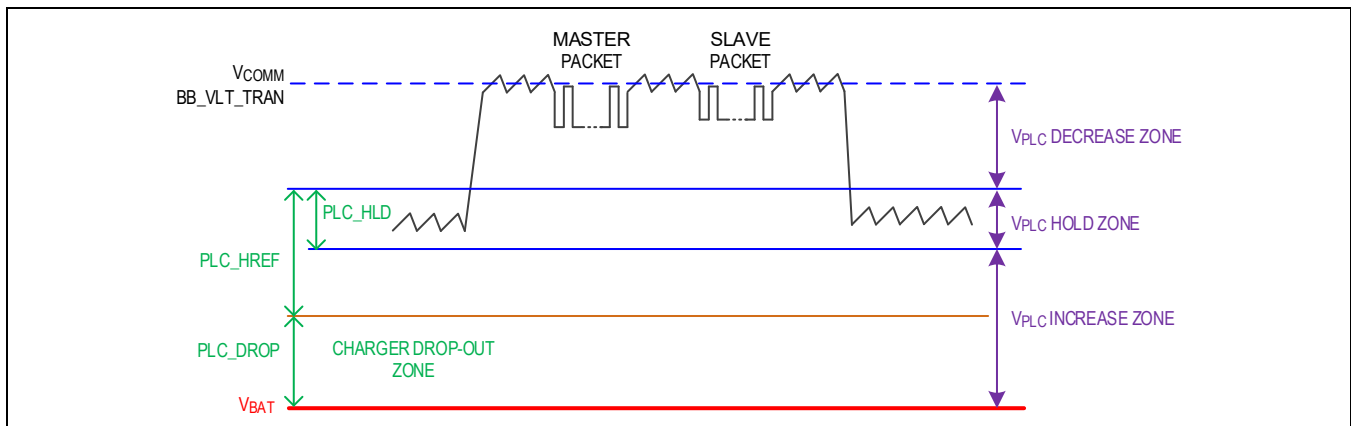


Figure 12. Slave Voltage Control Algorithm

### Ultra-Low Dropout Battery Charger

The battery charger on MAX20357 is a fully featured lithium-ion charger offering I<sup>2</sup>C programmable voltage thresholds through charging phases: precharge voltage VPChg, step charging voltage ChgStepRise, charge termination voltage BatReg, and top off current IChgDone. The MAX20357 also features safety timers, JEITA charging profile with thermistor and overtemperature protection with die temperature sensor. It starts charging from the precharge stage if battery voltage is lower than precharge voltage VPChg. Step charging feature allows higher charge rate at the beginning of the charge cycle during CC1. Once the battery voltage rises to step charge threshold ChgStepRise, the charger transitions to CC2 at a lower charge rate. If the battery voltage is charged up close to BatReg, there are two options to charge in final stage: CC track mode and CV mode. In CC track mode, charger current is regulated and reduced by fixed step as battery charges up. In CV mode, BAT pin voltage is regulated at BatReg and charging current naturally reduces as battery charges up. As shown in [Figure 13](#), in CC track mode, charger current is evaluated roughly every 1.3ms, if charge current hits natural charge current controlled by CV mode (dash line in [Figure 13](#)), the MAX20357 reduces charge current by 1/64 of CC2IFChg. Charger controls current directly in CC track mode, which prevents potential abrupt current change that is common in CV mode. The PLC line is protected from fluctuation of charger current which could lead to communication failure. CC track feature is enabled by default. It is highly recommended to keep the default setting to maintain a clean PLC line for reliable PLC communication.

The charging current options for precharge, CC1 and CC2 can be found in IPChg, CC1IFChg, and CC2IFChg. The voltage threshold from precharge to CC1, from CC1 to CC2, and charge termination voltage can be found in VPChg, ChgStepRise, and BatReg. The top-off current threshold can be found in IChgDone. The step charging profile is shown in [Figure 13](#).

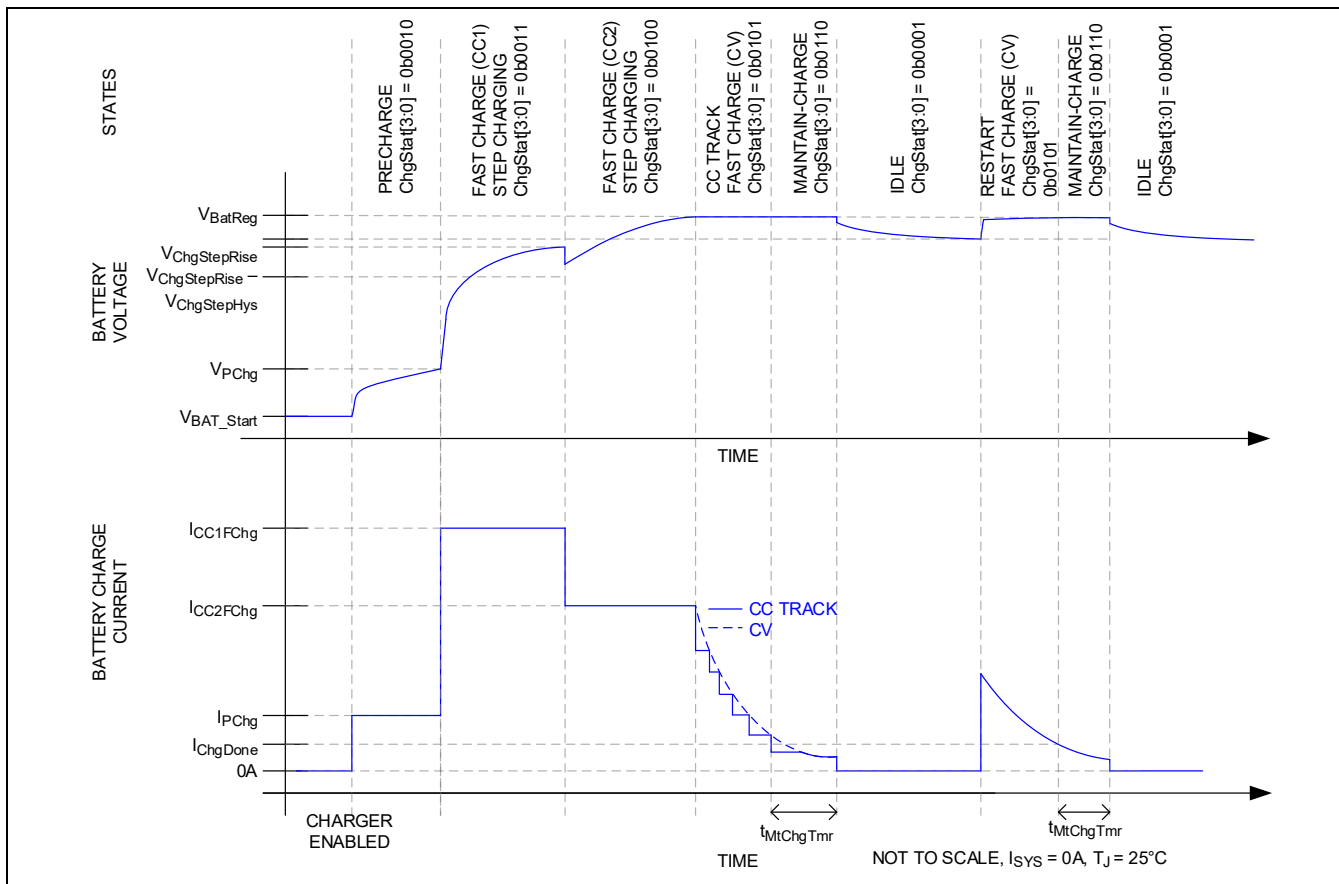


Figure 13. Step Charging Profile

There are also independently programmable temperature thresholds, which allow the user to select in which temperature ranges precharge, CC1, CC2 and battery regulation voltage may operate. Different JEITA compliant temperature operation strategy is I<sup>2</sup>C programmable. Timeout function for precharge, CC1 and full charge cycle is also designed to prevent overcharge of the battery. Detailed charger operation is shown in [Figure 14](#).

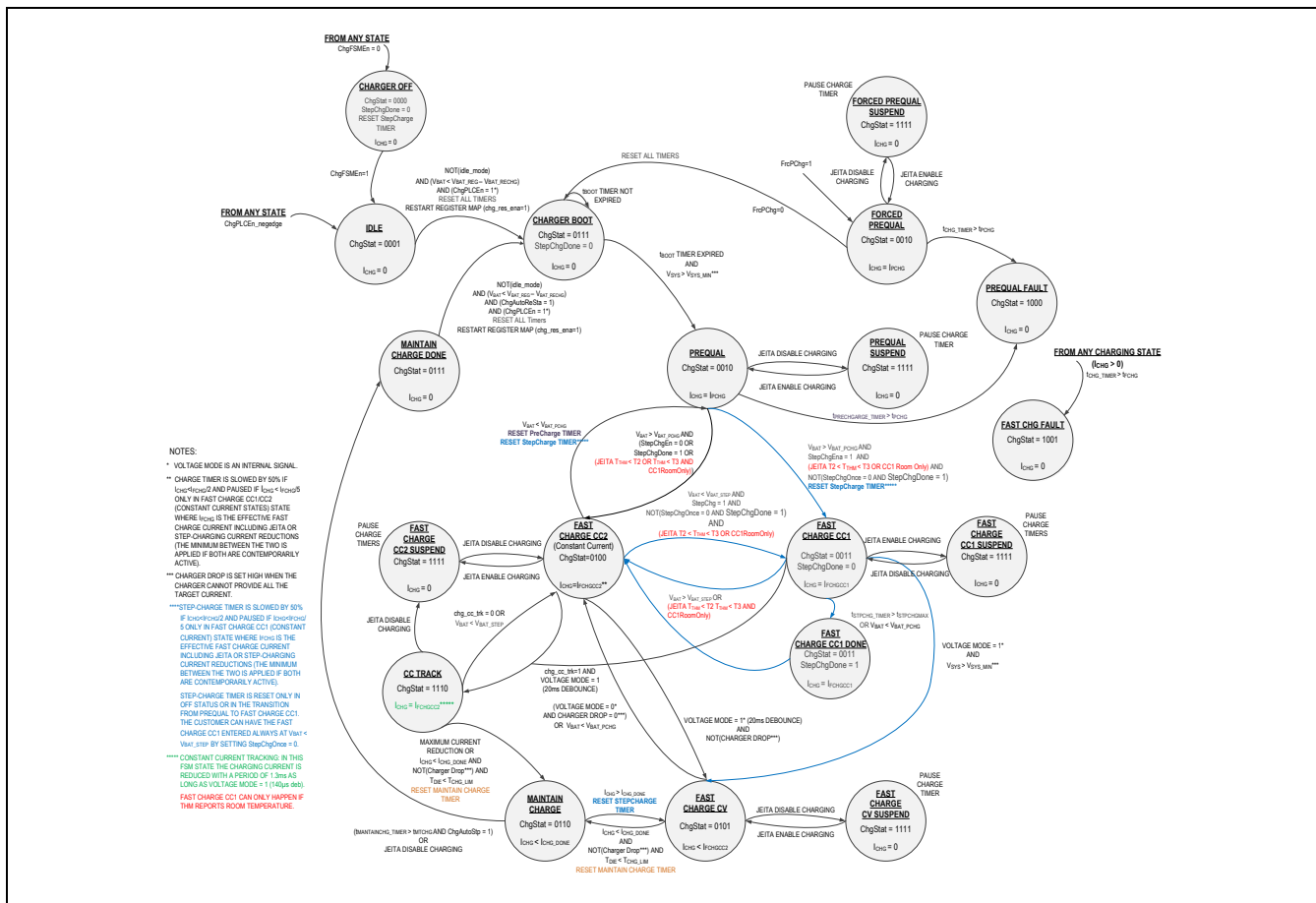


Figure 14. Battery Charger FSM Diagram

### Charger-Off State

As shown in [Figure 14](#), when PLC connection is not established, power is not applied from the MAX20355. The MAX20357 charger is in **Charger Off** state (ChgStat = 0b0000). After MAX20357 detects PLC connection, buck-boost voltage is applied to PLC pin, chn\_con\_sts status is set to 1 and chn\_con\_int interrupt is asserted at the first telemetry PING, signaling PLC connection is established. Charger transitions from **Charger Off** state to **Charger IDLE** state (ChgStat = 0b0001).

### Charger IDLE state

As shown in [Figure 14](#), the following events cause the charger to enter **Charger IDLE** state.

- PLC connection event. The charger transitions from **Charger Off** state to **Charger IDLE** state when the MAX20357 detects a PLC connection event.
- Disable charger when power is applied to PLC pin. If power is applied to PLC pin, the charger enters **Charger IDLE** state when charger is disabled ChgEn = 0.

The charger exits **Charger IDLE** state and starts boot sequence when all the following conditions are met:

- System is not in PLC IDLE mode. System could be put into PLC IDLE mode to reduce power dissipation after earbud battery is fully charged. In PLC IDLE mode, if charger is enabled ChgEn = 1 and charger auto-restart is enabled (ChgAutoReSta = 1), the system resumes from PLC IDLE mode automatically when battery voltage drops below recharge threshold  $BatReg - BatReChg$ .
- Charger is enabled ChgEn = 1.
- Battery voltage  $< BatReg - BatReChg$  (recharge threshold).

When the charger enters **Charger Boot** state, all charger timers reset. If `chg_res_ena = 1`, charger resets all charger-related registers when it goes through boot sequence.

### Charger IDLE state

As shown in [Figure 14](#), the following events cause the charger to enter **Charger IDLE** state.

- PLC connection event. The charger transitions from **Charger Off** state to **Charger IDLE** state when the MAX20357 detects a PLC connection event.
- Disable charger when power is applied to PLC pin. If power is applied to PLC pin, the charger enters **Charger IDLE** state when charger is disabled `ChgEn = 0`.

The charger exits **Charger IDLE** state and starts boot sequence when all the following conditions are met:

- System is not in PLC IDLE mode. System could be put into PLC IDLE mode to reduce power dissipation after earbud battery is fully charged. In PLC IDLE mode, if charger is enabled `ChgEn = 1` and charger auto-restart is enabled (`ChgAutoReSta = 1`), the system resumes from PLC IDLE mode automatically when battery voltage drops below recharge threshold `BatReg – BatReChg`.
- Charger is enabled `ChgEn = 1`.
- Battery voltage < `BatReg – BatReChg` (recharge threshold) or `skipCRFStart` is set to 1.

When the charger enters **Charger Boot** state, all charger timers reset. If `chg_res_ena = 1`, charger resets all charger-related registers when it goes through boot sequence.

### Precharge State

As shown in [Figure 14](#), the charger enters the precharge state (`ChgStat = 0b0010`) after charger boot sequence is completed and SYS pin voltage is regulated higher than or equal to minimum system voltage `SysMin`. If battery voltage is lower than `VPChg` or `FrcPChg = 1`, the charger remains in precharge state. In the precharge state, the battery charging current is `IPChg`.

The following events cause the charger to exit precharge state:

- Battery voltage rises above `VPChg`. If step-charging is enabled `CC1Enable = 1`, `CC1` is not configured to run at room temperature only `CC1RoomOnly = 0`, or `CC1` is configured to run at room temperature only `CC1RoomOnly = 1` and the thermistor monitoring reports room temperature, the charger enters **Fast-Charge Constant Current Mode 1** (`CC1`) state. By default, step-charging is enabled `CC1Enable = 1` and `CC1` is configured to run at any temperature `CC1RoomOnly = 0`.
- Battery voltage rises above `VPChg`. If step-charging is disabled `CC1Enable = 0`, or `CC1Enable = 1` and `CC1` is configured to run at room temperature only `CC1RoomOnly = 1` but battery is in cool or warm temperature zone, the charger enters **Fast-Charge Constant Current Mode 2** (`CC2`) state.
- Precharge timeout. If the charger remains in this state for longer than the charger precharge timer `PChgTmr`, the charger enters **Charger Fault-Precharge Timer PChgTmr Expired** state (`ChgStat = 0b1000`) and suspends charging.
- Charger safety timeout. If the charger safety timer `ChgTmr` expires while in precharge state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (`ChgStat = 0b1001`) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the [JEITA compliance](#) section for detailed description.
- Forced precharge. Charger can be forced to operate with precharge current `IPChg` in **Force precharge** state by setting `FrcPChg = 1`. The charger transitions to the charger boot sequence when disable forced precharge `FrcPChg = 0`.

### Fast-Charge Constant Current CC1 State

Once the battery voltage rises above precharge threshold `VPChg`, the charger allows a higher charge rate `CC1IFChg` at the beginning of the charge cycle during **Fast-Charge Constant Current Mode 1** (`CC1`) state. Set register bit `CC1Enable = 0` to disable the Step-charging feature, and the Charger transits from **precharge** state directly to **CC2** state. In the JEITA compliant thermistor temperature monitoring control, `CC1` can be configured to run at room temperature only by setting `CC1RoomOnly = 1`. In **CC1** state, charge current is regulated less than or equal to `CC1FChg`. See the [Reduced Charge Current](#) section for reasons that charge current may be less than `CC1IFChg`.

The following events cause the charger state machine to exit **CC1** state:

- Battery voltage rises to `ChgStepRise`. The charger enters **CC2** state.

- Battery voltage drops below VPChg. The charger goes through **Fast-Charge CC1 Done, CC2 state** and eventually goes back to **precharge** state. During this process, charge marks internal signal StepChgDone = 1. If battery voltage rises above VPChg again, it skips **CC1** state to protect battery.
- CC1 timeout. If the step-charge timer is enabled CC1TmoLimit = 1 and charger remains in this state for longer than CC1FChgTmr, it enters **CC2** state.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC1** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- Temperature measured from THM is out of room temperature zone and CC1 is allowed to operate in room temperature only. If CC1RoomOnly = 1 and the battery temperature transitions from Room to Cool or Warm, the charger enters **CC2** state.
- JEITA disable charging. The charger suspends charging due to temperature. See the [JEITA compliance](#) section for detailed description.

The battery charger dissipates the most power in the fast-charge constant current mode, which causes the die temperature to rise. If the die temperature approaches ChgThrmLim = 115°C, see the [Thermal Regulation](#) section for charger operation details.

### Fast-Charge Constant Current (CC2) State

The step-charge feature is enabled by default on the MAX20357. Once the battery voltage rises above step-charge threshold ChgStepRise, the charger enters **Fast-Charge Constant Current Mode 2 (CC2)** state with a lower charge rate CC2IFChg in order to avoid lithium plating and prolong the lifetime of the battery. ChgStepHys field sets the hysteresis for the step charge function to avoid hopping between **CC1** state and **CC2** state caused by high voltage drop from current reduction. In **CC2** state, charge current is regulated less than or equal to CC2IFChg. See the [Reduced Charge Current](#) section for reasons that charge current may be less than CC2IFChg.

The following events cause the charger state machine to exit **CC2** state:

- Battery voltage rises to BatReg. CC Track is enabled by default chg\_cc\_trk = 1, the charger enters **CC Track** state. If CC Track is disabled chg\_cc\_trk = 0, the charger enters **Fast-Charge Constant Voltage (CV)** state. It is highly recommended to keep CC Track enabled for better performance.
- Battery voltage drops below ChgStepRise – ChgStepHys. Charger goes back to **CC1** state.
- Battery voltage drops below VPChg. Charger goes back to **Precharge** state.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC2** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The Charger suspends charging due to temperature. See the [JEITA compliance](#) section for detailed description.

Pogo pin resistance may impose limit on maximum allowed step-charge threshold and CC2 charging current at termination voltage BatReg in order to prevent PLC communication failure.

### Constant Current Tracking State CC Track

The charger enters **Constant Current Tracking (CC Track)** state when the battery voltage is close to termination voltage BatReg if CC track is enabled chg\_cc\_trk = 1. In **CC Track** state, charger current is evaluated roughly every 1.3ms. If charge current hits the CV mode charger current at the same battery voltage, charger reduce charge current by one fixed step 1/64 of CC2IFChg as shown in [Figure 13](#). Charge current is reduced with controlled steps until charge current is less than termination current threshold IChgDone.

The following events cause the charger state machine to exit **CC Track** mode:

- Maximum charger current reduction is reached (charger current is reduced to 0.2 x CC2IFChg) or charger current is reduced below IChgDone, and charger is not in any current reduction mode. The charger enters **Maintain Charge** state and starts Maintain Charge timer.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in **CC Track** state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The Charger suspends charging due to temperature. See the [JEITA compliance](#) section for detailed description.



- **CC Track** state maintains a clean PLC line for data transfer and keeps battery voltage below regulation point in the meantime. By default, CC track is enabled. It is highly recommended to use this feature for more reliable PLC communication when earbud battery voltage is near fully charged.

#### Fast-Charge Constant Voltage (CV) State

As shown in [Figure 14](#), if CC track is disabled, charger enters **Fast-Charge Constant Voltage (CV)** state when the battery voltage is close to top-off voltage BatReg. In the **CV** state, the charger regulates the battery voltage at BatReg and the charge current decreases from CC2IFChg as the battery voltage increases. Battery regulation voltage can be less than BatReg due to temperature. See the [JEITA Compliance](#) section for JEITA reduction of battery regulation voltage.

The following events cause the charger state machine to exit **CV** state:

- Charge current drops below IChgDone and charger is not in any current reduction mode, it enters **Maintain Charge** state and starts Maintain Charge timer MtChgTmr.
- Charger safety timeout. If the charger safety timer ChgTmr expires while in CV state, the charger enters **Charger Fault-Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and suspends charging.
- JEITA disable charging. The charger suspends charging due to temperature. See the [JEITA compliance](#) section for detailed description.
- Battery voltage drops. Reduced battery voltage does not directly lead to **CV** state exit. As battery voltage drops, charge current keep increasing. The charger enters **CC2** state when charge current hits CC2IFChg.

In **CV** mode, there might be transient in charger current in order to regulate battery voltage, especially during telemetry PING. This current transient is present on PLC line and could lead to potential PLC communication failure. It is recommended to use **CC track** mode during this charging phase.

#### Maintain Charge State

Charger enters **Maintain Charge** state from the **CC Track** state or **CV** state when the charge current drops below IChgDone. In **Maintain Charge** state, the charger regulates the battery voltage at BatReg and starts Maintain Charge timer. The charge current is equal or lower than IChgDone. The charge current keeps decreasing in **Maintain Charge** state while the battery voltage is regulated at BatReg.

The following events cause the charger state machine to exit Maintain Charge state:

- If charger auto-stop is enabled (ChgAutoStop=1) and the maintain charge timer MtChgTmr expires, the charger enters Maintain Charge Timer Done state and stops charging.
- If charge current rises above IChgDone, charger goes back to **CV** state and reset the step charge timer CC1FChgTmr.
- JEITA disable charging. The Charger suspends charging due to temperature and enters **Maintain Charge Timer Done** state. See [JEITA compliance](#) section for detailed description.

If charger auto-stop is disabled (ChgAutoStop = 0), charger ignores maintain charger timer and stays in **Maintain Charge** state even if charger current drops below IChgDone. When the charger transitions in and out of **Maintain Charge** state, charger safety timer does not reset. Only local timer resets. If charger enters **Maintain Charge** state, maintain charge timer MtChgTmr resets and starts counting. If charger exits **Maintain Charge** state and enters **CV** state, step charge timer CC1IFChgTmr resets.

#### Maintain Charge Timer Done State

Charger enters **Maintain Charge Timer Done** state from **Maintain Charge** state after the Maintain Charge timer MtChgTmr is expired and charger auto-stop enabled ChgAutoStop = 1 or when JEITA suspends charging. In **Maintain Charge Timer Done** state, charger stops charging. If charger is enabled ChgEn = 1 and the charger auto-restart is enabled ChgAutoReSta = 1, the charger exits **Maintain Charge Timer Done** state and resumes charging once the battery voltage falls below recharge threshold BatReg - BatReChg. If the charger auto-restart is enabled ChgAutoReSta = 1 and the system is placed in PLC IDLE mode after earbud battery is fully charged, the MAX20357 automatically exits PLC IDLE mode and resumes charging once the battery voltage falls below recharge threshold BatReg - BatReChg.

#### Charger Timers

The battery charger provides a global charger safety timer ChgTmr and three local timers, precharge timer PChgTmr, step-charge timer CC1FChgTmr, and maintain charge timer MtChgTmr to ensure safe charging. These timers prevent the battery from being overcharged.

The safety timer ChgTmr runs through all charging states that have non-zero charger current, including **Precharge**, **CC1**, **CC2**, **CC Track**, **CV**, and **Maintain Charge**. When charger safety timer ChgTmr expires, charger enters **Charger Fault - Safety Timer ChgTmr Expired** state (ChgStat = 0b1001) and stops charging.

Precharge timer PChgTmr runs in Precharge state. Precharge timer PChgTmr resets when charger enters **Precharge** state, except from JEITA suspend charging state (ChgStat = 0b1111). When precharge timer PChgTmr expires, the charger enters **Charger Fault - PChgTmr Expired** state (ChgStat = 0b1000) and stops charging.

The charger can exit safety timer fault or precharge timer fault state by toggling ChgEn, soft reset or removal and re-connection of PLC. When charger enters **Charger Off** state (ChgStat = 0b0000) or **Charger IDLE** state (ChgStat = 0b0001) by the above behavior, charger can exit from charger fault state.

Step-charge timer CC1FChgTmr runs in **CC1** state. The step-charge timeout does not lead to any fault state. When it expires, charger is forced to enter CC2 state. Step-charge timer CC1FChgTmr resets when the charger enters **CC1** state from **Precharge** state, or when the charger goes from **Maintain Charge** state to **CV** state. Due to battery internal resistance and cable/PCB trace resistance, it is common that battery voltage detected from BAT pin drops when charger goes from **CC1** to **CC2** state. It is caused by reduced charge current from CC1FChg to CC2FChg. If charger enters **CC2** due to step-charge timeout, even if battery voltage detected from BAT pin drops below step-charge threshold ChgStepRise - ChgStepHys, it stays in **CC2** state. StepChgDone is reset to 0 when the charger enters charger boot sequence.

In **CC1** state, **CC2** state and **CC Track** state, both the local step-charge timer CC1FChgTmr (in CC1 state) and the global charger safety timer ChgTmr are slowed by 50% the fast-charge current is reduced to be between 20% and 50% of CC1/CC2 charge current. These two timers are paused when the fast-charge current is reduced to be below 20% of CC1/CC2 charge current. Note the slowdown of the above timers applies to any type of fast-charge current reduction, see the [Reduced Charge Current](#) section.

### Reduced Charge Current

Charger current can be less than the programmed value (IPChg, CC1FChg, CC2FChg) for any of the following reasons:

- JEITA controlled fast-charging current (CC1FChg, CC2FChg). When thermistor monitoring is enabled and the fast-charging current in cool, room, or warm temperature zone is programmed to be lower than  $1 \times \text{CC1FChg}/\text{CC2FChg}$ .
- The SYS LDO is enabled, and the PLC current limit is reached. The charge current is reduced in favor of the system load. System load always gets priority over the charger current.
- The SYS LDO is disabled, but the PLC current limit is lower than the programmed charger current. The charger current is regulated at the PLC current limit.
- The charger is under thermal regulation, see the [Thermal Regulation](#) section.

If the charger drop-out voltage drops down to the programmable threshold PLC\_DROP, charger current is actively reduced to maintain the charger input and output voltage difference  $V_{\text{PLC}} - V_{\text{BAT}}$  at PLC\_DROP. As shown in [Figure 14](#), when charger current is being actively reduced, some charger state transitions are unavailable.

### JEITA Compliance

To enhance safety when charging Li+ batteries, the MAX20357 features JEITA compliant temperature monitoring. Temperature measurement using an external NTC thermistor places the battery into one of five temperature zones: cold, cool, room, warm, and hot. When JEITA compliant thermistor monitoring is enabled, charging is always inhibited in cold and hot regions or if the thermistor cannot be detected. Charging behavior is configurable in warm, room, and cool regions using the I<sup>2</sup>C-controlled ThmEn parameter, as demonstrated in [Figure 15](#) – [Figure 18](#). Maintain charge state (ChgStat = 0b0110) only runs in room temperature zone when thermistor monitoring is enabled.

CC1 state has its dedicated I<sup>2</sup>C programmed temperature thresholds, which can be configured using the ChgT1ThrCC1-ChgT4ThrCC1. I<sup>2</sup>C-programmed temperature thresholds of precharge state, CC2 state, CC Track state and CV state can be configured using ChgT1ThrDef-ChgT4ThrDef. JEITA current control strategy in cool, room, and warm zone is programmable with the ThmCfg0-ThmCfg2 as shown in [Figure 15](#) – [Figure 18](#).

Note that JEITA measurements are continuous only if PLC is present. If PLC is not present and ThmEn setting is higher than 0x3, JEITA measurement is performed based on ModelGauge m5 EZ measurements at a maximum rate set by jta\_eoc\_sel.

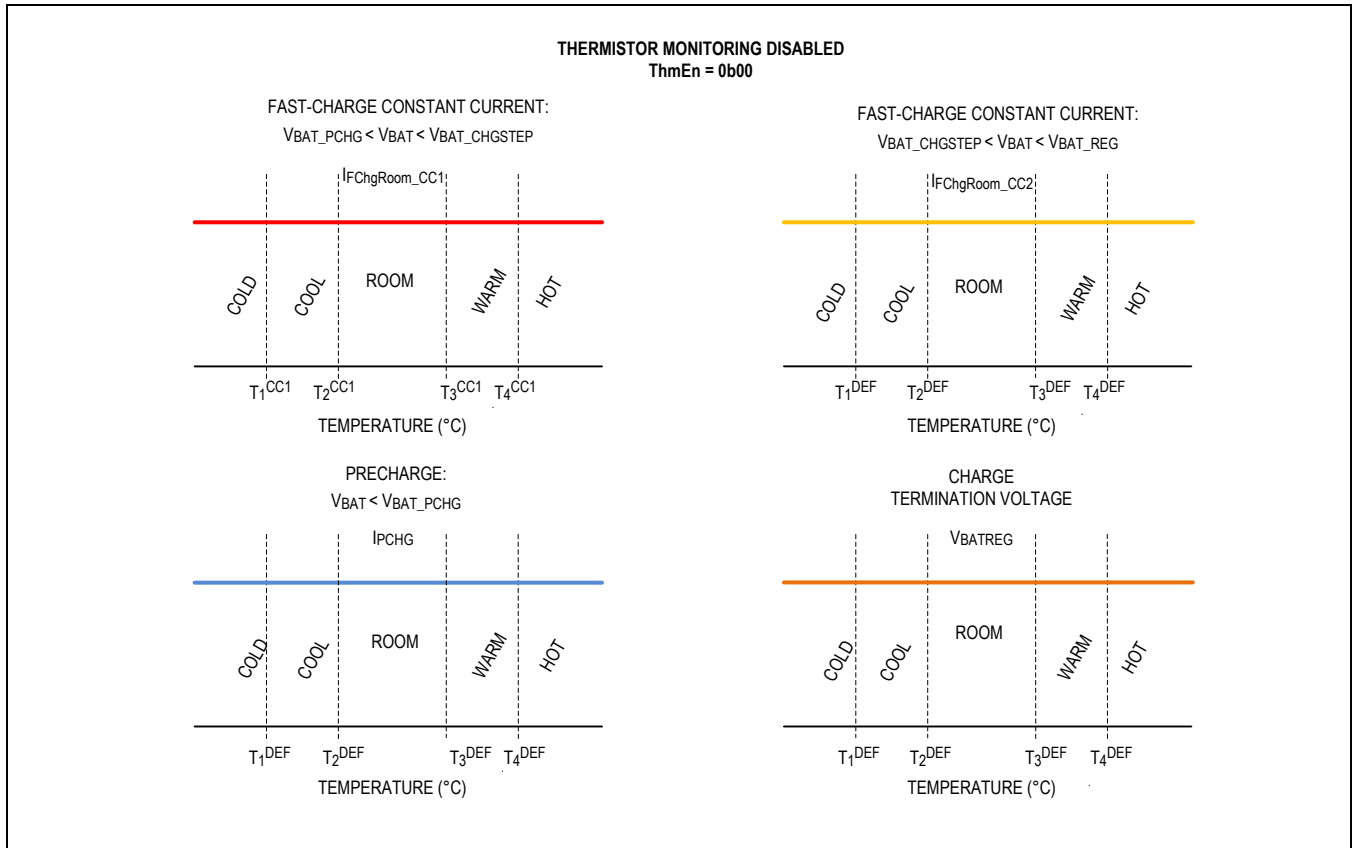


Figure 15. Temperature Monitoring Disabled

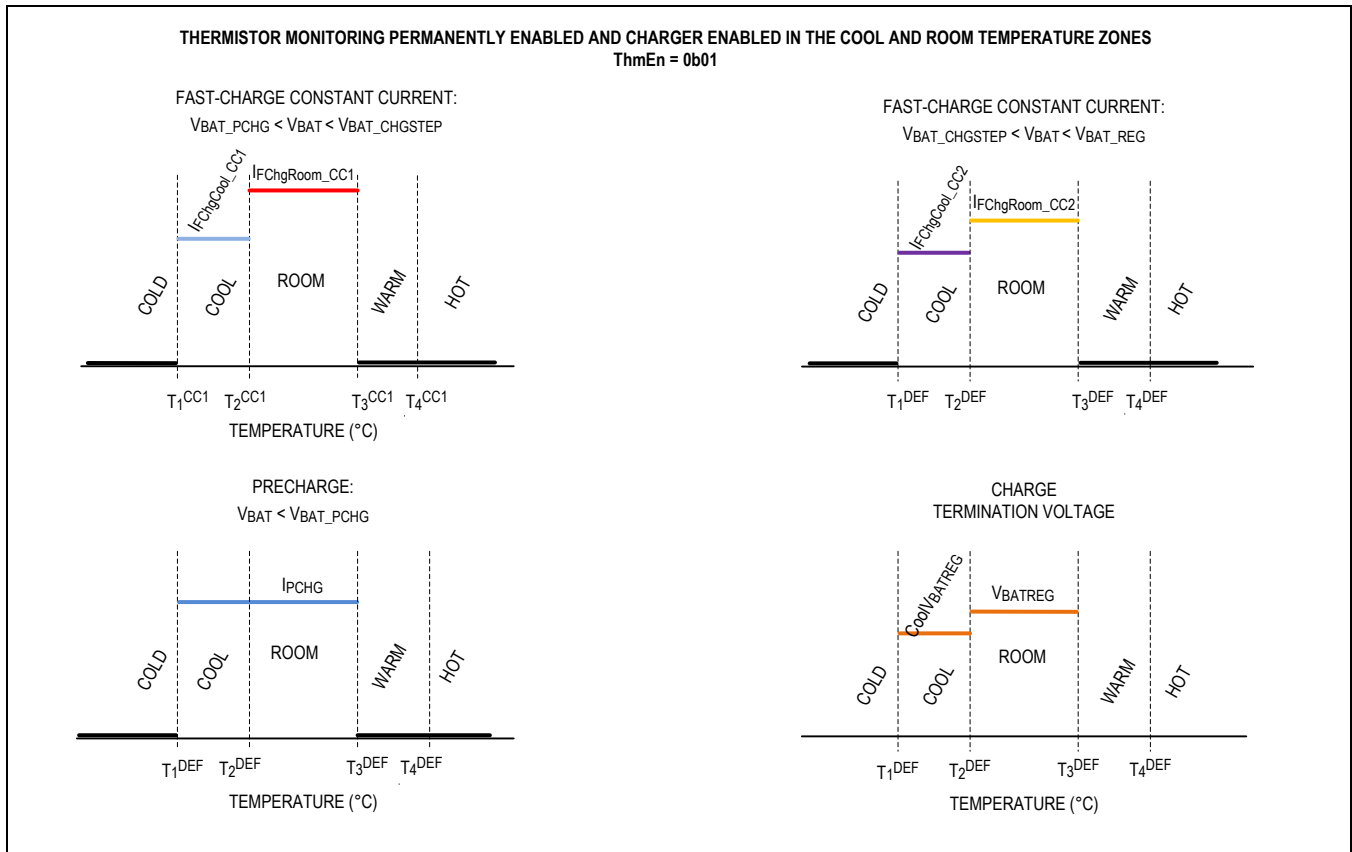


Figure 16. Charging Enabled in Cool and Room Regions

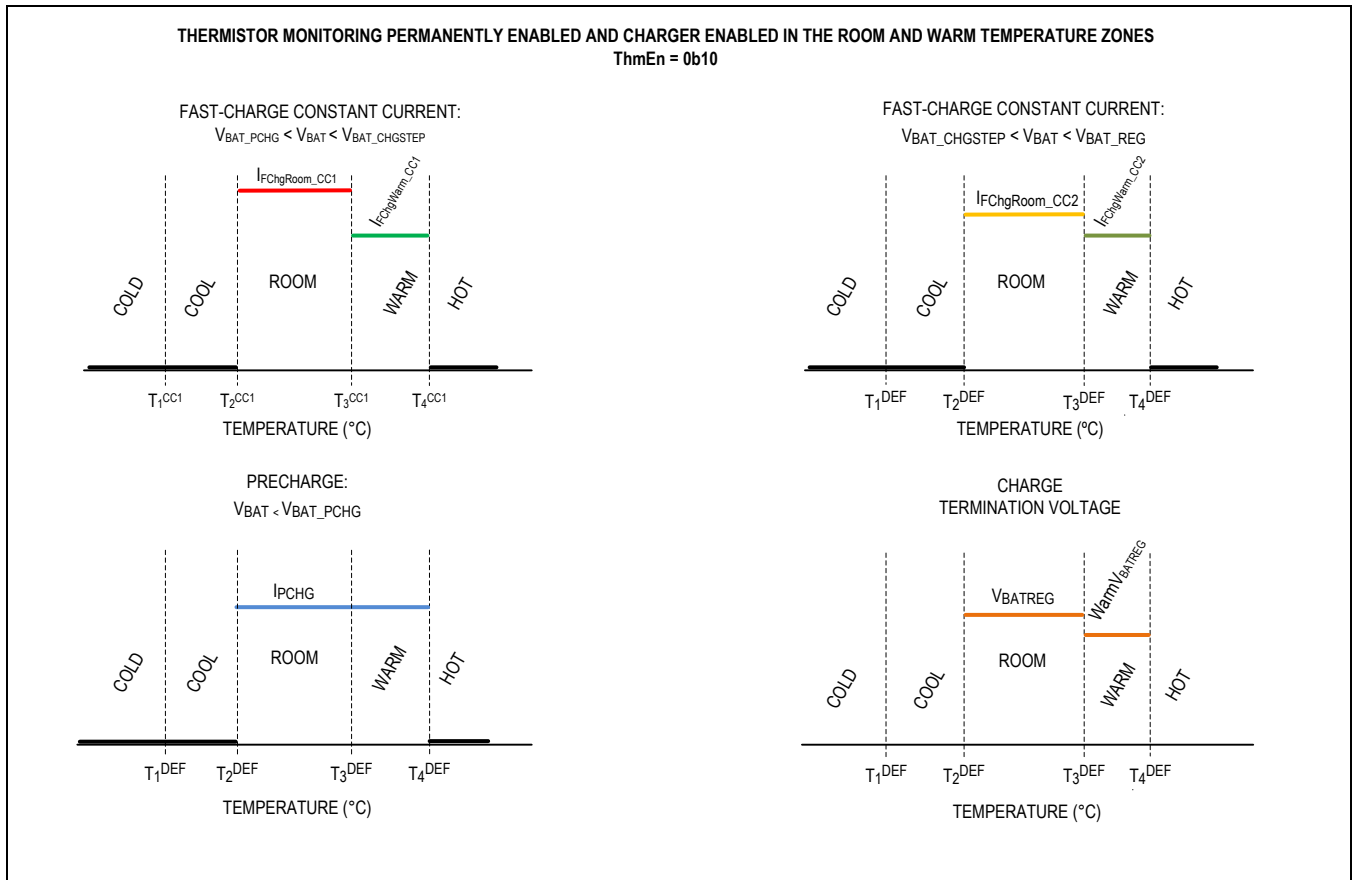


Figure 17. Charging Enabled in Room and Warm Regions

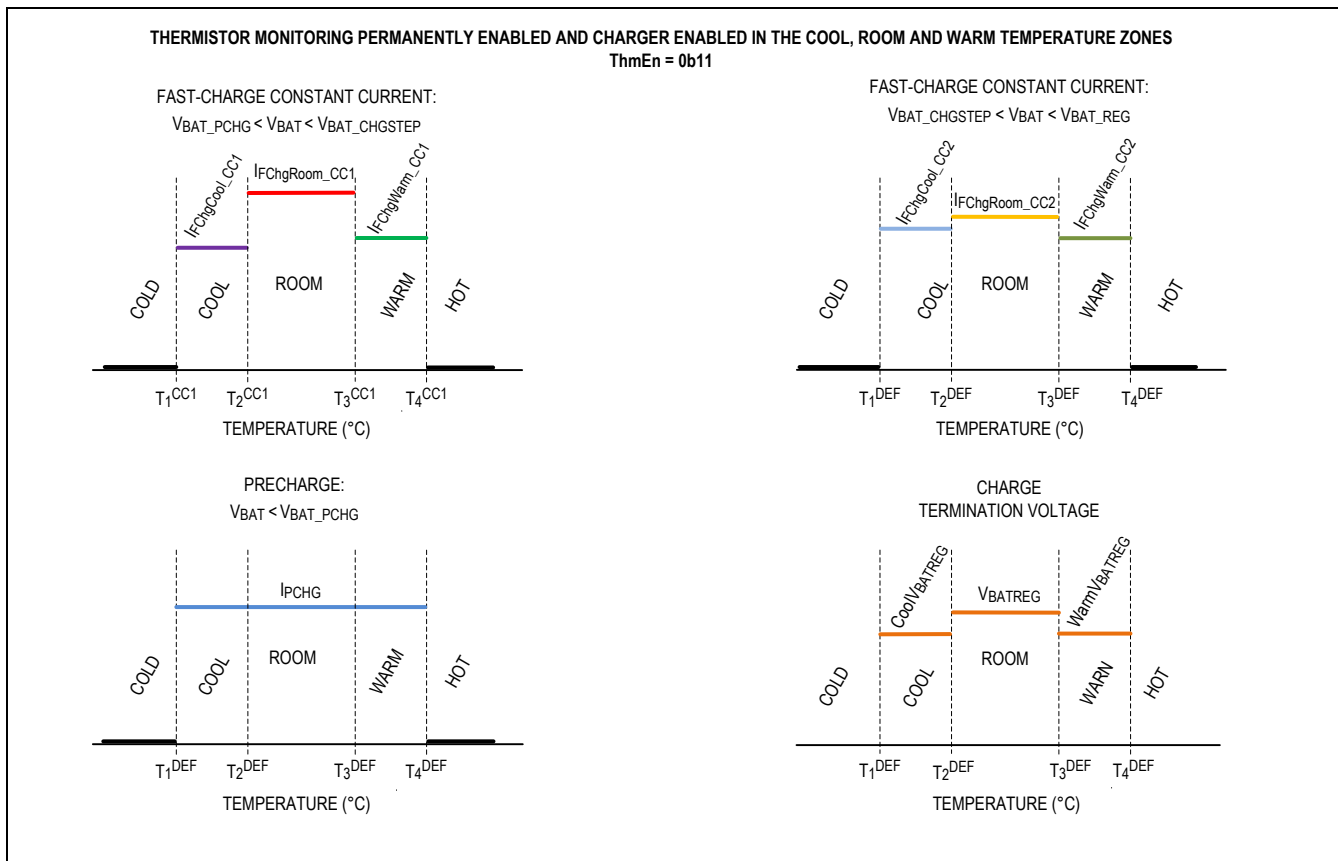


Figure 18. Charging Enabled in Cool Room and Warm Regions

### Thermal Regulation

In addition to PLC input current limit, the MAX20357 features thermal charge current regulation. This circuit acts to reduce charge current when the die temperature reaches a programmed thermal limit  $T_{SHDN\_PLC} - 3^{\circ}\text{C}$ , preventing further temperature increase.  $T_{SHDN\_PLC}$  is I<sup>2</sup>C programmable through ChgThrmLim. If the SYS LDO is enabled, the thermal regulation loop first reduces charge current in favor of the SYS load. As the charge current is reduced to zero, the charger is off. If the die temperature continues to increase, the thermal regulation loop reduces SYS LDO current, and the system load is supplemented by the battery. ChgThrmReg and its corresponding interrupt indicate if charger is under thermal regulation. If current is reduced to 0 but temperature still hits  $T_{SHDN\_PLC}$ , the MAX20357 enters thermal shutdown mode, waiting for temperature to drop below the threshold. The MAX20357 resumes operation once the temperature drops below thermal threshold. Note that all the registers reset to default when the MAX20357 goes out from thermal shutdown. This feature is designed to provide second overheating protection for earbud in addition to JEITA current operation.

## SYS LDO and Power Path

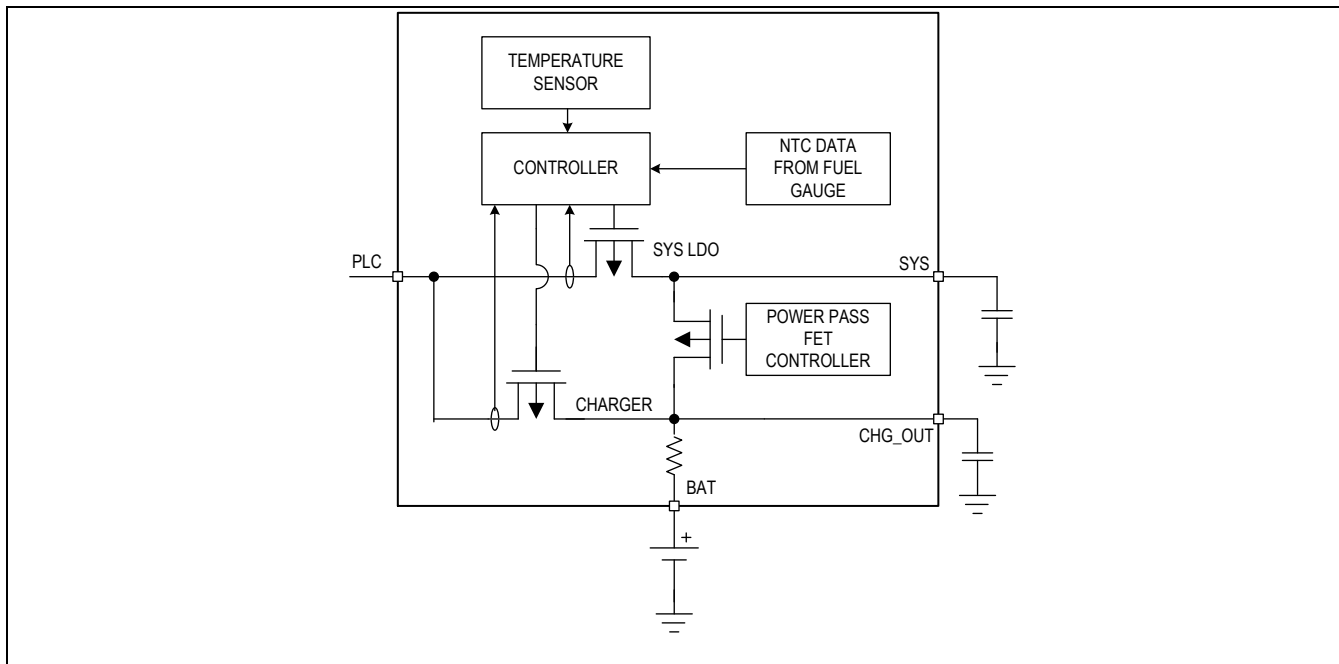


Figure 19. Input Limiter, Power Path, and Charger Block Diagram

### SYS LDO Default Mode

After power on reset, SYS LDO delivers power to the SYS output from the PLC line. When PLC is present, the SYS LDO output voltage reference is set based on the following rule:

$$V_{SYS} = \text{MAX}(V_{BAT}, \text{SysMin})$$

If  $V_{BAT}$  is lower than minimum system voltage  $\text{SysMin}$ , SYS LDO regulates SYS voltage at  $\text{SysMin}$  to maintain a constant supply voltage to prevent the earbud SoC from UVLO. If  $V_{BAT}$  is higher than minimum system voltage  $\text{SysMin}$ , the SYS LDO works in parallel with the charger by default and regulates  $V_{SYS} = V_{BAT}$ .

It should be noted that SYS LDO also decouples the SYS capacitance from the PLC line. On PLC pin, no capacitance should be attached in order to allow full data rate communication.

### SYS LDO Bypass Mode

As illustrated in the previous sections, PLC line is sensitive to load change, which may cause abrupt voltage change and corrupt PING packet. The MAX20357 features to bypass SYS LDO and support any transient load directly from the battery. When PLC is present, set  $\text{SysMinForce} = 1$  to force the SYS LDO to regulate  $V_{SYS} = \text{SysMin}$ . The SYS pin voltage is regulated based on the following rule:

$$V_{SYS} = \text{MAX}(V_{BAT} - \text{PP\_drp}, \text{SysMin})$$

When the battery voltage is sufficiently higher than minimum system voltage  $\text{SysMin}$  ( $V_{BAT} - \text{PP\_drp} > \text{SysMin}$ ), the power path FET is turned on and battery to SYS voltage drop is regulated to the programmable value  $\text{PP\_drp}$ . The SYS LDO attempts to regulate  $V_{SYS} = \text{SysMin}$ . However, due to the power path,  $V_{SYS}$  is clamped at  $\text{PP\_drp}$  lower than battery voltage, which is higher than  $\text{SysMin}$ . SYS LDO eventually turns off. All system load is supplied by battery. The PLC line current is regulated by the charger constant current control loop. PLC line is protected from any significant fluctuation caused by system load transient. To achieve reliable PLC communication and maintain a clean PLC channel, it is highly recommended to set  $\text{SysMinForce} = 1$  when the battery voltage is sufficiently higher than  $\text{SysMin}$ . When battery voltage is not sufficiently higher than  $\text{SysMin}$  ( $V_{BAT} - \text{PP\_drp} < \text{SysMin}$ ), power path is open and the SYS LDO regulates  $V_{SYS}$

= SysMin. System load is supplied from the PLC line. System designer needs to avoid applying any transient load during PLC PING since it may cause PLC communication failure and disconnection of PLC.

### Battery Only Mode

When the PLC is not present and the battery is alive, the power path FET is fully ON and the system load is supplied by the battery.

### Reverse Protection

The SYS LDO and the charger feature reverse protection preventing reverse conduction when  $V_{SYS}$  or  $V_{BAT}$  is higher than the PLC charging voltage. When the voltage difference between the two earbud batteries is large, and the minimum algorithm is elected in the MAX20355, PLC charging voltage is adjusted to track the lower earbud battery of the two. In the earbud with the higher battery voltage,  $V_{SYS}$  and  $V_{BAT}$  are higher than PLC charging voltage. In this condition, the SYS LDO and the charger are in reverse protection and current is not back driving PLC line. During reverse protection, the MAX20355 and MAX20357 are still exchanging battery voltage and SOC information through telemetry PINGs. The reverse protection feature allows the MAX20355 to track either battery without concern of back driving the PLC line.

### Mono-slave and Dual-slave Mode

The MAX20357 supports dual-slave mode to connect to PLC1 or PLC2 on the MAX20355, or mono-slave mode if PLC1 and PLC2 on MAX20355 are shorted. PLC input current upper limit is programmable through PLCCurr with maximum value of 200mA or 400mA depending on the state of the lchg\_x2 bit. The function lchg\_x2 bit is summarized as follows:

1. lchg\_x2 = 0. In dual-slave mode, PLC input current limit is set to operate in the range up to 200mA, SYS LDO output current and the charger current are both limited to PLCCurr, up to 200mA.
2. lchg\_x2 = 1. When PLC1 and PLC2 of the MAX20355 are shorted in mono-slave mode, lchg\_x2 can be set to 1 to double the PLC input current PLCCurr to 400mA. SYS LDO output current is limited by PLCCurr, up to 200mA. Charge current is limited by 2xPLCCurr, up to 400mA.

By setting lchg\_x2 to 1, the MAX20357 doubles PLC current limit PLCCurr and charger current CC1IFChg/CC2IFChg. The MAX20357 achieves up to 400mA charge current in mono-slave mode. Note that since the MAX20355 needs to short PLC1 and PLC2, it may cause current imbalance between two channels (Refer to the MAX20355 data sheet for detailed description). The PLC solution does not support to toggle between mono-slave and dual-slave mode during operation. Once the system is configured to mono-slave mode, PLC current sink PLCSnkSel and PLC voltage threshold PLCThrSel on both MAX20355 and MAX20357 are doubled automatically to compensate for higher buck-boost output voltage ripple created by PLC1 and PLC2 tied together.

### Battery Presence Detection

When pack protectors open due to a discharge-related fault, the pack protector turns off the discharge FET, placing a reverse-biased body diode in the discharge path and preventing further discharge. In this state, the system designer can decide that the battery has been damaged and that they would like to prevent a full charge cycle in the future. Even if the system designer does decide that the battery can be recovered, they can have concerns that the diode drop of the pack protector can cause the charger to believe that the battery is above the precharge voltage threshold, which would mean that the fast-charge current is applied.

In this scenario, it is useful for the system to understand before starting a full charge cycle whether a pack is present on the BAT node (with an open protector) or if the battery has simply been removed. The MAX20357 contains all of the necessary circuitry to allow the system designer to implement such a check.

One example of a simple algorithm to check for such a condition is to run the below check every time before starting a battery charging cycle:

1. Before enabling the charger, set BattPullDown = 1 to enable the pulldown resistor on the BAT node and monitor BatUVLOB status bit. This pulldown resistor discharges the capacitance on the BAT node in case the battery is not present or the pack protector is open. After some time, check BatUVLOB status and disable the BAT pulldown resistor. If BatUVLOB = 1 ( $V_{BAT} > BAT\_UVLO$ ), then the battery is present, and charging can be enabled. If BatUVLOB = 0, the BAT voltage is below the UVLO threshold. There are two possibilities for BatUVLOB = 0:
  - a. The battery is not present.
  - b. The pack protector is open.



2. To distinguish between the above two possibilities, set  $FrcPChg = 1$  and  $ChgEn = 1$  to enable charging and force the charger to operate in the Precharge state ( $ChgStat = 0b0010$ ) and monitor  $ChgVoltMode$  status bit. Such charging current and duration can close the pack protector if there is a battery present. After some time, if  $ChgVoltMode = 0$  ( $V_{BAT} < V_{BAT\_REG}$ ), this indicates that the pack protector is closed, and the battery is sinking the precharge current  $IPChg$ . Set  $FrcPChg = 0$  to disable force precharge and the charger enters the normal charging states determined by the battery voltage. If  $ChgVoltMode = 1$  ( $V_{BAT} \geq V_{BAT\_REG}$ ), set  $FrcPChg = 0$  and  $ChgEn = 0$  to disable charging. There are two possibilities for  $ChgVoltMode = 1$ :
  - a. The battery is not present. The precharge current  $IPChg$  quickly charges the capacitance at the  $CHG\_OUT$  node.
  - b. The battery is present and the forced precharge current  $IPChg$  closes the pack protector. However, the battery voltage is higher than termination voltage  $BatReg$ . Repeat step 1, if  $BatUVLOB = 1$ , this indicates the battery is present as the pack protector has closed and  $V_{BAT} > BAT\_UVLO$ .

Note that if the  $ChgGMD = 1$  ( $V_{PLC} - V_{BAT} < PLC\_DROP$ ), the battery presence detection mentioned above is not reliable as the limiter is not allowing the charger to force any current into the  $BAT$  node.

If THM pin is connected to the thermistor inside the battery pack, battery insertion/removal detection can also be reported by the integrated fuel gauge. If THM pin is connected to the thermistor on the PCB, use the procedure mentioned above to detect battery presence.

### PLC Operation Modes

The MAX20357 features multiple modes of operation that are designed to minimize power consumption in the end user's application. The transitions between modes and general operation are shown in [Figure 21](#). Behavior of main functional blocks in SEAL mode, OFF mode, and SYSUVLO mode is summarized in [Table 6](#).

**Table 5. Functional Block Status in Low Power Modes**

|                         | SYSUVLO                   | SEAL                      | OFF                       | DISABLE PLC<br>( $plc\_fsm\_ena = 0$ ) |
|-------------------------|---------------------------|---------------------------|---------------------------|--|
| Charger                 | OFF                       | OFF                       | OFF                       | OFF                                    |
| SYS LDO                 | OFF                       | OFF                       | OFF                       | OFF                                    |
| Power Path FET          | OFF                       | OFF                       | Fully ON                  | Fully ON                               |
| Fuel Gauge              | OFF                       | OFF                       | OFF                       | ON                                     |
| PLC                     | Passive impedance network | Passive impedance network | Passive impedance network | Passive network not connected          |
| I <sup>2</sup> C Access | No                        | No                        | No                        | Yes                                    |
| After Exiting           | OTP reload                | OTP reload                | OTP reload                | No OTP reload                          |

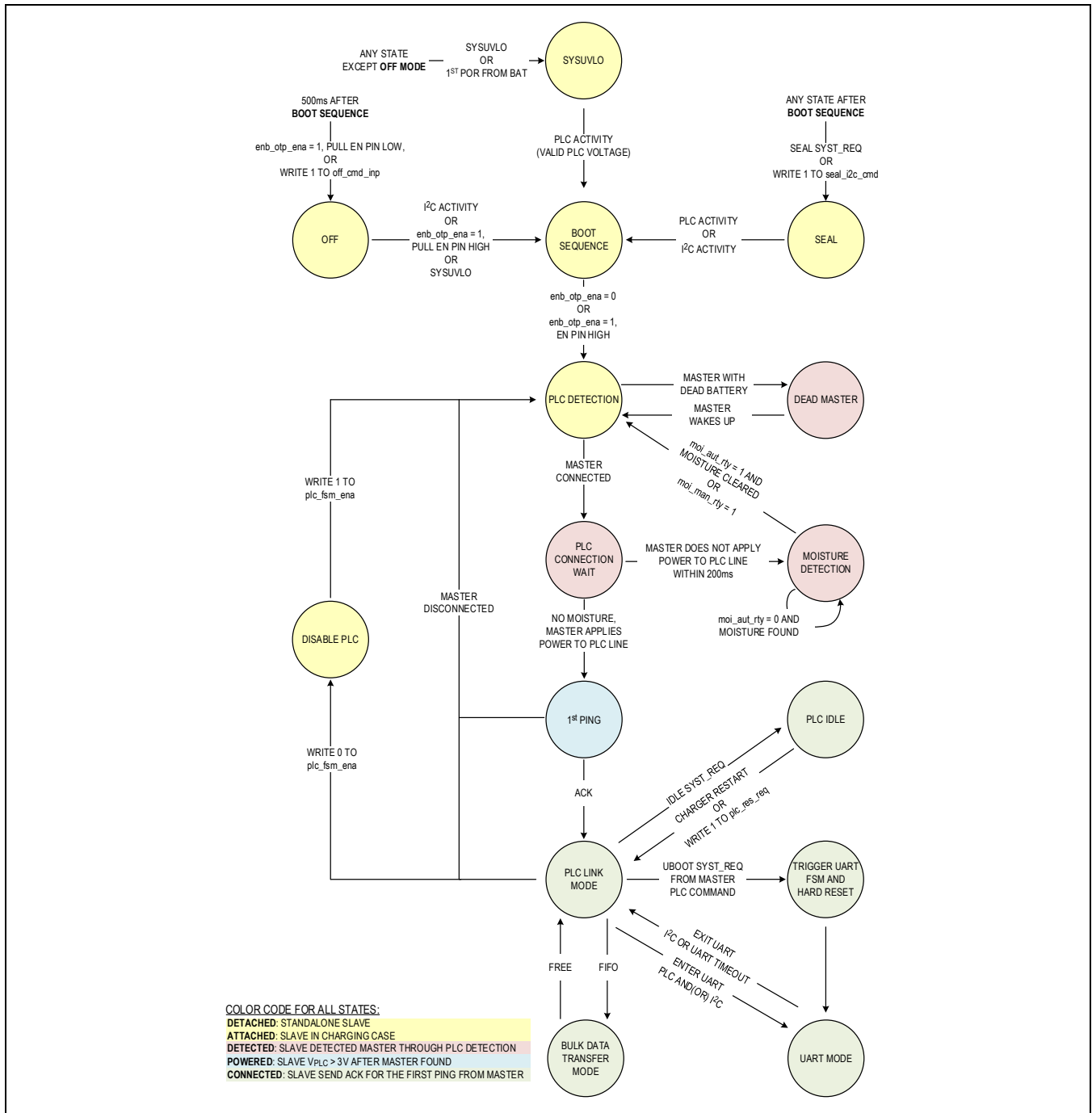


Figure 20. MAX20357 Device Operating Modes

The MAX20357 features multiple modes of operation that are designed to minimize power consumption in the end user's application. The transitions between modes and general operation are shown in [Figure 21](#). Behavior of main functional blocks in SEAL mode, OFF mode, and SYSUVLO mode is summarized in [Table 6](#).

Table 6. Functional Block Status in Low Power Modes

|  | SYSUVLO | SEAL | OFF | DISABLE PLC<br>(plc_fsm_ena = 0) |
|--|---------|------|-----|----------------------------------|
|--|---------|------|-----|----------------------------------|

Power Line  
Communication with  
ModelGauge Fuel Gauge  
and Charger

MAX20357

|                         |                           |                           |                           |                               |
|-------------------------|---------------------------|---------------------------|---------------------------|-------------------------------|
| Charger                 | OFF                       | OFF                       | OFF                       | OFF                           |
| SYS LDO                 | OFF                       | OFF                       | OFF                       | OFF                           |
| Power Path FET          | OFF                       | OFF                       | OFF                       | Fully ON                      |
| Fuel Gauge              | OFF                       | OFF                       | ON                        | ON                            |
| PLC                     | Passive impedance network | Passive impedance network | Passive impedance network | Passive network not connected |
| I <sup>2</sup> C Access | No                        | No                        | Yes                       | Yes                           |
| After Exiting           | OTP reload                | OTP reload                | No OTP reload             | No OTP reload                 |

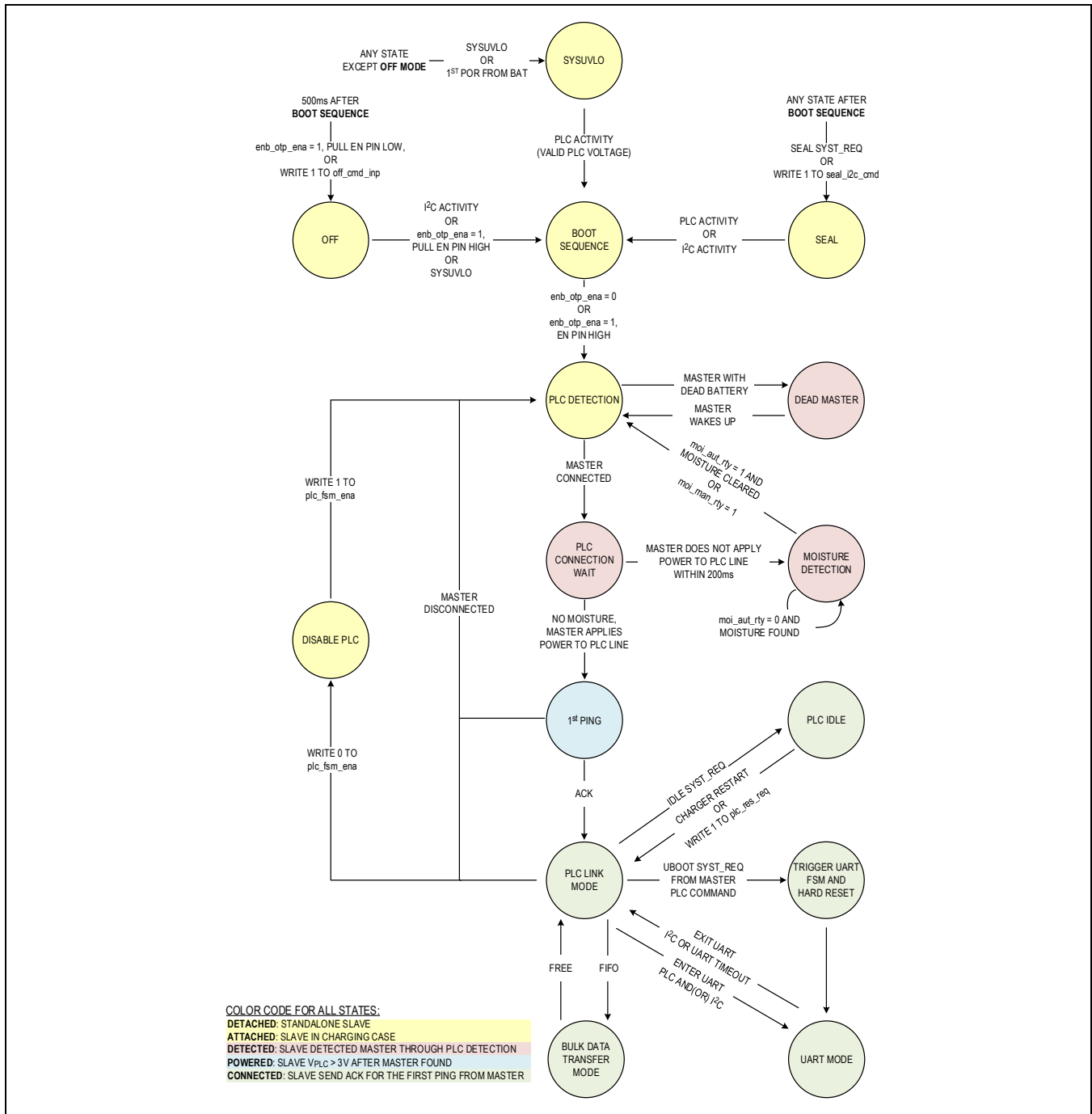


Figure 21. MAX20357 Device Operating Modes

### SYSULVO Mode

The MAX20357 enters SYSULVO mode after first power up from BAT pin, or when SYS pin voltage drops below SYSULVO threshold. The device exits SYSULVO mode when the device detects PLC voltage higher than 3V. OTP registers are reloaded after the device exits SYSULVO mode.

### SEAL Mode

The MAX20357 features SEAL mode, which puts the device into low-power mode for shipping. The MAX20357 enters SEAL mode by SEAL SYST\_REQ PLC command issued from the MAX20355, or by I<sup>2</sup>C SEAL request (write 1 to seal\_i2c\_cmd). The supply current in SEAL mode is reduced to 170nA (typ), power path FET is turned off, fuel gauge is shutdown, and all other blocks are placed into low-power mode. The device exits SEAL mode when the device detects PLC voltage higher than 3V or I<sup>2</sup>C activity. OTP registers are reloaded after the device exits SEAL mode.

### OFF Mode

The MAX20357 enters OFF mode by driving the EN low if EN pin function is enabled (enb\_otp\_ena = 1, default is 0), or by issuing OFF mode request through I<sup>2</sup>C (write 1 to off\_cmd\_inp). The supply current in OFF mode is reduced to 0.6μA (typ), I<sup>2</sup>C data is retained, power path FET is fully ON, fuel gauge is shutdown, and all other blocks are placed into a low-power mode. The device exits OFF mode when the EN bit is driven high in case enb\_otp\_ena = 1 or the device detects I<sup>2</sup>C activity. OTP registers are reloaded after device exits OFF mode. Note that enb\_otp\_ena is also reset to its default OTP setting after the device exits OFF mode.

### OFF Mode

The MAX20357 enters OFF mode by issuing OFF mode request through I<sup>2</sup>C (write 1 to off\_cmd\_inp), or by driving the EN low if EN pin function is enabled (enb\_otp\_ena = 1, default is 0). In the OFF mode, SYS power is cut off, I<sup>2</sup>C access is retained, and all other blocks are placed into a low-power mode. The device exits OFF mode when the device detects PLC voltage higher than 3V (default) or the EN bit is driven high (enb\_otp\_ena = 1). OFF mode offers a low power mode for the charge done use case, when battery is fully charged but the slave device remains in charging case.

### PLC Detection Mode

Standalone master or slave operates in PLC detection mode when the device is active. The PLC and moisture detection block diagram is shown in [Figure 22](#). In PLC detection mode, master sends PLC detection pulse through an internal pullup/pulldown resistor every 380ms. Slave sends PLC detection pulse through a similar pullup/pulldown resistor every 240ms. Master PLC is active, fuel gauge is on, and other blocks are in low-power mode; slave PLC is active, fuel gauge is on, power path FET is fully on, and other blocks are in low-power state. Both the master and slave contain a passive impedance clamp network, which allows the PLC device to detect its counterpart device even when the counterpart device has a dead battery. See the following sections for a detailed description of the master and slave connection detection scheme under various circumstances. PLC detection pulse or moisture measurement launched by the counterpart device is shown in a dashed line.

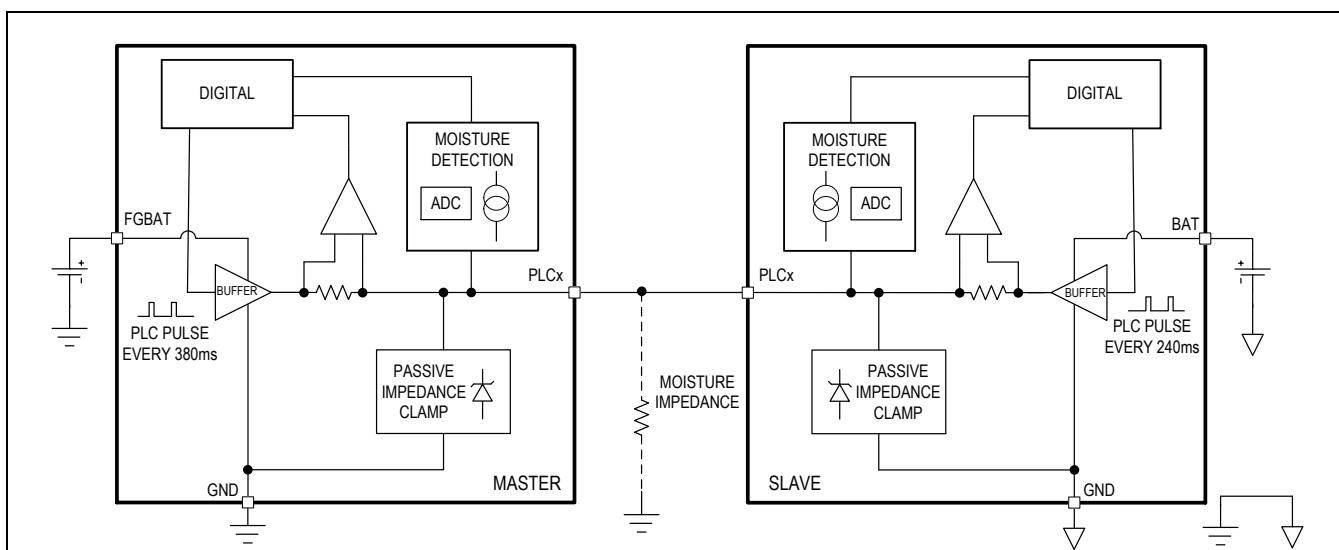


Figure 22. PLC and Moisture Detection Block Diagrams

### Active Master and Active Slave

As shown in [Figure 23](#), both the master and slave are in the PLC detection mode before the slave attached. After receiving slave's PLC detection pulse on the PLC line, the master sends a signature pulse (3x pulse) and automatically launches a moisture measurement. If there is no moisture, master connects the PLC line to a buck-boost output and holds PLC voltage to default charge voltage (default 3.5V) for 100ms. Then master increases PLC voltage to communication voltage (default 5.5V) and PING the slave. If master received ACK from slave, both devices enter PLC Link mode. After the master and slave build connection, ch1/2\_con\_sts status bit of MAX20355 and chn\_con\_sts status bit of MAX20357 are set, the corresponding interrupt bits are asserted accordingly.

If there is moisture found, the master does not turn on buck-boost to supply PLC1/2 pin and no power is applied to the slave. Moisture-related status and interrupt registers in MAX20355 are set indicating moisture detected. If the slave does not detect power applied through the PLC line within 200ms, it launches moisture measurement automatically. If moisture is not cleared, the slave stays in moisture detection mode and launches automatic moisture detection every 16s. Once the slave detects moisture is cleared, it proceeds to PLC detection mode to connect with the master. See the [Moisture Detection](#) section for a detailed description of the moisture feature.

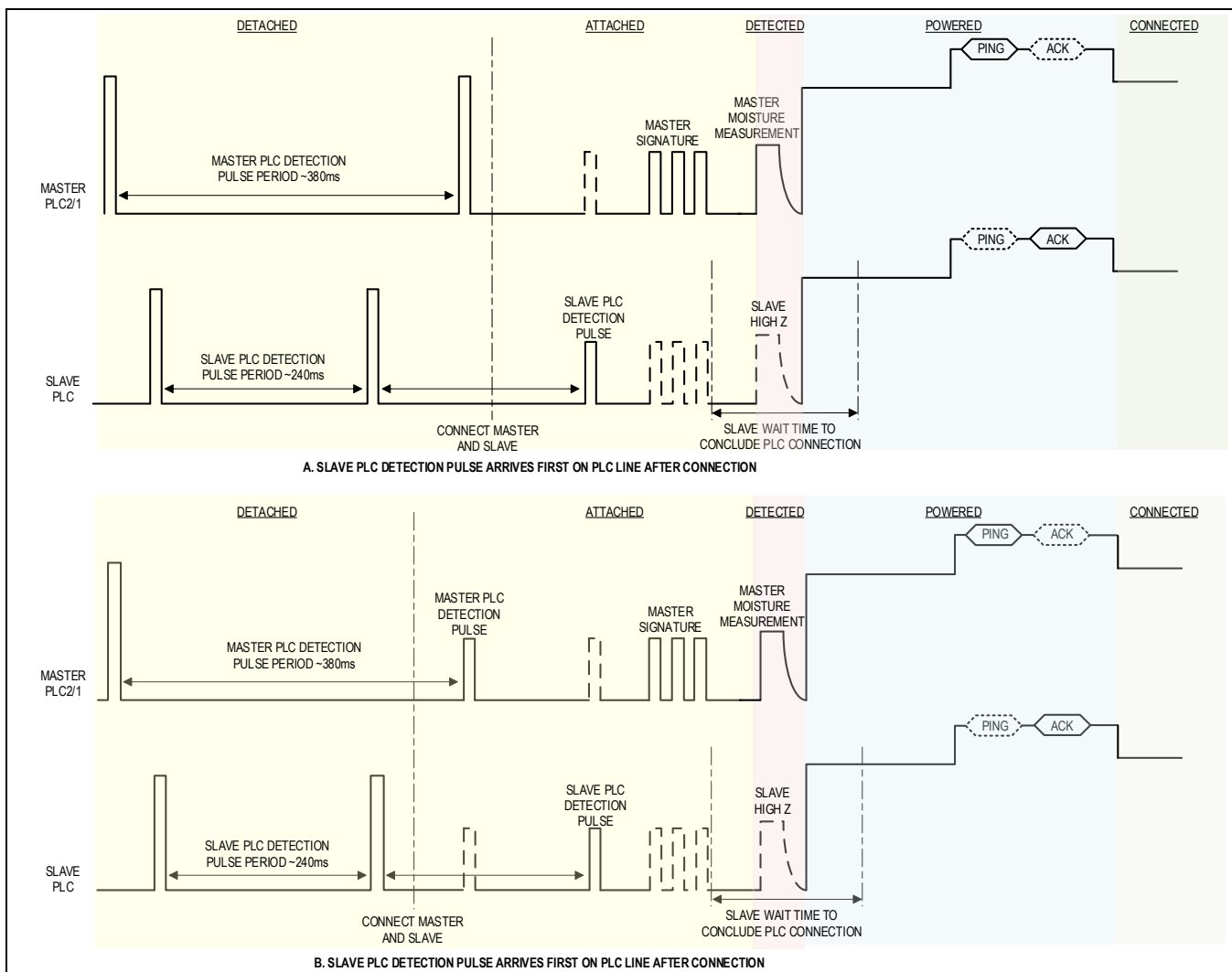


Figure 23. Active Master and Active Slave Connection

### Active Master and Dead Slave

Both master and slave offer passive impedance clamp networks for dead slave battery detection and moisture detection. As shown in [Figure 24](#), before connection, master is in PLC detection mode and slave is connected to a dead battery.

After the slave is attached to the master, the amplitude of the master's PLC detection pulse is clamped to 1.8V by slave's internal passive impedance clamp network. Master perceives its PLC detection pulse with reduced amplitude as 'something connected'. After 3x consecutive 'something connected' pulse, the master launches moisture measurement automatically. If there is no moisture, the master connects the PLC line to the buck-boost output and holds the PLC voltage to default charge voltage (default 3.5V) for 100ms. Then the master increases PLC voltage to communication voltage (default 5.5V) and PING the slave. If master received ACK from slave, both devices enter the PLC Link mode. After the master and slave build connection, ch1/2\_con\_sts status bit of MAX20355 and chn\_con\_sts status bit of MAX20357 are set, the corresponding interrupt bits are asserted accordingly.

Note that not only does the passive impedance clamp on slave creates a 'something connected' pulse on the master, but moisture between the PLC line and the ground can also create similar behavior. Master is not able to determine if it is real slave or moisture impedance before launching moisture detection. If there is moisture found, master does not connect the buck-boost output to PLC1/2 pin, and power is not applied to the slave. Moisture-related status and interrupt registers in MAX20355 are set indicating moisture detected. The MAX20357 remains in SYSUVLO mode.

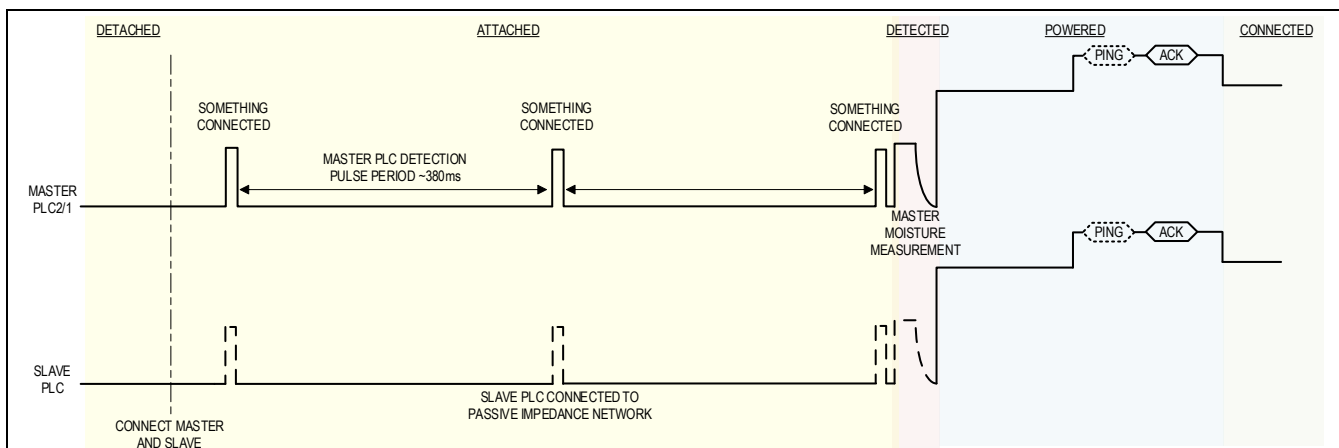


Figure 24. Active Master and Dead Slave Connection

### Dead Master and Active Slave

As shown in [Figure 25](#) before connection, the slave is in PLC Detection mode and master is connected to a dead battery. After slave is attached to the master, the slave's PLC detection pulse is clamped to 1.8V by master's passive impedance clamp network. The slave perceives its PLC detection pulse with reduced amplitude as 'something connected'. After 3x consecutive 'something connected' pulse, dead\_found interrupt is asserted in MAX20357 signaling dead master is detected, MAX20357 automatically launches a moisture measurement and continues sending PLC detection pulse. After master wakes up, master and slave follow the procedure described in 'Active Master and Active Slave' to build a connection.

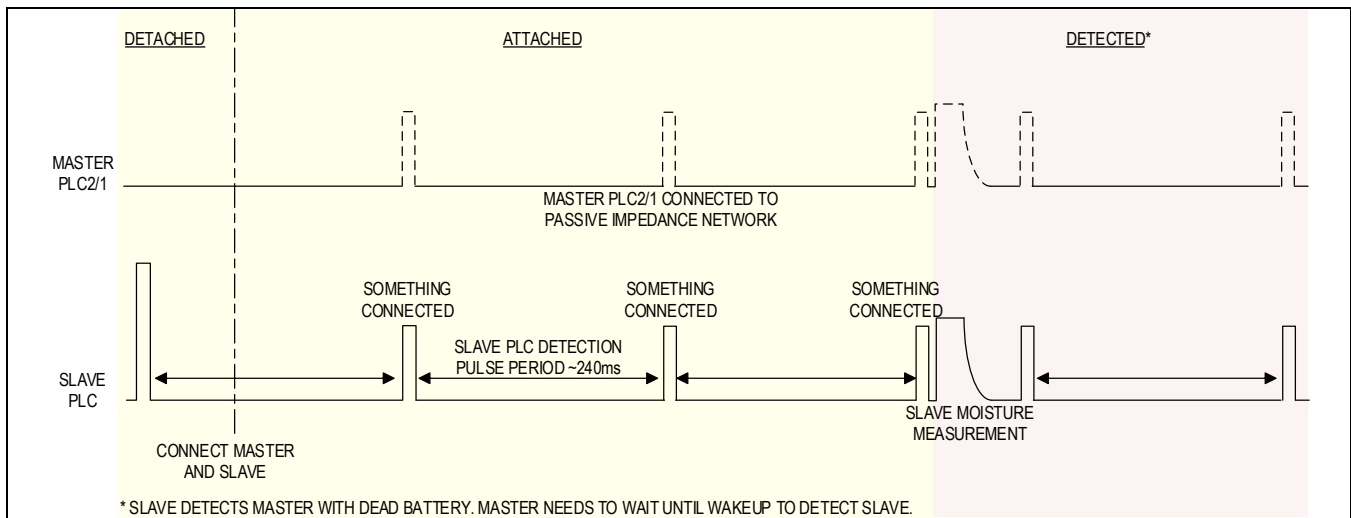


Figure 25. Dead Master and Active Slave Connection

### Moisture Detection

To prevent corrosion of the contacts if moisture is present on the PLC outputs, both the MAX20355 and MAX20357 offer a build-in moisture detection feature to check the resistance from the PLC output to GND. If the impedance detected is less than the I<sup>2</sup>C programmable moisture threshold, corresponding interrupts are flagged on both devices. The MAX20355 does not connect the buck-boost output to the PLC lines to start the charging process whenever moisture is detected. For both MAX20355 and MAX20357, moisture target current is set by RaccDetMlp (default 1 $\mu$ A) and voltage threshold is set by RaccDetMThr (default 700mV). The moisture threshold is then calculated as RaccDetMThr/RaccDetMlp (default 700k $\Omega$ ). Both the MAX20355 and MAX20357 can launch moisture detection before the PLC line is connected to the buck-boost output. After MAX20355 and MAX20357 build the PLC connection and enters the PLC link mode, manual moisture request is queued and proceeded after the PLC disconnection event. Note that after MAX20355 and MAX20357 build connection and starts charging, it is not able to measure moisture by applying source current and measuring voltage from ADC, since PLC voltage is already regulated by the buck-boost converter. The MAX20355 offers overcurrent protection for this use case to maintain system safety. The detailed description is in the overcurrent protection section. After POR, if no moisture is found previously, MAX20355 launches moisture detection under the following conditions:

3. After MAX20355 detects PLC pulse from the MAX20357 and sends signature pulse.
4. After MAX20355 detects 3x consecutive 'something connected' pulse. If the MAX20355 detects an equivalent resistance less than 17k $\Omega$  (typ) applied between PLC line and ground, the amplitude of PLC detection pulse reduces and MAX20355 recognizes it as 'something connected' pulse.
5. After manual moisture detection request through I<sup>2</sup>C bit moi\_man\_pl1/2. Manual moisture request is queued when buck-boost voltage is applied.
6. Automatic moisture detection every 16s if it is enabled through I<sup>2</sup>C bit moi\_det\_aut1/2. By default, moi\_det\_aut1/2 is set to 0 and automatic moisture detection is disabled.

After POR, if no moisture is found previously, the MAX20357 launches moisture detection under the following conditions:

7. After MAX20357 detects 3x consecutive 'something connected' pulse. If the MAX20357 detects an equivalent resistance less than 17k $\Omega$  (typ) applied between PLC line to ground, the amplitude of PLC detection pulse reduces and MAX20357 recognizes it as 'something connected' pulse.
8. After manual moisture detection request through I<sup>2</sup>C bit moi\_man\_pl. Manual moisture request is queued when buck-boost voltage is applied.
9. Automatic moisture detection every 16s. Automatic moisture detection is enabled by default.

During moisture detection, the MAX20355 and MAX20357 source a current through PLC pin and measure PLC voltage with built-in ADC. Moisture detection logic always starts from 1 $\mu$ A source current. If the ADC voltage reading RaccDetMThr is less than 0x3F – AdcRng, it increases current to 4 times and repeats the same measurement until the measured value is larger than 0x3F – AdcRng or maximum source current 64 $\mu$ A is reached. The moisture measurement



algorithm ensures that the target moisture sink current  $R_{accDetMlp}$  can be reached for the best accuracy. The ADC voltage readings are reported in  $ADCAvg$  and source current is reported in  $IP\_RES\_DET$ . Moisture resistance is calculated as  $ADCAvg/IP\_RES\_DET$ . Once the moisture measurement is completed, based on the measured result, corresponding interrupts are asserted as shown in [Figure 25](#). Note that the designed chip-level impedance measurement error is  $\pm 10\%$ . However, the actual measurement error in the application can be higher than  $\pm 10\%$  due to leakage current on PCB. Especially when moisture impedance is approaching  $1.5M\Omega$ , the leakage current is comparable to ADC source current. Since the leakage current varies depending on application schematic and layout design, the actual measurement error also varies from design to design.

**Table 7. Moisture Interrupt**

| MOISTURE INTERRUPT           | MOISTURE RESISTANCE   |
|------------------------------|---|
| res_det_gnd                  | $R_{MOI} < 458\Omega \pm 92\Omega$  |
| moi_irq_det                  | $R_{MOI} < R_{accDetMThr} / R_{accDetMlp}$ (default $700k\Omega$ )  |
| moi_dne_int                  | $R_{accDetMThr} / R_{accDetMlp}$ (default $700k\Omega$ ) $< R_{MOI} < 1.5M\Omega$   |
| res_det_opn                  | $R_{MOI} > 1.5M\Omega$  |
| res_det_abr                  | Significant variation during moisture measurement   |
| plc2/1_moi_det<br>(MAX20355) | $R_{MOI} < R_{accDetMThr} / R_{accDetMlp}$ (default $700k\Omega$ )<br>Set by automatic moisture detection conditions 1, 2 and 4 |
| plc_moi_det<br>(MAX20357)    | $R_{MOI} < R_{accDetMThr} / R_{accDetMlp}$ (default $700k\Omega$ )<br>Set by automatic moisture detection conditions 1 and 3    |

If moisture is detected, the MAX20355/MAX20357 continues sending PLC detection pulse by default to check resistance on the PLC line through its internal pullup resistor. If the equivalent moisture resistance measured is larger than  $17k\Omega$ , MAX20355 and MAX20357 perceive it as moisture removed and clears corresponding interrupts. Note that even moisture is detected in one standalone PLC device, if it is attached to its counterpart device, they are still able to pass the ATTACHED phase of the PLC connection detection process. After entering the DETECTED phase, MAX20355 launches moisture detection and fails to build a connection with the MAX20357. The system cycles between ATTACHED and DETECTED back and forth until moisture condition is removed. Automatic moisture retry on the MAX20355 can be disabled by setting  $moi\_aut\_rty1/2 = 0$ . Automatic retry on the MAX20357 cannot be disabled.

#### PLC IDLE Mode

Once the MAX20357 battery is fully charged, either MAX20355 or MAX20357 can put the system into PLC IDLE mode by IDLE SYST\_REQ PLC command to reduce unnecessary power losses. The current consumption of the MAX20357 in PLC IDLE mode is reduced to  $11\mu A$ . In PLC IDLE mode, master and slave suspend charging by removing power from the PLC line and starts handshaking pulsing protocol to check the presence of the other device. Both master and slave can request to resume PLC communication from PLC IDLE mode by writing 1 to  $plc\_res\_req$  through I<sup>2</sup>C. The system automatically resumes from the PLC IDLE mode if the MAX20357 charger auto-restart is enabled and MAX20357 battery voltage falls below charger restart threshold. [Figure 26](#) shows the waveform of the MAX20355 issuing IDLE SYST\_REQ PLC command to put the system into PLC IDLE mode.

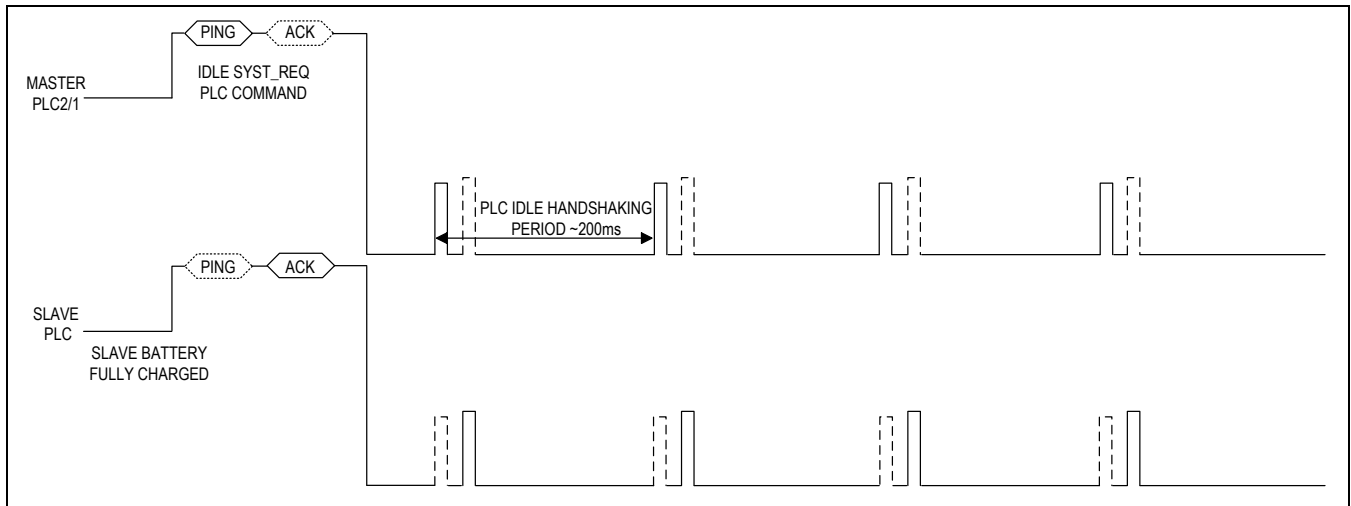


Figure 26. Enter PLC IDLE Mode After Slave Battery is Fully Charged.

Both MAX20355 and MAX20357 could detect the PLC disconnection (earbud removal) while in PLC IDLE mode, as shown in [Figure 27](#).

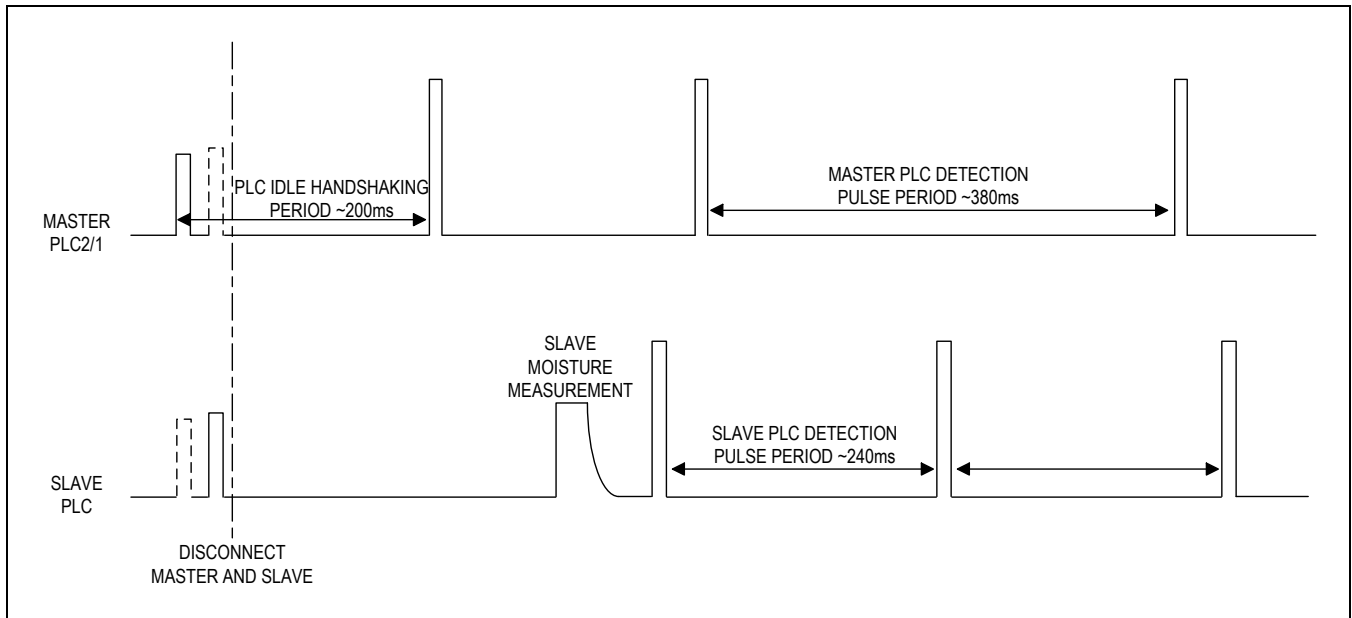


Figure 27. Master and Slave Disconnection While in PLC IDLE Mode

### Master/Slave Resets and UBOOT Mode

The MAX20357 has PLC and I<sup>2</sup>C controllable resets. All the resets can be performed by local I<sup>2</sup>C write or by PLC command from its counterpart device. The MAX20355/MAX20357 performs reset for its counterpart device through SYST\_REQ PLC command. See [Table 1](#) and [Table 2](#) for a detailed decode chart for reset commands. Different reset types are summarized in [Table 8](#).

**Table 8. Reset Types and Description**

|                   | DESCRIPTION   | MASTER                 |                          | SLAVE                  |                          |
|-------------------|---|------------------------|--------------------------|------------------------|--------------------------|
|                   |   | PLC*                   | I <sup>2</sup> C         | PLC*                   | I <sup>2</sup> C         |
| Fuel Gauge Reset  | Reset fuel gauge register   | SYST_REQ<br>FG reset   | fg_ena_byp<br>fg_ena_val | SYST_REQ<br>FG reset   | fg_ena_byp<br>fg_ena_val |
| Soft Reset        | Reset internal registers and FSMs<br>Only PLC, not including RAM or fuel gauge    | SYST_REQ<br>Soft reset | soft_reset               | SYST_REQ<br>Soft reset | soft_reset               |
| Hard Reset        | Cycle the power at MAX20357 SYS pin<br>MAX20357 charger is temporarily turned off | SYST_REQ<br>Hard reset | —                        | —                      | hard_reset               |
| Hard + Soft Reset | Soft reset + Hard reset   | SYST_REQ<br>X reset    | —                        | —                      | sft_hrd_rst              |
| UBOOT             | Hard reset and enters UART mode   | SYST_REQ<br>UBOOT      | —                        | —                      | uboot_i2c_cmd            |
| Off Mode          | Off mode  | —                      | off_cmd_inp              | —                      | off_cmd_inp              |
| Seal Mode         | MAX20357 Seal mode  | SYST_REQ<br>SEAL       | —                        | —                      | seal_i2c_cmd             |

\*PLC column lists the PLC commands that put its counterpart into the corresponding reset state

### General-Purpose Input Output (GPIO)

The MAX20355/MAX20357 each feature four general-purpose input/outputs (GPIO) controllable by its counterpart through PLC or local I<sup>2</sup>C write. Set GPIOPLCCtrx = 1 to control GPIOx by PLC, set GPIOPLCCtrx = 0 to control GPIO by I<sup>2</sup>C. When GPIOx is controlled by I<sup>2</sup>C, set GPIOEnResx = 1 to configure GPIOx as general-purpose input, set GPIOEnResx = 0 to configure GPIOx as general-purpose output.

When GPIOx is configured as general-purpose input (GPI), set GPIOEnPupx = 1 to have the GPIOx internally pulled up to the maximum of PLC line voltage and battery voltage, set GPIOEnPupx = 0 to have the GPIOx internally pulled down.

When GPIOx is configured as a general-purpose output (GPO), the GPO is in open-drain mode and requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a voltage rail that is higher than 1.4V (TYP). Set GPIODoutx = 1 to turn on the open-drain FET and output low, set GPIODoutx = 0 to turn off the open-drain FET and output high.

The GPI input status GPIODAI<sub>np4</sub>–GPIODAI<sub>np1</sub> still functions properly and does not collide when the GPIO is configured as an output. In other words, GPIO status, either configured as input or as output, is stored in GPIODAI<sub>np4</sub>–GPIODAI<sub>np1</sub>.

### Watchdog

The MAX20357 provides a watchdog function to reset the chip in case there is malfunction in slave SoC. Watchdog feature is enabled through wd\_eoc\_sel. There are three reset types: soft reset, hard reset, soft and hard reset. The reset types are I<sup>2</sup>C programmable also through wd\_rst\_type. wd\_eoc\_sel sets watchdog reset timer. If the watchdog is not serviced by reading wd\_itr\_clr with a period smaller than the timer limit, MAX20357 places a reset. Note that if the MAX20357 is in UART mode, hard reset, soft reset, hard and soft reset, or JEITA reset, the watchdog reset requests are queue and implemented until MAX20357 exits the listed modes. If the device is in SYSUVLO mode, OFF mode or SEAL mode, watchdog is disabled.

### High ESD Protected ESD Outputs

High-ESD protection on the MAX20357 PLC pin protect the device from high energy ESD damage up to 8kV contact discharge.

### ModelGauge M5 EZ Fuel Gauge with Integrated Sense Resistor

The MAX20355 and MAX20357 implement the Maxim ModelGauge m5 algorithm. The IC measures voltage, current, and temperature accurately to produce fuel gauge results. The ModelGauge m5 robust algorithm provides tolerance against battery diversity. This additional robustness enables simpler implementation for most applications and batteries by avoiding time-consuming battery characterization.

The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb-counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. The IC automatically compensates for aging, temperature, and discharge rate and provides an accurate state of charge (SOC) in percentage (%) and remaining capacity in milliampere-hours (mAh) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty. The IC provides accurate estimation of time-to-empty and time-to-full and provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer.

The IC contains a unique serial number. It can be used for cloud-based authentication. See the [Serial Number Feature](#) section for more information.

Communication to the host occurs over the standard I<sup>2</sup>C interface.

### ModelGauge m5 EZ Performance

The ModelGauge m5 EZ performance provides plug-and-play operation when the IC is connected to most lithium batteries. While the IC can be custom-tuned to the application's specific battery through a characterization process for ideal performance, the IC can provide good performance for most applications with no custom characterization required. [Table 9](#) and [Figure 28](#) show the performance of the ModelGauge m5 algorithm in applications using the ModelGauge m5 EZ configuration.

The ModelGauge m5 EZ provides good performance for most cell types. For some chemistries, such as lithium-iron-phosphate (LiFePO<sub>4</sub>) and Panasonic NCR/NCA series cells, it is suggested that the customer request a custom model from Maxim for best performance.

For even better fuel-gauging accuracy than ModelGauge m5 EZ, contact Maxim for information regarding cell characterization.

**Table 9. ModelGauge m5 EZ Performance**

| DESCRIPTION                    | AFTER FIRST CYCLE* (%) | AFTER SECOND CYCLE* (%) |
|--------------------------------|------------------------|-------------------------|
| Tests with less than 3% error  | 95                     | 97                      |
| Tests with less than 5% error  | 98.7                   | 99                      |
| Tests with less than 10% error | 100                    | 100                     |

\*Test conditions: +20°C and +40°C, run time of > 3 hours.

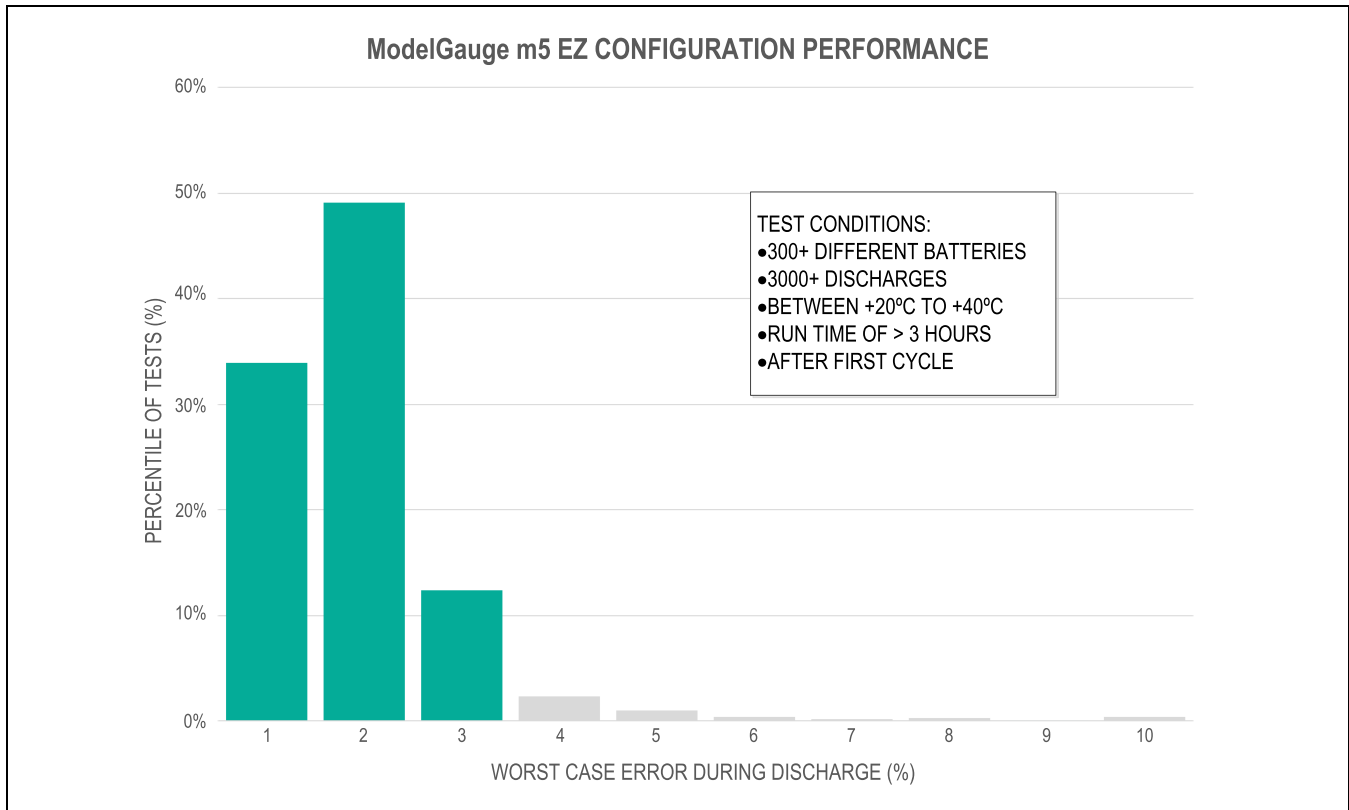


Figure 28. ModelGauge m5 EZ Configuration Performance

### Application Notes

Refer to the following application notes for additional reference material:

[User Guide 6597: MAX1726x ModelGauge m5 EZ User Guide](#)

- Documents full register set
- More details about ModelGauge m5 algorithm
- Discusses additional applications

[User Guide 6595: MAX1726x Software Implementation Guide](#)

- Guidelines for software drivers including example code

### Standard Register Formats

Unless otherwise stated during a given register's description, all fuel gauge registers of the MAX77658 follow the same format depending on the type of register. See [Table 10](#) for the resolution and range of any register described hereafter.

**Table 10. ModelGauge m5 Register Standard Resolutions**

| REGISTER TYPE | LSB SIZE  | MINIMUM VALUE | MAXIMUM VALUE | NOTES   |
|---------------|-----------|---------------|---------------|---|
| Capacity      | 0.125mAh  | 0.0mAh        | 8191.9mAh     |   |
| Percentage    | 1/256%    | 0.0%          | 255.9961%     | 1% LSb when reading only the upper byte.                                  |
| Voltage       | 1.25mV/16 | 0.0V          | 5.11992V      |   |
| Current       | 39.06µA   | -1.28A        | 1.27996A      | Signed two's-complement format.   |
| Temperature   | 1/256°C   | -128.0°C      | 127.996°C     | Signed two's-complement format. 1°C LSb when reading only the upper byte. |
| Resistance    | 1/4096Ω   | 0.0Ω          | 15.99976Ω     |   |
| Time          | 5.625s    | 0.0s          | 102.3984h     |   |

|         |  |  |  |  |
|---------|--|--|--|--|
| Special |  |  |  | Format details are included with the register description. |
|---------|--|--|--|--|

### ModelGauge m5 Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated. It causes the reported capacity error to increase over time and requires periodic corrections. Corrections are traditionally performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Voltage measurement-based SOC estimation has accuracy limitations due to imperfect cell modeling but does not accumulate offset error over time.

The MAX20355/MAX20357 includes an advanced voltage fuel gauge (VFG) that estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart empty compensation algorithm that automatically compensates for the effect of temperature condition and load condition to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward an empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG. See [Figure 29](#). The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, cancelling the coulomb-counter drift.

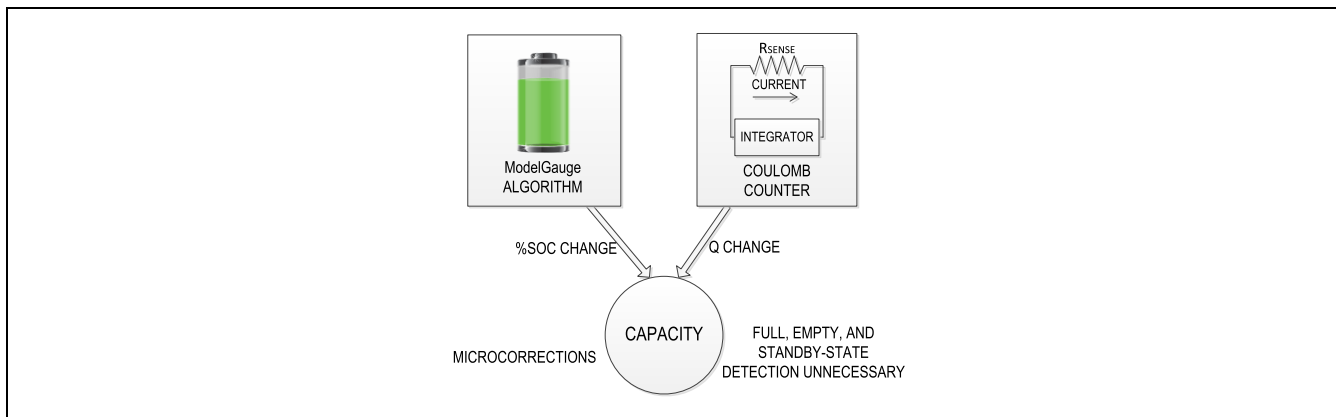


Figure 29. ModelGauge m5 Algorithm

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

## Analog Measurements

### Voltage Measurement

#### VCell Register (0x09)

Register Type: Voltage

VCell reports the voltage measured between BATT and GND

#### AvgVCell Register (0x19)

Register Type: Voltage

The AvgVCell register reports an average of the VCell register readings.

#### MaxMinVolt Register (0x1B)

Register Type: Special

Initial Value: 0x00FF

The MaxMinVolt register maintains the maximum and minimum of VCell register values since the device reset. At power-up, the maximum voltage value is set to 0x00 (the minimum) and the minimum voltage value is set to 0xFF (the maximum). Therefore, both values are changed to the voltage register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution.

| D15      | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------|-----|-----|-----|-----|-----|----|----|----------|----|----|----|----|----|----|----|
| MaxVCELL |     |     |     |     |     |    |    | MinVCELL |    |    |    |    |    |    |    |

**MaxVCELL:** Maximum VCell register reading

**MinVCELL:** Minimum VCell register reading

### Current Measurement

#### Current Register (0x0A)

Register Type: Current

The MAX20355/MAX20357 uses internal current sensing to monitor the current through the SYS FG pin. The measurement value is stored in two's-complement format. Measurement that exceeds maximum and minimum current range is stored as maximum and minimum values. The current register has a LSB value of 31.25 $\mu$ A, a register scale range of  $\pm 1.024$ A, and an allowable measurement range as described in the [Absolute Maximum Ratings](#).

#### AvgCurrent Register (0x0B)

Register Type: Current

The AvgCurrent register reports an average of current register readings.

#### MaxMinCurr Register (0x1C)

Register Type: Special

Initial Value: 0x807F

The MaxMinCurr register maintains the maximum and minimum current register values since the last IC reset or until cleared by host software. At power-up, the maximum current value is set to (most negative) and the minimum current value is set to 7Fh (most positive). Therefore, both values are changed to the current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum currents are each stored as two's complement 8-bit values with 160mA resolution.



| D15        | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------|-----|-----|-----|-----|-----|----|----|------------|----|----|----|----|----|----|----|
| MaxCurrent |     |     |     |     |     |    |    | MinCurrent |    |    |    |    |    |    |    |

**MaxCurrent:** Maximum Current register reading

**MinCurrent:** Minimum Current register reading

### Temperature Measurement

#### Temp Register (0x08)

Register Type: Temperature

The Temp register provides the temperature measured by the thermistor or die temperature based on the Config register setting.

#### MaxMinTemp Register (0x1A)

Register Type: Special Initial Value: 0x807F

The MaxMinTemp register maintains the maximum and minimum Temp register (0x08) values since the last fuel-gauge reset or until cleared by host software. At power-up, the maximum value is set to 0x80 (most negative) and the minimum value is set to 0x7F (most positive). Therefore, both values are changed to the Temp register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution.

| D15            | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7             | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------|-----|-----|-----|-----|-----|----|----|----------------|----|----|----|----|----|----|----|
| MaxTemperature |     |     |     |     |     |    |    | MinTemperature |    |    |    |    |    |    |    |

**MaxTemperature:** Maximum Temp register reading

**MinTemperature:** Minimum Temp register reading

#### DieTemp Register (0x34)

Register Type: Temperature

The DieTemp register provides the internal die temperature measurement. If Config.TSel = 0, DieTemp and Temp registers have the value of the die temperature.

### Power Measurement

#### Power Register (0xB1)

Instant power calculation from immediate current and voltage. The LSB is 1.6mW.

#### AvgPower Register (0xB3)

Filtered Average Power from the power register. LSB is 1.6mW.

### Alert Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, current, temperature, or state-of-charge. Interrupts are generated on the  $\overline{\text{ALRT}}$  pin open-drain output driver. An external pullup is required to generate a logic-high signal. Alerts can be triggered by any of the following conditions:

- Battery removal: ( $V_{TH} > V_{BAT} - V_{DET}$ ) and battery removal detection enabled (Ber = 1).
- Battery insertion: ( $V_{TH} < V_{BAT} - V_{DET-HYS}$ ) and battery insertion detection enabled (Bei = 1).
- Over/undervoltage: VAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undertemperature: TAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undercurrent: IAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/under SOC: SAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- 1% SOC change: RepSOC register bit d8 (1% bit) changed (dSOCen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the Status (0x00) register. Alerts generated by a threshold-level violation can be configured to be cleared only by software or cleared automatically when

the threshold level is no longer violated. See the Config (1Dh) and Config2 (BBh) register descriptions for details of the alert function configuration.

### Serial Number Feature

Each IC provides a unique serial number ID. To read this serial number, clear the AtRateEn and the DPEn bit in the Config2 register. The 128-bit serial information overwrites the Dynamic Power and AtRate output registers. To continue Dynamic Power and AtRate operations after reading the serial number, the host should set Config2.AtRateEn and Config2.DPEn to 1.

**Table 11. Serial Number Format**

| ADDRESS | Config2.AtRateEn = 1    Config2.DPEn = 1 | Config2.AtRateEn = 0 && Config2.DPEn = 0 |
|---------|--|--|
| 0xD4    | MaxPeakPower                             | Serial Number Word0                      |
| 0xD5    | SusPeakPower                             | Serial Number Word1                      |
| 0xD9    | MPPCurrent                               | Serial Number Word2                      |
| 0xDA    | SPPCurrent                               | Serial Number Word3                      |
| 0xDC    | AtQResidual                              | Serial Number Word4                      |
| 0xDD    | AtTTE                                    | Serial Number Word5                      |
| 0xDE    | AtAvSoc                                  | Serial Number Word6                      |
| 0xDF    | AtAvCap                                  | Serial Number Word7                      |

### ModelGauge m5 Memory Space

Registers that relate to functionality of the ModelGauge m5 fuel gauge are located on pages 0h-4h and are continued on pages Bh and Dh. See the [ModelGauge m5 Algorithm](#) section for details of specific register operation. Register locations marked reserved should not be written to.

**Table 12. ModelGauge m5 Register Memory Map**

| PAGE/WORD | 00h        | 10h        | 20h        | 30h        | 40h        | B0h           | D0h               |
|-----------|------------|------------|------------|------------|------------|---------------|-------------------|
| 0h        | Status     | FullCapRep | TTF        | Reserved   | Reserved   | Status2       | RSense / UserMem3 |
| 1h        | VAIrtTh    | TTE        | DevName    | Reserved   | Reserved   | Power         | ScOcvLim          |
| 2h        | TAIrtTh    | QRTTable00 | QRTTable10 | QRTTable20 | QRTTable30 | ID / UserMem2 | VGain             |
| 3h        | SAIrtTh    | FullSocThr | FullCapNom | Reserved   | RGain      | AvgPower      | SOCHold           |
| 4h        | AtRate     | RCell      | Reserved   | DieTemp    | Reserved   | IAIrtTh       | MaxPeakPower      |
| 5h        | RepCap     | Reserved   | Reserved   | FullCap    | dQAcc      | TTFCfg        | SusPeakPower      |
| 6h        | RepSOC     | AvgTA      | Reserved   | Reserved   | dPAcc      | CVMixCap      | PackResistance    |
| 7h        | Age        | Cycles     | AIN        | Reserved   | Reserved   | CVHalfTime    | SysResistance     |
| 8h        | Temp       | DesignCap  | LearnCfg   | RComp0     | Reserved   | CGTempCo      | MinSysVoltage     |
| 9h        | VCell      | AvgVCell   | FilterCfg  | TempCo     | ConvgCfg   | Curve         | MPPCurrent        |
| Ah        | Current    | MaxMinTemp | RelaxCfg   | VEmpty     | VFRemCap   | HibCfg        | SPPCurrent        |
| Bh        | AvgCurrent | MaxMinVolt | MiscCfg    | Reserved   | Reserved   | Config2       | ModelCfg          |
| Ch        | QResidual  | MaxMinCurr | TGain      | Reserved   | Reserved   | VRipple       | AtQResidual       |
| Dh        | MixSOC     | Config     | TOff       | FStat      | QH         | RippleCfg     | AtTTE             |
| Eh        | AvSOC      | IChgTerm   | CGain      | Timer      | Reserved   | TimerH        | AtAvSOC           |
| Fh        | MixCap     | AvCap      | COff       | ShdnTimer  | Reserved   | Reserved      | AtAvCap           |

## I<sup>2</sup>C Serial Communication

### General Description

The IC features a revision 3.0 I<sup>2</sup>C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device, relying on the master to generate a clock signal. SCL clock rates from 0Hz to 400kHz are supported.

I<sup>2</sup>C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

[Figure 30](#) shows the functional diagram for the I<sup>2</sup>C based communications controller. For additional information on I<sup>2</sup>C, refer to the I<sup>2</sup>C Bus Specification and User Manual which is available for free through the internet.

### Features

- I<sup>2</sup>C Revision 3.0 compatible serial communications channel
- Compatible with any bus timing up to 400kHz
- Does not utilize I<sup>2</sup>C clock stretching

### I<sup>2</sup>C Simplified Block Diagram

There are three pins (aside from GND) for the I<sup>2</sup>C-compatible interface. V<sub>IO</sub> determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface cannot drive the SCL line.

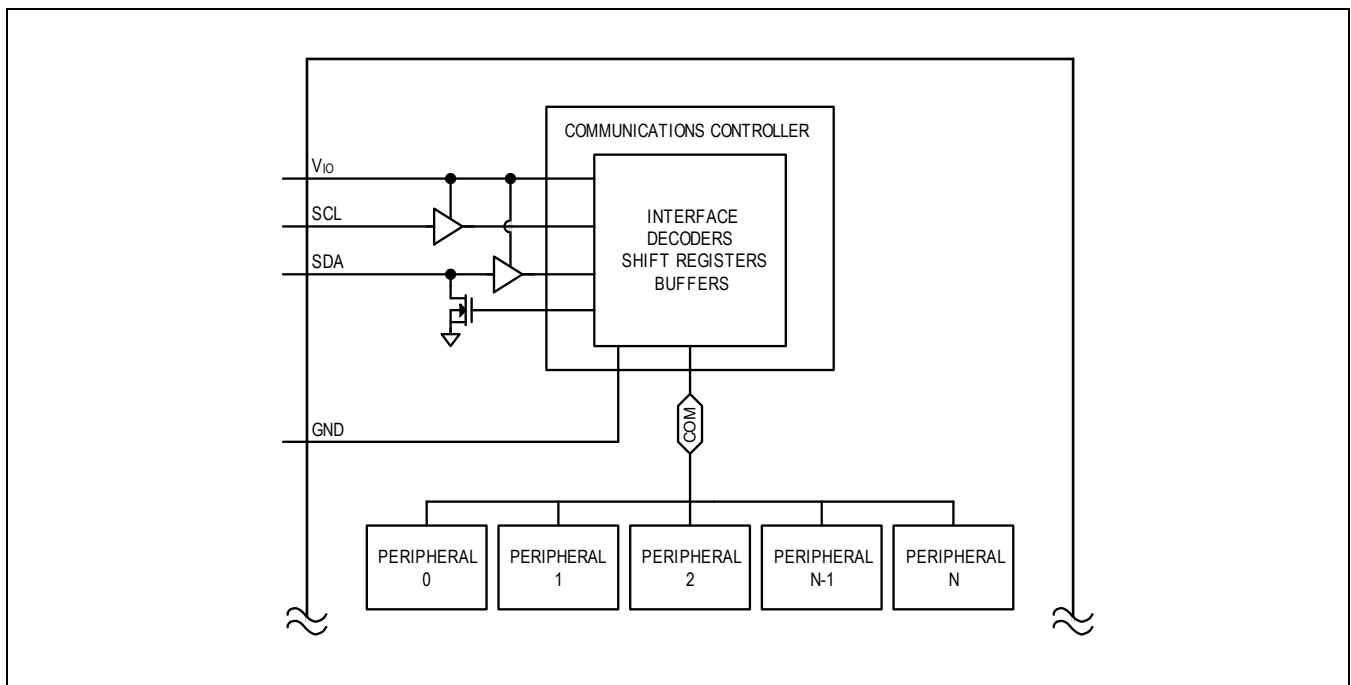


Figure 30. I<sup>2</sup>C Simplified Block Diagram

### I<sup>2</sup>C System Configuration

The I<sup>2</sup>C-compatible interface is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I<sup>2</sup>C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer

is a master. Any device that is being addressed by the master is considered a slave. The I<sup>2</sup>C-compatible interface operates as a slave on the I<sup>2</sup>C bus with transmit and receive capabilities.

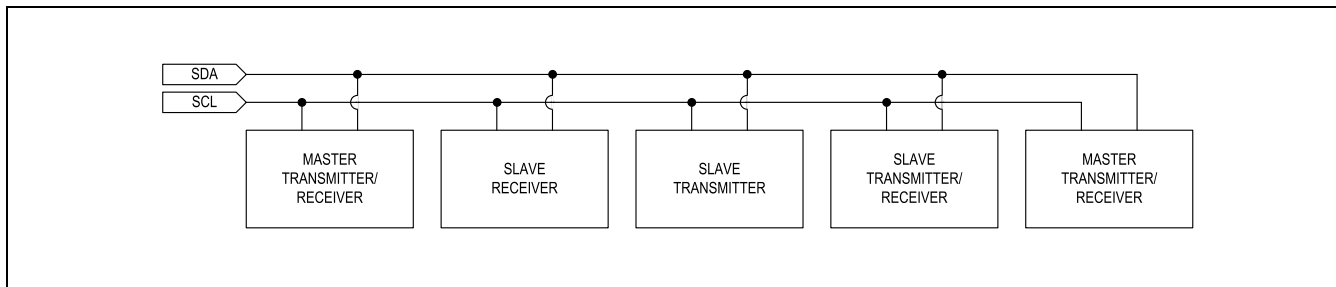


Figure 31. I<sup>2</sup>C System Configuration

### I<sup>2</sup>C Interface Power

The I<sup>2</sup>C interface derives its power from V<sub>IO</sub>. Typically, a power input such as V<sub>IO</sub> would require a local 0.1μF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V<sub>IO</sub> and the next closest capacitor (≥ 0.1μF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V<sub>IO</sub> to GND with a 0.1μF ceramic capacitor.

V<sub>IO</sub> accepts voltages from 1.7V to 3.6V (V<sub>IO</sub>). Cycling V<sub>IO</sub> does not reset the I<sup>2</sup>C registers. When V<sub>IO</sub> is less than V<sub>IOUVLO</sub> and V<sub>SYSA</sub> is less than V<sub>SYSAUVLO</sub>, SDA and SCL are high impedance.

### I<sup>2</sup>C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA, while SCL is high, are control signals. See the [I<sup>2</sup>C Start and Stop Conditions](#) section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

### I<sup>2</sup>C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See [Figure 32](#).

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the [I<sup>2</sup>C Acknowledge Bit](#) section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

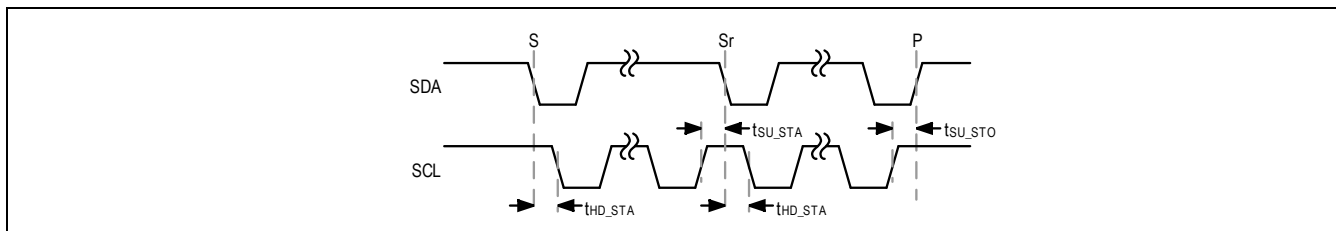


Figure 32. I<sup>2</sup>C Start and Stop Conditions

### I<sup>2</sup>C Acknowledge Bit

Both the I<sup>2</sup>C bus master and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each ninth-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See [Figure 33](#). To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

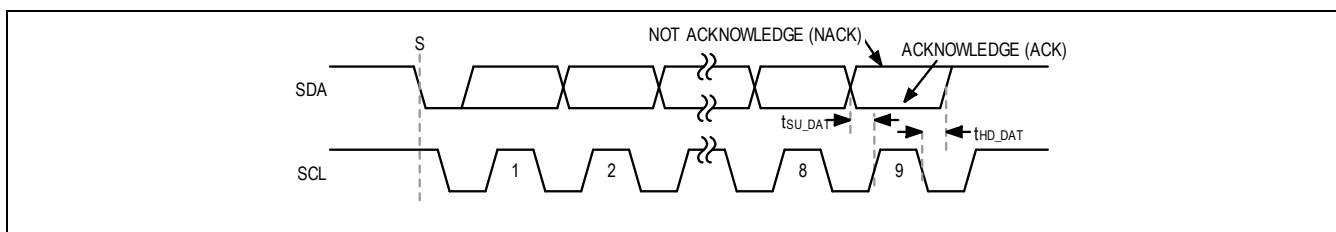


Figure 33. Acknowledge Bit

### I<sup>2</sup>C Slave Address

The I<sup>2</sup>C controller implements 7-bit slave addressing. The registers of the MAX20355/MAX20357 are divided into three blocks with separate slave addresses:

- The main block includes all the registers for the global resource, the power line communication, and the buck-boost regulator (MAX20355)/the charger (MAX20357). All the registers in the main block are 8-bit registers.
- The fuel gauge block includes all the registers for the fuel gauging. The fuel gauge registers are in 16-bit word.
- The RAM block is 128-byte space for mailbox and bulk data transfer. The RAM registers are 8-bit.

| MAX20355 ADDRESS   | 7-BIT SLAVE ADDRESS | 8-BIT WRITE ADDRESS | 8-BIT READ ADDRESS |
|--------------------|---------------------|---------------------|--------------------|
| PLC Address        | 0x28, 0b 010 1000   | 0x50, 0b 0101 0000  | 0x51, 0b 0101 0001 |
| Fuel Gauge Address | 0x36, 0b 011 0110   | 0x6C, 0b 0110 1100  | 0x6D, 0b 0110 1101 |
| RAM Address        | 0x40, 0b 100 0000   | 0x80, 0b 1000 0000  | 0x81, 0b 1000 0001 |
| MAX20357 ADDRESS   | 7-BIT SLAVE ADDRESS | 8-BIT WRITE ADDRESS | 8-BIT READ ADDRESS |
| PLC Address        | 0x15, 0b 001 0101   | 0x2A, 0b 0010 1010  | 0x2B, 0b 0010 1011 |
| Fuel Gauge Address | 0x36, 0b 011 0110   | 0x6C, 0b 0110 1100  | 0x6D, 0b 0110 1101 |
| RAM Address        | 0x55, 0b 101 0101   | 0xAA, 0b 1010 1010  | 0xAB, 0b 1010 1011 |

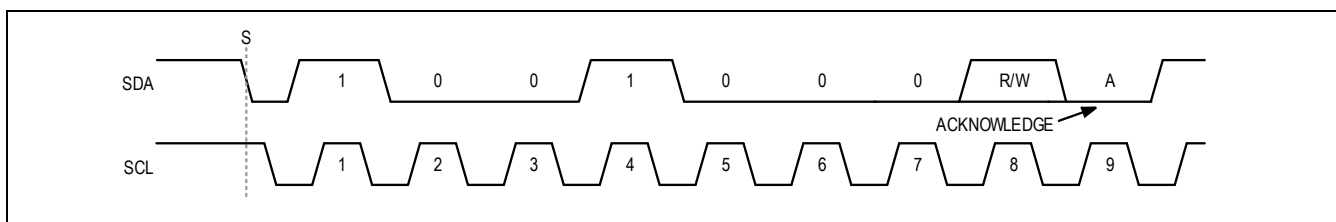


Figure 34. Slave Address Example

### I<sup>2</sup>C Clock Stretching

In general, the clock signal generation for the I<sup>2</sup>C bus is the responsibility of the master device. The I<sup>2</sup>C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

### I<sup>2</sup>C General Call Address

This device does not implement the I<sup>2</sup>C specifications general call address and does not acknowledge the general call address (0b0000\_0000).

### I<sup>2</sup>C Device ID

This device does not support the I<sup>2</sup>C Device ID feature.

### I<sup>2</sup>C Communication Speed

This device is compatible with any bus timing up to 400kHz. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant ( $C \times R$ ), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I<sup>2</sup>C Bus Specification and User Manual (available for free on the internet) for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6k $\Omega$  pullup resistors, and a 400kHz bus needs about 1.5k $\Omega$  pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power ( $V^2/R$ ).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I<sup>2</sup>C Bus Specification and User Manual. Major considerations concerning this part are:

- The I<sup>2</sup>C bus master uses current source pullups to shorten the signal rise.
- The I<sup>2</sup>C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the [I<sup>2</sup>C Communication Protocols](#) section.

### I<sup>2</sup>C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

#### Writing to a Single 8-bit Register

[Figure 35](#) shows the protocol for the I<sup>2</sup>C master device to write one byte of data to this device. This protocol is the same as the SMBus specification's write-byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ( $R/\overline{W} = 0$ ).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

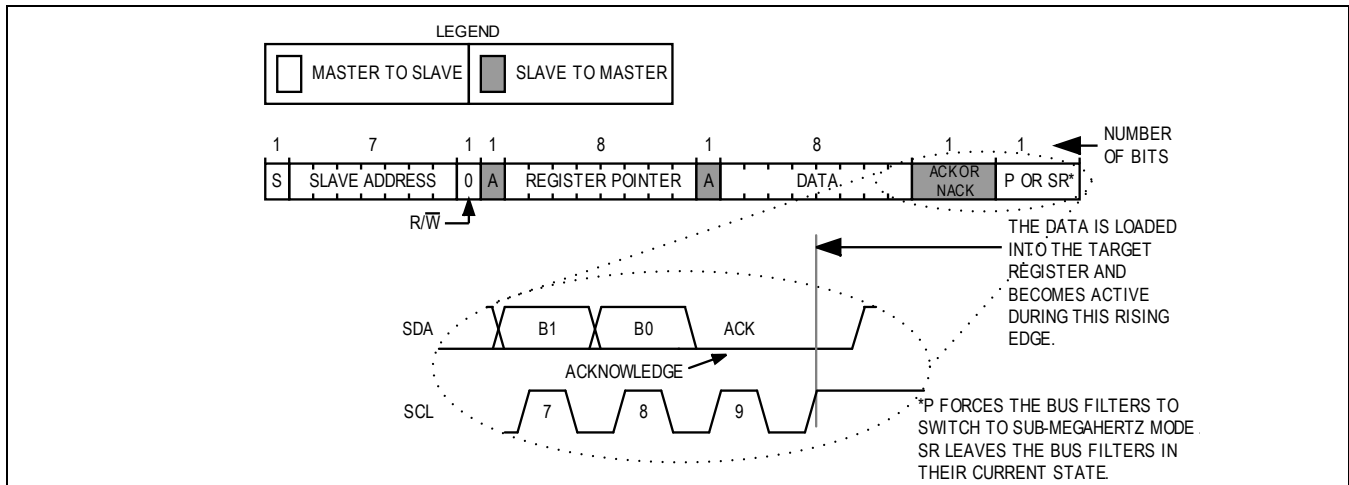


Figure 35. Writing to a Single 8-bit Register with the Write Byte Protocol

### Writing Multiple Bytes to Sequential Registers

Figure 36 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ( $R/\bar{W} = 0$ ).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge-related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

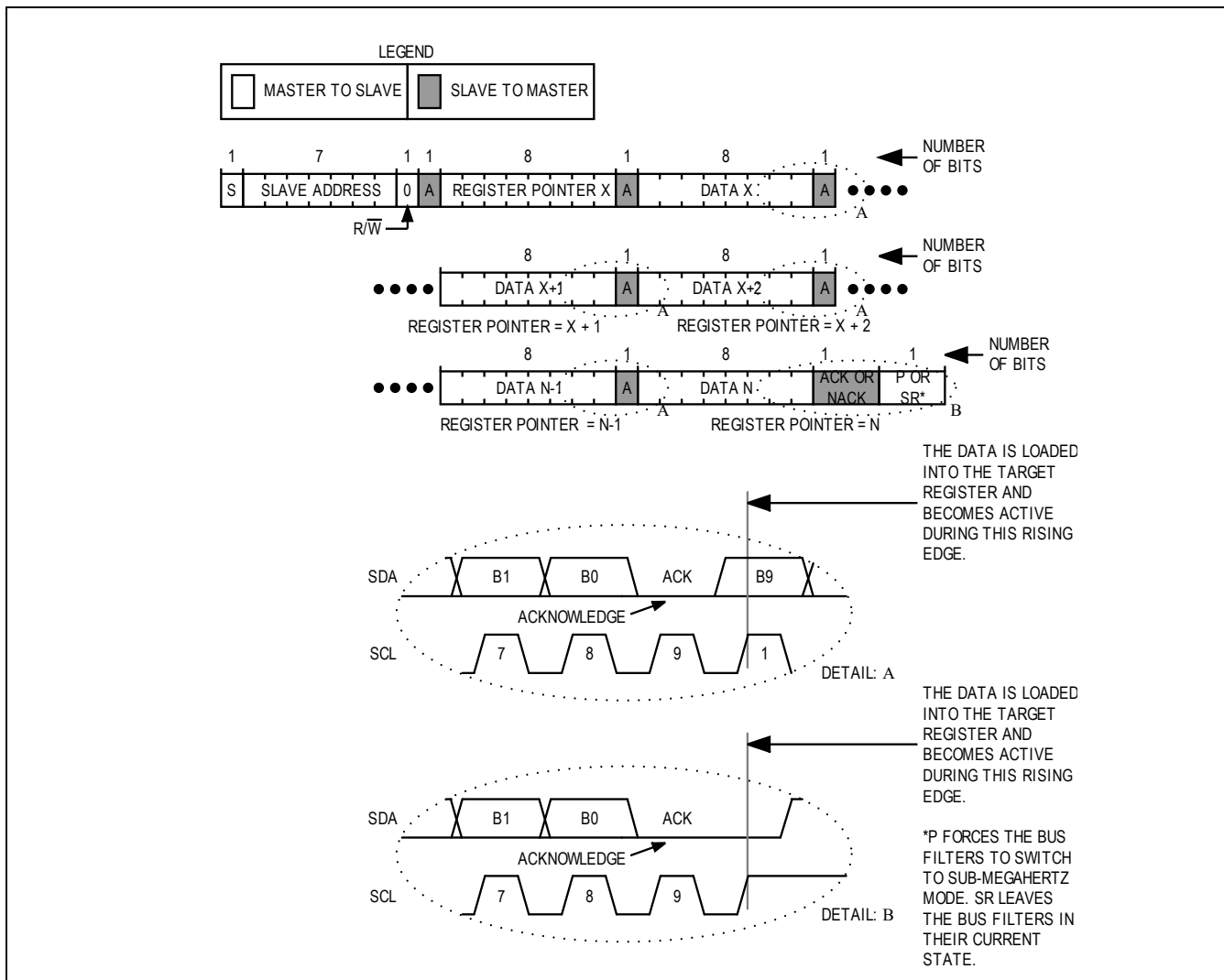


Figure 36. Writing to Sequential Registers X to N

### Writing to 16-bit Registers

The Write Data protocol is used to transmit data to the registers of the fuel gauge at memory addresses from 00h to FFh. Addresses 00h to FFh can be written as a block. The memory address is sent by the bus master as a single byte value immediately after the slave address. The LSB of the data to be stored is written immediately after the memory address byte is acknowledged. Because the address is automatically incremented after the last bit of each 16-bit word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus master continues an auto-incremented write transaction beyond address FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See [Figure 37](#) for an example of the Write Data communication sequence.



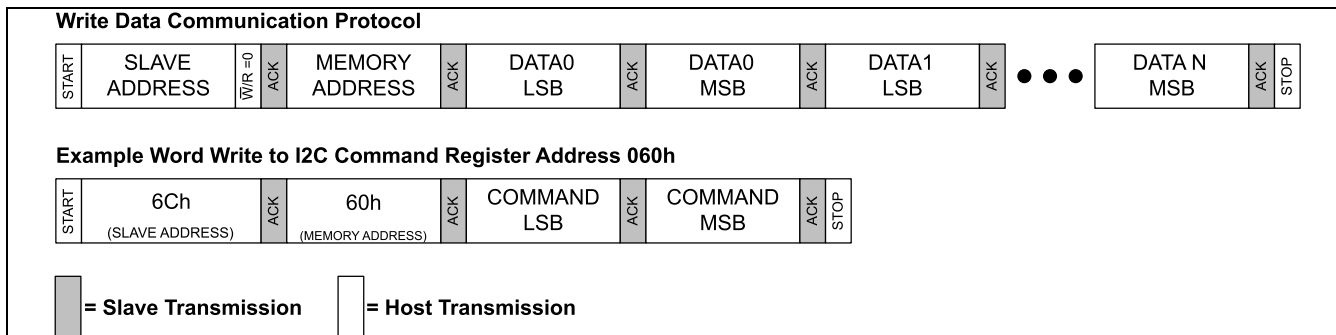


Figure 37. Example I<sup>2</sup>C Write 16-bit Data Communication Sequence

### Reading from a Single Register

Figure 38 shows the protocol for the I<sup>2</sup>C master device to read one byte of data. This protocol is the same as the SMBus specification's read-byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ( $R/\overline{W} = 0$ ).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit ( $R/\overline{W} = 1$ ).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

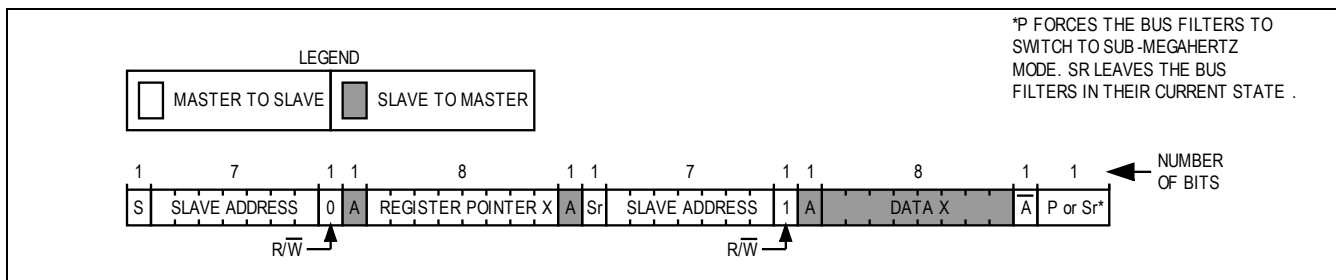


Figure 38. Reading from a Single Register with the Read Byte Protocol

### Reading from Sequential Registers

Figure 39 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit ( $R/\overline{W} = 0$ ).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.

5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit ( $R/\bar{W} = 1$ ).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a Sr leaves the bus input filters in their current state.

Note that when this device receives a stop it does not modify its register pointer. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

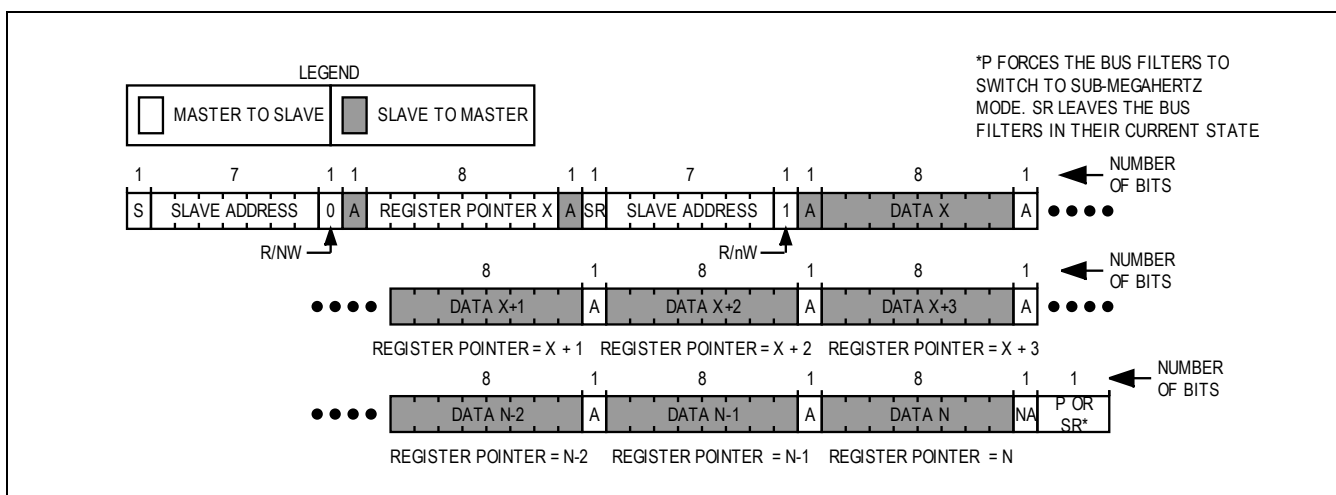


Figure 39. Reading Continuously from Sequential Registers X to N

## Applications Information

### PLC Current Sink and Detection Threshold

The MAX20355 and MAX20357 PLC sink current and detection threshold are specially paired to maintain good performance. Buck-boost ripple is the major source of noise inside the system. The MAX20355 self-cancels the effect of the buck-boost ripple since the noise is created by itself. The MAX20357 is not able to cancel the noise. To compensate for the ripple noise, all the PLC sink current PLCSnkSel options of the MAX20355 are higher than MAX20357 PLC sink current as shown in [Table 13](#) and [Table 14](#).

Table 13. PLC Detection Pair (MAX20355 Data Packet)

| DECODE | MAX20355 PLCSnkSel | MAX20357 PLCThrSel |
|--------|--------------------|--------------------|
| 0b00   | 88mA               | 75mV               |
| 0b01   | 105.4mA            | 90mV               |
| 0b10   | 123mA              | 105mV              |
| 0b11   | 140.5mA            | 120mV              |

Table 14. PLC Detection Pair (MAX20357 Data Packet)

| DECODE | MAX20357 PLCSnkSel | MAX20355 PLCThrSel |
|--------|--------------------|--------------------|
| 0b00   | 50.3mA             | 40mV               |
| 0b01   | 70.4mA             | 56mV               |
| 0b10   | 90.4mA             | 70mV               |

|      |         |      |
|------|---------|------|
| 0b11 | 110.5mA | 84mV |
|------|---------|------|

PLC voltage detection threshold needs to be placed in the middle of the PLC signal for better performance. For each MAX20355 sink current PLCSnkSel, the MAX20357 offers one paired voltage detection threshold PLCThrSel. Make sure always use the same code for the MAX20355 PLCSnkSel and the MAX20357 PLCThrSel ([Table 13](#)). Similarly, use the same code for the MAX20357 PLCSnkSel and the MAX20355 PLCThrSel ([Table 14](#)). It is recommended to start from code '00'. If the external noise is too strong and code '00' does not offer good performance, increase the sink current by moving to larger codes. Note there is a tradeoff between susceptibility to noise and power consumption. Higher sink current offers a better anti-interference ability, but also higher power consumption.

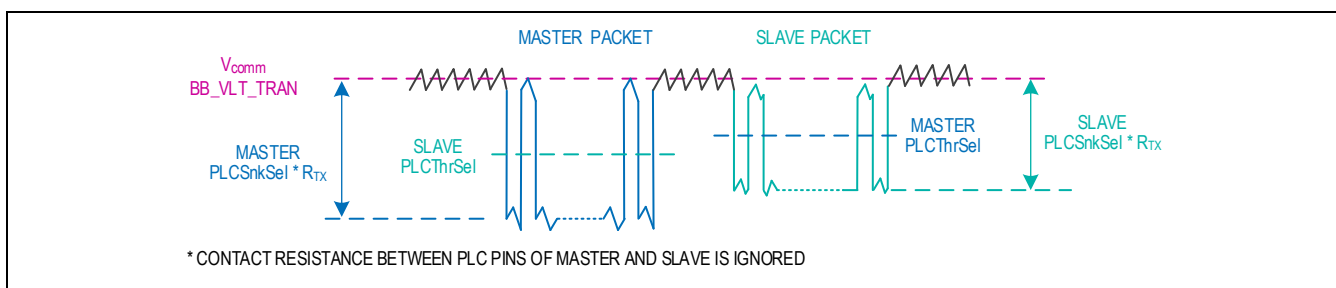


Figure 40. PLC Current Sink and Detection Threshold

## Typical Application Circuit

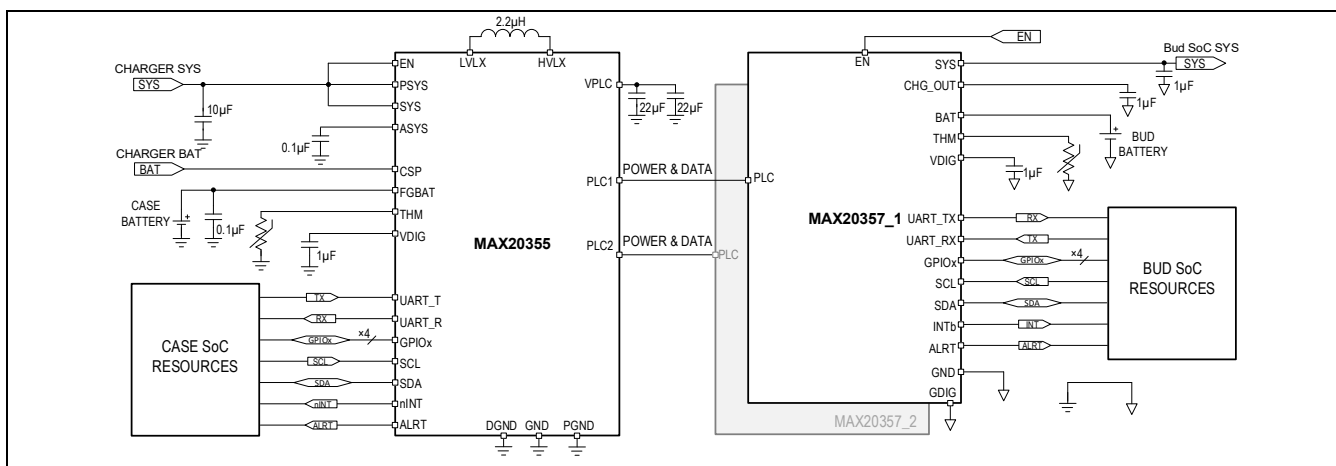


Figure 41. Typical Application Circuit

## PCB Layout Guidelines

[Figure 42](#) shows a PCB layout example. Please take following guidelines as references to design the PCB:

1. Place the SYS capacitor ( $C_{SYS}$ ) close to the SYS pin.
2. Place the CHG\_OUT capacitor ( $C_{CHG\_OUT}$ ) close to the CHG\_OUT pin.
3. Place the VDIG capacitor ( $C_{VDIG}$ ) close to the VDIG pin. Proximity to the IC provides a stable supply for the internal circuitry.
4. Keep the power traces and load connections short and wide. This is to minimize PCB conduction loss and to improve the heat dissipation.
5. Multiple vias are recommended for all paths that carry high currents (PLC, SYS, and BAT). Placements of vias should create the shortest possible current loops and must not obstruct the flow of currents or mirror currents in the ground plane.
6. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. Select ceramic capacitors that maintain capacitance over temperature and DC bias.

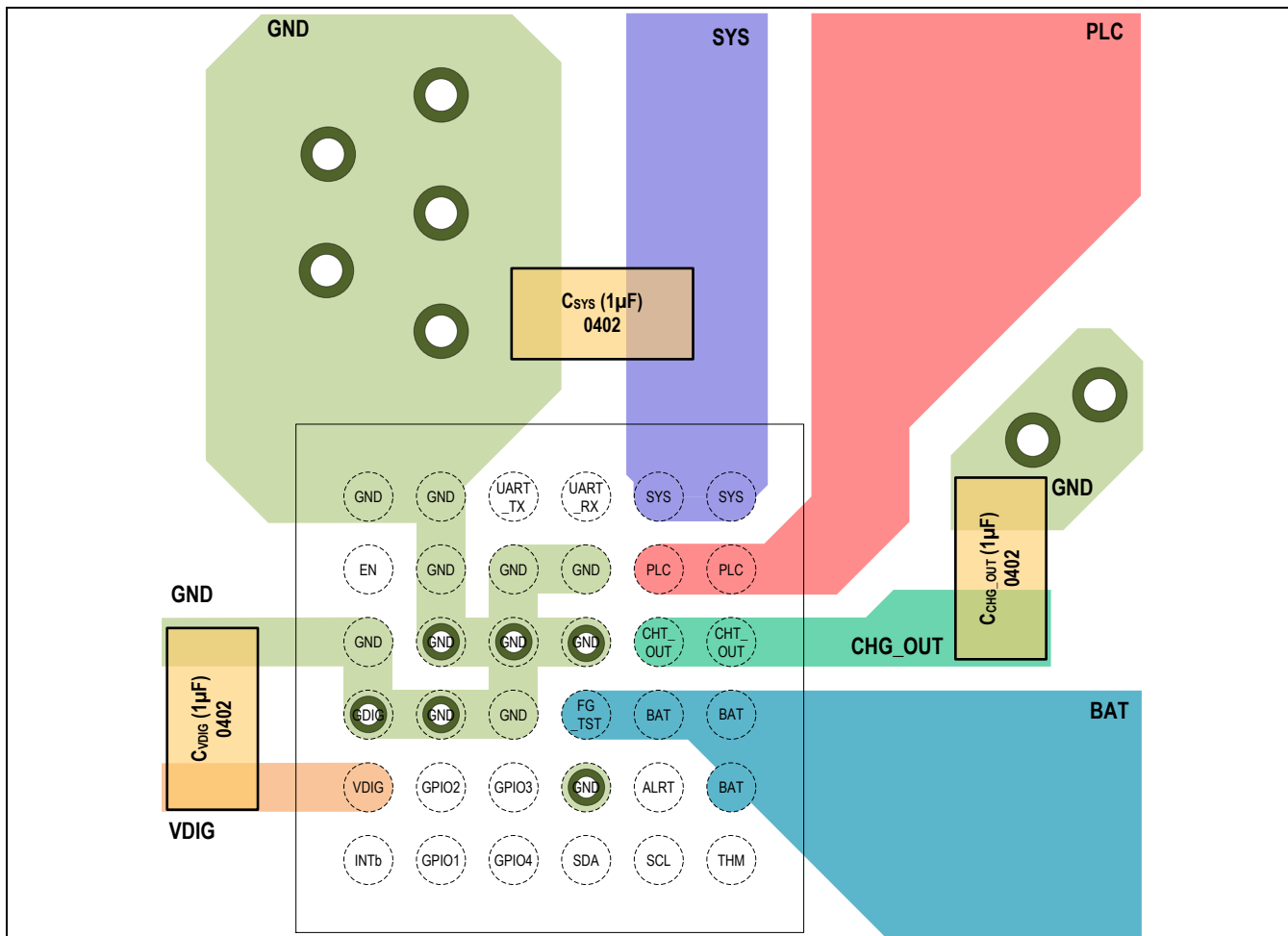


Figure 42. Layout Guideline

## Register Map

### MAX20357 (Slave address 0x15)

| ADDRESS               | NAME                                  | MSB              |             |             |          |              | LSB          |
|-----------------------|---------------------------------------|------------------|-------------|-------------|----------|--------------|--------------|
| <b>USER_INTERRUPT</b> |                                       |                  |             |             |          |              |              |
| 0x00                  | <a href="#">REVISION_ID[7:0]</a><br>1 | Revision_id[7:0] |             |             |          |              |              |
| 0x01                  | <a href="#">Status0[7:0]</a>          | chn_con_sts      | chn_wty_sts | chn_idl_sts | srt_xfer | lng_xfer     | ThmStat[2:0] |
| 0x02                  | <a href="#">Status1[7:0]</a>          | JeitalsReg       | ChgRestaB   | ChgThrmReg  | CC1Tmo   | ChgStat[3:0] |              |

Power Line  
Communication with  
ModelGauge Fuel Gauge  
and Charger

MAX20357

| ADDRESS         | NAME                          | MSB             |                 |                 |                 |                  |                  |                 | LSB           |
|-----------------|-------------------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-----------------|---------------|
| 0x03            | <a href="#">Status2[7:0]</a>  | PLCSumAct       | PLCSumCurr[5:0] |                 |                 |                  |                  |                 | -             |
| 0x04            | <a href="#">Status3[7:0]</a>  | SysMinReg       | ChgRev          | ChgVoltMode     | ChgVoltStp      | ChgGMD           | LDOGMD           | PLCOk           | SysRev        |
| 0x05            | <a href="#">Status4[7:0]</a>  | plc_status[7:0] |                 |                 |                 |                  |                  |                 |               |
| 0x06            | <a href="#">Status5[7:0]</a>  | itf_rdy_sts     | BatUVLOB        | dead_batt       | plc_moi_det     | botcode_ltc[3:0] |                  |                 |               |
| 0x07            | <a href="#">Status6[7:0]</a>  | -               | -               | -               | urt_swcn        | chg_prqip        | swc_off_mod[2:0] |                 |               |
| 0x08            | <a href="#">Int0[7:0]</a>     | PLCSumActInt    | PLCSumCurrInt   | ChgThrmRegInt   | CC1Tmolnt       | ChgStatInt       | SysMinRegInt     | ChgRestaBlnt    | ThmStatInt    |
| 0x09            | <a href="#">Int1[7:0]</a>     | JeitalsRegInt   | ChgRevInt       | ChgVoltModeInt  | ChgVoltStplnt   | ChgGMDInt        | LDOGMDInt        | PLCokInt        | SysRevInt     |
| 0x0A            | <a href="#">Int2[7:0]</a>     | chn_con_Int     | chn_wty_Int     | chn_idl_Int     | srt_xfer_Rise   | srt_xfer_Fall    | plc_new_dat      | plc_cmd_dne     | plc_cmd_err   |
| 0x0B            | <a href="#">Int3[7:0]</a>     | lng_xfer_Int    | BatUVLOBInt     | moi_dne_int     | plc_moi_detInt  | moi_irq_det      | res_det_abr      | res_det_opn     | res_det_gnd   |
| 0x0C            | <a href="#">Int4[7:0]</a>     | urt_tmo_fit     | urt_modfail     | urt_moddone     | urt_swcnInt     | dead_found       | -                | swc_off_modlrq  | chg_prqipIrq  |
| 0x0D            | <a href="#">Int5[7:0]</a>     | itf_rdy_stsInt  | -               | -               | -               | -                | wd_itr_clr       | -               | -             |
| 0x0E            | <a href="#">IntMask0[7:0]</a> | PLCSumActIntM   | PLCSumCurrIntM  | ChgThrmRegIntM  | CC1TmolntM      | ChgStatIntM      | SysMinRegIntM    | ChgRestaBlntM   | ThmStatIntM   |
| 0x0F            | <a href="#">IntMask1[7:0]</a> | JeitalsRegIntM  | ChgRevIntM      | ChgVoltModeIntM | ChgVoltStplntM  | ChgGMDIntM       | LDOGMDIntM       | PLCokIntM       | SysRevIntM    |
| 0x10            | <a href="#">IntMask2[7:0]</a> | chn_con_IntM    | chn_wty_IntM    | chn_idl_IntM    | srt_xfer_RiseM  | srt_xfer_FallM   | plc_new_datM     | plc_cmd_dneM    | plc_cmd_errM  |
| 0x11            | <a href="#">IntMask3[7:0]</a> | lng_xfer_IntM   | BatUVLOBIntM    | moi_dne_intM    | plc_moi_detIntM | moi_irq_detM     | res_det_abrM     | res_det_opnM    | res_det_gndM  |
| 0x12            | <a href="#">IntMask4[7:0]</a> | urt_tmo_fitM    | urt_modfailM    | urt_moddoneM    | urt_swcnIntM    | dead_foundM      | 0                | swc_off_modlrqM | chg_prqipIrqM |
| 0x13            | <a href="#">IntMask5[7:0]</a> | itf_rdy_stsIntM | 0               | 0               | -               | -                | wd_itr_clrM      | -               | -             |
| <b>USER_BOT</b> |                               |                 |                 |                 |                 |                  |                  |                 |               |

| ADDRESS                   | NAME                                   | MSB              |                   |                 |             |              |                  |                   | LSB         |
|---------------------------|--|------------------|-------------------|-----------------|-------------|--------------|------------------|-------------------|-------------|
| 0x1A                      | <a href="#">SYSTEM_REG0[7:0]</a>       | off_cmd_inp      | soft_reset        | hard_reset      | sft_hrd_rst | seal_i2c_cmd | 0                | Stay_ON           | enb_otp_ena |
| 0x1B                      | <a href="#">BOT_CMD[7:0]</a>           | fg__reset        | fg_ena_byp        | fg_ena_val      | -           | -            | -                | -                 | jta_hrs_ena |
| 0x1C                      | <a href="#">BOT_RDB[7:0]</a>           | reset_mode[2:0]  |                   |                 | -           | -            | -                | -                 | -           |
| <b>USER_UART</b>          |  |                  |                   |                 |             |              |                  |                   |             |
| 0x20                      | <a href="#">UART_Ctr0[7:0]</a>         | -                | -                 | -               | -           | -            | urt_auto_en      | rxs_tmo_tim[1:0]  |             |
| 0x21                      | <a href="#">UART_Ctr1[7:0]</a>         | -                | tmo_tmr_ena       | i2c_urt_mod     | i2c_urt_ena | i2c_urt_abr  | i2c_urt_swc      | i2c_tx__swc       | i2c_rx__swc |
| <b>USER_SYSTEM_CONFIG</b> |  |                  |                   |                 |             |              |                  |                   |             |
| 0x30                      | <a href="#">SYSTEM_CONFIG0[7:0]</a>    | chg_wkp_ena      | low_pwr_ena       | -               | lchg_x2     | chg_res_ena  | i2c_ldo_ena      | SYSUVLOThSel[1:0] |             |
| 0x31                      | <a href="#">PLC_CONFIG0[7:0]</a>       | PLCSnkSel[1:0]   |                   | -               | -           | -            | -                | PLCThrSel[1:0]    |             |
| 0x32                      | <a href="#">PLC_CONFIG1[7:0]</a>       | otp_sum_rev      | frc_i2c_sum       | PLCCurr[5:0]    |             |              |                  |                   |             |
| 0x33                      | <a href="#">PLC_CONFIG2[7:0]</a>       | plc_dsc_otp      | PLC_DROP[2:0]     |                 |             | PLC_HLD[1:0] |                  | PLC_HREF[1:0]     |             |
| 0x34                      | <a href="#">PLC_CONFIG3[7:0]</a>       | plc_monitor      | plc_con_sts       | plc_config[2:0] |             |              | DAT_MAX_RTY[2:0] |                   |             |
| 0x35                      | <a href="#">PLC_CONFIG4[7:0]</a>       | plc_fsm_ena      | RAM_is_full       | fifo_master     | fifo_slave  | plc_is_full  | png_timeout      | plc_res_req       | cont_stream |
| 0x36                      | <a href="#">PLC_CONFIG5[7:0]</a>       | no_fifo_slave    | no_seal_mode      | no_uart_mde     | no_idle_mde | -            | -                | -                 | swp_plc_ram |
| 0x37                      | <a href="#">PLC_ARG[7:0]</a>           | plc_cmd_arg[7:0] |                   |                 |             |              |                  |                   |             |
| 0x38                      | <a href="#">PLC_CMD[7:0]</a>           | plc_run_trg      | plc_command[6:0]  |                 |             |              |                  |                   |             |
| 0x39                      | <a href="#">PLC_RX[7:0]</a>            | -                | plc_rx_bytes[6:0] |                 |             |              |                  |                   |             |
| 0x3A                      | <a href="#">Master feed back0[7:0]</a> | mst_SOC_val[7:0] |                   |                 |             |              |                  |                   |             |
| 0x3B                      | <a href="#">Master feed back1[7:0]</a> | mst_FGready      | -                 | -               | -           | -            | -                | -                 | -           |

| ADDRESS             | NAME                                | MSB                  |                 |                  |                    |                  |                      |                  | LSB       |
|---------------------|-------------------------------------|----------------------|-----------------|------------------|--------------------|------------------|----------------------|------------------|-----------|
| 0x3C                | <a href="#">WATCHDOG0[7:0]</a><br>1 | -                    | -               | -                | -                  | wd_rst_type[1:0] |                      | wd__eoc_sel[1:0] |           |
| 0x3D                | <a href="#">SYS_MIN0[7:0]</a>       | PP_drp[2:0]          |                 |                  | SysMinForce        | SysMin[3:0]      |                      |                  |           |
| <b>USER_CHARGER</b> |                                     |                      |                 |                  |                    |                  |                      |                  |           |
| 0x40                | <a href="#">ILimCtrlChg[7:0]</a>    | -                    | -               | -                | -                  | ChgThrmLim[3:0]  |                      |                  |           |
| 0x41                | <a href="#">ChgCur0[7:0]</a>        | -                    | CC1IFChg[6:0]   |                  |                    |                  |                      |                  |           |
| 0x42                | <a href="#">ChgCur1[7:0]</a>        | -                    | CC2IFChg[6:0]   |                  |                    |                  |                      |                  |           |
| 0x43                | <a href="#">ChgCntl0[7:0]</a>       | ChgEn                | ChgAutoStop     | ChgAutoResta     | -                  | -                | CC1Room Only         | CC1TmoLimit      | CC1Enable |
| 0x44                | <a href="#">ChgCntl1[7:0]</a>       | BatReChg[1:0]        |                 | BatReg[5:0]      |                    |                  |                      |                  |           |
| 0x45                | <a href="#">ChgCntl2[7:0]</a>       | -                    | VPChg[2:0]      |                  |                    | IPChg[1:0]       |                      | IChgDone[1:0]    |           |
| 0x46                | <a href="#">ChgTmr[7:0]</a>         | MtChgTmr[1:0]        |                 | PChgTmr[1:0]     |                    | CC1FChgTmr[1:0]  |                      | ChgTmr[1:0]      |           |
| 0x47                | <a href="#">ChgCfg0[7:0]</a>        | -                    | ChgStepHys[2:0] |                  |                    | ChgStepRise[3:0] |                      |                  |           |
| 0x48                | <a href="#">ThmCfg0[7:0]</a>        | ChgCoolCC1IFChg[2:0] |                 |                  | ChgCoolBatReg[1:0] |                  | ChgCoolCC2IFChg[2:0] |                  |           |
| 0x49                | <a href="#">ThmCfg1[7:0]</a>        | ChgRoomCC1IFChg[2:0] |                 |                  | ChgRoomBatReg[1:0] |                  | ChgRoomCC2IFChg[2:0] |                  |           |
| 0x4A                | <a href="#">ThmCfg2[7:0]</a>        | ChgWarmCC1IFChg[2:0] |                 |                  | ChgWarmBatReg[1:0] |                  | ChgWarmCC2IFChg[2:0] |                  |           |
| 0x4B                | <a href="#">ThmCfg3[7:0]</a>        | -                    | -               | ChgT1ThrDef[2:0] |                    |                  | ChgT1ThrCC1[2:0]     |                  |           |
| 0x4C                | <a href="#">ThmCfg4[7:0]</a>        | -                    | -               | ChgT2ThrDef[2:0] |                    |                  | ChgT2ThrCC1[2:0]     |                  |           |
| 0x4D                | <a href="#">ThmCfg5[7:0]</a>        | -                    | -               | ChgT3ThrDef[2:0] |                    |                  | ChgT3ThrCC1[2:0]     |                  |           |
| 0x4E                | <a href="#">ThmCfg6[7:0]</a>        | -                    | -               | ChgT4ThrDef[2:0] |                    |                  | ChgT4ThrCC1[2:0]     |                  |           |
| 0x4F                | <a href="#">ThmCfg7[7:0]</a>        | jta_eoc_sel[1:0]     |                 | -                | -                  | THMPUSE          | ThmEn[2:0]           |                  |           |
| 0x50                | <a href="#">ChgCtr1[7:0]</a>        | i2c_crf_ena          | chg_cc_trk      | ChgStsFCMr g     | vlt_dne_ena        | -                | lng_xfer_op t        | -                | -         |
| 0x51                | <a href="#">ChgCtr2[7:0]</a>        | BattUvloEn a         | BattPullDown    | FrcPChg          | -                  | -                | -                    | vlt_ctr_plc[1:0] |           |
| <b>USER_GPIO</b>    |                                     |                      |                 |                  |                    |                  |                      |                  |           |

| ADDRESS                        | NAME                                 | MSB                  |                |                |                  |                  |                  |                  | LSB                  |
|--------------------------------|--------------------------------------|----------------------|----------------|----------------|------------------|------------------|------------------|------------------|----------------------|
| 0x58                           | <a href="#">GPIO1[7:0]</a>           | -                    | -              | -              | GPIOCompE<br>na1 | GPIOPLC<br>Ctr1  | GPIOEnRe<br>s1   | GPIOEnPup<br>1   | GIODout_<br>1        |
| 0x59                           | <a href="#">GPIO2[7:0]</a>           | -                    | -              | -              | GPIOCompE<br>na2 | GPIOPLC<br>Ctr2  | GPIOEnRe<br>s2   | GPIOEnPup<br>2   | GIODout_<br>2        |
| 0x5A                           | <a href="#">GPIO3[7:0]</a>           | -                    | -              | -              | GPIOCompE<br>na3 | GPIOPLC<br>Ctr3  | GPIOEnRe<br>s3   | GPIOEnPup<br>3   | GIODout_<br>3        |
| 0x5B                           | <a href="#">GPIO4[7:0]</a>           | -                    | -              | -              | GPIOCompE<br>na4 | GPIOPLC<br>Ctr4  | GPIOEnRe<br>s4   | GPIOEnPup<br>4   | GIODout_<br>4        |
| 0x5C                           | <a href="#">GPIO_rdb1[7:0]</a>       | GIODAImp<br>_4       | GIODAImp_<br>3 | GIODAImp_<br>2 | GIODAImp_<br>_1  | -                | -                | -                | GPIOCmos<br>En       |
| 0x5D                           | <a href="#">GPIO_rdb2[7:0]</a>       | -                    | -              | -              | -                | master_G<br>PIO4 | master_GP<br>IO3 | master_GPI<br>O2 | master_GPI<br>O1     |
| <b>USER_DOP_PORT</b>           |                                      |                      |                |                |                  |                  |                  |                  |                      |
| 0x60                           | <a href="#">SOC_byte_1[7:0]</a>      | AVGVCELL_byte_1[7:0] |                |                |                  |                  |                  |                  |                      |
| 0x61                           | <a href="#">SOC_byte_0[7:0]</a>      | AVGVCELL_byte_0[7:0] |                |                |                  |                  |                  |                  |                      |
| 0x62                           | <a href="#">VCELL_byte_1[7:0]</a>    | VCELL_byte_1[7:0]    |                |                |                  |                  |                  |                  |                      |
| 0x63                           | <a href="#">VCELL_byte_0[7:0]</a>    | VCELL_byte_0[7:0]    |                |                |                  |                  |                  |                  |                      |
| 0x64                           | <a href="#">TTE_byte_1[7:0]</a>      | TTE_byte_1[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x65                           | <a href="#">TTE_byte_0[7:0]</a>      | TTE_byte_0[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x66                           | <a href="#">AVGVCELL_byte_1[7:0]</a> | SOC_byte_1[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x67                           | <a href="#">AVGVCELL_byte_0[7:0]</a> | SOC_byte_0[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x68                           | <a href="#">TTF_byte_1[7:0]</a>      | TTF_byte_1[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x69                           | <a href="#">TTF_byte_0[7:0]</a>      | TTF_byte_0[7:0]      |                |                |                  |                  |                  |                  |                      |
| 0x6A                           | <a href="#">READY_REG[7:0]</a>       | dop_rdy_sig          | -              | dop_i2c_ena    | ttf_reg_rdy      | soc_reg_rdy      | tte_reg_rdy      | vcell_reg_rdy    | avgvcell_re<br>g_rdy |
| <b>USER_MOISTURE_DETECTION</b> |                                      |                      |                |                |                  |                  |                  |                  |                      |



| ADDRESS | NAME                              | MSB              |                |                  |            |   |                |                 | LSB         |
|---------|-----------------------------------|------------------|----------------|------------------|------------|---|----------------|-----------------|-------------|
| 0x70    | <a href="#">ADC_CTRL1[7:0]</a>    | –                | AdcGndTrh[3:0] |                  |            |   | ResDetRty[2:0] |                 |             |
| 0x71    | <a href="#">ADC_CTRL2[7:0]</a>    | –                | –              | AdcRng[5:0]      |            |   |                |                 |             |
| 0x72    | <a href="#">ADC_CTRL3[7:0]</a>    | –                | –              | –                | –          | – | AdcAvgNum[2:0] |                 |             |
| 0x73    | <a href="#">ADC_CTRL4[7:0]</a>    | –                | –              | AdcNoiseCtr[5:0] |            |   |                |                 |             |
| 0x74    | <a href="#">MOI_DET_REG1[7:0]</a> | –                | –              | –                | –          | – | –              | RaccDetMlp[1:0] |             |
| 0x75    | <a href="#">MOI_DET_REG2[7:0]</a> | RaccDetMThr[7:0] |                |                  |            |   |                |                 |             |
| 0x76    | <a href="#">MOI_DET_REG3[7:0]</a> | –                | moi_det_aut    | –                | moi_man_pl | – | moi_man_rty    | –               | moi_aut_rty |
| 0x77    | <a href="#">IP_RES_REG[7:0]</a>   | –                | –              | –                | –          | – | –              | IP_RES_DET[1:0] |             |
| 0x78    | <a href="#">ADC_VAL1[7:0]</a>     | ADCAvg[7:0]      |                |                  |            |   |                |                 |             |
| 0x79    | <a href="#">ADC_VAL2[7:0]</a>     | ADCMax[7:0]      |                |                  |            |   |                |                 |             |
| 0x7A    | <a href="#">ADC_VAL3[7:0]</a>     | ADCMin[7:0]      |                |                  |            |   |                |                 |             |

## Register Details

### [REVISION\\_ID \(0x0\)](#)

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | Revision_id[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x11             |   |   |   |   |   |   |   |
| Access Type | Read Only        |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                              |
|-------------|------|--|
| Revision_id | 7:0  | Information about the hardware revision. |

### [Status0 \(0x1\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|-----|---|---|---|---|---|---|---|---|

| Field       | chn_con_sts | chn_wty_sts | chn_idl_sts | srt_xfer  | lng_xfer  | ThmStat[2:0] |
|-------------|-------------|-------------|-------------|-----------|-----------|--------------|
| Reset       | 0x0         | 0x0         | 0x0         | 0x0       | 0x0       | 0x0          |
| Access Type | Read Only   | Read Only   | Read Only   | Read Only | Read Only | Read Only    |

| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
| chn_con_sts | 7    | PLC connection status.  | 0x0: Disconnected<br>0x1: Connected   |
| chn_wty_sts | 6    | Waiting status to conclude connection with master.                  | 0x0: Not in waiting state<br>0x1: In waiting state  |
| chn_idl_sts | 5    | PLC idle status   | 0x0: Not in idle state<br>0x1: Idle state   |
| srt_xfer    | 4    | Short transfer. Set for PLC PING and all PLC command.               | 0x0: No short transfer<br>0x1: Short transfer ongoing   |
| lng_xfer    | 3    | Long transfer. Set for DOUT_REQ PLC command and bulk data transfer. | 0x0: No long transfer<br>0x1: Long transfer ongoing   |
| ThmStat     | 2:0  | JEITA status from thermistor monitoring.                            | 0x0: Cold zone ( $V_{THM\_COLD} < V_{THM} < V_{THM\_DIS}$ )<br>0x1: Cool zone ( $V_{THM\_COOL} < V_{THM} < V_{THM\_COLD}$ )<br>0x2: Room zone ( $V_{THM\_WARM} < V_{THM} < V_{THM\_COOL}$ )<br>0x3: Warm zone ( $V_{THM\_HOT} < V_{THM} < V_{THM\_WARM}$ )<br>0x4: Hot zone ( $V_{THM} < V_{THM\_HOT}$ )<br>0x5: No thermistor detected ( $V_{THM} > V_{THM\_DIS}$ )<br>0x6: Thermistor monitoring disabled. ThmEn = 0x0.<br>0x7: Thermistor monitoring disabled. PLC voltage is not present. ThmEn is not 0x0. |

### Status1 (0x2)

| BIT         | 7          | 6         | 5          | 4         | 3            | 2 | 1 | 0 |
|-------------|------------|-----------|------------|-----------|--------------|---|---|---|
| Field       | JeitalsReg | ChgRestaB | ChgThrmReg | CC1Tmo    | ChgStat[3:0] |   |   |   |
| Reset       | 0x0        | 0x0       | 0x0        | 0x0       | 0x0          |   |   |   |
| Access Type | Read Only  | Read Only | Read Only  | Read Only | Read Only    |   |   |   |

| BITFIELD   | BITS | DESCRIPTION  | DECODE   |
|------------|------|--|--|
| JeitalsReg | 7    | JEITA status of charge current/voltage.  | 0x0: Charge current/voltage is not reduced because of JEITA settings<br>0x1: Charge current/voltage is reduced because of JEITA settings               |
| ChgRestaB  | 6    | Charger restart status. Auto-cleared after charger restart complete. Valid only when charger is enabled ChgEn = 1. | 0x0: No charger restart event<br>0x1: Charger restarts   |
| ChgThrmReg | 5    | Charger thermal shutdown status. Valid only when PLC voltage is present and charger is enabled ChgEn = 1.          | 0x0: Charger operating normally or disabled.<br>0x1: Charger current being actively reduced due to die temperature approaching thermal shutdown limit. |

| BITFIELD | BITS | DESCRIPTION   | DECODE  |
|----------|------|---|---|
| CC1Tmo   | 4    | CC1 timeout status. CC1 timer is set by CC1FChgTmr. | 0x0: CC1 timeout not expired<br>0x1: CC1 Timeout expired  |
| ChgStat  | 3:0  | Charger mode status.                                | 0x0: Charger off<br>0x1: Charger IDLE mode<br>0x2: Pre-charge in progress<br>0x3: Fast-charge constant current mode 1 (CC1) in progress<br>0x4: Fast-charge constant current mode 2 (CC2) in progress<br>0x5: Fast-charge constant voltage mode (CV) in progress<br>0x6: Maintain charge in progress<br>0x7: Maintain charge done<br>0x8: Charger Fault - PChgTmr Expired<br>0x9: Charger Fault - ChgTmr Expired<br>0xE: CC Tracking in progress<br>0xF: Charging suspended due to violation of JEITA temperature limits<br>Other: Reserved |

### Status2 (0x3)

| BIT         | 7         | 6               | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|-----------------|---|---|---|---|---|---|
| Field       | PLCSumAct | PLCSumCurr[5:0] |   |   |   |   |   | – |
| Reset       | 0x0       | 0x0             |   |   |   |   |   | – |
| Access Type | Read Only | Read Only       |   |   |   |   |   | – |

| BITFIELD   | BITS | DESCRIPTION  | DECODE  |
|------------|------|--|---|
| PLCSumAct  | 7    | PLC current limit status.  | 0x0: PLC input current is less than PLCCurr<br>0x1: PLC input current is equal to PLCCurr |
| PLCSumCurr | 6:1  | Realtime PLC input current limit. PLC input current is sum current of charger and SYS LDO. | Decode chart same as PLCCurr.   |

### Status3 (0x4)

| BIT         | 7         | 6         | 5           | 4          | 3         | 2         | 1         | 0         |
|-------------|-----------|-----------|-------------|------------|-----------|-----------|-----------|-----------|
| Field       | SysMinReg | ChgRev    | ChgVoltMode | ChgVoltStp | ChgGMD    | LDOGMD    | PLCOk     | SysRev    |
| Reset       | 0x0       | 0x0       | 0x0         | 0x0        | 0x0       | 0x0       | 0x0       | 0x0       |
| Access Type | Read Only | Read Only | Read Only   | Read Only  | Read Only | Read Only | Read Only | Read Only |

| BITFIELD  | BITS | DESCRIPTION            | DECODE  |
|-----------|------|------------------------|---|
| SysMinReg | 7    | SYS voltage reference. | 0x0: V <sub>sys</sub> is regulated at BAT<br>0x1: V <sub>sys</sub> is regulated at SysMin |

| BITFIELD    | BITS | DESCRIPTION  | DECODE  |
|-------------|------|--|---|
| ChgRev      | 6    | Charger reverse protection status.   | 0x0: $V_{BAT} < V_{PLC}$<br>Charger is in reverse protection<br>0x1: $V_{PLC} > V_{BAT}$  |
| ChgVoltMode | 5    | Charger battery voltage regulation status.   | 0x0: $V_{BAT} < V_{BAT\_REG}$<br>0x1: $V_{BAT} \geq V_{BAT\_REG}$   |
| ChgVoltStp  | 4    | Charger step charge status. Valid only when charger is enabled ChgEn = 1.                        | 0x0: $V_{BAT} < V_{BAT\_STPCHG}$<br>0x1: $V_{BAT} \geq V_{BAT\_STPCHG}$   |
| ChgGMD      | 3    | Charger dropout status. Valid only when PLC voltage is present and charger is enabled ChgEn = 1. | 0x0: Charger current is not reduced due to dropout condition $V_{PLC} - V_{CHG\_OUT} > V_{PLC\_DROP}$<br>0x1: Charger current is actively reduced due to a dropout condition $V_{PLC} - V_{CHG\_OUT} < V_{PLC\_DROP}$ |
| LDOGMD      | 2    | SYS LDO dropout status. Valid only when PLC voltage is present and SYS LDO is active.            | 0x0: SYS LDO current is not reduced due to dropout condition $V_{PLC} - V_{SYS} > V_{PLC\_DROP}$<br>0x1: SYS LDO current is actively reduced due to a dropout condition $V_{PLC} - V_{SYS} < V_{PLC\_DROP}$           |
| PLCOk       | 1    | PLC voltage status.  | 0: $V_{PLC} < V_{PLCDET}$ : PLC input voltage not present<br>1: $V_{PLC} > V_{PLCDET}$  |
| SysRev      | 0    | SYS LDO reverse protection status.   | 0x0: $V_{PLC} < V_{SYS}$<br>SYS LDO is in reverse protection<br>0x1: $V_{PLC} > V_{SYS}$  |

#### Status4 (0x5)

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | plc_status[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION  | DECODE   |
|------------|------|--|--|
| plc_status | 7:0  | PLC communication status. Valid on plc_cmd_dne or plc_cmd_err interrupt. | 0x00: NO_PLC_ERROR. No error.<br>0x10: NACK_TO_CMD. Master sends NACK to slave command request.<br>0x11: NACK_TO_DATA. Master sends NACK to slave data packet. Only valid for short data transfer.<br>0x12: NOPLC_ON_CMD. PLC voltage disappears during PING.<br>0x14: NACK_N_DOUTR. NACK limit to DOUT_REQ is hit. Only valid for bulk data transfer. NACK limit is set by plc_config.<br>0x15: ERR_N_DOUTR. NACK limit to data packet is hit. Only valid for bulk data transfer. NACK limit is set by DAT_MAX_RTY.<br>0x18: MST_TMO_ERR. Slave is waiting for a (N)ACK from master but there is no response until timeout.<br>0x19: PLC_BUSY_ERR. Timer expired and slave receives more than 128 bytes of data.<br>0x1B: BAD_CMD_TX, Write wrong command or command argument in PLC_CMD and PLC_ARG.<br>0x1C: BAD_CMD_RX, Expect (N)ACK from master but receive other packet.<br>0x1D: PLC_DATA_ERR, Received corrupted (N)ACK |

| BITFIELD | BITS | DESCRIPTION | DECODE                                  |
|----------|------|-------------|---|
|          |      |             | packets from master.<br>Other: Reserved |

### Status5 (0x6)

| BIT         | 7           | 6         | 5         | 4           | 3                | 2 | 1 | 0 |
|-------------|-------------|-----------|-----------|-------------|------------------|---|---|---|
| Field       | itf_rdy_sts | BatUVLOB  | dead_batt | plc_moi_det | botcode_ltc[3:0] |   |   |   |
| Reset       | 0x1         | 0x0       | 0x0       | 0x0         | 0x0              |   |   |   |
| Access Type | Read Only   | Read Only | Read Only | Read Only   | Read Only        |   |   |   |

| BITFIELD    | BITS | DESCRIPTION  | DECODE   |
|-------------|------|--|--|
| itf_rdy_sts | 7    | OTP Loading Complete.  | 0x0: OTP loading not completed<br>0x1: OTP loading completed                                 |
| BatUVLOB    | 6    | Battery voltage UVLO status. Valid only when PLC input voltage is present, PLCOk = 1, chn_con_sts = 1 and chn_wty_sts = 0.                   | 0x0: $V_{BAT} < V_{BAT\_UVLO}$<br>0x1: $V_{BAT} > V_{BAT\_UVLO}$                             |
| dead_batt   | 5    | Dead battery found. Dead battery check is performed when device is waked up from SYSUVLO, SEAL and soft + hard reset by discharging BAT pin. | 0x0: Active battery<br>0x1: Dead battery   |
| plc_moi_det | 4    | PLC moisture detection status.   | 0x0: No moisture detected<br>0x1: Moisture detected  |
| botcode_ltc | 3:0  | Specify what cause the device to restart   | 0x0: Nothing<br>0x1: OFF<br>0x2: SEAL<br>0x4: SYSUVLO<br>0x8: Thermal shutdown<br>Others: NA |

### Status6 (0x7)

| BIT         | 7 | 6 | 5 | 4           | 3           | 2                | 1 | 0 |
|-------------|---|---|---|-------------|-------------|------------------|---|---|
| Field       | – | – | – | urt_swc_opn | chg_prq_inp | swc_off_mod[2:0] |   |   |
| Reset       | – | – | – | 0x0         | 0x0         | 0x0              |   |   |
| Access Type | – | – | – | Read Only   | Read Only   | Read Only        |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| urt_swc_opn | 4    | UART switches are open due to UART timeout after 0.5s of UART line idle. Valid only when tmo_tmr_ena = 1. | 0x0: No UART switch open event due to timeout<br>0x1: UART switch is open due to timeout.                        |
| chg_prq_inp | 3    | Pre-charge status. Valid only when ChgEn = 1.   | 0x0: $V_{BAT} < V_{BAT\_PCHG}$<br>0x1: $V_{BAT} \geq V_{BAT\_PCHG}$  |
| swc_off_mod | 2:0  | Indicator for device shutdown within 20ms.  | 0x0: Nothing<br>0x1: OFF (in 20ms)<br>0x2: SEAL (in 20ms)<br>0x3: SYSUVLO (in 20ms)<br>0x4: Others<br>Others: NA |

### Int0 (0x8)

| BIT         | 7            | 6             | 5             | 4           | 3           | 2            | 1            | 0           |
|-------------|--------------|---------------|---------------|-------------|-------------|--------------|--------------|-------------|
| Field       | PLCSumActInt | PLCSumCurrInt | ChgThrmRegInt | CC1TmoInt   | ChgStatInt  | SysMinRegInt | ChgRestaBInt | ThmStatInt  |
| Reset       | 0x0          | 0x0           | 0x0           | 0x0         | 0x0         | 0x0          | 0x0          | 0x0         |
| Access Type | Write, Read  | Write, Read   | Write, Read   | Write, Read | Write, Read | Write, Read  | Write, Read  | Write, Read |

| BITFIELD      | BITS | DESCRIPTION  | DECODE   |
|---------------|------|--|--|
| PLCSumActInt  | 7    | PLC sum current limit interrupt. Asserted if a change occurs on PLCSumAct.     | 0x0: Status is not changed<br>0x1: Status is changed |
| PLCSumCurrInt | 6    | PLC sum current interrupt. Asserted if a change occurs on PLCSumCurr.          | 0x0: Status is not changed<br>0x1: Status is changed |
| ChgThrmRegInt | 5    | Charger thermal shutdown interrupt. Asserted if a change occurs on ChgThrmReg. | 0x0: Status is not changed<br>0x1: Status is changed |
| CC1TmoInt     | 4    | CC1 timeout interrupt. Asserted if a change occurs on CC1Tmo.                  | 0x0: Status is not changed<br>0x1: Status is changed |
| ChgStatInt    | 3    | Charger mode interrupt. Asserted if a change occurs on ChgStat.                | 0x0: Status is not changed<br>0x1: Status is changed |
| SysMinRegInt  | 2    | SYS voltage reference interrupt. Asserted if a change occurs on SysMinReg.     | 0x0: Status is not changed<br>0x1: Status is changed |
| ChgRestaBInt  | 1    | Charger restart interrupt. Asserted if a change occurs on ChgRestaB.           | 0x0: Status is not changed<br>0x1: Status is changed |
| ThmStatInt    | 0    | JEITA thermal monitoring interrupt. Asserted if a change occurs on ThmStat.    | 0x0: Status is not changed<br>0x1: Status is changed |

**Int1 (0x9)**

| BIT                | 7             | 6           | 5               | 4             | 3           | 2           | 1           | 0           |
|--------------------|---------------|-------------|-----------------|---------------|-------------|-------------|-------------|-------------|
| <b>Field</b>       | JeitalsRegInt | ChgRevInt   | ChgVoltModelInt | ChgVoltStpInt | ChgGMDInt   | LDOGMDInt   | PLCokInt    | SysRevInt   |
| <b>Reset</b>       | 0x0           | 0x0         | 0x0             | 0x0           | 0x0         | 0x0         | 0x0         | 0x0         |
| <b>Access Type</b> | Write, Read   | Write, Read | Write, Read     | Write, Read   | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD        | BITS | DESCRIPTION   | DECODE  |
|-----------------|------|---|---|
| JeitalsRegInt   | 7    | JEITA charger current/voltage interrupt. Asserted if a change occurs on JeitalsReg.       | 0x0: Status is not changed<br>0x1: Status is changed  |
| ChgRevInt       | 6    | Charger reverse protection interrupt. Asserted if a change occurs on ChgRev.              | 0x0: Status is not changed<br>0x1: Status is changed  |
| ChgVoltModelInt | 5    | Charger battery voltage regulation interrupt. Asserted if a change occurs on ChgVoltMode. | 0x0: Status is not changed<br>0x1: Status is changed  |
| ChgVoltStpInt   | 4    | Charger step charge interrupt. Asserted if a change occurs on ChgVoltstp.                 | 0x0: Status is not changed<br>0x1: Status is changed  |
| ChgGMDInt       | 3    | Charger dropout interrupt. Asserted if a change occurs on ChgGMD.                         | 0: Charger current is not actively being reduced to regulate V <sub>CHGOUT</sub><br>1: Charger current actively being reduced to regulate V <sub>CHGOUT</sub> |
| LDOGMDInt       | 2    | SYS LDO dropout interrupt. Asserted if a change occurs on LDOGMD.                         | 0x0: Status is not changed<br>0x1: Status is changed  |
| PLCokInt        | 1    | PLC voltage interrupt. Asserted if a change occurs on PLCOk.                              | 0x0: Status is not changed<br>0x1: Status is changed  |
| SysRevInt       | 0    | SYS LDO reverse protection interrupt. Asserted if a change occurs on SysRev.              | 0x0: Status is not changed<br>0x1: Status is changed  |

**Int2 (0xA)**

| BIT                | 7           | 6           | 5           | 4             | 3             | 2           | 1           | 0           |
|--------------------|-------------|-------------|-------------|---------------|---------------|-------------|-------------|-------------|
| <b>Field</b>       | chn_con_Int | chn_wty_Int | chn_idl_Int | srt_xfer_Rise | srt_xfer_Fall | plc_new_dat | plc_cmd_dne | plc_cmd_err |
| <b>Reset</b>       | 0x0         | 0x0         | 0x0         | 0x0           | 0x0           | 0x0         | 0x0         | 0x0         |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read | Write, Read   | Write, Read   | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| chn_con_Int | 7    | PLC connection interrupt. Asserted if a change occurs on chn_con_sts. | 0x0: Status is not changed<br>0x1: Status is changed |

| BITFIELD      | BITS | DESCRIPTION  | DECODE   |
|---------------|------|--|--|
| chn_wty_Int   | 6    | PLC waiting interrupt. Asserted if a change occurs on chn_wty_sts .        | 0x0: Status is not changed<br>0x1: Status is changed                       |
| chn_idl_Int   | 5    | PLC idle interrupt. Asserted if a change occurs on chn_idl_sts.            | 0x0: Status is not changed<br>0x1: Status is changed                       |
| srt_xfer_Rise | 4    | Short transfer rising interrupt. Asserted if srt_xfer changes from 0 to 1. | 0x0: Status does not change from 0 to 1<br>0x1: Status changes from 0 to 1 |
| srt_xfer_Fall | 3    | Short transfer rising interrupt. Asserted if srt_xfer changes from 1 to 0. | 0x0: Status does not change from 1 to 0<br>0x1: Status changes from 1 to 0 |
| plc_new_dat   | 2    | PLC new data interrupt.  | 0x0: No new data available<br>0x1: New data available in RAM               |
| plc_cmd_dne   | 1    | PLC command done interrupt.  | 0x0: PLC command not completed<br>0x1: PLC command done                    |
| plc_cmd_err   | 0    | PLC command error interrupt.   | 0x0: PLC command no error<br>0x1: PLC command error occurred               |

### Int3 (0xB)

| BIT         | 7            | 6           | 5           | 4              | 3           | 2           | 1           | 0           |
|-------------|--------------|-------------|-------------|----------------|-------------|-------------|-------------|-------------|
| Field       | lng_xfer_Int | BatUVLOInt  | moi_dne_int | plc_moi_detInt | moi_irq_det | res_det_abr | res_det_opn | res_det_gnd |
| Reset       | 0x0          | 0x0         | 0x0         | 0x0            | 0x0         | 0x0         | 0x0         | 0x0         |
| Access Type | Write, Read  | Write, Read | Write, Read | Write, Read    | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD       | BITS | DESCRIPTION   | DECODE   |
|----------------|------|---|--|
| lng_xfer_Int   | 7    | Long transfer interrupt. Asserted if a change occurs on lng_xfer.   | 0x0: Status is not changed<br>0x1: Status is changed   |
| BatUVLOInt     | 6    | Battery voltage UVLO interrupt. Asserted if a change occurs on BatUVLOB.  | 0x0: Status is not changed<br>0x1: Status is changed   |
| moi_dne_int    | 5    | Moisture detection done interrupt. It occurs when a moisture measure is completed.  | 0x0: Moisture measurement is not completed<br>0x1: Moisture measurement is completed             |
| plc_moi_detInt | 4    | Moisture detection interrupt for PLC. It occurs when a moisture is detected on PLC. Asserted if a change occurs on plc_moi_det. | 0x0: Status is not changed<br>0x1: Status is changed   |
| moi_irq_det    | 3    | Moisture detection measurement valid result interrupt.  | 0x0: Moisture detection valid value not detected<br>0x1: Moisture detection valid value detected |
| res_det_abr    | 2    | Abort resistive measurement result interrupt.   | 0x0: Abort resistive value not detected<br>0x1: Abort resistive value detected                   |
| res_det_opn    | 1    | Open resistive measurement result interrupt.  | 0x0: Open resistive value not detected<br>0x1: Open resistive value detected                     |
| res_det_gnd    | 0    | Ground resistive measurement result interrupt.  | 0x0: Ground resistive value not detected<br>0x1: Ground resistive value detected                 |



**Int4 (0xC)**

| BIT                | 7           | 6           | 5           | 4              | 3           | 2 | 1              | 0              |
|--------------------|-------------|-------------|-------------|----------------|-------------|---|----------------|----------------|
| <b>Field</b>       | urt_tmo_flt | urt_modfail | urt_moddone | urt_swc_opnInt | dead_found  | – | swc_off_modIrq | chg_prq_inplrQ |
| <b>Reset</b>       | 0x0         | 0x0         | 0x0         | 0x0            | 0x0         | – | 0x0            | 0x0            |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read | Write, Read    | Write, Read | – | Write, Read    | Write, Read    |

| BITFIELD       | BITS | DESCRIPTION  | DECODE   |
|----------------|------|--|--|
| urt_tmo_flt    | 7    | UART timeout interrupt.  | 0x0: UART mode timeout not expired<br>0x1: UART mode timeout expired |
| urt_modfail    | 6    | UART mode fail interrupt.  | 0x0: UART mode not failed<br>0x1: UART mode failed                   |
| urt_moddone    | 5    | UART mode done interrupt. Asserted when device enters/exits UART mode.                 | 0x0: No UART mode done event<br>0x1: UART mode done                  |
| urt_swc_opnInt | 4    | UART switch open due to timeout interrupt. Asserted if a change occurs on urt_swc_opn. | 0x0: Status is not changed<br>0x1: Status is changed                 |
| dead_found     | 3    | PLC detection found master in dead battery condition.                                  | 0x0: No dead master<br>0x1: Dead master found                        |
| swc_off_modIrq | 1    | Asserted if a change occurs on swc_off_mod.  | 0x0: Status is not changed<br>0x1: Status is changed                 |
| chg_prq_inplrQ | 0    | Asserted if a change occurs on chg_prq_inp.  | 0x0: Status is not changed<br>0x1: Status is changed                 |

**Int5 (0xD)**

| BIT                | 7              | 6 | 5 | 4 | 3 | 2           | 1 | 0 |
|--------------------|----------------|---|---|---|---|-------------|---|---|
| <b>Field</b>       | itf_rdy_stsInt | – | – | – | – | wd__itr_clr | – | – |
| <b>Reset</b>       | 0x1            | – | – | – | – | 0x0         | – | – |
| <b>Access Type</b> | Write, Read    | – | – | – | – | Write, Read | – | – |

| BITFIELD       | BITS | DESCRIPTION   | DECODE   |
|----------------|------|---|--|
| itf_rdy_stsInt | 7    | OTP loading complete. Device is ready to communicate via I2C after this bit is asserted. Asserted if a change occurs on itf_rdy_sts.      | 0x0: Status is not changed<br>0x1: Status is changed                         |
| wd__itr_clr    | 2    | Read this bit with in watchdog time limit to prevent device reset. This bit may reset itself if watchdog type choose to reset the device. | 0x0: Bit read. Device will not reset<br>0x1: Bit not read since last timeout |

**IntMask0 (0xE)**

| BIT         | 7                 | 6                  | 5                  | 4              | 3               | 2                 | 1                 | 0               |
|-------------|-------------------|--------------------|--------------------|----------------|-----------------|-------------------|-------------------|-----------------|
| Field       | PLCSumActInt<br>M | PLCSumCurrInt<br>M | ChgThrmRegInt<br>M | CC1Tmolnt<br>M | ChgStatInt<br>M | SysMinRegInt<br>M | ChgRestaBInt<br>M | ThmStatInt<br>M |
| Reset       | 0x0               | 0x0                | 0x0                | 0x0            | 0x0             | 0x0               | 0x0               | 0x0             |
| Access Type | Write, Read       | Write, Read        | Write, Read        | Write, Read    | Write, Read     | Write, Read       | Write, Read       | Write, Read     |

| BITFIELD       | BITS | DESCRIPTION                    | DECODE                       |
|----------------|------|--------------------------------|------------------------------|
| PLCSumActIntM  | 7    | PLCSumActInt interrupt mask.   | 0x0: Masked<br>0x1: Unmasked |
| PLCSumCurrIntM | 6    | PLCSumCurrInt interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| ChgThrmRegIntM | 5    | ChgThrmRegIntM interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| CC1TmolntM     | 4    | CC1Tmolnt interrupt mask.      | 0x0: Masked<br>0x1: Unmasked |
| ChgStatIntM    | 3    | ChgStatInt interrupt mask.     | 0x0: Masked<br>0x1: Unmasked |
| SysMinRegIntM  | 2    | SysMinRegInt interrupt mask.   | 0x0: Masked<br>0x1: Unmasked |
| ChgRestaBIntM  | 1    | ChgRestaBInt interrupt mask.   | 0x0: Masked<br>0x1: Unmasked |
| ThmStatIntM    | 0    | ThmStatInt interrupt mask.     | 0x0: Masked<br>0x1: Unmasked |

**IntMask1 (0xF)**

| BIT         | 7              | 6           | 5               | 4              | 3           | 2           | 1           | 0           |
|-------------|----------------|-------------|-----------------|----------------|-------------|-------------|-------------|-------------|
| Field       | JeitalsRegIntM | ChgRevIntM  | ChgVoltModelntM | ChgVoltStpIntM | ChgGMDIntM  | LDOGMDIntM  | PLCokIntM   | SysRevIntM  |
| Reset       | 0x0            | 0x0         | 0x0             | 0x0            | 0x0         | 0x0         | 0x0         | 0x0         |
| Access Type | Write, Read    | Write, Read | Write, Read     | Write, Read    | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD        | BITS | DESCRIPTION                    | DECODE                       |
|-----------------|------|--------------------------------|------------------------------|
| JeitalsRegIntM  | 7    | JeitalsRegInt interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| ChgRevIntM      | 6    | ChgRevInt interrupt mask.      | 0x0: Masked<br>0x1: Unmasked |
| ChgVoltModelntM | 5    | ChgVoltModelnt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| ChgVoltStpIntM  | 4    | ChgVoltStpInt interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| ChgGMDIntM      | 3    | ChgGMDInt interrupt mask.      | 0x0: Masked<br>0x1: Unmasked |

| BITFIELD   | BITS | DESCRIPTION               | DECODE                       |
|------------|------|---------------------------|------------------------------|
| LDOGMDIntM | 2    | LDOGMDInt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| PLCokIntM  | 1    | PLCokInt interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| SysRevIntM | 0    | SysRevInt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |

### IntMask2 (0x10)

| BIT         | 7            | 6            | 5            | 4              | 3              | 2            | 1            | 0            |
|-------------|--------------|--------------|--------------|----------------|----------------|--------------|--------------|--------------|
| Field       | chn_con_IntM | chn_wty_IntM | chn_idl_IntM | srt_xfer_RiseM | srt_xfer_FallM | plc_new_datM | plc_cmd_dneM | plc_cmd_errM |
| Reset       | 0x0          | 0x0          | 0x0          | 0x0            | 0x0            | 0x0          | 0x0          | 0x0          |
| Access Type | Write, Read  | Write, Read  | Write, Read  | Write, Read    | Write, Read    | Write, Read  | Write, Read  | Write, Read  |

| BITFIELD       | BITS | DESCRIPTION                  | DECODE                       |
|----------------|------|------------------------------|------------------------------|
| chn_con_IntM   | 7    | chn_con_Int interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| chn_wty_IntM   | 6    | chn_wty_Int interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| chn_idl_IntM   | 5    | chn_idl_Int interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| srt_xfer_RiseM | 4    | srt_xfer_Int interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| srt_xfer_FallM | 3    | srt_xfer_Int interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| plc_new_datM   | 2    | plc_new_dat interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| plc_cmd_dneM   | 1    | plc_cmd_dne interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |
| plc_cmd_errM   | 0    | plc_cmd_err interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |

### IntMask3 (0x11)

| BIT         | 7             | 6            | 5            | 4               | 3            | 2            | 1            | 0            |
|-------------|---------------|--------------|--------------|-----------------|--------------|--------------|--------------|--------------|
| Field       | lng_xfer_IntM | BatUVLOBIntM | moi_dne_intM | plc_moi_detIntM | moi_irq_detM | res_det_abrM | res_det_opnM | res_det_gndM |
| Reset       | 0x0           | 0x0          | 0x0          | 0x0             | 0x0          | 0x0          | 0x0          | 0x0          |
| Access Type | Write, Read   | Write, Read  | Write, Read  | Write, Read     | Write, Read  | Write, Read  | Write, Read  | Write, Read  |

| BITFIELD        | BITS | DESCRIPTION                    | DECODE                       |
|-----------------|------|--------------------------------|------------------------------|
| Ing_xfer_IntM   | 7    | Ing_xfer_Int interrupt mask.   | 0x0: Masked<br>0x1: Unmasked |
| BatUVLOBIntM    | 6    | BatUVLOBInt interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| moi_dne_intM    | 5    | moi_dne_int interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| plc_moi_detIntM | 4    | plc_moi_detInt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| moi_irq_detM    | 3    | moi_irq_det interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| res_det_abrM    | 2    | res_det_abr interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| res_det_opnM    | 1    | res_det_opn interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| res_det_gndM    | 0    | res_det_gnd interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |

#### IntMask4 (0x12)

| BIT         | 7            | 6            | 5            | 4               | 3           | 2           | 1               | 0              |
|-------------|--------------|--------------|--------------|-----------------|-------------|-------------|-----------------|----------------|
| Field       | urt_tmo_fitM | urt_modfailM | urt_moddoneM | urt_swc_opnIntM | dead_foundM | 0           | swc_off_modIrqM | chg_prq_inplrM |
| Reset       | 0x0          | 0x0          | 0x0          | 0x0             | 0x0         | 0x0         | 0x0             | 0x0            |
| Access Type | Write, Read  | Write, Read  | Write, Read  | Write, Read     | Write, Read | Write, Read | Write, Read     | Write, Read    |

| BITFIELD        | BITS | DESCRIPTION                    | DECODE                       |
|-----------------|------|--------------------------------|------------------------------|
| urt_tmo_fitM    | 7    | urt_tmo_fit interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| urt_modfailM    | 6    | urt_modfail interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| urt_moddoneM    | 5    | urt_moddone interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |
| urt_swc_opnIntM | 4    | urt_swc_opnInt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| dead_foundM     | 3    | dead_found interrupt mask.     | 0x0: Masked<br>0x1: Unmasked |
| 0               | 2    | Reserved.                      | Keep 0. Do not change.       |
| swc_off_modIrqM | 1    | swc_off_modIrq interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| chg_prq_inplrM  | 0    | chg_prq_inplr interrupt mask.  | 0x0: Masked<br>0x1: Unmasked |

#### IntMask5 (0x13)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|-----|---|---|---|---|---|---|---|---|

|                    |                 |             |             |   |   |              |   |   |
|--------------------|-----------------|-------------|-------------|---|---|--------------|---|---|
| <b>Field</b>       | itf_rdy_stsIntM | 0           | 0           | – | – | wd__itr_clrM | – | – |
| <b>Reset</b>       | 0x1             | 0b0         | 0b0         | – | – | 0x0          | – | – |
| <b>Access Type</b> | Write, Read     | Write, Read | Write, Read | – | – | Write, Read  | – | – |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>             | <b>DECODE</b>                |
|-----------------|-------------|--------------------------------|------------------------------|
| itf_rdy_stsIntM | 7           | itf_rdy_stsInt interrupt mask. | 0x0: Masked<br>0x1: Unmasked |
| 0               | 6           | Reserved                       | Keep 0. Do not change.       |
| 0               | 5           | Reserved                       | Keep 0. Do not change.       |
| wd__itr_clrM    | 2           | wd__itr_clr interrupt mask.    | 0x0: Masked<br>0x1: Unmasked |

### SYSTEM\_REG0 (0x1A)

|                    |             |             |             |             |              |             |             |             |
|--------------------|-------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|
| <b>BIT</b>         | <b>7</b>    | <b>6</b>    | <b>5</b>    | <b>4</b>    | <b>3</b>     | <b>2</b>    | <b>1</b>    | <b>0</b>    |
| <b>Field</b>       | off_cmd_inp | soft_reset  | hard_reset  | sft_hrd_rst | seal_i2c_cmd | 0           | Stay_ON     | enb_otp_ena |
| <b>Reset</b>       | 0x0         | 0x0         | 0x0         | 0x0         | 0x0          | 0x0         | 0x1         | 0x0         |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read  | Write, Read | Write, Read | Write, Read |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>                              | <b>DECODE</b>  |
|-----------------|-------------|---|--|
| off_cmd_inp     | 7           | OFF mode request.                               | 0x0: No request<br>0x1: Request to enter OFF mode                      |
| soft_reset      | 6           | soft reset request.                             | 0x0: No request<br>0x1: Request soft reset                             |
| hard_reset      | 5           | Hard reset request. Autoclear after hard reset. | 0x0: No request<br>0x1: Request hard reset                             |
| sft_hrd_rst     | 4           | Soft and hard reset request.                    | 0x0: No request<br>0x1: Request soft and hard reset                    |
| seal_i2c_cmd    | 3           | SEAL request.                                   | 0x0: No request<br>0x1: Request to enter SEAL mode                     |
| 0               | 2           | Reserved.                                       | Keep 0. Do not change.   |
| Stay_ON         | 1           | Device stays on after turn on.                  | 0x0: 500ms shutdown timer enabled<br>0x1: Device remains ON            |
| enb_otp_ena     | 0           | EN pin functionality.                           | 0x0: EN pin does not control OFF mode<br>0x1: EN pin controls OFF mode |

### BOT\_CMD (0x1B)

|              |            |            |            |          |          |          |          |             |
|--------------|------------|------------|------------|----------|----------|----------|----------|-------------|
| <b>BIT</b>   | <b>7</b>   | <b>6</b>   | <b>5</b>   | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b>    |
| <b>Field</b> | fg___reset | fg_ena_byp | fg_ena_val | –        | –        | –        | –        | jta_hrs_ena |

|                    |             |             |             |   |   |   |   |             |
|--------------------|-------------|-------------|-------------|---|---|---|---|-------------|
| <b>Reset</b>       | 0x0         | 0x0         | 0x0         | - | - | - | - | 0x0         |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read | - | - | - | - | Write, Read |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>   | <b>DECODE</b>   |
|-----------------|-------------|--|---|
| fg___reset      | 7           | Fuel Gauge reset. Autoclear when done.   | 0x0: No request<br>0x1: Request fuel gauge reset  |
| fg_ena_byp      | 6           | Fuel gauge manual enable functionality.  | 0x0: Fuel gauge manual enable feature disabled<br>0x1: Fuel gauge manual enable feature enabled |
| fg_ena_val      | 5           | Fuel gauge manual enable. Valid if fg_ena_byp = 1.                                 | 0x0: Fuel gauge off<br>0x1: Fuel gauge on   |
| jta_hrs_ena     | 0           | Enable JEITA hard reset when there is no PLC present. Valid only when ThmEn > 0x3. | 0x0: Disable<br>0x1: Enable   |

### BOT\_RDB (0x1C)

| <b>BIT</b>         | <b>7</b>        | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
|--------------------|-----------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Field</b>       | reset_mode[2:0] |          |          | -        | -        | -        | -        | -        |
| <b>Reset</b>       | 0x0             |          |          | -        | -        | -        | -        | -        |
| <b>Access Type</b> | Read Only       |          |          | -        | -        | -        | -        | -        |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>   | <b>DECODE</b>   |
|-----------------|-------------|--|---|
| reset_mode      | 7:5         | Last reset conducted by the device since the device is on. | 0x0: No reset<br>0x1: Soft reset<br>0x2: Hard reset<br>0x3: Hard and soft reset<br>0x4: UBOOT Reset<br>Others: NA |

### UART\_Ctr0 (0x20)

| <b>BIT</b>         | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b>    | <b>1</b>         | <b>0</b> |
|--------------------|----------|----------|----------|----------|----------|-------------|------------------|----------|
| <b>Field</b>       | -        | -        | -        | -        | -        | urt_auto_en | rxs_tmo_tim[1:0] |          |
| <b>Reset</b>       | -        | -        | -        | -        | -        | 0x0         | 0x0              |          |
| <b>Access Type</b> | -        | -        | -        | -        | -        | Write, Read | Write, Read      |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>             | <b>DECODE</b>               |
|-----------------|-------------|--------------------------------|-----------------------------|
| urt_auto_en     | 2           | UART automtatic switch enable. | 0x0: Disable<br>0x1: Enable |

| BITFIELD    | BITS | DESCRIPTION  | DECODE   |
|-------------|------|--|--|
| rxs_tmo_tim | 1:0  | UART automatic switch timeout from RX to TX.<br>Valid only when urt_auto_en = 1. | 0x0: 8µs<br>0x1: 32µs<br>0x2: 64µs<br>0x3: 128µs |

### UART\_Ctr1 (0x21)

| BIT         | 7 | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|-------------|---|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field       | – | tmo_tmr_ena | i2c_urt_mod | i2c_urt_ena | i2c_urt_abr | i2c_urt_swc | i2c_tx__swc | i2c_rx__swc |
| Reset       | – | 0b1         | 0b0         | 0b0         | 0b0         | 0b0         | 0b0         | 0b0         |
| Access Type | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION                                 | DECODE   |
|-------------|------|---|--|
| tmo_tmr_ena | 6    | UART timeout.                               | 0x0: Disable<br>0x1: Enable  |
| i2c_urt_mod | 5    | UART enter/exit through PLC or I2C control. | 0x0: UART enter and exit controlled by PLC<br>0x1: UART enter and exit controlled by I2C |
| i2c_urt_ena | 4    | Enter UART mode (I2C).                      | 0x0: Not enter UART mode<br>0x1: Enter UART mode   |
| i2c_urt_abr | 3    | Abort UART mode (I2C).                      | 0x0: Not abort<br>0x1: Abort   |
| i2c_urt_swc | 2    | UART switch PLC or I2C control.             | 0x0: PLC control<br>0x1: I2C control   |
| i2c_tx__swc | 1    | TX switch I2C enable.                       | 0x0: Open<br>0x1: Closed   |
| i2c_rx__swc | 0    | RX switch I2C enable.                       | 0x0: Open<br>0x1: Closed   |

### SYSTEM\_CONFIG0 (0x30)

| BIT         | 7           | 6           | 5 | 4           | 3           | 2           | 1                 | 0 |
|-------------|-------------|-------------|---|-------------|-------------|-------------|-------------------|---|
| Field       | chg_wkp_ena | low_pwr_ena | – | lchg_x2     | chg_res_ena | i2c_ldo_ena | SYSUVLOThSel[1:0] |   |
| Reset       | 0x1         | 0x1         | – | 0x0         | 0x0         | 0x1         | 0x0               |   |
| Access Type | Write, Read | Write, Read | – | Write, Read | Write, Read | Write, Read | Write, Read       |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
| chg_wkp_ena | 7    | Charger wakeup control when V <sub>BAT</sub> is less than recharge voltage threshold. | 0x0: V <sub>BAT</sub> greater than recharge voltage threshold doesn't wake up the PLC FSM<br>0x1: V <sub>BAT</sub> less than re-charge voltage threshold wakes up the PLC FSM |
| low_pwr_ena | 6    | Low power mode enable.  | 0x0: Disable<br>0x1: Enable   |

| BITFIELD     | BITS | DESCRIPTION   | DECODE  |
|--------------|------|---|---|
| lchg_x2      | 4    | PLC, charger and SYS LDO current limit control.   | 0x0: PLCCurr default setting. PLC can sink up to 200mA (typ). SYS LDO can sink up to 200mA (typ), Charge current register default setting. Charger can sink up to 200mA (typ).<br>0x1: PLCCurr register setting doubled. PLC can sink up to 400mA (typ). SYS LDO can sink up to 200mA (typ), Charge current register setting doubled. can sink up to 400mA (typ). |
| chg_res_ena  | 3    | Enable Initialization reset for charger section of the register map:<br>ILimCtrChg, ChgCur0/1, ChgCntl0/1/2, ChgTmr, ChgCfg0, ThmCfg0/1/2/3/4/5/6/7, ChgCtr1/2. | 0x0: No Initialization reset for the charger section of the register map<br>0x1: Initialization reset for the charger section of the register map. Initialization occurs when charger FSM starts.   |
| i2c_ldo_ena  | 2    | SYS LDO enable control.   | 0x0: SYS LDO Disabled<br>0x1: SYS LDO Enabled   |
| SYSUVLOThSel | 1:0  | SYSUVLO falling voltage threshold.  | 0x0: 2.7V<br>0x1: 2.9V<br>0x2: 3.0V<br>0x3: 3.2V  |

### PLC CONFIG0 (0x31)

| BIT         | 7              | 6 | 5 | 4 | 3 | 2 | 1              | 0 |
|-------------|----------------|---|---|---|---|---|----------------|---|
| Field       | PLCSnkSel[1:0] |   | – | – | – | – | PLCThrSel[1:0] |   |
| Reset       | 0x1            |   | – | – | – | – | 0x1            |   |
| Access Type | Write, Read    |   | – | – | – | – | Write, Read    |   |

| BITFIELD  | BITS | DESCRIPTION                   | DECODE  |
|-----------|------|-------------------------------|---|
| PLCSnkSel | 7:6  | PLC trasmission sink current. | 0x0: 50.3 mA<br>0x1: 70.4 mA<br>0x2: 90.4 mA<br>0x3: 110.5 mA |
| PLCThrSel | 1:0  | PLC pulse voltage threshold.  | 0x0: 75 mV<br>0x1: 90 mV<br>0x2: 105 mV<br>0x3: 120 mV        |

### PLC CONFIG1 (0x32)

| BIT         | 7           | 6           | 5            | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|--------------|---|---|---|---|---|
| Field       | otp_sum_rev | frc_i2c_sum | PLCCurr[5:0] |   |   |   |   |   |
| Reset       | 0x1         | 0x0         | 0x3F         |   |   |   |   |   |
| Access Type | Write, Read | Write, Read | Write, Read  |   |   |   |   |   |



| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
| otp_sum_rev | 7    | Minimize the PLC Current in case $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$ . Valid only if $frc\_i2c\_sum=0$ . | 0x0: PLC Current does not set to minimum value on $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$<br>0x1: PLC Current set to its minimum value on $V_{PLC} < V_{SYS}$ or $V_{PLC} < V_{BAT}$       |
| frc_i2c_sum | 6    | Force PLC current limit to PLCCurr.   | 0x0: PLC current limit internally controlled. PLC current limit can be lower than PLCCurr depending on charger operating condition.<br>0x1: PLC Current limit directly controlled by PLCCurr. |
| PLCCurr     | 5:0  | PLC input current limit. Sum of SYS LDO and charge current.   | LSB is 3.125mA. The full scale is 200mA.  |

### PLC CONFIG2 (0x33)

| BIT         | 7           | 6             | 5 | 4 | 3            | 2 | 1             | 0 |
|-------------|-------------|---------------|---|---|--------------|---|---------------|---|
| Field       | plc_dsc_otp | PLC_DROP[2:0] |   |   | PLC_HLD[1:0] |   | PLC_HREF[1:0] |   |
| Reset       | 0b1         | 0x2           |   |   | 0b1          |   | 0x1           |   |
| Access Type | Write, Read | Write, Read   |   |   | Write, Read  |   | Write, Read   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| plc_dsc_otp | 7    | PLC discharge enable control under SYSUVLO.   | 0x0: No discharge<br>0x1: Discharge  |
| PLC_DROP    | 6:4  | Charger dropout ( $V_{PLC} - V_{CHG\_OUT}$ ) and SYS LDO ( $V_{PLC}-V_{SYS}$ ) dropout threshold. | 0x0: 50mV<br>0x1: 75mV<br>0x2: 100mV<br>0x3: 125mV<br>0x4: 150mV<br>0x5: 175mV<br>0x6: 200mV<br>0x7: 225mV |
| PLC_HLD     | 3:2  | $V_{BAT} + V_{PLC\_HREF} - V_{PLC\_HLD}$ defines lower limit of the PLC voltage.                  | 0x0: 50 mV<br>0x1: 62.5 mV<br>0x2: 75 mV<br>0x3: 87.5 mV   |
| PLC_HREF    | 1:0  | $V_{BAT} + V_{PLC\_HREF}$ defines upper limit of PLC voltage.                                     | 0x0: 112.5 mV<br>0x1: 125 mV<br>0x2: 137.5 mV<br>0x3: 150 mV   |

### PLC CONFIG3 (0x34)

| BIT         | 7           | 6           | 5               | 4 | 3 | 2                | 1 | 0 |
|-------------|-------------|-------------|-----------------|---|---|------------------|---|---|
| Field       | plc_monitor | plc_con_sts | plc_config[2:0] |   |   | DAT_MAX_RTY[2:0] |   |   |
| Reset       | 0x0         | 0x0         | 0x7             |   |   | 0x7              |   |   |
| Access Type | Write, Read | Write, Read | Write, Read     |   |   | Write, Read      |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
| plc_monitor | 7    | Slave monitors PLC line for PLC communication as soon as PLC supply is present if master detection FSM is disabled.   | 0x0: Slave monitors PLC line<br>0x1: Slave does not monitor PLC line                      |
| plc_con_sts | 6    | Toggle to choose slave connection state indicator.  | 0x0: Enter connect state after first PING<br>0x1: Enter connect state when PLC is present |
| plc_config  | 5:3  | Bulk transfer auto-retry of DOUT_REQ. Maximum NACK to DOUT_REQ from master before slave detect an error in DATA transfers. Only works in bulk data transfer mode. | 0x0: 1<br>0x1: 2<br>0x2: 4<br>0x3: 8<br>0x4: 16<br>0x5: 32<br>0x6: 64<br>0x7: 128         |
| DAT_MAX_RTY | 2:0  | Auto-retry numbers of data packet. Maximum NACK to data packet from master before error flag is asserted in data transfers. Valid for bulk data transfer only.    | 0x0: 1<br>0x1: 2<br>0x2: 3<br>0x3: 4<br>0x4: 5<br>0x5: 6<br>0x6: 7<br>0x7: 8              |

**PLC CONFIG4 (0x35)**

| BIT         | 7           | 6           | 5           | 4          | 3           | 2           | 1           | 0           |
|-------------|-------------|-------------|-------------|------------|-------------|-------------|-------------|-------------|
| Field       | plc_fsm_ena | RAM_is_full | fifo_master | fifo_slave | plc_is_full | png_timeout | plc_res_req | cont_stream |
| Reset       | 0b1         | 0b0         | 0b0         | 0x0        | 0x0         | 0x0         | 0b0         | 0b0         |
| Access Type | Write, Read | Write, Read | Read Only   | Read Only  | Read Only   | Read Only   | Write, Read | Write, Read |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| plc_fsm_ena | 7    | PLC FSM enable control.   | 0x0: PLC FSM disabled<br>0x1: PLC FSM enabled  |
| RAM_is_full | 6    | Valid for both bulk data transfer and mailbox data transfer. When data is received, this bit is set together with plc_new_dat and plc_rx_bytes. RAM_is_full remains at 1 until write 1 from I <sup>2</sup> C to clear. Make sure to clear RAM_is_full after PLC data is read through I <sup>2</sup> C. Writing RAM_is_full to one will signal to the device that RAM is ready to receive new data packet. If the device receives new DOUT_REQ but RAM_is_full remains to 1, the device will NACK to DOUT_REQ. | 0x0: No new data received on PLC line<br>0x1: New data received via PLC line, Ready to be read. Write to 1 to clear. |
| fifo_master | 5    | FIFO master.  | 0x0: Not in FIFO master mode<br>0x1: FIFO master mode  |
| fifo_slave  | 4    | FIFO slave.   | 0x0: Not in FIFO slave mode<br>0x1: FIFO slave mode  |

| BITFIELD    | BITS | DESCRIPTION  | DECODE   |
|-------------|------|--|--|
| plc_is_full | 3    | Valid only for bulk data transfer. It indicates the RAM buffer is full. Data received via PLC is not read yet. Device will NACK to next PLC DOUT_REQ.  | 0x0: At least one RAM is free<br>0x1: Both RAMs are full   |
| png_timeout | 2    | Indicator to show last PING packet from master is 268.5ms ago. This is just a flag to monitor the condition. Device does not take any action after timer is expired.   | 0x0: Last PING packet was received less than 268.5ms ago (typ)<br>0x1: Last PING packet was received more than 268.5ms ago (typ) |
| plc_res_req | 1    | PLC IDLE resume request. Autocleared when done.  | 0x0: No request<br>0x1: Request to resume from PLC IDLE  |
| cont_stream | 0    | Valid only for bulk data transfer. If device is sending data in bulk transfer mode, when this bit is set to 1, only first packet transfer must be triggered with plc_run_trg. Other packets will be sent automatically after plc_cmd_dne interrupt. New data packet needs to be filled in to RAM via I <sup>2</sup> C before plc_cmd_dne of previous DOUT_REQ command. | 0x0: No continuous stream<br>0x1: Continuous stream  |

#### PLC\_CONFIG5 (0x36)

| BIT         | 7             | 6           | 5           | 4           | 3 | 2 | 1 | 0           |
|-------------|---------------|-------------|-------------|-------------|---|---|---|-------------|
| Field       | no_fifo_slave | no_seal_mde | no_uart_mde | no_idle_mde | – | – | – | swp_plc_ram |
| Reset       | 0x0           | 0x0         | 0x1         | 0x0         | – | – | – | 0x0         |
| Access Type | Write, Read   | Write, Read | Write, Read | Write, Read | – | – | – | Write, Read |

| BITFIELD      | BITS | DESCRIPTION  | DECODE   |
|---------------|------|--|--|
| no_fifo_slave | 7    | Nack to FIFO SYST_REQ PLC command.   | 0x0: Disable. Send ACK to FIFO SYST_REQ<br>0x1: Enable. Send NACK to FIFO SYST_REQ                         |
| no_seal_mde   | 6    | Nack to SEAL SYST_REQ PLC command.   | 0x0: Disable. Send ACK to SEAL SYST_REQ PLC command<br>0x1: Enable. Send NACK to SEAL SYST_REQ PLC command |
| no_uart_mde   | 5    | Nack to UART_REQ PLC command.  | 0x0: Disable. Send ACK to UART_REQ<br>0x1: Enable. Send NACK to UART_REQ                                   |
| no_idle_mde   | 4    | NACK to IDLE SYST_REQ PLC command.   | 0x0: Disable. Send ACK to IDLE_REQ<br>0x1: Enable. Send NACK to IDLE_REQ                                   |
| swp_plc_ram   | 0    | Swap PLC RAM control. Set this bit to 1 to read back data filled to RAM from master SoC in mailbox data transfer. Make sure to keep this bit to 0 when triggering data transfer. | 0x0: Automatic control<br>0x1: RAM readback on I2C   |

**PLC\_ARG (0x37)**

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | plc_cmd_arg[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00             |   |   |   |   |   |   |   |
| Access Type | Write, Read      |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION           | DECODE  |
|-------------|------|-----------------------|---|
| plc_cmd_arg | 7:0  | PLC command argument. | <p><b>SET_GPIO:</b><br/>{GPIOEnRes4, GPIOEnRes3, GPIOEnRes2, GPIOEnRes1, GPIODout_4, GPIODout_3, GPIODout_2, GPIODout_1}</p> <p><b>DOUT_REQ:</b><br/>Number of bytes = plc_cmd_arg1 + 1</p> <p><b>UART_REQ:</b><br/>0x0: Manual configuration of UART direction via I2C command (All switches are OFF)<br/>0x1: Master PLC1 master receiving, slave transmitting (RX switches are ON)<br/>0x2: Master PLC1 master transmitting, slave receiving (TX switches are ON)<br/>0x3: Master PLC1 local loop back (TX and RX switches are ON)<br/>0x4: Master PLC2 master receiving, slave transmitting (RX switches are ON)<br/>0x8: Master PLC2 master transmitting, slave receiving (TX switches are ON)<br/>0xC: Master PLC2 local loop back (TX and RX switches are ON)</p> <p><b>SYST_REQ:</b><br/>0x1: Soft reset<br/>0x3: Fuel gauge reset<br/>0x4: FIFO request<br/>0x5: Free request<br/>0x6: PLC IDLE mode request</p> |

**PLC\_CMD (0x38)**

| BIT         | 7           | 6                | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|------------------|---|---|---|---|---|---|
| Field       | plc_run_trg | plc_command[6:0] |   |   |   |   |   |   |
| Reset       | 0b0         | 0x0              |   |   |   |   |   |   |
| Access Type | Write, Read | Write, Read      |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| plc_run_trg | 7    | PLC command trigger. Write 1 to trigger a PLC command. Autocleared when command is sent out through PLC line during PING. | 0x0: No command in progress<br>0x1: Command running                  |
| plc_command | 6:0  | Command to send on PLC interface:   | 0x00: SYST_REQ<br>0x03: SET_GPIO<br>0x05: DOUT_REQ<br>0x06: UART_REQ |

### PLC\_RX (0x39)

| BIT         | 7 | 6                 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------------|---|---|---|---|---|---|
| Field       | – | plc_rx_bytes[6:0] |   |   |   |   |   |   |
| Reset       | – | 0x0               |   |   |   |   |   |   |
| Access Type | – | Read Only         |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION   | DECODE                              |
|--------------|------|---|-------------------------------------|
| plc_rx_bytes | 6:0  | Number of bytes received on PLC line during last DOUT_REQ command. This register is set together with plc_new_dat interrupt and RAM_is_full flag. | Number of bytes = plc_rx_bytes + 1. |

### Master feed back0 (0x3A)

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | mst_SOC_val[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0              |   |   |   |   |   |   |   |
| Access Type | Read Only        |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION  | DECODE  |
|-------------|------|--|---|
| mst_SOC_val | 7:0  | Master SOC byte1 from master fuel gauge. Valid if mst_FGready = 1. | LSB is 1% of full charge. The full scale is 256%. |

### Master feed back1 (0x3B)

| BIT   | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------|---|---|---|---|---|---|---|
| Field | mst_FGready | – | – | – | – | – | – | – |

|                    |           |   |   |   |   |   |   |   |
|--------------------|-----------|---|---|---|---|---|---|---|
| <b>Reset</b>       | 0x0       | - | - | - | - | - | - | - |
| <b>Access Type</b> | Read Only | - | - | - | - | - | - | - |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>      | <b>DECODE</b>                      |
|-----------------|-------------|-------------------------|------------------------------------|
| mst_FGready     | 7           | Master SOC is reliable. | 0x0: Not reliable<br>0x1: Reliable |

### WATCHDOG0 (0x3C)

| <b>BIT</b>         | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b>         | <b>2</b> | <b>1</b>         | <b>0</b> |
|--------------------|----------|----------|----------|----------|------------------|----------|------------------|----------|
| <b>Field</b>       | -        | -        | -        | -        | wd_rst_type[1:0] |          | wd__eoc_sel[1:0] |          |
| <b>Reset</b>       | -        | -        | -        | -        | 0x0              |          | 0x0              |          |
| <b>Access Type</b> | -        | -        | -        | -        | Write, Read      |          | Write, Read      |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>  |
|-----------------|-------------|---|--|
| wd_rst_type     | 3:2         | Watchdog reset type   | 0x0: Watchdog is OFF<br>0x1: Hard reset<br>0x2: Soft reset<br>0x3: Hard + soft reset |
| wd__eoc_sel     | 1:0         | Watchdog timer. Device skips the the first watchdog timeout reset after UART exit, soft reset, hard reset, soft + hard reset and JEITA reset. | 0x0: 4s<br>0x1: 8s<br>0x2: 16s<br>0x3: 32s   |

### SYS\_MIN0 (0x3D)

| <b>BIT</b>         | <b>7</b>    | <b>6</b> | <b>5</b> | <b>4</b>    | <b>3</b>    | <b>2</b> | <b>1</b> | <b>0</b> |
|--------------------|-------------|----------|----------|-------------|-------------|----------|----------|----------|
| <b>Field</b>       | PP_drp[2:0] |          |          | SysMinForce | SysMin[3:0] |          |          |          |
| <b>Reset</b>       | 0x2         |          |          | 0x0         | 0x0         |          |          |          |
| <b>Access Type</b> | Write, Read |          |          | Write, Read | Write, Read |          |          |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>  |
|-----------------|-------------|---|--|
| PP_drp          | 7:5         | CHG_OUT-SYS drop. Valid when PLC is present and power path FET is active. | 0x0: 25mV<br>0x1: 37.5mV<br>0x2: 50mV<br>0x3: 62.5mV<br>0x4: 75mV<br>0x5: 87.5mV<br>0x6: 100mV<br>0x7: 112.5mV |
| SysMinForce     | 4           | Control bit to force V <sub>sys</sub> reference to SysMin.                | 0x0: V <sub>sys</sub> regulated to V <sub>BAT</sub><br>0x1: V <sub>sys</sub> regulated to SysMin               |

| BITFIELD | BITS | DESCRIPTION                     | DECODE   |
|----------|------|---------------------------------|--|
| SysMin   | 3:0  | Minimum SYS regulating voltage. | 0x0: 3.0V<br>0x1: 3.1V<br>0x2: 3.2V<br>0x3: 3.3V<br>0x4: 3.4V<br>0x5: 3.5V<br>0x6: 3.6V<br>0x7: 3.7V<br>0x8: 3.8V<br>0x9: 3.9V<br>0xA: 4.0V<br>0xB: 4.1V<br>0xC: 4.2V<br>0xD: 4.3V<br>0xE: 4.4V<br>0xF: 4.5V |

**ILimCtrlChg (0x40)**

| BIT         | 7 | 6 | 5 | 4 | 3               | 2 | 1 | 0 |
|-------------|---|---|---|---|-----------------|---|---|---|
| Field       | - | - | - | - | ChgThrmLim[3:0] |   |   |   |
| Reset       | - | - | - | - | 0xF             |   |   |   |
| Access Type | - | - | - | - | Write, Read     |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                 | DECODE   |
|------------|------|-----------------------------|--|
| ChgThrmLim | 3:0  | Thermal shutdown threshold. | 0x0: 40°C<br>0x1: 45°C<br>0x2: 50°C<br>0x3: 55°C<br>0x4: 60°C<br>0x5: 65°C<br>0x6: 70°C<br>0x7: 75°C<br>0x8: 80°C<br>0x9: 85°C<br>0xA: 90°C<br>0xB: 95°C<br>0xC: 100°C<br>0xD: 105°C<br>0xE: 110°C<br>0xF: 115°C |

**ChgCur0 (0x41)**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|-----|---|---|---|---|---|---|---|---|

|                    |   |               |
|--------------------|---|---------------|
| <b>Field</b>       | – | CC1IFChg[6:0] |
| <b>Reset</b>       | – | 0x43          |
| <b>Access Type</b> | – | Write, Read   |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>                                  | <b>DECODE</b>  |
|-----------------|-------------|---|--|
| CC1IFChg        | 6:0         | Fast charge constant current zone 1 charge current. | 0x0 to 0x3C: 5mA to 65mA. LSB 1mA.<br>0x3D to 0x4F: 70mA to 160mA. LSB 5mA.<br>0x50 to 0x53: 170mA to 200mA. LSB 10mA.<br>0x54 to 0xFF: 200mA. |

### ChgCur1 (0x42)

| <b>BIT</b>         | <b>7</b> | <b>6</b>      | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
|--------------------|----------|---------------|----------|----------|----------|----------|----------|----------|
| <b>Field</b>       | –        | CC2IFChg[6:0] |          |          |          |          |          |          |
| <b>Reset</b>       | –        | 0x2D          |          |          |          |          |          |          |
| <b>Access Type</b> | –        | Write, Read   |          |          |          |          |          |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>                                  | <b>DECODE</b>  |
|-----------------|-------------|---|--|
| CC2IFChg        | 6:0         | Fast charge constant current zone 2 charge current. | 0x0 to 0x3C: 5mA to 65mA. LSB 1mA.<br>0x3D to 0x4F: 70mA to 160mA. LSB 5mA.<br>0x50 to 0x53: 170mA to 200mA. LSB 10mA.<br>0x54 to 0xFF: 200mA. |

### ChgCntl0 (0x43)

| <b>BIT</b>         | <b>7</b>    | <b>6</b>    | <b>5</b>     | <b>4</b> | <b>3</b> | <b>2</b>    | <b>1</b>    | <b>0</b>    |
|--------------------|-------------|-------------|--------------|----------|----------|-------------|-------------|-------------|
| <b>Field</b>       | ChgEn       | ChgAutoStop | ChgAutoReSta | –        | –        | CC1RoomOnly | CC1TmoLimit | CC1Enable   |
| <b>Reset</b>       | 0x0         | 0x1         | 0x1          | –        | –        | 0x0         | 0x0         | 0x1         |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read  | –        | –        | Write, Read | Write, Read | Write, Read |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>      | <b>DECODE</b>               |
|-----------------|-------------|-------------------------|-----------------------------|
| ChgEn           | 7           | Charger enable control. | 0x0: Disable<br>0x1: Enable |



| BITFIELD     | BITS | DESCRIPTION   | DECODE  |
|--------------|------|---|---|
| ChgAutoStop  | 6    | Charger auto-stop control. This bit controls if charger is allowed to transit from maintain charge state to maintain charge done state. | 0x0: Auto-stop disabled<br>0x1: Auto-stop enabled   |
| ChgAutoReSta | 5    | Charger auto-restart control.   | 0x0: Charger remains in maintain-charge done even when V <sub>BAT</sub> is less than recharge threshold.<br>0x1: Charger automatically restarts when V <sub>BAT</sub> drops below recharge threshold. |
| CC1RoomOnly  | 2    | Run charger in CC1 state under room temperature only. Temperature is detected from THM pin.   | 0x0: Run CC1 in any temperature range<br>0x1: Run CC1 in Room temperature only  |
| CC1TmoLimit  | 1    | This bit controls if charger skips CC1 phase and proceeds to CC2 phase after CC1 timeout. CC1 timer is set by CC1FChgTmr.               | 0x0: Run CC1 phase with timer limitation<br>0x1: Run CC1 phase with no timer limitation   |
| CC1Enable    | 0    | Enable CC1 charging phase. Write to 0 to skip or disable CC1 charging phase.  | 0x0: CC1 phase disabled<br>0x1: CC1 phase enabled   |

### ChgCntl1 (0x44)

| BIT         | 7             | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|-------------|---|---|---|---|---|
| Field       | BatReChg[1:0] |   | BatReg[5:0] |   |   |   |   |   |
| Reset       | 0x2           |   | 0xF         |   |   |   |   |   |
| Access Type | Write, Read   |   | Write, Read |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION   | DECODE  |
|----------|------|---|---|
| BatReChg | 7:6  | Charger re-charge threshold in relation to BatReg[3:0]. | 0x0: V <sub>BatReg</sub> - 50mV<br>0x1: V <sub>BatReg</sub> - 100mV<br>0x2: V <sub>BatReg</sub> - 150mV<br>0x3: V <sub>BatReg</sub> - 200mV |
| BatReg   | 5:0  | Charger battery regulation voltage.                     | Battery regulation voltage = BatReg x 0.01V + 4.05V.<br>Capped to 4.6V. Do not recommend to set the value > 0x38.                           |

### ChgCntl2 (0x45)

| BIT         | 7 | 6           | 5 | 4 | 3           | 2 | 1             | 0 |
|-------------|---|-------------|---|---|-------------|---|---------------|---|
| Field       | – | VPChg[2:0]  |   |   | IPChg[1:0]  |   | IChgDone[1:0] |   |
| Reset       | – | 0x3         |   |   | 0x2         |   | 0x2           |   |
| Access Type | – | Write, Read |   |   | Write, Read |   | Write, Read   |   |

| BITFIELD | BITS | DESCRIPTION                                  | DECODE  |
|----------|------|--|---|
| VChg     | 6:4  | Charger pre-charge voltage rising threshold. | 0x0: 2.70V<br>0x1: 2.80V<br>0x2: 2.90V<br>0x3: 3.00V<br>0x4: 3.10V<br>0x5: 3.20V<br>0x6: 3.30V<br>0x7: 3.40V  |
| IPChg    | 3:2  | Charger pre-charge current.                  | 0x0: 0.05 x I <sub>CC2IFChg</sub><br>0x1: 0.10 x I <sub>CC2IFChg</sub><br>0x2: 0.20 x I <sub>CC2IFChg</sub><br>0x3: 0.30 x I <sub>CC2IFChg</sub>      |
| IChgDone | 1:0  | Charger charge-done current threshold.       | 0b00: 0.025 x I <sub>CC2IFChg</sub><br>0b01: 0.05 x I <sub>CC2IFChg</sub><br>0b10: 0.10 x I <sub>CC2IFChg</sub><br>0b11: 0.20 x I <sub>CC2IFChg</sub> |

### ChgTmr (0x46)

| BIT         | 7             | 6 | 5            | 4 | 3               | 2 | 1           | 0 |
|-------------|---------------|---|--------------|---|-----------------|---|-------------|---|
| Field       | MtChgTmr[1:0] |   | PChgTmr[1:0] |   | CC1FChgTmr[1:0] |   | ChgTmr[1:0] |   |
| Reset       | 0x0           |   | 0x0          |   | 0x0             |   | 0x0         |   |
| Access Type | Write, Read   |   | Write, Read  |   | Write, Read     |   | Write, Read |   |

| BITFIELD   | BITS | DESCRIPTION  | DECODE  |
|------------|------|--|---|
| MtChgTmr   | 7:6  | Charger maintain charge timer.   | 0x0: 0min<br>0x1: 15min<br>0x2: 30min<br>0x3: 60min     |
| PChgTmr    | 5:4  | Charger pre-charge timer.  | 0x0: 30min<br>0x1: 60min<br>0x2: 120min<br>0x3: 240min  |
| CC1FChgTmr | 3:2  | Charger fast charge CC1 timer.   | 0x0: 30min<br>0x1: 60min<br>0x2: 120min<br>0x3: 240min  |
| ChgTmr     | 1:0  | Charger Safety Timer. Runs during Pre-charge, CC1, CC2, and CC track/CV charge phases. | 0x0: 75min<br>0x1: 150min<br>0x2: 300min<br>0x3: 600min |

### ChgCfg0 (0x47)

| BIT   | 7 | 6               | 5 | 4 | 3                | 2 | 1 | 0 |
|-------|---|-----------------|---|---|------------------|---|---|---|
| Field | – | ChgStepHys[2:0] |   |   | ChgStepRise[3:0] |   |   |   |
| Reset | – | 0x5             |   |   | 0x2              |   |   |   |

|             |   |             |             |
|-------------|---|-------------|-------------|
| Access Type | - | Write, Read | Write, Read |
|-------------|---|-------------|-------------|

| BITFIELD    | BITS | DESCRIPTION                                       | DECODE   |
|-------------|------|---|--|
| ChgStepHys  | 6:4  | Charger step charge voltage threshold hysteresis. | 0x0: 100mV<br>0x1: 200mV<br>0x2: 300mV<br>0x3: 400mV<br>0x4: 500mV<br>Others: 600mV  |
| ChgStepRise | 3:0  | Charger step charge voltage rising threshold.     | 0x0: 3.80V<br>0x1: 3.85V<br>0x2: 3.90V<br>0x3: 3.95V<br>0x4: 4.00V<br>0x5: 4.05V<br>0x6: 4.10V<br>0x7: 4.15V<br>0x8: 4.20V<br>0x9: 4.25V<br>0xA: 4.30V<br>0xB: 4.35V<br>0xC: 4.40V<br>0xD: 4.45V<br>0xE: 4.50V<br>0xF: 4.55V |

**ThmCfg0 (0x48)**

| BIT         | 7                    | 6 | 5 | 4                  | 3 | 2                    | 1 | 0 |
|-------------|----------------------|---|---|--------------------|---|----------------------|---|---|
| Field       | ChgCoolCC1IFChg[2:0] |   |   | ChgCoolBatReg[1:0] |   | ChgCoolCC2IFChg[2:0] |   |   |
| Reset       | 0x4                  |   |   | 0x2                |   | 0x4                  |   |   |
| Access Type | Write, Read          |   |   | Write, Read        |   | Write, Read          |   |   |

| BITFIELD        | BITS | DESCRIPTION   | DECODE   |
|-----------------|------|---|--|
| ChgCoolCC1IFChg | 7:5  | Charger cool zone CC1 fast-charge current reduction.    | 0x0: 0.2 x I <sub>CC1FChg</sub><br>0x1: 0.3 x I <sub>CC1FChg</sub><br>0x2: 0.4 x I <sub>CC1FChg</sub><br>0x3: 0.5 x I <sub>CC1FChg</sub><br>0x4: 0.6 x I <sub>CC1FChg</sub><br>0x5: 0.7 x I <sub>CC1FChg</sub><br>0x6: 0.8 x I <sub>CC1FChg</sub><br>0x7: 1.0 x I <sub>CC1FChg</sub> |
| ChgCoolBatReg   | 4:3  | Charger cool zone battery regulation voltage reduction. | 0x0: V <sub>BatReg</sub> - 150mV<br>0x1: V <sub>BatReg</sub> - 100mV<br>0x2: V <sub>BatReg</sub> - 50mV<br>0x3: V <sub>BatReg</sub>  |
| ChgCoolCC2IFChg | 2:0  | Charger cool zone CC2 fast-charge current reduction.    | 0x0: 0.2 x I <sub>CC2FChg</sub><br>0x1: 0.3 x I <sub>CC2FChg</sub><br>0x2: 0.4 x I <sub>CC2FChg</sub><br>0x3: 0.5 x I <sub>CC2FChg</sub><br>0x4: 0.6 x I <sub>CC2FChg</sub><br>0x5: 0.7 x I <sub>CC2FChg</sub><br>0x6: 0.8 x I <sub>CC2FChg</sub><br>0x7: 1.0 x I <sub>CC2FChg</sub> |

**ThmCfg1 (0x49)**

| BIT                | 7                    | 6 | 5 | 4                  | 3 | 2                    | 1 | 0 |
|--------------------|----------------------|---|---|--------------------|---|----------------------|---|---|
| <b>Field</b>       | ChgRoomCC1IFChg[2:0] |   |   | ChgRoomBatReg[1:0] |   | ChgRoomCC2IFChg[2:0] |   |   |
| <b>Reset</b>       | 0x7                  |   |   | 0x3                |   | 0x7                  |   |   |
| <b>Access Type</b> | Write, Read          |   |   | Write, Read        |   | Write, Read          |   |   |

| BITFIELD        | BITS | DESCRIPTION   | DECODE   |
|-----------------|------|---|--|
| ChgRoomCC1IFChg | 7:5  | Charger room zone CC1 fast-charge current reduction.    | 0x0: 0.2 x I <sub>CC1FChg</sub><br>0x1: 0.3 x I <sub>CC1FChg</sub><br>0x2: 0.4 x I <sub>CC1FChg</sub><br>0x3: 0.5 x I <sub>CC1FChg</sub><br>0x4: 0.6 x I <sub>CC1FChg</sub><br>0x5: 0.7 x I <sub>CC1FChg</sub><br>0x6: 0.8 x I <sub>CC1FChg</sub><br>0x7: 1.0 x I <sub>CC1FChg</sub> |
| ChgRoomBatReg   | 4:3  | Charger room zone battery regulation voltage reduction. | 0x0: V <sub>BatReg</sub> - 150mV<br>0x1: V <sub>BatReg</sub> - 100mV<br>0x2: V <sub>BatReg</sub> - 50mV<br>0x3: V <sub>BatReg</sub>  |
| ChgRoomCC2IFChg | 2:0  | Charger room zone CC2 fast-charge current reduction.    | 0x0: 0.2 x I <sub>CC2FChg</sub><br>0x1: 0.3 x I <sub>CC2FChg</sub><br>0x2: 0.4 x I <sub>CC2FChg</sub><br>0x3: 0.5 x I <sub>CC2FChg</sub><br>0x4: 0.6 x I <sub>CC2FChg</sub><br>0x5: 0.7 x I <sub>CC2FChg</sub><br>0x6: 0.8 x I <sub>CC2FChg</sub><br>0x7: 1.0 x I <sub>CC2FChg</sub> |

**ThmCfg2 (0x4A)**

| BIT                | 7                    | 6 | 5 | 4                  | 3 | 2                    | 1 | 0 |
|--------------------|----------------------|---|---|--------------------|---|----------------------|---|---|
| <b>Field</b>       | ChgWarmCC1IFChg[2:0] |   |   | ChgWarmBatReg[1:0] |   | ChgWarmCC2IFChg[2:0] |   |   |
| <b>Reset</b>       | 0x3                  |   |   | 0x1                |   | 0x3                  |   |   |
| <b>Access Type</b> | Write, Read          |   |   | Write, Read        |   | Write, Read          |   |   |

| BITFIELD        | BITS | DESCRIPTION   | DECODE   |
|-----------------|------|---|--|
| ChgWarmCC1IFChg | 7:5  | Charger warm zone CC1 fast-charge current reduction.    | 0x0: 0.2 x I <sub>CC1FChg</sub><br>0x1: 0.3 x I <sub>CC1FChg</sub><br>0x2: 0.4 x I <sub>CC1FChg</sub><br>0x3: 0.5 x I <sub>CC1FChg</sub><br>0x4: 0.6 x I <sub>CC1FChg</sub><br>0x5: 0.7 x I <sub>CC1FChg</sub><br>0x6: 0.8 x I <sub>CC1FChg</sub><br>0x7: 1.0 x I <sub>CC1FChg</sub> |
| ChgWarmBatReg   | 4:3  | Charger warm zone battery regulation voltage reduction. | 0x0: V <sub>BatReg</sub> - 150mV<br>0x1: V <sub>BatReg</sub> - 100mV<br>0x2: V <sub>BatReg</sub> - 50mV<br>0x3: V <sub>BatReg</sub>  |

| BITFIELD        | BITS | DESCRIPTION  | DECODE   |
|-----------------|------|--|--|
| ChgWarmCC2IFChg | 2:0  | Charger warm zone CC2 fast-charge current reduction. | 0x0: 0.2 x I <sub>CC2IFChg</sub><br>0x1: 0.3 x I <sub>CC2IFChg</sub><br>0x2: 0.4 x I <sub>CC2IFChg</sub><br>0x3: 0.5 x I <sub>CC2IFChg</sub><br>0x4: 0.6 x I <sub>CC2IFChg</sub><br>0x5: 0.7 x I <sub>CC2IFChg</sub><br>0x6: 0.8 x I <sub>CC2IFChg</sub><br>0x7: 1.0 x I <sub>CC2IFChg</sub> |

### ThmCfg3 (0x4B)

| BIT         | 7 | 6 | 5                | 4 | 3 | 2                | 1 | 0 |
|-------------|---|---|------------------|---|---|------------------|---|---|
| Field       | – | – | ChgT1ThrDef[2:0] |   |   | ChgT1ThrCC1[2:0] |   |   |
| Reset       | – | – | 0x4              |   |   | 0x4              |   |   |
| Access Type | – | – | Write, Read      |   |   | Write, Read      |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
| ChgT1ThrDef | 5:3  | JEITA T1 cold default temperature threshold. V <sub>THM</sub> rising threshold between cold and cool zone. Applies for BatReg and CC2 JEITA reduction settings. | 0x0: -20°C<br>0x1: -15°C<br>0x2: -10°C<br>0x3: -5°C<br>0x4: 0°C<br>0x5: 5°C<br>0x6: 10°C<br>0x7: 15°C |
| ChgT1ThrCC1 | 2:0  | JEITA T1 CC1 cold temperature threshold. V <sub>THM</sub> rising threshold between cold and cool zone. Applies for CC1 JEITA reduction settings.                | 0x0: -20°C<br>0x1: -15°C<br>0x2: -10°C<br>0x3: -5°C<br>0x4: 0°C<br>0x5: 5°C<br>0x6: 10°C<br>0x7: 15°C |

### ThmCfg4 (0x4C)

| BIT         | 7 | 6 | 5                | 4 | 3 | 2                | 1 | 0 |
|-------------|---|---|------------------|---|---|------------------|---|---|
| Field       | – | – | ChgT2ThrDef[2:0] |   |   | ChgT2ThrCC1[2:0] |   |   |
| Reset       | – | – | 0x5              |   |   | 0x5              |   |   |
| Access Type | – | – | Write, Read      |   |   | Write, Read      |   |   |

| BITFIELD    | BITS | DESCRIPTION  | DECODE  |
|-------------|------|--|---|
| ChgT2ThrDef | 5:3  | JEITA T2 cool default temperature threshold. V <sub>THM</sub> rising threshold between cool and room | 0x0: -10°C<br>0x1: -5°C<br>0x2: 0°C<br>0x3: 5°C |

| BITFIELD    | BITS | DESCRIPTION   | DECODE  |
|-------------|------|---|---|
|             |      | zone. Applies for BatReg and CC2 JEITA reduction settings.  | 0x4: 10°C<br>0x5: 15°C<br>0x6: 20°C<br>0x7: 25°C  |
| ChgT2ThrCC1 | 2:0  | JEITA T2 CC1 cool temperature threshold. $V_{THM}$ rising threshold between cool and room zone. Applies for CC1 JEITA reduction settings. | 0x0: -10°C<br>0x1: -5°C<br>0x2: 0°C<br>0x3: 5°C<br>0x4: 10°C<br>0x5: 15°C<br>0x6: 20°C<br>0x7: 25°C |

### ThmCfg5 (0x4D)

| BIT         | 7 | 6 | 5                | 4 | 3 | 2                | 1 | 0 |
|-------------|---|---|------------------|---|---|------------------|---|---|
| Field       | – | – | ChgT3ThrDef[2:0] |   |   | ChgT3ThrCC1[2:0] |   |   |
| Reset       | – | – | 0x2              |   |   | 0x2              |   |   |
| Access Type | – | – | Write, Read      |   |   | Write, Read      |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| ChgT3ThrDef | 5:3  | JEITA T3 warm default temperature threshold. $V_{THM}$ falling threshold between warm and room zone. Applies for BatReg and CC2 JEITA reduction settings. | 0x0: 20°C<br>0x1: 25°C<br>0x2: 30°C<br>0x3: 35°C<br>0x4: 40°C<br>0x5: 45°C<br>0x6: 50°C<br>0x7: 55°C |
| ChgT3ThrCC1 | 2:0  | JEITA T3 CC1 warm temperature threshold. $V_{THM}$ falling threshold between warm and room zone. Applies for CC1 JEITA reduction settings.                | 0x0: 20°C<br>0x1: 25°C<br>0x2: 30°C<br>0x3: 35°C<br>0x4: 40°C<br>0x5: 45°C<br>0x6: 50°C<br>0x7: 55°C |

### ThmCfg6 (0x4E)

| BIT         | 7 | 6 | 5                | 4 | 3 | 2                | 1 | 0 |
|-------------|---|---|------------------|---|---|------------------|---|---|
| Field       | – | – | ChgT4ThrDef[2:0] |   |   | ChgT4ThrCC1[2:0] |   |   |
| Reset       | – | – | 0x2              |   |   | 0x2              |   |   |
| Access Type | – | – | Write, Read      |   |   | Write, Read      |   |   |

| BITFIELD    | BITS | DESCRIPTION   | DECODE   |
|-------------|------|---|--|
| ChgT4ThrDef | 5:3  | JEITA T4 hot default temperature threshold. $V_{THM}$ falling threshold between hot and warm zone. Applies for BatReg and CC2 JEITA reduction settings. | 0x0: 35°C<br>0x1: 40°C<br>0x2: 45°C<br>0x3: 50°C<br>0x4: 55°C<br>0x5: 60°C<br>0x6: 65°C<br>0x7: 70°C |
| ChgT4ThrCC1 | 2:0  | JEITA T4 CC1 hot temperature threshold. $V_{THM}$ falling threshold between hot and warm zone. Applies for CC1 JEITA reduction settings.                | 0x0: 35°C<br>0x1: 40°C<br>0x2: 45°C<br>0x3: 50°C<br>0x4: 55°C<br>0x5: 60°C<br>0x6: 65°C<br>0x7: 70°C |

### ThmCfg7 (0x4F)

| BIT         | 7                | 6 | 5 | 4 | 3           | 2           | 1 | 0 |
|-------------|------------------|---|---|---|-------------|-------------|---|---|
| Field       | jta_eoc_sel[1:0] |   | – | – | THMPUSel    | ThmEn[2:0]  |   |   |
| Reset       | 0x0              |   | – | – | 0x0         | 0x0         |   |   |
| Access Type | Write, Read      |   | – | – | Write, Read | Write, Read |   |   |

| BITFIELD    | BITS | DESCRIPTION  | DECODE  |
|-------------|------|--|---|
| jta_eoc_sel | 7:6  | JEITA measurement period. Valid only when PLC is not present and ThmEn > 0x3. New setting of this bit can be effective only after ThmEn is set to 0 and then set to > 0x03 values. | 0x0: Every 1s<br>0x1: Every 2s<br>0x2: Every 4s<br>0x3: Every 8s  |
| THMPUSel    | 3    | THM internal pullup resistance.  | 0x0: 10kΩ<br>0x1: 100kΩ   |
| ThmEn       | 2:0  | Charger thermistor monitoring control. JEITA temperature is measured from THM pin.   | 0x0: Thermistor monitoring disabled.<br>0x1: Thermistor monitoring enabled when PLC is present. Battery is charged in the cool and room temperature zones due to JEITA.<br>0x2: Thermistor monitoring enabled when PLC is present. Battery is charged in the room and warm temperature zones due to JEITA.<br>0x3: Thermistor monitoring enabled when PLC is present. Battery is charged in the cool, room and warm temperature zones due to JEITA.<br>0x4: Thermistor monitoring permanently enabled, but charger not affected by JEITA.<br>0x5: Thermistor monitoring permanently enabled. Battery is charged only in the cool and room temperature zones due to JEITA.<br>0x6: Thermistor monitoring permanently enabled. Battery is charged only in the room and warm temperature zones due to JEITA.<br>0x7: Thermistor monitoring permanently enabled. Battery is charged only in the cool, room and warm temperature zones due to JEITA. |

**ChgCtr1 (0x50)**

| BIT                | 7           | 6           | 5           | 4           | 3 | 2            | 1 | 0 |
|--------------------|-------------|-------------|-------------|-------------|---|--------------|---|---|
| <b>Field</b>       | i2c_crf_ena | chg_cc_trk  | ChgStsFCMrg | vlt_dne_ena | – | lng_xfer_opt | – | – |
| <b>Reset</b>       | 0x1         | 0x1         | 0x0         | 0x0         | – | 0x0          | – | – |
| <b>Access Type</b> | Write, Read | Write, Read | Write, Read | Write, Read | – | Write, Read  | – | – |

| BITFIELD     | BITS | DESCRIPTION  | DECODE  |
|--------------|------|--|---|
| i2c_crf_ena  | 7    | Battery recharge threshold comparator enable.  | 0x0: Battery recharge monitor disabled<br>0x1: Battery recharge monitor enabled   |
| chg_cc_trk   | 6    | CC track enable. Charger uses CV mode if CC track is disabled. Recommend to keep this bit to 1 to enable CC track. | 0x0: Disable<br>0x1: Enable   |
| ChgStsFCMrg  | 5    | Combine CC track/CV mode with CC2 reported in ChgStat.   | 0x0: All internal states are reported<br>0x1: CC track and CV mode are merged in CC2  |
| vlt_dne_ena  | 4    | Skip Mantain Charge status in case of JEITA voltage regulation.  | 0x0: Enable charging in Mantain Charge under JEITA battery voltage reduction condition.<br>0x1: Disable charging in Mantain Charge under JEITA battery voltage reduction condition. Skip charger Mantain Charge status. |
| lng_xfer_opt | 2    | Bit to enable charger's freeze during Long PLC xfer  | 0x0: Charger freeze only in short transfer: PING and PLC commands.<br>0x1: Charger freeze in all PLC transfers: PING, PLC command and bulk data transfer.   |

**ChgCtr2 (0x51)**

| BIT                | 7           | 6            | 5           | 4 | 3 | 2 | 1                | 0 |
|--------------------|-------------|--------------|-------------|---|---|---|------------------|---|
| <b>Field</b>       | BattUvloEna | BattPullDown | FrcPChg     | – | – | – | vlt_ctr_plc[1:0] |   |
| <b>Reset</b>       | 0x0         | 0x0          | 0x0         | – | – | – | 0x0              |   |
| <b>Access Type</b> | Write, Read | Write, Read  | Write, Read | – | – | – | Read Only        |   |

| BITFIELD     | BITS | DESCRIPTION  | DECODE  |
|--------------|------|--|---|
| BattUvloEna  | 7    |  |   |
| BattPullDown | 6    | Battery voltage pull down by internal pulldown resistor. | 0: Pulldown resistor disabled<br>1: Pulldown resistor enabled                     |
| FrcPChg      | 5    | Charger forced precharge mode. Valid only if ChgEn = 1.  | 0: Charger operating normally<br>1: Charge current is forced to precharge current |
| vlt_ctr_plc  | 1:0  | PLC voltage up/down request from slave to master         | 0x1: Decrease<br>0x2: Increase<br>Others: Hold                                    |



**GPIO1 (0x58)**

| BIT         | 7 | 6 | 5 | 4            | 3           | 2           | 1           | 0           |
|-------------|---|---|---|--------------|-------------|-------------|-------------|-------------|
| Field       | – | – | – | GPIOCompEna1 | GPIOPLCCtr1 | GPIOEnRes1  | GPIOEnPup1  | GIODout_1   |
| Reset       | – | – | – | 0x1          | 0x1         | 0x0         | 0x0         | 0x0         |
| Access Type | – | – | – | Write, Read  | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD     | BITS | DESCRIPTION   | DECODE                               |
|--------------|------|---|--------------------------------------|
| GPIOCompEna1 | 4    | GPIO comparator enable.   | 0x0: Disable<br>0x1: Enable          |
| GPIOPLCCtr1  | 3    | GPIO I2C or PLC control   | 0x0: I2C control<br>0x1: PLC control |
| GPIOEnRes1   | 2    | GPIO input or output configuration.                             | 0x0: Output<br>0x1: Input            |
| GPIOEnPup1   | 1    | GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1. | 0x0: Pull down<br>0x1: Pull up       |
| GIODout_1    | 0    | GPIO open drain output. Needs external pullup.                  | 0x0: High<br>0x1: Low                |

**GPIO2 (0x59)**

| BIT         | 7 | 6 | 5 | 4            | 3           | 2           | 1           | 0           |
|-------------|---|---|---|--------------|-------------|-------------|-------------|-------------|
| Field       | – | – | – | GPIOCompEna2 | GPIOPLCCtr2 | GPIOEnRes2  | GPIOEnPup2  | GIODout_2   |
| Reset       | – | – | – | 0x1          | 0x1         | 0x0         | 0x0         | 0x0         |
| Access Type | – | – | – | Write, Read  | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD     | BITS | DESCRIPTION   | DECODE                               |
|--------------|------|---|--------------------------------------|
| GPIOCompEna2 | 4    | GPIO comparator enable.   | 0x0: Disable<br>0x1: Enable          |
| GPIOPLCCtr2  | 3    | GPIO I2C or PLC control   | 0x0: I2C control<br>0x1: PLC control |
| GPIOEnRes2   | 2    | GPIO input or output configuration.                             | 0x0: Output<br>0x1: Input            |
| GPIOEnPup2   | 1    | GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1. | 0x0: Pull down<br>0x1: Pull up       |
| GIODout_2    | 0    | GPIO open drain output. Needs external pull-up.                 | 0x0: High<br>0x1: Low                |

**GPIO3 (0x5A)**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|-----|---|---|---|---|---|---|---|---|

|                    |   |   |   |             |             |             |             |             |
|--------------------|---|---|---|-------------|-------------|-------------|-------------|-------------|
| <b>Field</b>       | – | – | – | GPIOcmpEna3 | GPIOPLCCtr3 | GPIOEnRes3  | GPIOEnPup3  | GIODout_3   |
| <b>Reset</b>       | – | – | – | 0x1         | 0x1         | 0x0         | 0x0         | 0x0         |
| <b>Access Type</b> | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>                        |
|-----------------|-------------|---|--------------------------------------|
| GPIOcmpEna3     | 4           | GPIO comparator enable.   | 0x0: Disable<br>0x1: Enable          |
| GPIOPLCCtr3     | 3           | GPIO I2C or PLC control   | 0x0: I2C control<br>0x1: PLC control |
| GPIOEnRes3      | 2           | GPIO input or output configuration.                             | 0x0: Output<br>0x1: Input            |
| GPIOEnPup3      | 1           | GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1. | 0x0: Pull down<br>0x1: Pull up       |
| GIODout_3       | 0           | GPIO open drain output. Needs external pull-up.                 | 0x0: High<br>0x1: Low                |

#### GPIO4 (0x5B)

|                    |          |          |          |             |             |             |             |             |
|--------------------|----------|----------|----------|-------------|-------------|-------------|-------------|-------------|
| <b>BIT</b>         | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b>    | <b>3</b>    | <b>2</b>    | <b>1</b>    | <b>0</b>    |
| <b>Field</b>       | –        | –        | –        | GPIOcmpEna4 | GPIOPLCCtr4 | GPIOEnRes4  | GPIOEnPup4  | GIODout_4   |
| <b>Reset</b>       | –        | –        | –        | 0x1         | 0x1         | 0x0         | 0x0         | 0x0         |
| <b>Access Type</b> | –        | –        | –        | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>                        |
|-----------------|-------------|---|--------------------------------------|
| GPIOcmpEna4     | 4           | GPIO comparator enable.   | 0x0: Disable<br>0x1: Enable          |
| GPIOPLCCtr4     | 3           | GPIO I2C or PLC control   | 0x0: I2C control<br>0x1: PLC control |
| GPIOEnRes4      | 2           | GPIO input or output configuration.                             | 0x0: Output<br>0x1: Input            |
| GPIOEnPup4      | 1           | GPIO input pullup or pulldown resistor. Active if GPIOEnRes =1. | 0x0: Pull down<br>0x1: Pull up       |
| GIODout_4       | 0           | GPIO open drain output. Needs external pull-up.                 | 0x0: High<br>0x1: Low                |

#### GPIO\_rdb1 (0x5C)

|              |            |            |            |            |          |          |          |            |
|--------------|------------|------------|------------|------------|----------|----------|----------|------------|
| <b>BIT</b>   | <b>7</b>   | <b>6</b>   | <b>5</b>   | <b>4</b>   | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b>   |
| <b>Field</b> | GIODAImp_4 | GIODAImp_3 | GIODAImp_2 | GIODAImp_1 | –        | –        | –        | GPIOCmosEn |
| <b>Reset</b> | 0x0        | 0x0        | 0x0        | 0x0        | –        | –        | –        | 0x0        |

|                    |           |           |           |           |   |   |   |             |
|--------------------|-----------|-----------|-----------|-----------|---|---|---|-------------|
| <b>Access Type</b> | Read Only | Read Only | Read Only | Read Only | – | – | – | Write, Read |
|--------------------|-----------|-----------|-----------|-----------|---|---|---|-------------|

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>                                  | <b>DECODE</b>                 |
|-----------------|-------------|---|-------------------------------|
| GPIOAInp_4      | 7           | GPIO input status. Valid only when GPIOCompEna = 1. | 0x0: Low<br>0x1: High         |
| GPIOAInp_3      | 6           | GPIO input status. Valid only when GPIOCompEna = 1. | 0x0: Low<br>0x1: High         |
| GPIOAInp_2      | 5           | GPIO input status. Valid only when GPIOCompEna = 1. | 0x0: Low<br>0x1: High         |
| GPIOAInp_1      | 4           | GPIO input status. Valid only when GPIOCompEna = 1. | 0x0: Low<br>0x1: High         |
| GPIOCmosEn      | 0           | GPIO input logic threshold.                         | 0x0: 1.8V VDIG<br>0x1: VCCINT |

### GPIO\_rdb2 (0x5D)

| <b>BIT</b>         | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b>     | <b>2</b>     | <b>1</b>     | <b>0</b>     |
|--------------------|----------|----------|----------|----------|--------------|--------------|--------------|--------------|
| <b>Field</b>       | –        | –        | –        | –        | master_GPIO4 | master_GPIO3 | master_GPIO2 | master_GPIO1 |
| <b>Reset</b>       | –        | –        | –        | –        | 0x0          | 0x0          | 0x0          | 0x0          |
| <b>Access Type</b> | –        | –        | –        | –        | Read Only    | Read Only    | Read Only    | Read Only    |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>   | <b>DECODE</b>         |
|-----------------|-------------|----------------------|-----------------------|
| master_GPIO4    | 3           | Master GPIO4 status. | 0x0: Low<br>0x1: High |
| master_GPIO3    | 2           | Master GPIO3 status. | 0x0: Low<br>0x1: High |
| master_GPIO2    | 1           | Master GPIO2 status. | 0x0: Low<br>0x1: High |
| master_GPIO1    | 0           | Master GPIO1 status. | 0x0: Low<br>0x1: High |

### SOC byte 1 (0x60)

| <b>BIT</b>         | <b>7</b>             | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
|--------------------|----------------------|----------|----------|----------|----------|----------|----------|----------|
| <b>Field</b>       | AVGVCELL_byte_1[7:0] |          |          |          |          |          |          |          |
| <b>Reset</b>       | 0x0                  |          |          |          |          |          |          |          |
| <b>Access Type</b> | Read Only            |          |          |          |          |          |          |          |

| BITFIELD        | BITS | DESCRIPTION   | DECODE   |
|-----------------|------|---|--|
| AVGVCELL_byte_1 | 7:0  | Average cell voltage byte1 readback from fuel gauge. It is moving average of last 45 seconds. | Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V. |

**SOC byte 0 (0x61)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | AVGVCELL_byte_0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0                  |   |   |   |   |   |   |   |
| Access Type | Read Only            |   |   |   |   |   |   |   |

| BITFIELD        | BITS | DESCRIPTION   | DECODE   |
|-----------------|------|---|--|
| AVGVCELL_byte_0 | 7:0  | Average cell voltage byte0 readback from fuel gauge. It is moving average of last 45 seconds. | Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V. |

**VCELL byte 1 (0x62)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | VCELL_byte_1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0               |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                  | DECODE   |
|--------------|------|--|--|
| VCELL_byte_1 | 7:0  | Cell voltage byte1 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V. |

**VCELL byte 0 (0x63)**

| BIT         | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------|---|---|---|---|---|---|---|
| Field       | VCELL_byte_0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0               |   |   |   |   |   |   |   |
| Access Type | Read Only         |   |   |   |   |   |   |   |

| BITFIELD     | BITS | DESCRIPTION                                  | DECODE   |
|--------------|------|--|--|
| VCELL_byte_0 | 7:0  | Cell voltage byte0 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 78.125uV. The full scale is 5.12V. |

**TTE byte 1 (0x64)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TTE_byte_1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                   | DECODE   |
|------------|------|---|--|
| TTE_byte_1 | 7:0  | Time to empty byte1 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours. |

**TTE byte 0 (0x65)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TTE_byte_0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                   | DECODE   |
|------------|------|---|--|
| TTE_byte_0 | 7:0  | Time to empty byte0 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours. |

**AVGVCELL byte 1 (0x66)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | SOC_byte_1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                         | DECODE  |
|------------|------|-------------------------------------|---|
| SOC_byte_1 | 7:0  | SOC byte1 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 0.00390625% of full charge. The full scale is 256%. |

**AVGVCELL byte 0 (0x67)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | SOC_byte_0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                         | DECODE  |
|------------|------|-------------------------------------|---|
| SOC_byte_0 | 7:0  | SOC byte0 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 0.00390625% of full charge. The full scale is 256%. |

**TTF byte 1 (0x68)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TTF_byte_1[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                  | DECODE   |
|------------|------|--|--|
| TTF_byte_1 | 7:0  | Time to full byte1 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours. |

**TTF byte 0 (0x69)**

| BIT         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Field       | TTF_byte_0[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x0             |   |   |   |   |   |   |   |
| Access Type | Read Only       |   |   |   |   |   |   |   |

| BITFIELD   | BITS | DESCRIPTION                                  | DECODE   |
|------------|------|--|--|
| TTF_byte_0 | 7:0  | Time to full byte0 readback from fuel gauge. | Concatenate byte1 and byte0: LSB is 5.625s. The full scale is 102.4 hours. |

### READY REG (0x6A)

| BIT         | 7           | 6 | 5           | 4           | 3           | 2           | 1             | 0                |
|-------------|-------------|---|-------------|-------------|-------------|-------------|---------------|------------------|
| Field       | dop_rdy_sig | – | dop_i2c_ena | ttf_reg_rdy | soc_reg_rdy | tte_reg_rdy | vcell_reg_rdy | avgvcell_reg_rdy |
| Reset       | 0x0         | – | 0b1         | 0b0         | 0x0         | 0x0         | 0x0           | 0x0              |
| Access Type | Read Only   | – | Write, Read | Read Only   | Read Only   | Read Only   | Read Only     | Read Only        |

| BITFIELD         | BITS | DESCRIPTION                     | DECODE                             |
|------------------|------|---------------------------------|------------------------------------|
| dop_rdy_sig      | 7    | DOP port ready.                 | 0x0: Not ready<br>0x1: Ready       |
| dop_i2c_ena      | 5    | Enable the DOP PORT sniffer.    | 0x0: Disable<br>0x1: Enable        |
| ttf_reg_rdy      | 4    | TTF byte value is reliable.     | 0x0: Not reliable<br>0x1: Reliable |
| soc_reg_rdy      | 3    | SOC byte value is reliable      | 0x0: Not reliable<br>0x1: Reliable |
| tte_reg_rdy      | 2    | TTE byte value is reliable      | 0x0: Not reliable<br>0x1: Reliable |
| vcell_reg_rdy    | 1    | VCELL byte value is reliable    | 0x0: Not reliable<br>0x1: Reliable |
| avgvcell_reg_rdy | 0    | AVGVCELL byte value is reliable | 0x0: Not reliable<br>0x1: Reliable |

### ADC CTRL1 (0x70)

| BIT         | 7 | 6              | 5 | 4 | 3 | 2              | 1 | 0 |
|-------------|---|----------------|---|---|---|----------------|---|---|
| Field       | – | AdcGndTrh[3:0] |   |   |   | ResDetRty[2:0] |   |   |
| Reset       | – | 0x4            |   |   |   | 0x1            |   |   |
| Access Type | – | Write, Read    |   |   |   | Write, Read    |   |   |

| BITFIELD  | BITS | DESCRIPTION   | DECODE  |
|-----------|------|---|---|
| AdcGndTrh | 6:3  | ADC Ground Threshold.   | LSB = 5.882mV                                     |
| ResDetRty | 2:0  | Number of Resistive Measurement Retries. The device retries the measurement if one of the following conditions is true: | 0x0: No retry.<br>>0x0: Number of retry attempts. |

| BITFIELD | BITS | DESCRIPTION   | DECODE |
|----------|------|---|--------|
|          |      | 1. (maximum ADC reading = 0xFF) AND (pullup current = 1µA) AND (average ADC reading < (0xFF - ADCNoiseClampRng[5:0]))<br>2. (maximum ADC reading = 0xFF) AND (pullup current ≠ 1µA)<br>If the condition is still true after this number of retries, the Abort result is reported. |        |

### ADC\_CTRL2 (0x71)

| BIT         | 7 | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------|---|---|---|---|---|
| Field       | – | – | AdcRng[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x9         |   |   |   |   |   |
| Access Type | – | – | Write, Read |   |   |   |   |   |

| BITFIELD | BITS | DESCRIPTION  | DECODE        |
|----------|------|--|---------------|
| AdcRng   | 5:0  | ADC Shift Factor. It applies to resistive measurements used in Moisture Detection. This register must NOT be set lower than the default value. | LSB = 5.882mV |

### ADC\_CTRL3 (0x72)

| BIT         | 7 | 6 | 5 | 4 | 3 | 2              | 1 | 0 |
|-------------|---|---|---|---|---|----------------|---|---|
| Field       | – | – | – | – | – | AdcAvgNum[2:0] |   |   |
| Reset       | – | – | – | – | – | 0x0            |   |   |
| Access Type | – | – | – | – | – | Write, Read    |   |   |

| BITFIELD  | BITS | DESCRIPTION   | DECODE   |
|-----------|------|---|--|
| AdcAvgNum | 2:0  | Number of Samples in ADC Reading Averaging. It applies to any resistive measurements used in moisture detection and accessory mode detection. | 0x0: 1 sample<br>0x1: 2 samples<br>0x2: 4 samples<br>0x3: 8 samples<br>0x4: 16 samples<br>0x5: 32 samples<br>0x6: 64 samples<br>0x7: 128 samples |



**ADC\_CTRL4 (0x73)**

| BIT         | 7 | 6 | 5                | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|------------------|---|---|---|---|---|
| Field       | – | – | AdcNoiseCtr[5:0] |   |   |   |   |   |
| Reset       | – | – | 0x0              |   |   |   |   |   |
| Access Type | – | – | Write, Read      |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION  | DECODE        |
|-------------|------|--|---------------|
| AdcNoiseCtr | 5:0  | ADC Result Margin to Account for External Noise and Avoid Result Clamping Close to Full-Scale. This register must NOT be changed from the default value. | LSB = 5.882mV |

**MOI\_DET\_REG1 (0x74)**

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1               | 0 |
|-------------|---|---|---|---|---|---|-----------------|---|
| Field       | – | – | – | – | – | – | RaccDetMlp[1:0] |   |
| Reset       | – | – | – | – | – | – | 0x0             |   |
| Access Type | – | – | – | – | – | – | Write, Read     |   |

| BITFIELD   | BITS | DESCRIPTION   | DECODE   |
|------------|------|---|--|
| RaccDetMlp | 1:0  | Target current used to specify moisture resistance threshold. | 0x0: 1µA<br>0x1: 4µA<br>0x2: 16µA<br>0x3: 64µA |

**MOI\_DET\_REG2 (0x75)**

| BIT         | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field       | RaccDetMThr[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x77             |   |   |   |   |   |   |   |
| Access Type | Write, Read      |   |   |   |   |   |   |   |

| BITFIELD    | BITS | DESCRIPTION                           | DECODE         |
|-------------|------|---------------------------------------|----------------|
| RaccDetMThr | 7:0  | Moisture detection voltage threshold. | LSB = 5.882mV. |

**MOI\_DET\_REG3 (0x76)**

| BIT         | 7 | 6           | 5 | 4           | 3 | 2           | 1 | 0           |
|-------------|---|-------------|---|-------------|---|-------------|---|-------------|
| Field       | – | moi_det_aut | – | moi_man_pl  | – | moi_man_rty | – | moi_aut_rty |
| Reset       | – | 0x1         | – | 0b0         | – | 0b0         | – | 0x1         |
| Access Type | – | Write, Read | – | Write, Read | – | Write, Read | – | Write, Read |

| BITFIELD    | BITS | DESCRIPTION  | DECODE  |
|-------------|------|--|---|
| moi_det_aut | 6    | Enable automatic moisture detection on PLC, performed with 16s rate starting 16s after device turn on.   | 0x0: Disabled<br>0x1: Enabled                             |
| moi_man_pl  | 4    | Manual moisture request on PLC. Write 1 to launch manual moisture detection. Autoclearing when done.   | 0x0: No moisture in progress<br>0x1: Moisture in progress |
| moi_man_rty | 2    | Manual retry for master detection in case of moisture found. Only valid when moisture is previously found. Write 1 to launch moisture retry. This allow the master detection to run moisture detection again. Autoclearing when retry is done. | 0x0: No retry request<br>0x1: Retry request running       |
| moi_aut_rty | 0    | Enable the automatic re-arm of moisture detection for PLC detection if moisture is found. System re-arm moisture automatically when moisture disappear.  | 0x0: Disable<br>0x1: Enabled                              |

**IP (0x77)**

| BIT         | 7 | 6 | 5 | 4 | 3 | 2 | 1               | 0 |
|-------------|---|---|---|---|---|---|-----------------|---|
| Field       | – | – | – | – | – | – | IP_RES_DET[1:0] |   |
| Reset       | – | – | – | – | – | – | 0x0             |   |
| Access Type | – | – | – | – | – | – | Read Only       |   |

| BITFIELD   | BITS | DESCRIPTION   | DECODE   |
|------------|------|---|--|
| IP_RES_DET | 1:0  | Final current used when moisture measurement is complete. It is set to 0x0 if the result is Abort or Open. It is set to 0x3 if the result is Short. | 0x0: 1µA<br>0x1: 4µA<br>0x2: 16µA<br>0x3: 64µA |

**ADC\_VAL1 (0x78)**

|                    |             |          |          |          |          |          |          |          |
|--------------------|-------------|----------|----------|----------|----------|----------|----------|----------|
| <b>BIT</b>         | <b>7</b>    | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>Field</b>       | ADCAvg[7:0] |          |          |          |          |          |          |          |
| <b>Reset</b>       | 0x0         |          |          |          |          |          |          |          |
| <b>Access Type</b> | Read Only   |          |          |          |          |          |          |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>               |
|-----------------|-------------|---|-----------------------------|
| ADCAvg          | 7:0         | Final Average ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. | LSB = 5.882mV = 0.392% typ. |

**ADC\_VAL2 (0x79)**

|                    |             |          |          |          |          |          |          |          |
|--------------------|-------------|----------|----------|----------|----------|----------|----------|----------|
| <b>BIT</b>         | <b>7</b>    | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>Field</b>       | ADCMax[7:0] |          |          |          |          |          |          |          |
| <b>Reset</b>       | 0x0         |          |          |          |          |          |          |          |
| <b>Access Type</b> | Read Only   |          |          |          |          |          |          |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>               |
|-----------------|-------------|---|-----------------------------|
| ADCMax          | 7:0         | Final Maximum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. | LSB = 5.882mV = 0.392% typ. |

**ADC\_VAL3 (0x7A)**

|                    |             |          |          |          |          |          |          |          |
|--------------------|-------------|----------|----------|----------|----------|----------|----------|----------|
| <b>BIT</b>         | <b>7</b>    | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| <b>Field</b>       | ADCMin[7:0] |          |          |          |          |          |          |          |
| <b>Reset</b>       | 0x0         |          |          |          |          |          |          |          |
| <b>Access Type</b> | Read Only   |          |          |          |          |          |          |          |

| <b>BITFIELD</b> | <b>BITS</b> | <b>DESCRIPTION</b>  | <b>DECODE</b>               |
|-----------------|-------------|---|-----------------------------|
| ADCMin          | 7:0         | Final Minimum ADC Reading. It is set to 0x00 if the result is Abort or Ground, and to 0xFF if the result is Open. | LSB = 5.882mV = 0.392% typ. |



### Ordering Information

| PART NUMBER   | TEMP RANGE    | PIN-PACKAGE |
|---------------|---------------|-------------|
| MAX20357EWX+  | -40°C to 85°C | 36-WLP      |
| MAX20357EWX+T | -40°C to 85°C | 36-WLP      |