MAX2223

Ultra-Wideband, Direct-Conversion, L-Band Satellite Tuner

General Description

The MAX2223 low-cost, direct-conversion tuner IC is designed for satellite set-top and very small aperture terminal (VSAT) applications. The device directly converts the satellite signals from the LNB to baseband using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The device includes an LNA and an RF variable-gain amplifier, I and Q down-converting mixers, and baseband amplifiers. The RF variable-gain amplifier provides more than 70dB of gain control range. The device supports an RF bandwidth of 1GHz.

The device includes fully monolithic VCOs, as well as a complete fractional-N frequency synthesizer. Additionally, an on-chip crystal oscillator is provided along with a buffered output for driving additional tuners and demodulators. Synthesizer programming and device configuration are accomplished with a 2-wire serial interface. The IC features a VCO auto-select (VAS) function that automatically selects the proper VCO. For multituner applications, the device can be configured to have one of two 2-wire interface addresses. A low-power standby mode is available whereupon the signal path is shutdown while leaving the reference oscillator, digital interface, and buffer circuits active, providing a method to reduce power in single and multituner applications.

A small number of passive components are needed to form a complete broadband satellite tuner DVB-S2 RF front-end solution. The tuner is available in a very small, 5mm x 5mm, 28-pin TQFN package.

Applications

- VSATs

Benefits and Features

- 925MHz to 2175MHz Frequency Range
- Monolithic VCO
  - Low Phase Noise: -97dBc/Hz at 10kHz
  - No Calibration Required
- High Dynamic Range: -75dBm to 0dBm
- 1GHz RF Bandwidth Supported
- Single +3.3V ±5% Supply
- Low-Power Standby Mode
- Address Pin for Multituner Applications
- Differential I/Q Interface
- I^2C-Compatible, 2-Wire Serial Interface
- Very Small, 5mm x 5mm, 28-Pin TQFN Package

***Ordering Information* appears at end of data sheet.**

19-100597; Rev 1; 9/20

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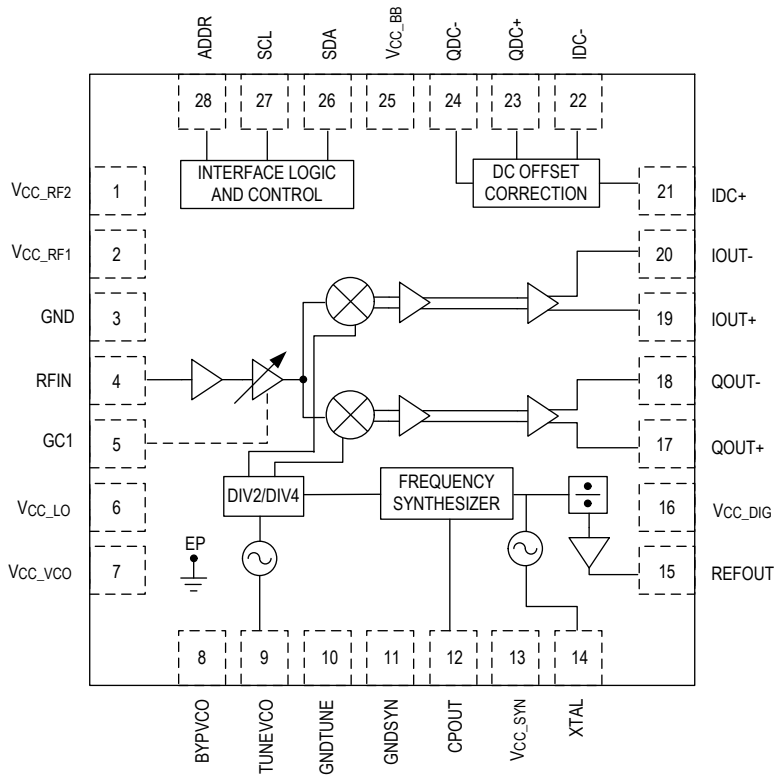
Block Diagram



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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +3.9V
All Other Pins to GND ..... -0.3V to (V_{CC} + 0.3)V
RF Input Power: RFIN ..... +10dBm
BYPVCO, CPOUT, XTAL, REFOUT, IOUT_, QOUT_, IDC_, QDC_ to GND Short-Circuit Protection 10s
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C) 2.75W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

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Package Code	T2855+3
Outline Number	21-0140
Land Pattern Number	90-0023
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	11°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	11°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(**AC Parameter Global Conditions**: MAX2223 Evaluation Kit: V_{CC} = +3.13V to +3.47V, T_A = -40°C to +85°C, default register settings. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1), **DC Parameter Global Conditions**: MAX2223 Evaluation Kit: $V_{CC\_}$ = +3.13V to +3.47V, f_{XTAL} = 27MHz, T_A = -40°C to +85°C, V_{GC1} = +0.5V (max gain), default register settings. No input signals at RF, baseband I/Os are open circuited. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC / SUPPLY						
Supply Voltage	V_{CC}		3.13	3.3	3.47	V
Supply Current		Receive mode, bit STBY = 0		140	180	mA
		Standby mode, bit STBY = 1		3		
DC / ADDRESS SELECT INPUT (ADDR)						
Digital Input-Voltage High	V_{IH}		2.4			V
Digital Input-Voltage Low	V_{IL}				0.5	V
Digital Input-Current High	I_{IH}				50	µA

Electrical Characteristics (continued)

(**AC Parameter Global Conditions**: MAX2223 Evaluation Kit: V_{CC} = +3.13V to +3.47V, T_A = -40°C to +85°C, default register settings. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1), **DC Parameter Global Conditions**: MAX2223 Evaluation Kit: $V_{CC\_}$ = +3.13V to +3.47V, f_{XTAL} = 27MHz, T_A = -40°C to +85°C, V_{GC1} = +0.5V (max gain), default register settings. No input signals at RF, baseband I/Os are open circuited. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input-Current Low	I_{IL}		-50			µA
DC / ANALOG GAIN-CONTROL INPUT (GC1)						
Input Voltage Range		Maximum gain = 0.5V	0.5		2.7	V
Input Bias Current			-50		+50	µA
DC / VCO TUNING VOLTAGE INPUT (TUNEVCO)						
Input Voltage Range			0.4		2.3	V
DC / 2-WIRE SERIAL INPUTS (SCL, SDA)						
Clock Frequency					400	kHz
Input Logic-Level High			0.7 x V_{CC}			V
Input Logic-Level Low					0.3 x V_{CC}	V
Input Leakage Current		Digital inputs = GND or V_{CC}		±0.1	±1	µA
DC / 2-WIRE SERIAL OUTPUT (SDA)						
Output Logic-Level Low		I_{SINK} = 1mA			0.4	V
AC / MAIN SIGNAL PATH PERFORMANCE						
Input Frequency Range			925		2175	MHz
Gain		f_{IN} = 2175MHz	57.5	64		dB
RF Gain Flatness		925MHz to 2175MHz		4	6	dB
RF Gain-Control Range (GC1)		0.5V < V_{GC1} < 2.7V, 2175MHz	65	73		dB
In-Band Input IP3		(Note 3)		16		dBm
Out-of-Band Input IP3		(Note 4)		16		dBm
Input IP2		(Note 5)		32		dBm
Noise Figure		V_{GC1} = 0.5V (max gain)		8		dB
		V_{GC1} is adjusted to back off RF gain by 10dB relative to maximum (Note 2)		9	12.5	
Minimum RF Input Return Loss		925MHz < f_{RF} < 2175MHz in 75Ω system		12		dB
AC / BASEBAND OUTPUT CHARACTERISTICS						
Nominal Differential Output Voltage Swing		Differential R_{LOAD} = 100Ω		330		mV_{P-P}
CW Input Minimum Image Rejection at Band Edge		f_{LO} = 1.5GHz, CW input at 1.0GHz or 2.0GHz		12		dB

Electrical Characteristics (continued)

(**AC Parameter Global Conditions**: MAX2223 Evaluation Kit: V_{CC} = +3.13V to +3.47V, T_A = -40°C to +85°C, default register settings. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1), **DC Parameter Global Conditions**: MAX2223 Evaluation Kit: $V_{CC\_}$ = +3.13V to +3.47V, f_{XTAL} = 27MHz, T_A = -40°C to +85°C, V_{GC1} = +0.5V (max gain), default register settings. No input signals at RF, baseband I/Os are open circuited. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Drift of Image Component with Temperature		f_{LO} = 1.5GHz, CW input at 1.0GHz or 2.0GHz, temperature drift between -5°C and +27°C (Note 6)		30		dB
Differential I/Q Output Impedance		Real Z_O, from 1MHz to 550MHz		100		Ω
Output 1dB Compression Voltage		Differential. R_{LOAD} = 100Ω		1		V_{P-P}
Baseband Highpass -3dB Frequency Corner		47nF capacitors at IDC_, QDC_		400		Hz
Output In-Band Spurious		Composite spurs within DC to 500MHz (Note 7)		-25		dBc
AC / FREQUENCY SYNTHESIZER						
LO-Divider Frequency Range			925		2175	MHz
LO-Divider Range (N)			30		185	
Reference-Divider Frequency Range			18		30	MHz
Reference-Divider Range (R)			1		1	
Phase-Detector Comparison Frequency			18		30	MHz
AC / VOLTAGE-CONTROLLED OSCILLATOR AND LO GENERATION						
LO Frequency Range			925		2175	MHz
LO Phase Noise		f_{OFFSET} = 10kHz		-96		
		f_{OFFSET} = 100kHz		-101		dBc/Hz
		f_{OFFSET} = 1MHz		-122		
AC / XTAL/REFERENCE OSCILLATOR INPUT AND OUTPUT BUFFER						
Frequency Range			12		30	MHz
Input Overdrive Level		AC-coupled sine-wave input		1		V_{P-P}
XTAL Output-Buffer Divider Range			1		8	
XTAL Output Voltage Swing		12MHz to 30MHz, C_{LOAD} = 10pF	0.7	1.5	2	V_{P-P}
XTAL Output Duty Cycle				50		%

Note 1: Min/max values are production tested at T_A = +25°C. Min/max limits at T_A = -40°C and T_A = +85°C are guaranteed by design and characterization.

Note 2: Guaranteed by design and characterization at T_A = +25°C.

Note 3: In-band IIP3 test conditions: GC1 set to provide the nominal baseband output drive when mixing down a -3dBm tone at 2000MHz to 50MHz baseband (f_{LO} = 1950MHz). Two tones at -6dBm each are applied at 2000MHz and 2001MHz. The IM3 tone at 49MHz is measured at baseband, but is referred to the RF input.

Note 4: Out-of-band IIP3 test conditions: GC1 set to provide the nominal baseband differential output drive when mixing down a -3dBm tone at 1730MHz to 230MHz baseband (f_{LO} = 1500MHz). Two tones at -6dBm each are applied at 1730MHz and 2480MHz. The IM3 tone at 520MHz is measured at baseband, but is referred to the RF input.

Note 5: Input IP2 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -3dBm tone at 2175MHz to 5MHz baseband (f_{LO} = 2170MHz). Two tones at -6dBm each are applied at 925MHz and 1250MHz. The IM2 tone at 5MHz is measured at baseband, but is referred to the RF input.

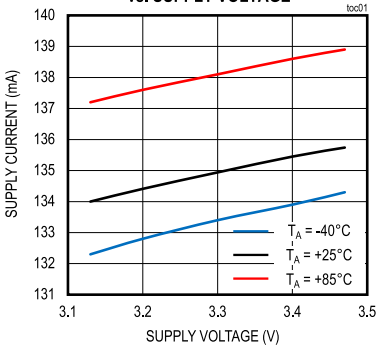
Note 6: A complex image component is expressed as $c = (1-\eta e^{j\varphi})/(1 + \eta e^{j\varphi})$, with η the gain imbalance and φ the phase imbalance. The drift of image component (in unit of dB) is $20\log_{10}|c_1-c_2|$, where c_1 and c_2 are complex values of the image component at two different temperatures.

Note 7: GC1 set to provide the nominal baseband output drive when mixing down a -66dBm tone at 1505MHz to 5MHz baseband (f_{LO} = 1500MHz).

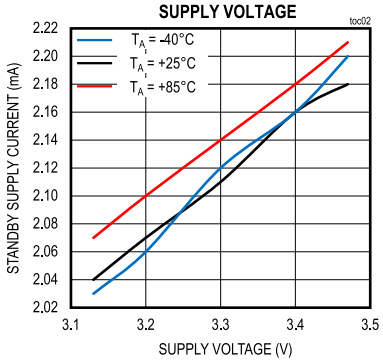
Typical Operating Characteristics

(MAX2223 Evaluation Kit: V_{CC} = +3.3V, T_A = +25°C, V_{GC1} = +0.5V, default register settings, unless otherwise noted.)

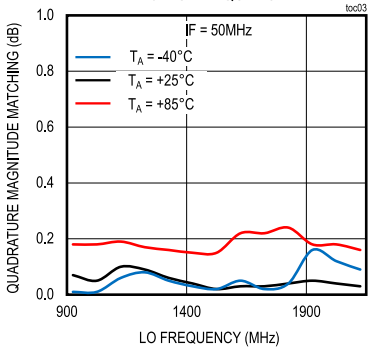
SUPPLY CURRENT vs. SUPPLY VOLTAGE



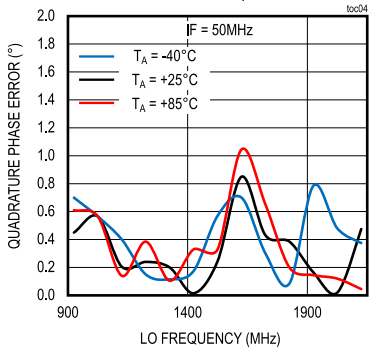
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



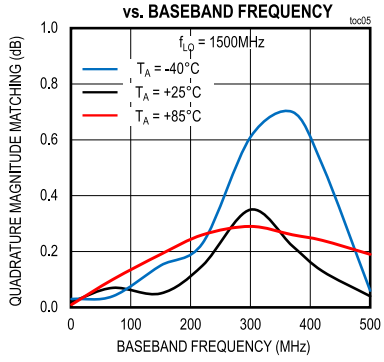
QUADRATURE MAGNITUDE MATCHING vs. LO FREQUENCY



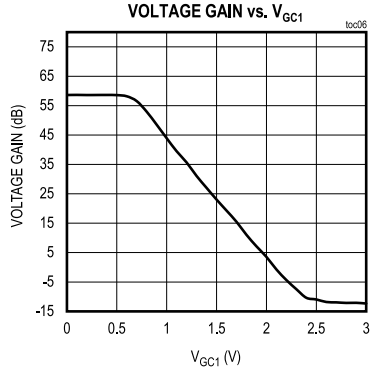
QUADRATURE PHASE ERROR vs. LO FREQUENCY



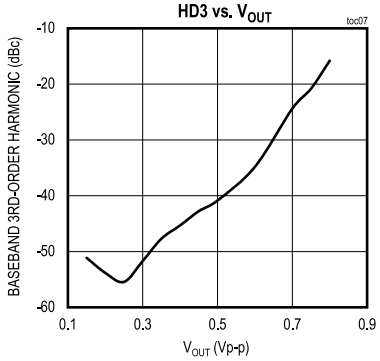
QUADRATURE MAGNITUDE MATCHING vs. BASEBAND FREQUENCY



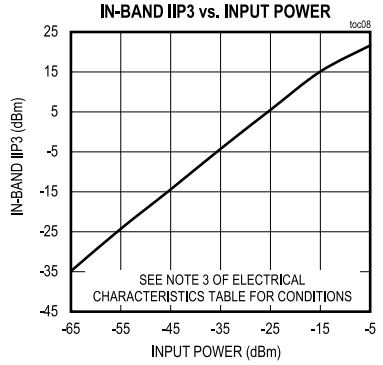
VOLTAGE GAIN vs. V_{GC1}



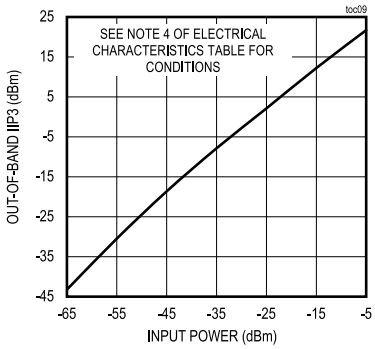
HD3 vs. V_{OUT}



IN-BAND IIP3 vs. INPUT POWER

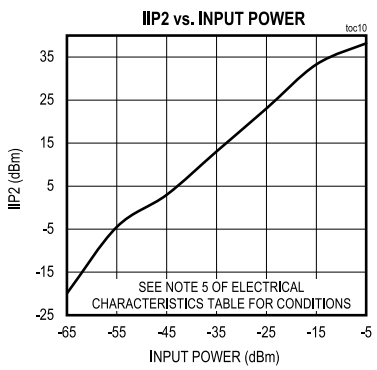


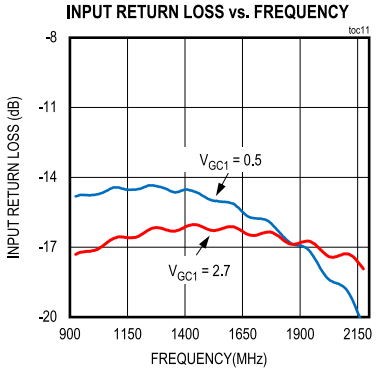
OUT-OF-BAND IIP3 vs. INPUT POWER



Typical Operating Characteristics (continued)

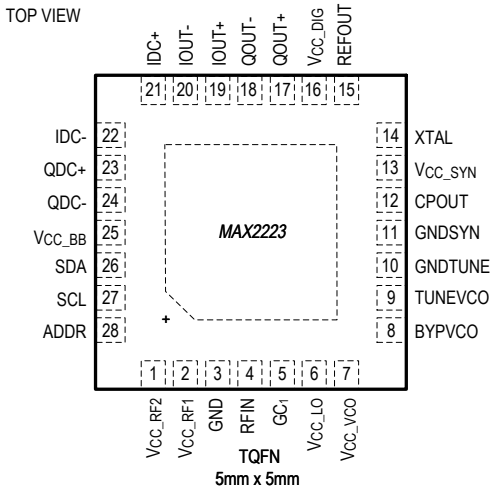
(MAX2223 Evaluation Kit: V_{CC} = +3.3V, T_A = +25°C, V_{GC1} = +0.5V, default register settings, unless otherwise noted.)





Pin Configuration

28 TQFN



Pin Description

PIN	NAME	FUNCTION
1	V_{CC_RF2}	DC Power Supply for LNA. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
2	V_{CC_RF1}	DC Power Supply for LNA. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.

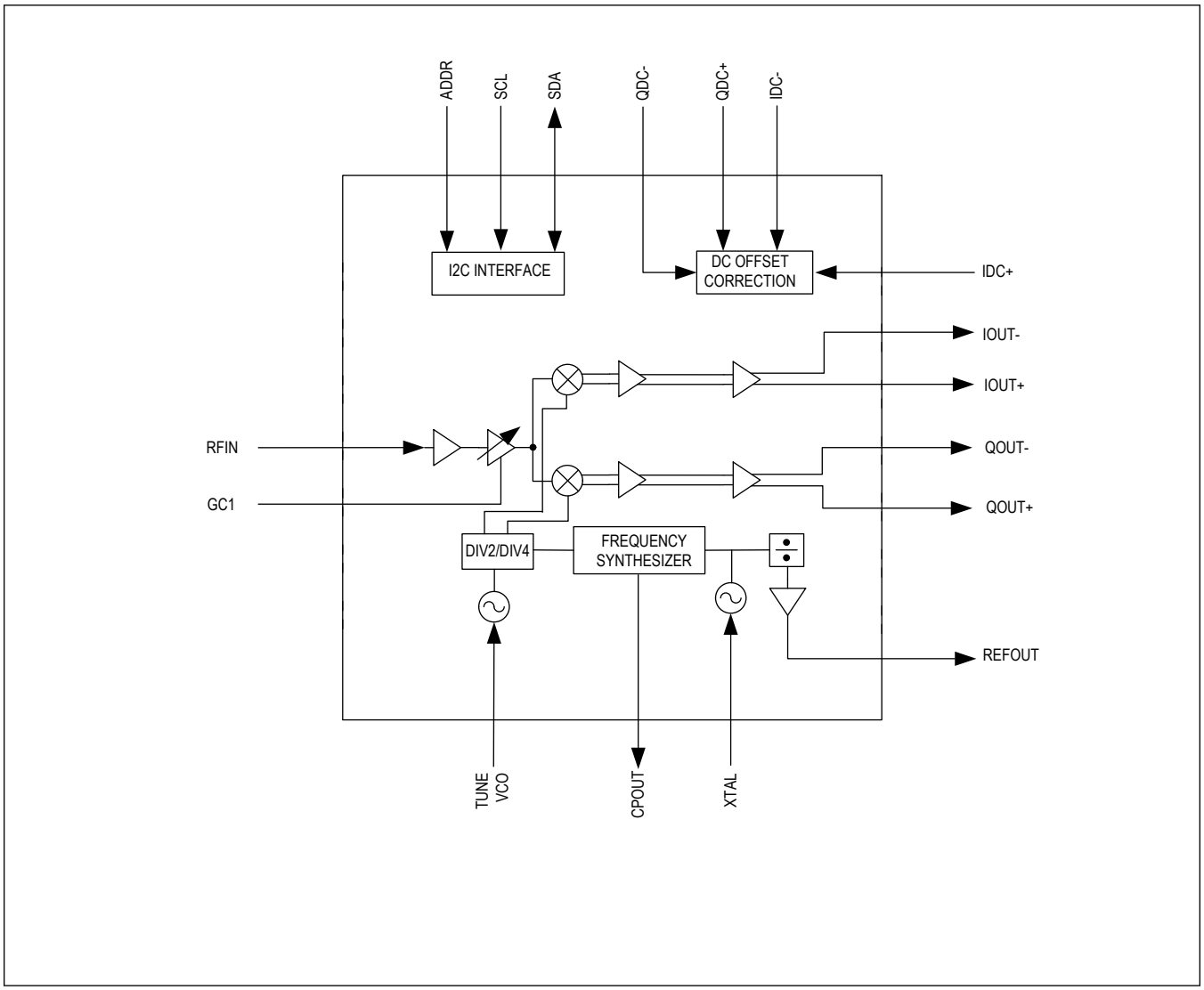
Pin Description (continued)

PIN	NAME	FUNCTION
3	GND	Ground. Connect to the PCB ground plane.
4	RFIN	RF Input. Connect to an RF source through a DC-blocking capacitor.
5	GC_1	RF Gain-Control Input. High-impedance analog input with a 0.5V to 2.7V operating range. V_{GC1} = 0.5V corresponds to the maximum gain setting.
6	V_{CC_LO}	DC Power Supply for LO Generation Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
7	V_{CC_VCO}	DC Power Supply for VCO Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
8	BYPVCO	Internal VCO Bias Bypass. Bypass to GND with a 100nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
9	TUNEVCO	High-Impedance VCO Tune Input. Connect the PLL loop filter output directly to this pin with as short of a connection as possible.
10	GNDTUNE	Ground for TUNEVCO. Connect to the PCB ground plane.
11	GNDSYN	Ground for Synthesizer. Connect to the PCB ground plane.
12	CPOUT	Charge-Pump Output. Connect this output to the PLL loop filter input with the shortest connection possible.
13	V_{CC_SYN}	DC Power Supply for Synthesizer Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
14	XTAL	Crystal-Oscillator Interface. Use with an external parallel-resonance-mode crystal through a series 1nF capacitor. See the *Typical Application Circuit*.
15	REFOUT	Crystal-Oscillator Buffer Output. A DC-blocking capacitor must be used when driving external circuitry.
16	V_{CC_DIG}	DC Power Supply for Digital Logic Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
17	QOUT+	Quadrature Baseband Differential Positive Output. AC-couple with 47nF capacitor to the demodulator input.
18	QOUT-	Quadrature Baseband Differential Negative Output. AC-couple with 47nF capacitor to the demodulator input.
19	IOUT+	In-Phase Baseband Differential Postive Output. AC-couple with 47nF capacitor to the demodulator input.
20	IOUT-	In-Phase Baseband Differential Negative Output. AC-couple with 47nF capacitor to the demodulator input.
21	IDC+	I-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from IDC- to IDC+.
22	IDC-	I-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from IDC- to IDC+.
23	QDC+	Q-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from QDC- to QDC+.
24	QDC-	Q-Channel Baseband DC Offset Correction. Connect a 47nF ceramic chip capacitor from QDC- to QDC+.

Pin Description (continued)

PIN	NAME	FUNCTION
25	V_{CC_BB}	DC Power Supply for Baseband Circuits. Connect to a +3.3V low-noise supply. Bypass to GND with a 1nF capacitor connected as close as possible to the pin. Do not share capacitor ground vias with other ground connections.
26	SDA	2-Wire Serial-Data Interface. Requires 21kΩ pullup resistor to V_{CC}.
27	SCL	2-Wire Serial-Clock Interface. Requires 21kΩ pullup resistor to V_{CC}.
28	ADDR	I^2C Address. Must be connected to either ground (logic 0) or supply (logic 1).
—	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation.

Functional Diagram



Detailed Description

The MAX2223 amplifies and downconverts RF signals in the 925MHz to 2175MHz range directly to the baseband I/Q signals. An RF bandwidth of up to 1GHz is supported.

2-Wire Serial Interface

The MAX2223 uses a 2-wire I^2C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX2223 and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX2223 behaves as a slave device that transfers and receives data to and from the master. SDA and SCL must be pulled high with external pullup resistors (1kΩ or greater) for proper bus operation. Pullup resistors should be referenced to the MAX2223's V_{CC}.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte in or out of the MAX2223 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX2223 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX2223 has a 7-bit slave address that must be sent to the device following a START condition to initiate communication. The slave address is internally programmed to 1100000. The eighth bit (R/$\overline{W}$) following the 7-bit address determines whether a read or write operation occurs.

The MAX2223 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 1).

The write/read address is C0/C1 if ADDR pin is connected to ground. The write/read address is C2/C3 if the ADDR pin is connected to V_{CC}.

Write Cycle

When addressed with a write command, the MAX2223 allows the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition, followed by the seven slave address bits and a write bit (R/$\overline{W}$ = 0). The MAX2223 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register (the register it wishes to write to) to the slave. If the slave acknowledges the address, the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit. The MAX2223 again issues an ACK if the data is successfully written to the register. The master can

continue to write data to the successive internal registers with the MAX2223 acknowledging each successful transfer, or it can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Read Cycle

When addressed with a read command, the MAX2223 allows the master to read back a single register, or multiple successive registers.

A read cycle begins with the bus master issuing a START condition followed by the seven slave address

bits and a write bit (R/$\overline{W}$ = 0). The MAX2223 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read. The slave acknowledges the address. Then, a START condition is issued by the master, followed by the seven slave address bits and a read bit (R/$\overline{W}$ = 1). The MAX2223 issues an ACK if the slave address byte is successfully received. The MAX2223 starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK and continue to read successive registers, or the master can terminate the transmission by issuing a NACK. The read cycle does not terminate until the master issues a STOP condition.

Figure 3 illustrates an example in which registers 0, 1, and 2 are read back.

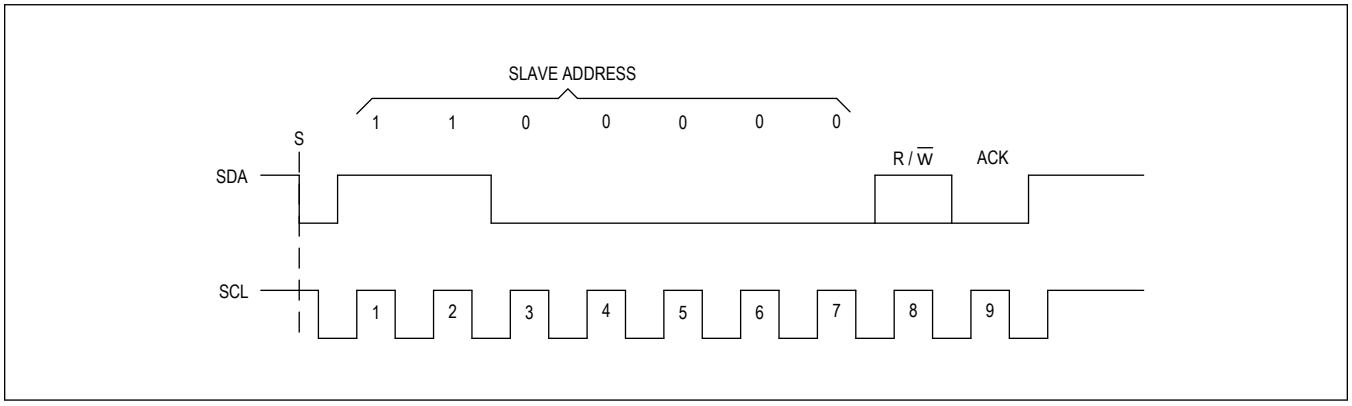


Figure 1. MAX2223 Slave Address Byte with ADDR Pin Connected to Ground

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	1100000	0	—	0x00	—	0x0E	—	0xD8	—	0xE1	—	

Figure 2. Write Registers 0, 1, and 2 with 0x0E, 0xD8, and 0xE1, Respectively—Example

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	READ FROM STATUS BYTE-1 REGISTER	ACK	READ FROM STATUS BYTE-2 REGISTER	ACK/NACK	STOP
	1100000	1	—	—	—	—	—	

Figure 3. Receive Data from Read Registers—Example

Register Map

Memory Map

ADDRESS	NAME	MSB							LSB
Register Block									
0x00	N-Divider MSB[7:0]	FRAC	N[14:8]						
0x01	N-Divider LSB[7:0]	N[7:0]							
0x02	Charge Pump[7:0]	CPMP[1:0]		CPLIN[1:0]		F[3:0]			
0x03	F-Divider MSB[7:0]	F[15:8]							
0x04	F-Divider LSB[7:0]	F[7:0]							
0x05	XTAL Buffer and Reference Divider[7:0]	XD[2:0]			R[4:0]				
0x06	PLL[7:0]	D	CPS	ICP	RESERVED[4:0]				
0x07	VCO[7:0]	VCO[4:0]				VAS	ADL	ADE	
0x08	RESERVED[7:0]	RESERVED[7:0]							
0x09	Control[7:0]	STBY	RESERVED	PWDN	RESERVED	RESERVED[3:0]			
0x0A	Shutdown[7:0]	RESERVED	PLL	DIV	VCO	BB	RFMIX	RFVGA	FE
0x0B	Test[7:0]	CPTST[2:0]			RESERVED	TURBO	LDMUX[2:0]		
0x0C	Status Byte-1[7:0]	POR	VASA	VASE	LD	RESERVED[3:0]			
0x0D	Status Byte-2[7:0]	VCOSBR[4:0]				ADC[2:0]			

Register Details

N-Divider MSB (0x00)

BIT	7	6	5	4	3	2	1	0
Field	FRAC	N[14:8]						
Reset	0x1	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
FRAC	7	Users must program to 1 after powering up the device
N	6:0	Sets the most significant bits of the PLL integer division number (N). N can range from 19 to 251

N-Divider LSB (0x01)

BIT	7	6	5	4	3	2	1	0
Field	N[7:0]							
Reset	0x23							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
N	7:0	Sets the least significant bits of the PLL integer-divide number. N can range from 19 to 251.

Charge Pump (0x02)

BIT	7	6	5	4	3	2	1	0
Field	CPMP[1:0]		CPLIN[1:0]		F[3:0]			
Reset	0x0		0x0		0x2			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION
CPMP	7:6	Charge-pump minimum pulse width. Users must program to 00 upon powering up the device
CPLIN	5:4	Controls charge-pump linearity. Users must program to 01 upon powering up the device
F	3:0	Sets the 4 most significant bits of the PLL fractional divide number. Default value is F = 194,180 decimal

F-Divider MSB (0x03)

BIT	7	6	5	4	3	2	1	0
Field	F[15:8]							
Reset	0xF6							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
F	7:0	Sets the most significant bits of the PLL fractional-divide number (F). Default value is F = 194,180 decimal

F-Divider LSB (0x04)

BIT	7	6	5	4	3	2	1	0
Field	F[7:0]							
Reset	0x84							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
F	7:0	Sets the least significant bits of the PLL fractional-divide number (F). Default value is F = 194,180 decimal

XTAL Buffer and Reference Divider (0x05)

BIT	7	6	5	4	3	2	1	0
Field	XD[2:0]			R[4:0]				
Reset	0x0			0x1				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION
XD	7:5	Sets the crystal-divider setting. 000 = Divide by 1. 001 = Divide by 2. 011 = Divide by 3. 100 = Divide by 4. 101 through 110 = All divide values from 5 (101) to 7 (110). 111 = Divide by 8.
R	4:0	Sets the PLL reference-divider (R) number. Users must program to 00001 upon powering up the device. 00001 = Divide by 1; other values are not tested.

PLL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	D	CPS	ICP	RESERVED[4:0]				
Reset	0x1	0x1	0x0	0x0				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
D	7	VCO divider setting. 0 = Divide by 2. Use for LO frequencies ≥ 1125MHz. 1 = Divide by 4. Use for LO frequencies < 1125MHz.
CPS	6	Charge-pump current mode. 0 = Charge-pump current controlled by ICP bit. 1 = Charge-pump current controlled by VCO autoselect (VAS)
ICP	5	Charge-pump current. 0 = 600µA (typ) 1 = 1200µA (typ)
RESERVED	4:0	Reserved

VCO (0x07)

BIT	7	6	5	4	3	2	1	0
Field	VCO[4:0]					VAS	ADL	ADE
Reset	0x19					0x1	0x0	0x0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
VCO	7:3	Controls which VCO is activated when using manual VCO programming mode. This also serves as the starting point for the VCO autoselection (VAS) mode
VAS	2	VCO autoselection (VAS) circuit. 0 = Disable VCO selection must be programmed through I^2C. 1 = Enable VCO selection controlled by autoselection circuit.
ADL	1	Enables or disables the VCO tuning voltage ADC latch when the VCO autoselect mode (VAS) is disabled. 0 = Disables the ADC latch. 1 = Latches the ADC value.

BITFIELD	BITS	DESCRIPTION
ADE	0	Enables or disables VCO tuning voltage ADC read when the VCO autoselect mode (VAS) is disabled. 0 = Disables ADC read. 1 = Enables ADC read.

RESERVED (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RESERVED	7:0	Reserved

Control (0x09)

BIT	7	6	5	4	3	2	1	0
Field	STBY	RESERVED	PWDN	RESERVED	RESERVED[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
STBY	7	Software standby control. 0 = Normal operation. 1 = Disables the signal path and frequency synthesizer leaving only the 2-wire bus, crystal oscillator, XTALOUT buffer, and XTALOUT buffer divider active.
RESERVED	6	Reserved
PWDN	5	Factory use only. 0 = Normal operation; other value is not tested.
RESERVED	4	Reserved
RESERVED	3:0	Reserved: User must program 0x5 when powering up the device.

Shutdown (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	PLL	DIV	VCO	BB	RFMIX	RFVGA	FE
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RESERVED	7	Reserved
PLL	6	PLL enable. 0 = Normal operation. 1 = Shuts down the PLL. Value not tested.

BITFIELD	BITS	DESCRIPTION
DIV	5	Divider enable. 0 = Normal operation. 1 = Shuts down the divider. Value not tested.
VCO	4	VCO enable. 0 = Normal operation. 1 = Shuts down the VCO. Value not tested.
BB	3	Baseband enable. 0 = Normal operation. 1 = Shuts down the baseband. Value not tested.
RFMIX	2	RF mixer enable. 0 = Normal operation. 1 = Shuts down the RF mixer. Value not tested.
RFVGA	1	RF VGA enable. 0 = Normal operation. 1 = Shuts down the RF VGA. Value not tested.
FE	0	Front-end enable. 0 = Normal operation. 1 = Shuts down the front-end. Value not tested.

Test (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	CPTST[2:0]			RESERVED	TURBO	LDMUX[2:0]		
Reset	0x0			0x0	0x1	0x0		
Access Type	Write, Read			Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
CPTST	7:5	Charge-pump test modes. 000 = Normal operation (default).
RESERVED	4	Reserved
TURBO	3	Charge-pump fast lock. Users must program to 1 after powering up the device.
LDMUX	2:0	REFOUT output. 000 = Normal operation; other values are not tested.

Status Byte-1 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	POR	VASA	VASE	LD	RESERVED[3:0]			
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION
POR	7	Power-on reset status. 0 = Chip status register has been read with a stop condition since last power-on. 1 = Power-on reset (power cycle) has occurred. Default values have been loaded in registers.

BITFIELD	BITS	DESCRIPTION
VASA	6	Indicates whether VCO autoselection was successful. 0 = Indicates the autoselect function is disabled or unsuccessful VCO selection. 1 = Indicates successful VCO autoselection.
VASE	5	Status indicator for the autoselect function. 0 = Indicates the autoselect function is active. 1 = Indicates the autoselect process is inactive.
LD	4	PLL lock detector. TURBO bit must be programmed to 1 for valid LD reading. 0 = Unlocked. 1 = Locked.
RESERVED	3:0	Reserved

Status Byte-2 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	VCOSBR[4:0]					ADC[2:0]		
Reset								
Access Type	Read Only					Read Only		

BITFIELD	BITS	DESCRIPTION
VCOSBR	7:3	VCO band readback
ADC	2:0	VAS ADC output readback. 000 = Out of lock. 001 = Locked. 010 = VAS locked. 101 = VAS locked. 110 = Locked. 111 = Out of lock.

Applications Information

RF Input

The RF input of the MAX2223 is internally matched to 75Ω. Only a DC-blocking capacitor is needed. See *Typical Application Circuit*.

RF Gain Control

The MAX2223 features a variable-gain low-noise amplifier providing 73dB of RF gain range. The voltage control (V_{GC1}) range is 0.5V (minimum attenuation) to 2.7V (maximum attenuation).

DC Offset Cancellation

The DC offset cancellation is required to maintain the I/Q output dynamic range. Connecting an external capacitor between IDC+ and IDC-forms a highpass filter for the I channel and an external capacitor between QDC+ and QDC-forms a highpass filter for the Q channel. Keep the value of the external capacitor less than 47nF to form a typical highpass corner frequency of 250Hz.

XTAL Oscillator

The MAX2223 contains an internal reference oscillator, reference output divider, and output buffer. All that is required is to connect a crystal through a series 1nF capacitor. To minimize parasitics, place the crystal and series capacitor as close as possible to pin 14 (XTAL). See Table 1 for crystal (XTAL) ESR requirements.

Table 1. Maximum Crystal ESR Requirement

ESR_{MAX} (Ω)	XTAL FREQUENCY (MHz)
60	$18 < f_{XTAL} \leq 30$

Programming the Fractional-N Synthesizer

The MAX2223 utilizes a fractional-N type synthesizer for LO frequency programming. To program the frequency synthesizer, the N and F values are encoded as straight binary numbers. Determination of these values is illustrated by the following example:

f_{LO} is 2170MHz

f_{XTAL} is 27MHz

Phase-detector comparison frequency is from 18MHz to 30MHz.

R divider = R[4:0] = 1

f_{COMP} = 27MHz/1 = 27MHz

D = f_{LO}/f_{COMP} = 2170/27 = 80.37470

Integer portion:

N = 80

N[14:8] = 0

N[7:0] = 0101 0000

Fractional portion:

F = 0.370370 x 220 = 388,361 (round up the decimal portion)

F = 0101 1110 1101 0000 1001

Note: When changing LO frequencies, all the divider registers (integer and fractional) must be programmed to activate the VAS function regardless of whether individual registers are changed.

VCO Autoselect (VAS)

The MAX2223 includes 24 VCO bands. The local oscillator frequency can be manually selected by programming the VCO[4:0] bits in the VCO register. The selected VCO band is reported in the Status Byte-2 register.

Alternatively, the MAX2223 can be set to autonomously select a VCO band by setting the VAS bit in the VCO register to logic-high. The VAS routine is initiated once the F-Divider LSB register word (register 0x4) is loaded.

Thus, it is important to write register 0x4 **after** any of the following PLL related bits have been changed:

N-Divider bits (registers 0x0 and/or 0x1)

F-Divider bits (registers 0x3 and/or 0x4)

Reference Divider bits (register 0x5)

D24, CPS, or ICP bits (register 0x6)

This will ensure all intended bits have been programmed **before** the VAS is initiated and the PLL is locked. The VCO band value programmed in the VCO[4:0] register serves as the starting point for the automatic VCO selection process.

During the selection process, the VASE bit in the Status Byte-1 register is cleared to indicate the autoselection function is active. Upon successful completion, bits VASE and VASA are set and the VCO band selected is reported in the Status Byte-2 register. If the search is unsuccessful, VASA is cleared and VASE is set. This indicates that search has ended but no good VCO band has been found, and occurs when trying to tune to a frequency outside the specified frequency range.

3-Bit ADC

The MAX2223 has an internal 3-bit ADC connected to the VCO tune pin (TUNEVCO). This ADC can be used for checking the lock status of the VCO.

Table 2 summarizes the ADC output bits and the VCO lock indication. The VCO autoselect routine only selects a VCO in the “VAS locked” range. This allows room for a VCO to drift over temperature and remain in a valid “locked” range.

The ADC must first be enabled by setting the ADE bit in the VCO register. The ADC reading is latched by a subsequent programming of the ADC latch bit (ADL = 1). The ADC value is reported in the Status Byte-2 register.

Table 2. ADC Trip Points and Lock Status

ADC[2:0]	LOCK STATUS
000	Out of lock
001	Locked
010	VAS locked
101	VAS locked
110	Locked
111	Out of lock

Standby Mode

The MAX2223 features normal operating mode and standby mode using the I^2C interface. Setting a logic high to the STBY bit in the Control register puts the device into standby mode, during which only the 2-wire-compatible bus, the crystal oscillator, the XTAL buffer, and the XTAL buffer divider are active.

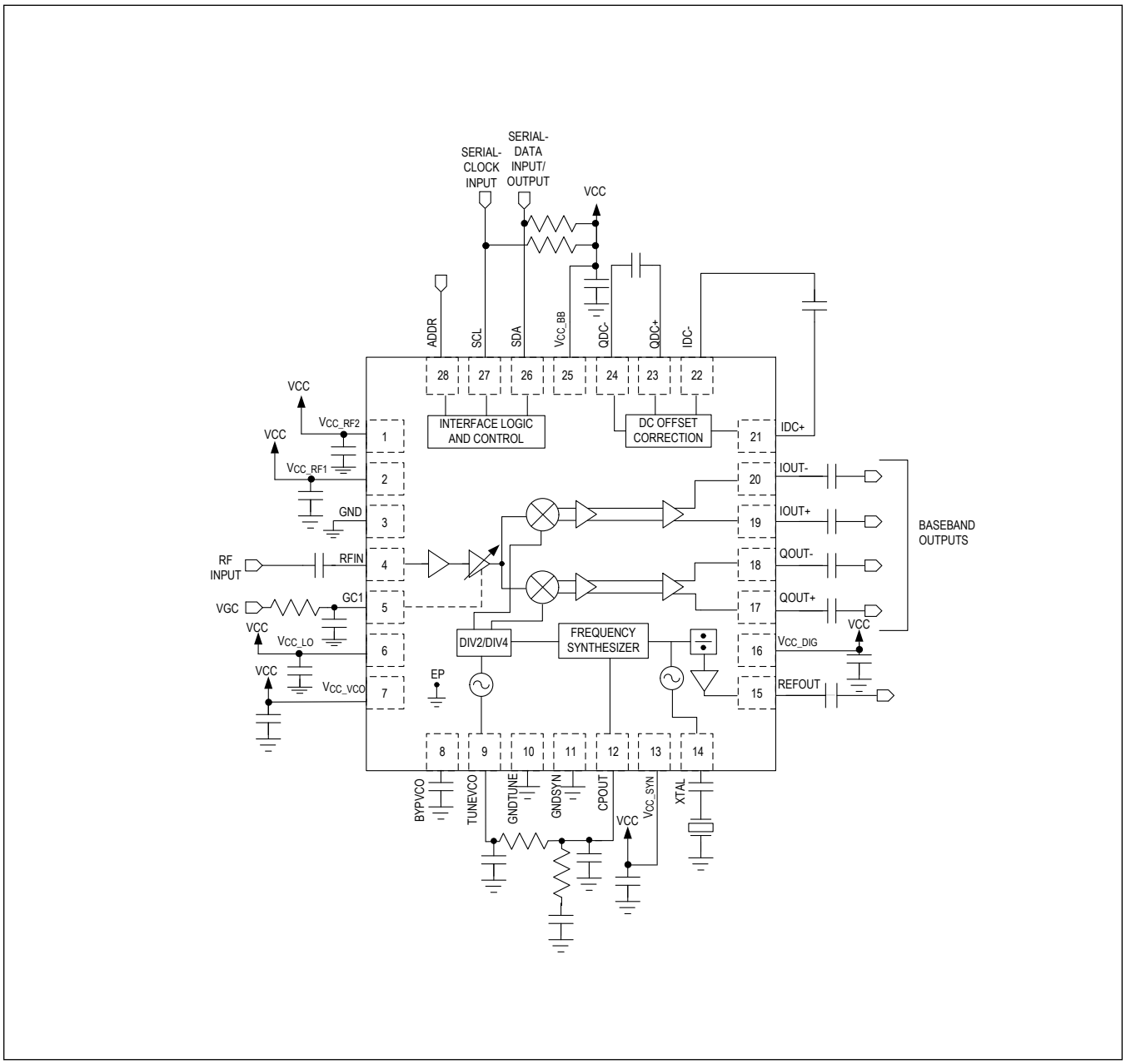
In all cases, register settings loaded prior to entering shutdown are saved upon transition back to active mode. Default register values are provided for the user’s convenience only. It is the user’s responsibility to load all the registers no sooner than 100µs after the device is powered up.

Layout Considerations

The MAX2223 EV kit serves as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. For proper operation, the exposed paddle must

be soldered evenly to the board's ground plane. Use abundant vias beneath the exposed paddle for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each V_{CC} pin to ground with a 1nF capacitor placed as close as possible to the pin.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX2223ETI+	-40°C to +85°C	28 TQFN-EP*

EP = Exposed paddle.*

+ Denotes a lead(Pb)-free/RoHS-compliant package.