Click here to ask an associate for production status of specific part numbers.

MAX22256/MAX22258

Compact, 36V H-Bridge Transformer Driver for Isolated Supplies

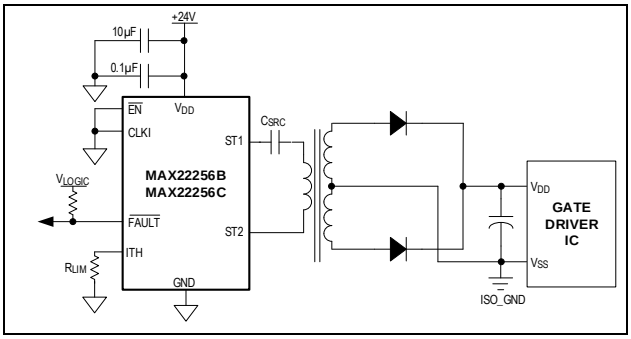
Product Highlights

- Simple, Flexible Design
  - 5V to 36V Supply Range
  - Up to 91% Efficiency
  - Provides over 15W to Transformer
  - Undervoltage Lockout
  - Internal or External Clock Source
  - Synchronous Clock Output (MAX22258)
  - Programmable Overcurrent Threshold
  - 30ns to 200ns Adjustable Deadtime (MAX22258)
- Robust Integrated System Protection
  - Fault Detection and Indication
  - Overcurrent Limiting up to 1A
  - Over-Temperature Protection
  - Precision Internal Clock Source (±6%) Prevents Excessive Transformer Core Losses Due to Frequency Shift
  - Wide Temperature Range: -40°C to +125°C
- Space Savings
  - Small 3mm x 3mm 10-Pin TDFN Package (MAX22256A/B/C) with 0.5mm Pitch
  - Small 4mm x 5mm 14-Pin TSSOP Package (MAX22258) with 0.65mm Pitch

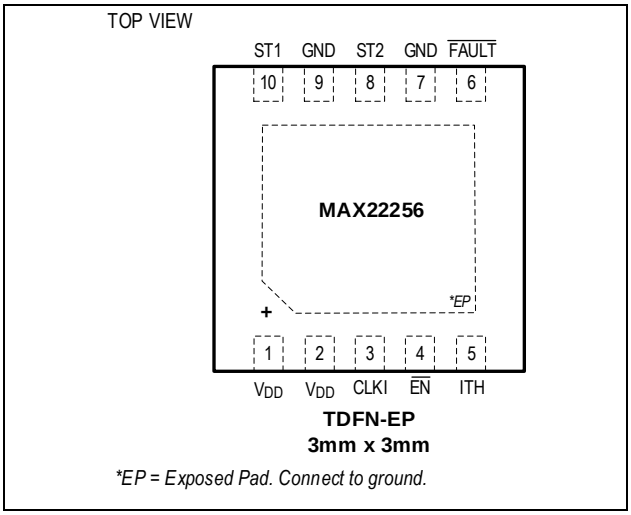
Key Applications

- Isolated Motor Drive Gate Power Supply
  The MAX22256/MAX22258 family provides a simple solution for making isolated power supplies over 15W. These devices drive a transformer's primary coil with up to 650mA$_{RMS}$ of current from a wide 5V to 36V DC supply. The MAX22256B/C are optimized for LLC-type resonant topology, improving efficiency, and reducing switching noise.
- Isolated +24V PLC Field Supply
  The MAX22256/MAX22258 family features a resistor-adjustable current limit that allows indirect limiting of the secondary-side load current and protects the primary power source in the event of secondary- or field-side failure.

Simplified Application Diagram



Pin Description



TDFN-EP
3mm x 3mm

**EP = Exposed Pad. Connect to ground.*

A $\overline{\text{FAULT}}$ output alerts the main controller during an over-temperature or over-current condition. These devices feature a low-power mode to reduce the overall supply current to 0.7mA (typ) when the driver is not in use.

The device can be operated using the accurate internal oscillator or driven by an external clock to synchronize multiple devices and precisely set the switching frequency.

***Ordering Information* appears at end of data sheet.**

19-101440; Rev 1; 3/22

Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to 40V

$\overline{FAULT}$ to GND ..... -0.3V to 40V

ST1, ST2 ..... -0.3V to V_{DD} + 0.3V

CLKI, $\overline{EN}$ to GND ..... -0.3V to 6V

CLKO to GND (MAX22258) ..... -0.3V to 6V

ITH to GND ..... -0.3V to MIN (V_{DD} + 0.3V, 6V)

DTC to GND (MAX22258) ..... -0.3V to MIN (V_{DD} + 0.3V, 5.3V)

$\overline{FAULT}$ Continuous Current 50mA

ST1, ST2 Continuous Current ..... ±1.1A

Continuous Power Dissipation Multilayer Board

T1033+3C (T_A = +70°C, derate 24.4mW/°C above +70°C) 1951.2mW

U14E+3C (T_A = +70°C, derate 25.6mW/°C above +70°C) 2051.3mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10-pin TDFN-EP (3mm x 3mm)

Package Code	T1033+1C
Outline Number	*21-0137*
Land Pattern Number	*90-0003*
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

14-pin TSSOP-EP (4mm x 5mm)

Package Code	U14E+3C
Outline Number	*21-0108*
Land Pattern Number	*90-0119*
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	39°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD517. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 5V to 36V, $\overline{EN}$ = Low, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, T_A = +25°C.) (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage Range	V_{DD}		5		36	V
Supply Current	I_{DD}	V_{DD} = 5V, R_{LIM} = 1.2kΩ, C_L = 500pF, V_{CLKI} = 0V		4.7	8	mA
Shutdown Supply Current	I_{DIS}	$V_{\overline{EN}}$ = high, V_{CLKI} = 0V		0.7	1.12	mA
Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD} rising	4.5	4.65	4.75	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVHYST}			230		mV
DRIVER						
High-Side Driver Output On-Resistance	R_{OH}	ST1 = ST2 = high, $I_{ST1, ST2}$ = +200mA, R_{LIM} = 1.2kΩ		0.52	0.95	Ω
Low-Side Driver Output On-Resistance	R_{OL}	ST1 = ST2 = low, $I_{ST1, ST2}$ = -200mA, R_{LIM} = 1.2kΩ		0.26	0.486	Ω
ST1, ST2 Current Limit	I_{LIM}	R_{LIM} = 1.2kΩ	0.9	1.0	1.1	A
		R_{LIM} = 6.2kΩ	0.18	0.2	0.22	
ST1, ST2 Leakage Current	I_{LKG}	$V_{\overline{EN}}$ = high, V_{CLKI} = 0V, ST1/ST2 is 0V or V_{DD}	-1		+1	µA
LOGIC INTERFACE (CLKI, $\overline{EN}$, CLKO, $\overline{FAULT}$)						
Input High Voltage	V_{IH}	CLKI, $\overline{EN}$	2			V
Input Low Voltage	V_{IL}	CLKI, $\overline{EN}$			0.8	V
Input Hysteresis	V_{HYS}	CLKI, $\overline{EN}$		800		mV
Input Leakage Current	I_{INLKG}	CLKI, $\overline{EN}$	-1		+1	µA
$\overline{FAULT}$ Output Leakage Current	I_{LKG_FAULT}	$\overline{FAULT}$ is not asserted, V_{FAULT} = 36V			10	µA
CLKO Output Leakage Current	I_{LKG_CLKO}	CLKO is high impedance, V_{CLKO} = 5V			1	µA
Output Voltage Low	V_{OL}	CLKO, $\overline{FAULT}$, output is asserted, I_{OL} = 10mA			0.4	V
PROTECTION						
Thermal-Shutdown Threshold	T_{SHDN}			+160		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		°C
SWITCHING CHARACTERISTICS						
ST1, ST2 Switching Frequency	f_{SW}	V_{CLKI} = 0V	423	450	477	kHz
CLKI Input Frequency	f_{EXT}	External clock applied to CLKI, $f_{ST1, ST2}$ = f_{CLKI} / 2	200		2000	kHz
CLKO Output Frequency	f_{CLKO}	(MAX22258 only)	200		2000	kHz
Turn-On Time	t_{ON}	Delay from $\overline{EN}$ to ST1, ST2 switching, $f_{ST1, ST2}$ = 2MHz		51	56	µs
		Delay from $\overline{EN}$ to ST1, ST2 switching, $f_{ST1, ST2}$ = 2kHz		61	67	
ST1/ST2 Duty Cycle	D	Minimum dead time	49	50	51	%

(V_{DD} = 5V to 36V, $\overline{EN}$ = Low, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, T_A = +25°C.) (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ST1/ST2 Rise Time	t_{RISE}	R_L = 1kΩ, C_L = 50pF, *Figure 1* (Note 2)			3	6	ns
ST1/ST2 Fall Time	t_{FALL}	R_L = 1kΩ, C_L = 50pF, *Figure 1* (Note 2)			3	6	ns
Fixed Dead Time	t_{DT_FIX}	*Figure 1*	MAX22256A	27	30	33	ns
			MAX22256B	54	60	66	
			MAX22256C	92	100	108	
Adjustable Dead Time	t_{DT_ADJ}	(MAX22258 only) *Figure 1*	R_{DTC} = 12kΩ	29	35	41	ns
			R_{DTC} = 82kΩ	160	200	240	
Adjustable Dead Time Accuracy		12kΩ ≤ R_{DTC_EXT} ≤ 82kΩ		-20		+20	%
Watchdog Timeout	t_{WDG}			29	32	35	µs
Current Limit Blanking Time	t_{BLANK}	*Figure 2*		2.0	2.4	2.8	ms
Current Limit Autoretry Time	t_{RETRY}	*Figure 2*		68	76	84	ms

Note 1: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design. Not production tested.

Timing Diagrams

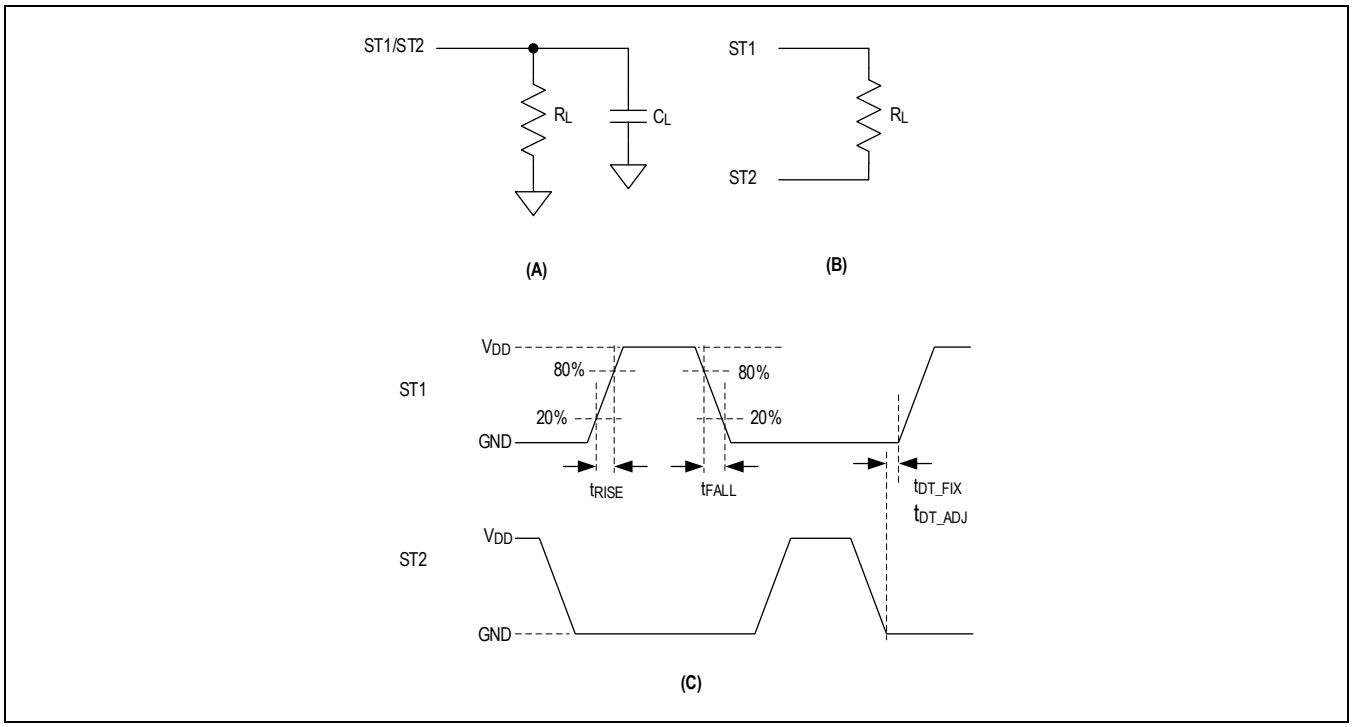


Figure 1. Test Circuits (A and B) and Timing Diagram (C) for Rise, Fall, and Dead Times

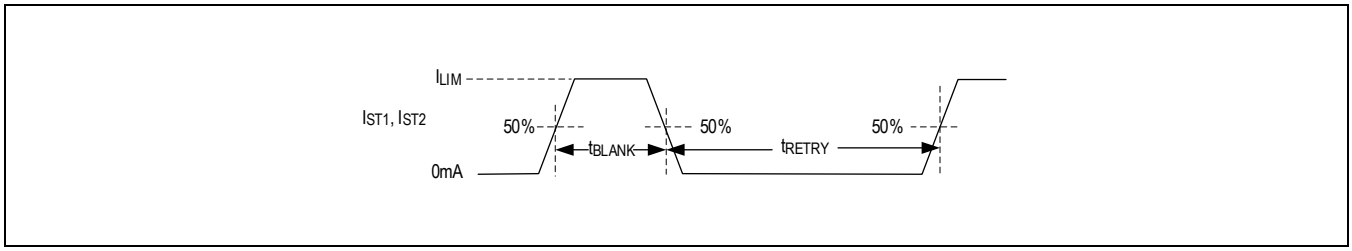
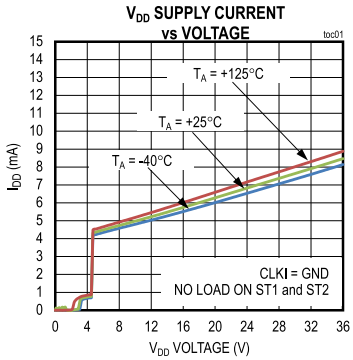
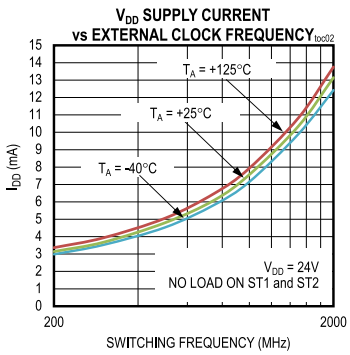


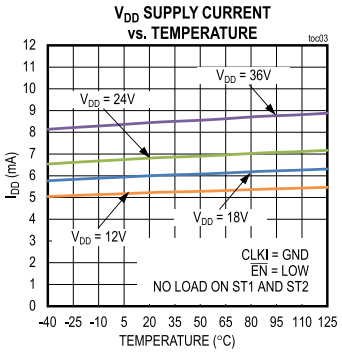
Figure 2. Timing Diagram for Current Limiting

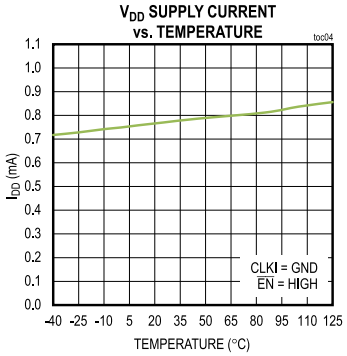
Typical Operating Characteristics

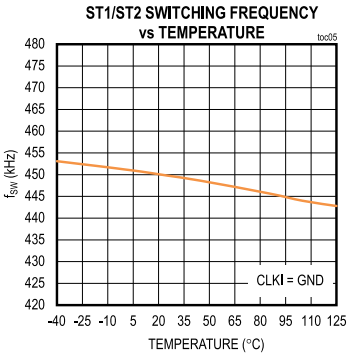
V_{DD} = 24V, CLKI = GND, T_A = +25°C, unless otherwise noted.

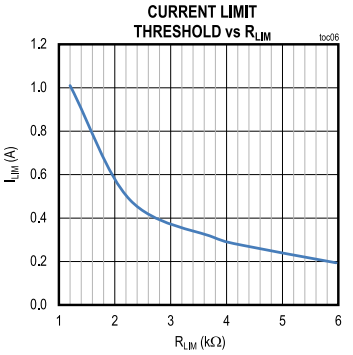


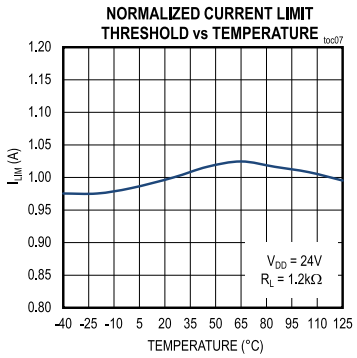


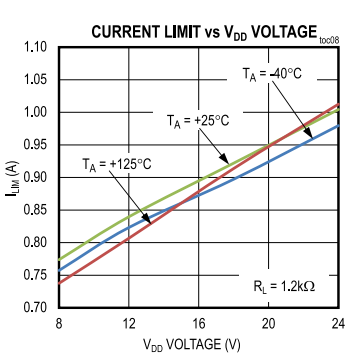


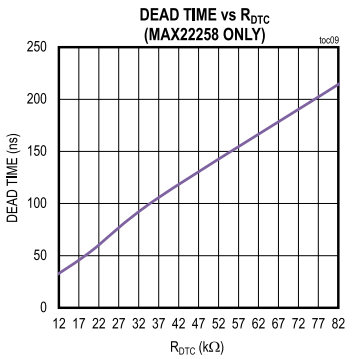




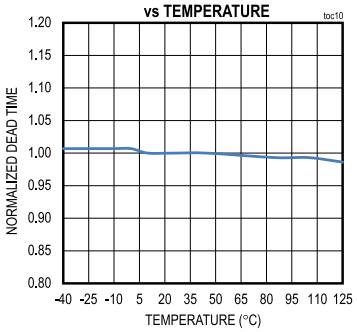




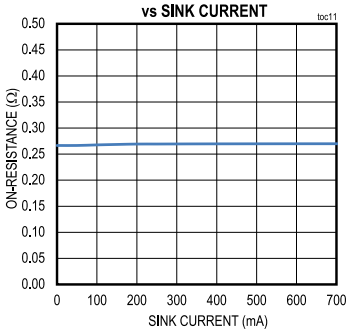




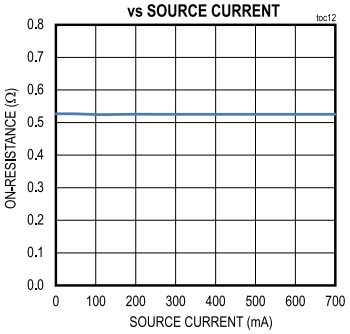
NORMALIZED DEAD TIME vs TEMPERATURE



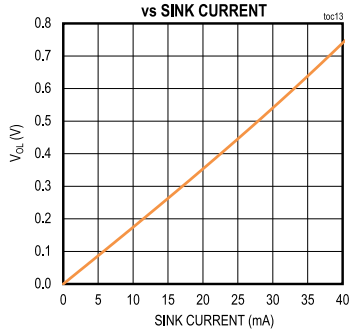
ST1/ST2 LOW-SIDE ON-RESISTANCE vs SINK CURRENT



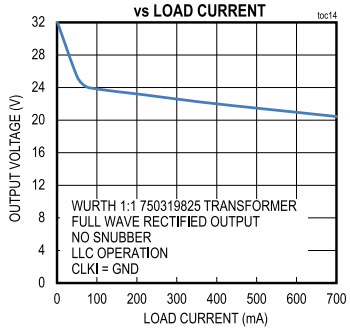
ST1/ST2 HIGH-SIDE ON-RESISTANCE vs SOURCE CURRENT



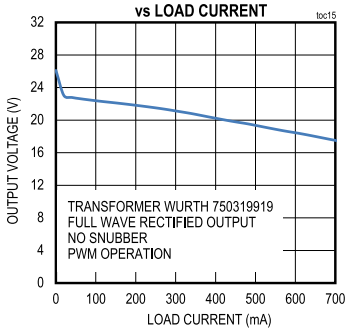
$\overline{FAULT}$ OUTPUT VOLTAGE HIGH vs SINK CURRENT



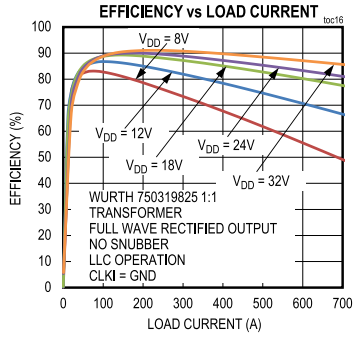
ISOLATED OUTPUT VOLTAGE vs LOAD CURRENT



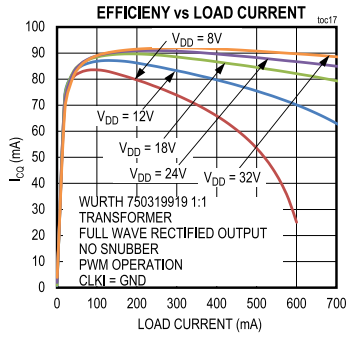
ISOLATED OUTPUT VOLTAGE vs LOAD CURRENT



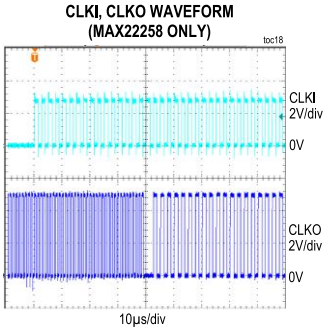
EFFICIENCY vs LOAD CURRENT



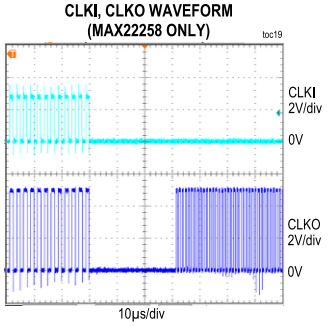
EFFICIENY vs LOAD CURRENT



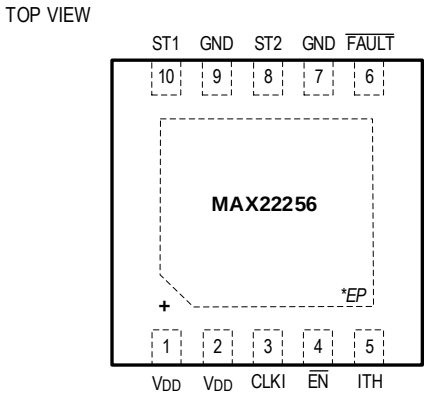
CLKI, CLKO WAVEFORM (MAX22258 ONLY)



CLKI, CLKO WAVEFORM (MAX22258 ONLY)

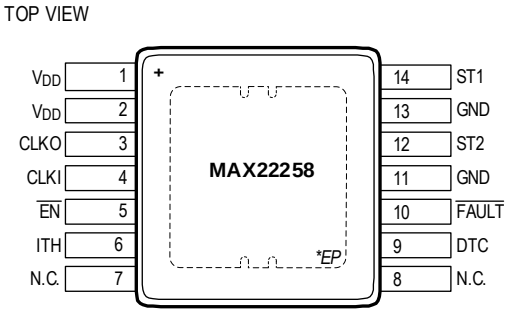


Pin Configurations



TDFN-EP
3mm x 3mm

**EP = Exposed Pad. Connect to ground.*



TSSOP

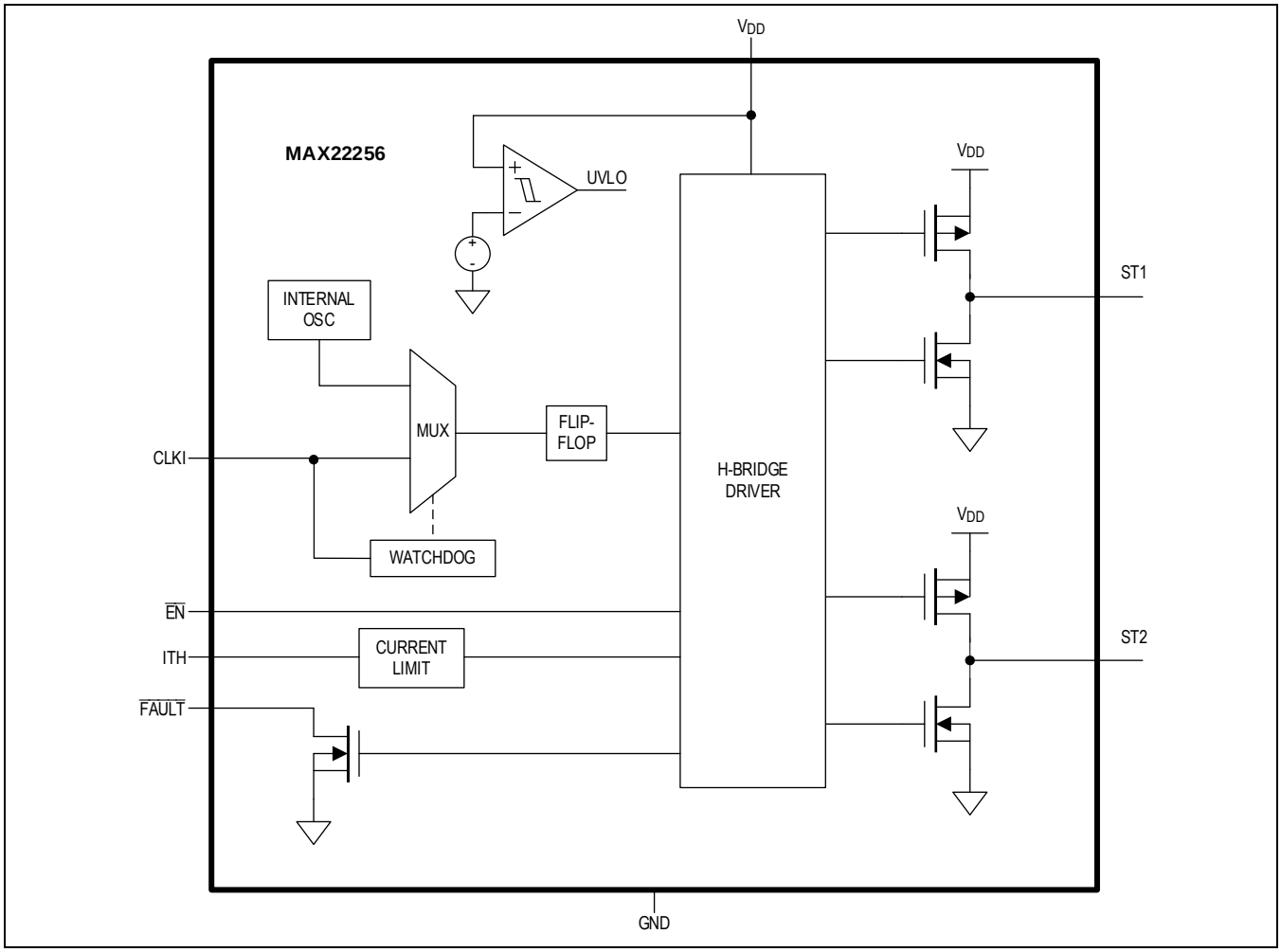
**EP = Exposed Pad*

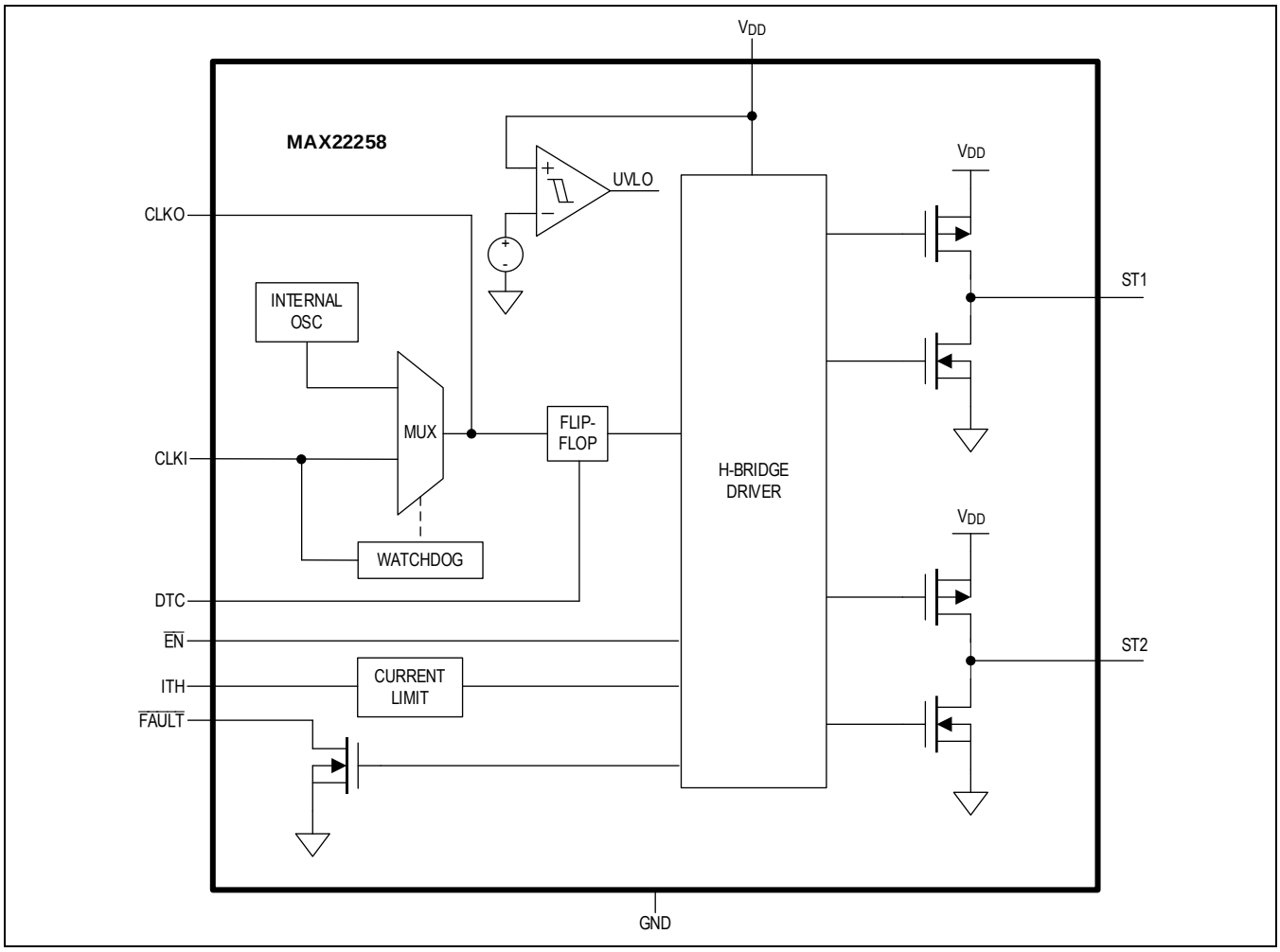
Pin Descriptions

PIN		NAME	FUNCTION
MAX22256	MAX22258		
1, 2	1, 2	V_{DD}	Power Supply Input. Bypass V_{DD} to ground with a 0.1µF capacitor and a 10µF capacitor as close as possible to the device.
–	3	CLKO	Open-Drain Clock Output. Connect CLKO to an external device(s) to provide a synchronous clock.
3	4	CLKI	Clock Input. Connect CLKI to GND to enable internal clocking. Apply a clock signal to CLKI to enable external clocking. See the *Internal Oscillator and External Clock* section for more information.
4	5	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ low to enable the device. Drive $\overline{EN}$ high to disable the device. CLKO on the MAX22258 is not disabled when $\overline{EN}$ is high.
5	6	ITH	Overcurrent Threshold Adjustment. Connect a resistor (R_{LIM}) from ITH to GND to set the overcurrent threshold for the ST1 and ST2 outputs. Do not exceed 10pF of capacitance to GND on ITH. See the *Overcurrent Limiting* section for more information.
6	10	$\overline{FAULT}$	Open-Drain Fault Output. $\overline{FAULT}$ asserts during an overcurrent and/or thermal shutdown event. $\overline{FAULT}$ is high impedance during normal operation.

–	9	DTC	Dead Time Control. Connect a resistor from DTC to GND (R_{DTC}) to set the dead time between ST1 and ST2 during normal operation. See the *Dead Time Control* section for more information.
7, 9	11, 13	GND	Ground
8	12	ST2	Transformer Drive Output 2
10	14	ST1	Transformer Drive Output 1
EP	EP	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. Do not use EP as the main ground connection.
–	7, 8	N.C.	Not Connected. Not internally connected.

Functional Diagrams




VDD
MAX22258
UVLO
CLKO
INTERNAL OSC
MUX
FLIP-FLOP
CLKI
WATCHDOG
DTC
EN
ITH
CURRENT LIMIT
FAULT
H-BRIDGE DRIVER
VDD
ST1
VDD
ST2
GND

Detailed Description

The MAX22256/MAX22258 integrated primary-side controllers and H-bridge drivers for isolated power-supply circuits feature a precision on-board oscillator, protection circuitry, and internal MOSFETs to provide up to 650mA$_{RMS}$ of current to the primary winding of a transformer. These devices feature an internal 450kHz (typ) oscillator and can also be driven by an external clock to synchronize multiple devices and control EMI. An internal flip-flop stage guarantees a fixed 50% duty-cycle to prevent DC current flow in the transformer as long as the clock period is constant.

The MAX22256/MAX22258 operate from a wide single-supply voltage range from 5V to 36V and include undervoltage lockout for controlled startup. Break-before-make switching is integrated to prevent cross-conduction of the H-bridge MOSFETs. A resistor-adjustable overcurrent limit allows primary-side limiting of load currents on the transformer's secondary side and thermal shutdown circuitry provides additional protection against excessive power dissipation.

The MAX22256A features a 30ns (typ) dead time for conventional H-bridge switching topologies. The MAX22256B/C feature a fixed dead time of 60ns (typ) and 100ns (typ), respectively, and are optimized for the zero-voltage switching of an LLC topology. The MAX22258 features a resistor-programmable dead time and a synchronized clock output (CLKO).

Isolated Power Supply

The MAX22256/MAX22258 allow a versatile range of secondary side rectification circuits. Select the primary-to-secondary transformer winding ratio to adjust the isolated output voltage. The MAX22256/MAX22258 drive the primary side of the transformer with up to 650mA$_{RMS}$ of current with a supply up to +36V.

Power-Up and Undervoltage Lockout

The MAX22256/MAX22258 feature a 4.65V (typ) undervoltage lockout threshold to ensure a controlled state during power-up and to prevent operation before the oscillator has stabilized. During power-up and normal operation, if the V_{DD} supply voltage drops below $V_{UVLO,}$ the undervoltage-lockout protection forces the device into disable mode. ST1 and ST2 are high impedance in disable mode.

Low-Power Disable Mode

Drive the $\overline{EN}$ input high to put the MAX22256/MAX22258 into low-power disabled mode. ST1 and ST2 are high impedance when $\overline{EN}$ is high. CLKO on the MAX22258 is not disabled when $\overline{EN}$ is high.

Drive $\overline{EN}$ low for normal operation.

Dead Time Control

The MAX22256 features a fixed precision dead time. The MAX22256A features a 30ns (typ) dead time for conventional H-bridge switching topologies. The MAX22256B and MAX22256C feature a fixed dead time (t_{DEAD_FIX}) of 60ns (typ) and 100ns (typ), respectively, and are optimized for the zero-voltage switching of an LLC topology.

The MAX22258 features a resistor-adjustable dead time (t_{DEAD}). Connect a resistor between the DTC pin and GND (R_{DTC}) to set the dead time. Calculate the DTC resistance for as:

$$R_{DTC}\ (k\Omega) = (1.2 \times t_{DEAD}) \times (333 \times 10^{9})$$

Transients on ST1/ST2 During the Dead Time

During the dead time, the voltage at the ST1 and ST2 pins may temporarily exceed the Absolute Maximum Ratings due to the inductive load presented by the transformer. This transient voltage will not damage the device.

Internal Oscillator and External Clock

The MAX22256/MAX22258 feature an internal oscillator that drives the H-bridge when the CLKI is low for the 32µs (typ) watchdog timeout. When the internal oscillator is enabled, the ST1 and ST2 outputs switch at 450kHz (typ).

To use the device with a switching frequency other than 450kHz (typ), connect an external clock source to CLKI. The MAX22256/MAX22258 switch on the rising edge of the external clock signal and an internal flip-flop divides the external clock by two to generate a switching signal with a 50% duty cycle. As a result, the ST1 and ST2 outputs switch at one-half the frequency of the clock signal at CLKI.

The MAX22258 also includes an open-drain clock output (CLKO) that can be used to synchronize multiple devices. CLKO switches at the 450kHz (typ) switching frequency when CLKI is low, or at the frequency of the external clock frequency applied to CLKI.

Watchdog

A stalled clock can cause excessive DC current to flow through the primary winding of the transformer when ST1 and ST2 stop switching. The MAX22256/MAX22258 feature an internal watchdog circuit to prevent damage from this condition. When the CLKI input stops switching for the 32µs (typ) watchdog timeout, the device uses the internal oscillator to switch ST1 and ST2. ST1 and ST2 switch at 450kHz (typ) when CLKI is low.

Overcurrent Limiting

The MAX22256/MAX22258 limit the ST1/ST2 output current up to 1A. Connect an external resistor (R_{LIM}) between the ITH pin and GND to set the current limit. Use the following equation to calculate the R_{LIM} resistance for the desired current limit:

$$R_{LIM}(k\Omega) = \frac{1.2 \times 10^3}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current threshold in the range of 200mA ≤ I_{LIM} ≤ 1000mA (typ). Use a 1% resistor for R_{LIM} for increased accuracy. Ensure that the overcurrent threshold set by R_{LIM} is at least 40% higher than the expected maximum operating current.

When the load current exceeds the limit for longer than the 2.4ms (typ) blanking time, the ST1 and ST2 driver outputs are disabled and $\overline{FAULT}$ asserts. ST1 and ST2 are reenabled (and $\overline{FAULT}$ deasserts) after the 76ms (typ) autoretry time. If the overcurrent condition has been removed, ST1 and ST2, and $\overline{FAULT}$ operate normally. If the overcurrent condition persists, however, the driver outputs are re-disabled and $\overline{FAULT}$ reasserts. This autoretry cycle continues until the load current is reduced. The duty cycle of the load current and $\overline{FAULT}$ output is approximately 3% when a continuous fault condition is present.

$\overline{FAULT}$ Output

The open-drain $\overline{FAULT}$ output asserts when an overcurrent event is detected on the MAX22256/MAX22258 and/or when the device is in thermal shutdown.

When the load current exceeds the set overcurrent limit threshold, the ST1 and ST2 driver outputs are disabled and $\overline{FAULT}$ is asserted. $\overline{FAULT}$ deasserts when the ST1 and ST2 driver outputs are reenabled after the autoretry delay, but is then reasserted, as the driver outputs are re-disabled, if the overcurrent condition has not been removed. As a result, $\overline{FAULT}$ may toggle during a continuous overcurrent condition.

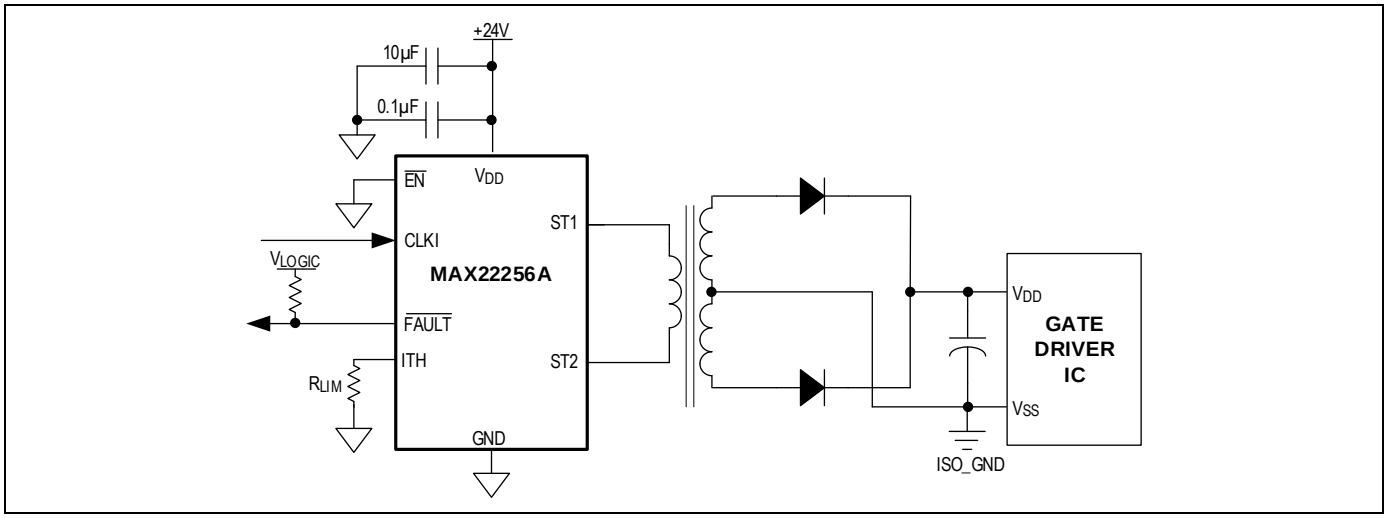
$\overline{FAULT}$ is continuously asserted for the entire duration of an overtemperature/thermal shutdown event.

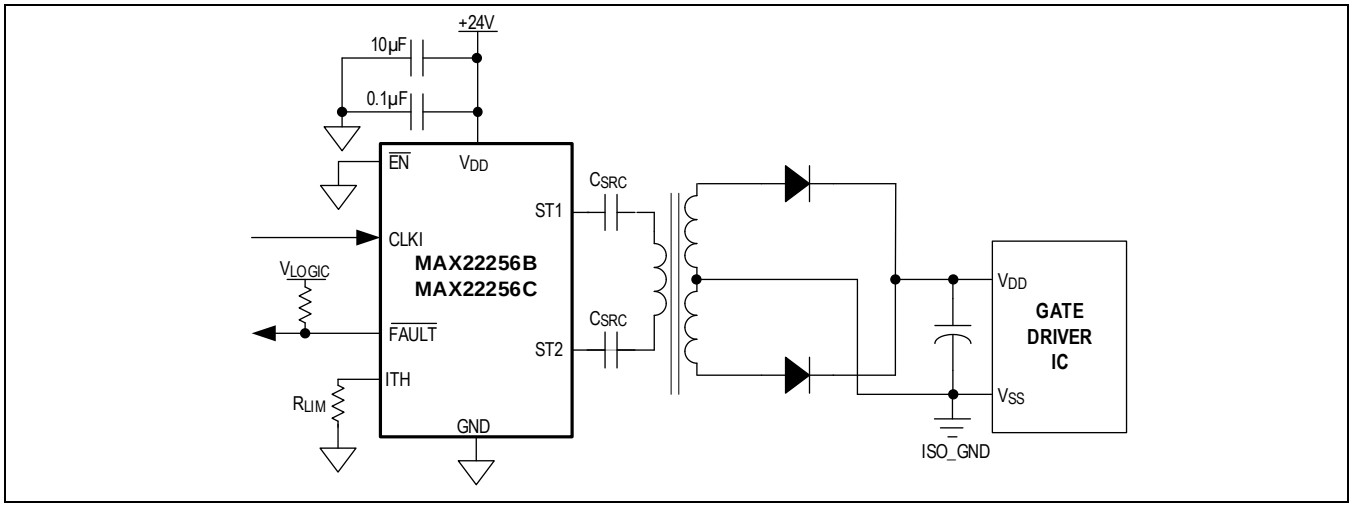
Thermal Shutdown

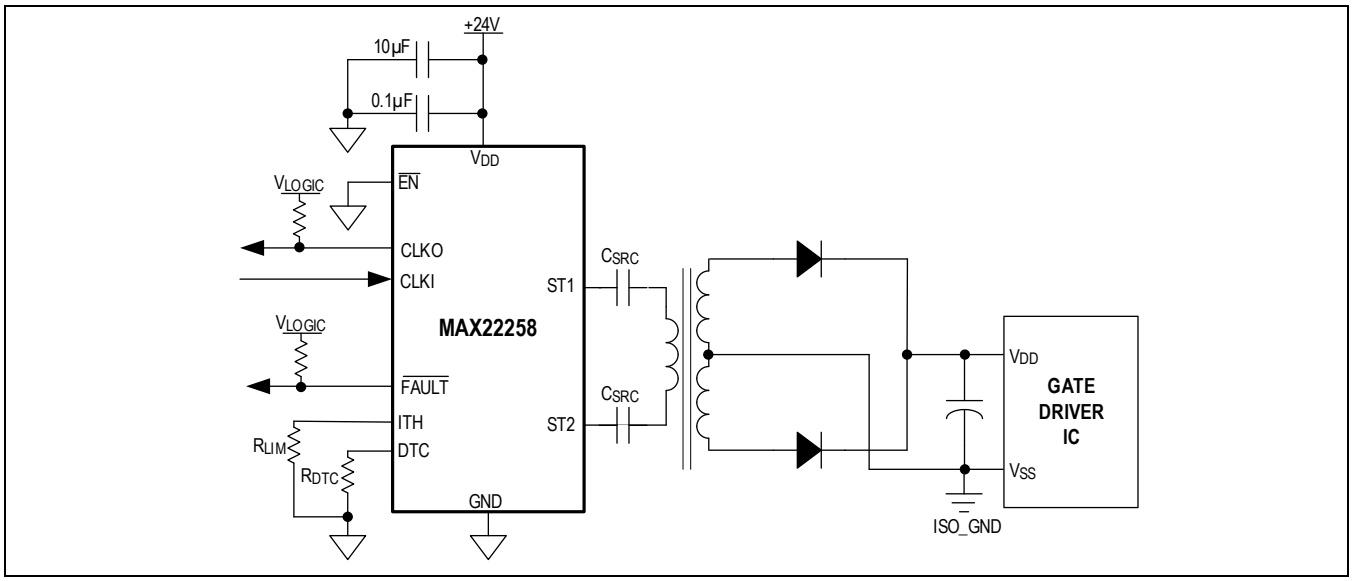
The MAX22256/MAX22258 are protected from thermal damage with an integrated thermal-shutdown circuit. When the junction temperature of the devices exceeds the +160°C (typ) thermal shutdown threshold, ST1 and ST2 are disabled and $\overline{FAULT}$ asserts. CLKO on the MAX22258 is not disabled during an thermal shutdown.

The driver outputs are reenabled and $\overline{FAULT}$ deasserts when the junction temperature falls the 10°C (typ) thermal shutdown hysteresis.

Typical Application Circuits







Ordering Information

PART NUMBER	DEAD TIME (ns)	CLOCK OUTPUT	ADJUSTABLE DEAD TIME	TEMP RANGE	PIN-PACKAGE
MAX22256AATB+	30	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22256AATB+T	30	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22256BATB+*	60	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22256BATB+T*	60	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22256CATB+*	100	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22256CATB+T*	100	NO	NO	-40°C to +125°C	10 TDFN-EP
MAX22258AUD+	ADJ	YES	YES	-40°C to +125°C	14 TSSOP-EP
MAX22258AUD+T	ADJ	YES	YES	-40°C to +125°C	14 TSSOP-EP

+Denotes a lead(Pb)-free/RoHS-compliant package.

EP = Exposed pad

**Future Product—contact factory for availability*

Chip Information

PROCESS: BiCMOS