Click here for production status of specific part numbers.

MAX22513

Surge Protected Dual Driver IO-Link Device Transceiver with DC-DC

General Description

The MAX22513 dual-channel low power IO-Link device transceiver features a selectable control interface, internal high-efficiency DC-DC buck regulator, two internal linear regulators, and integrated surge protection for robust communication. The device features low-on resistance drivers (C/Q and DO/DI), selectable driver current limits, and overcurrent protection to reduce power dissipation in small sensor applications.

The DC-DC buck regulator supplies up to 300mA load current and has an adjustable output voltage (from 2.5V to 12V). Internal linear regulators generate 5V and 3.3V, supplying up to 50mA of current.

The MAX22513 can be controlled using SPI or I^2C interfaces, providing flexibility for microcontrollers, and extensive control and diagnostic features. Both full- and half-duplex SPI are supported. The internal MCLK oscillator provides a clock source to a microcontroller for IO-Link communication.

The MAX22513 features extensive integrated protection to ensure robust communication in harsh industrial environments. All four IO pins (V_{24}, C/Q, DO/DI, and GND), are reverse voltage protected, short circuit protected, and feature integrated ±1kV/500Ω surge protection.

The MAX22513 is available in a tiny WLP package (4.1mm x 2.1mm) or 28-pin TQFN-EP package (3.5mm x 5.5mm) and operates over the -40°C to +125°C temperature range.

Applications

- IO-Link Sensor and Actuator Devices
- Industrial Sensors

Benefits and Features

- High Configurability and Integration Reduces SKU
  - Configurable C/Q and DO/DI Drivers
    - PNP, NPN, and Push-Pull Modes
    - Individual Slew Rate Control for Drivers
    - Selectable Driver Current Limit: 50mA to 250mA
  - Control and Monitoring with I^2C or SPI
    - Half- and Full-Duplex SPI Modes
  - Integrated High-Efficiency DC-DC Buck Regulator
    - Selectable Switching Frequency
      - 921kHz (typ) or 1.229MHz (typ)
    - 300mA (max) Load
    - Output Voltage from 2.5V to 12V
  - Internal 5V and 3.3V Linear Regulators
  - Accurate Oscillator for IO-Link Communication
- Integrated Protection Enables Robust Systems
  - Integrated ±1kV/500Ω Surge Protection
  - Glitch Filters for Improved Burst Resilience
  - Selectable Overcurrent Configuration
  - Hot-Plug and Reverse Polarity Protection
  - -40°C to +125°C Operating Temperature Range
- Optimized for Small Sensor Designs
  - Low Power Dissipation:
    - 2Ω (typ) On-Resistance for C/Q and DO/DI Drivers
  - Available in Two Tiny Packages:
    - 28-Pin TQFN-EP (3.5mm x 5.5mm)
    - WLP (4.1mm x 2.1mm)

***Ordering Information* appears at end of data sheet.**

19-100455; Rev 4; 7/19

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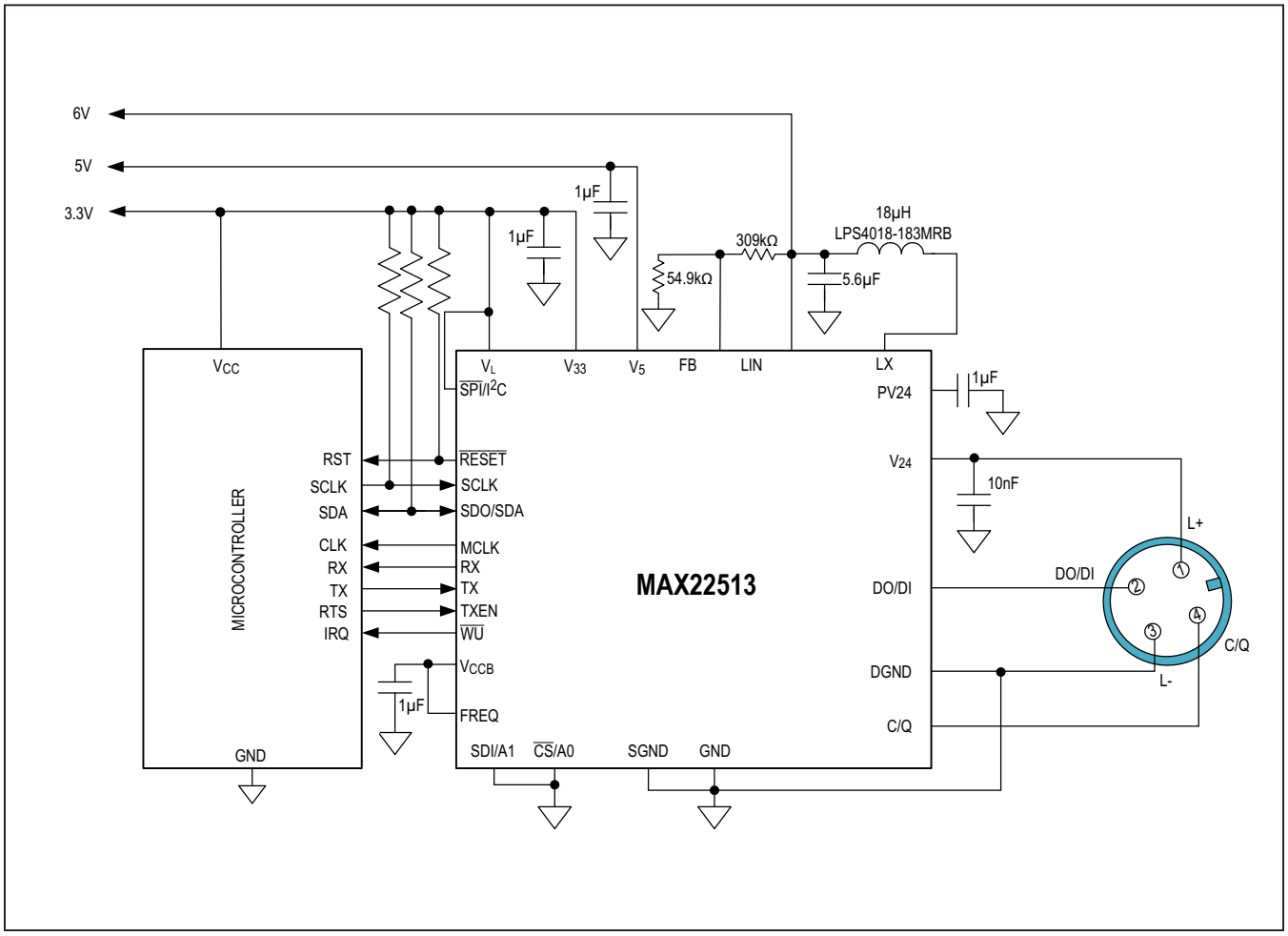
I²C Interface Application Circuit



Absolute Maximum Ratings

(All voltages referenced to GND unless otherwise noted.)
V_{24} (Continuous) ..... -36V to +36V
V_{24} (Peak, 100µs) ..... -52V to +65V
PV24 (Continuous) (Note 1) ..... max(-0.3V, V_{24} - 3V) to +36V
PV24 (Peak, 100µs) ..... max(-0.3V, V_{24} - 52V) to min(+52V, V_{24} + 52V)
LX ..... -0.3V to (PV24 + 0.3V)
LIN (Continuous) ..... max(-0.3V, V_5 - 0.3V) to +36V
LIN (Peak, 100µs) ..... max(-0.3V, V_5 - 0.3V) to +52V
C/Q, DO/DI (Continuous) ..... max(-36V, V_{24} - 36V) to min(+36V, V_{24} + 36V)
C/Q, DO/DI (Peak, 100µs) ..... max(-52V, V_{24} - 52V) to min(+52V, V_{24} + 52V)
V_5, FB, V_{CCB}, $\overline{RESET}$, FREQ ..... -0.3V to +6V
V_L ..... -0.3V to +6V
V_{33} ..... -0.3V to (V_5 + 0.3V)
LOGIC INPUTS .....
$\overline{SPI}$/I²C, $\overline{CS}$/A0, SCLK, SDI/A1, SDO/SDA, TX, TXEN, LO/LI ..... -0.3V to (V_L + 0.3V)
LOGIC OUTPUTS
$\overline{WU}$, SDO/SDA, RX, LO/LI, MCLK ..... -0.3V to (V_L + 0.3V)
$\overline{IRQ}$ ..... -0.3V to +6V
DGND, SGND ..... -0.3V to +0.3V
Continuous Current into V_{24}, LX, GND, or DGND ..... ±1A
Continuous Current into PV24 ..... ±300mA
Peak Current into PV24 (100µs) ..... ±1A
Continuous Current into C/Q and DO/DI ..... ±500mA
Continuous Current into Any Other Pin ..... ±50mA
Continuous Power Dissipation (28-pin TQFN) (T_A = +70°C (derate at 28.6mW/°C above +70°C)) 2280mW
Continuous Power Dissipation (30-bump WLP) (T_A = +70°C (derate at 20.76mW/°C above +70°C)) 3850mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +165°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) (TQFN only, soldering, 10 sec) ..... +300°C
Bump Reflow Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: During power-up, (V_{24} - PV24) voltage can be up to +52V until the internal active diode turns on.

Package Information

PACKAGE TYPE: 28 TQFN	
Package Code	T283555+1C
Outline Number	**21-0184**
Land Pattern Number	**90-0123**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	2.7°C/W

PACKAGE TYPE: 8 x 4 WLP	
Package Code	W322A4+1
Outline Number	**21-100247**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	48.16°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS / POWER SUPPLY							
V_{24} Supply Voltage	V_{24}			8		36	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising		7.0	7.6	8	V
		V_{24} falling		6.6	7.0	7.5	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}				550		mV
V_{24} Low Voltage Warning Threshold	V_{24_W}	V_{24} falling		14.5	16	18	V
V_{24} Supply Current	I_{24}	No load on C/Q or DO/DI, V_5 powered externally, DC-DC disabled, MCLK disabled	C/Q and DO/DI disabled		0.042	0.075	mA
			C/Q and DO/DI are in push-pull and are high or low		0.46	0.65	
		DC-DC enabled, MCLK enabled, C/Q and DO/DI in push-pull and are high or low (see *Typical Application Circuits*)			3.75		
V_5 Supply Voltage	V_5	V_5 supplied externally		4.5		5.5	V
V_5 Undervoltage Lockout Threshold	V_{5UVLOR}	V_5 rising		4.0		4.25	V
	V_{5UVLOF}	V_5 falling		3.95		4.25	
V_5 Supply Current	I_5	No load on C/Q or DO/DI, V_5 powered externally, DC-DC disabled, MCLK disabled, V_{33} enabled, no load on V_{33}	C/Q and DO/DI disabled		0.91	1.2	mA
			C/Q and DO/DI in push-pull mode, no load on C/Q, DO/DI		1.89	2.4	
V_L Logic Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}			0.5	0.84	1.2	V
V_L Logic Level Supply Current	I_L	All logic inputs at GND or V_L, no load on any logic outputs, MCLK disabled			15	30	µA

DC Electrical Characteristics (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS / DC-DC SWITCHING REGULATOR							
Input Voltage Range	V_{24_DC}	V_{24} is the input to the DC-DC		8		36	V
DC-DC Turn-on Delay	t_{DC_ON}	Delay from V_{24} crossing V_{24UVLO} threshold until the DC-DC regulator finishes soft-start			2.22		ms
Switching Frequency	f_{DC_H}	FREQ = high	BUCKSS = 0	1.198	1.223	1.260	MHz
	f_{DC_HSPRD}		BUCKSS = 1		1.229		
	f_{DC_L}	FREQ = low	BUCKSS = 0	898.6	921.6	944.6	kHz
	f_{DC_LSPRD}		BUCKSS = 1		921.6		
Spread Spectrum	Δf_{DC_SPRD}	FREQ = high, BUCKSS = 1			7		%
Feedback (FB) Regulation Voltage	V_{DC_FB}				0.9		V
Output Voltage Accuracy	ACC_{DCFB}			-1	0	+1	%
Feedback (FB) OK Threshold	V_{DC_FBOK}	FB rising		91.5	95.3	99.4	$\%V_{DC\_FB}$
Feedback (FB) Low Threshold	$V_{DC\_FBTHLOW}$			61	64	72	$\%V_{DC\_FB}$
LX On-Resistance (High Side)	R_{DC_HS}	From V_{24} to LX, LX is sinking current (Note 3)			1.4	2.6	Ω
LX On-Resistance (Low Side)	R_{DC_LS}	From LX to GND (Note 3)			0.85	1.7	Ω
Active Diode On-Resistance	R_{DC_ACT}	DC current (Note 3)			5.1	10	Ω
Peak Current into Active Diode	I_{DC_ACTMAX}	(Note 3)				200	mA
Maximum LX Current Ripple	ΔI_{DC_LX}				100		%
High-Side Peak Current Limit	$I_{DC\_HS(LIM)}$			650	750	860	mA
Low-Side Current Limit	$I_{DC\_LS(MAX)}$			-375	-300	-240	mA
DC-DC Autoretry Period	$T_{DCRETRY}$				22		ms
External Capacitance on PV24	C_{DC_PV24}			1			µF
DC CHARACTERISTICS / 5V LINEAR REGULATOR (V_5)							
V_5 Input Supply Voltage	V_{LIN}			6		36	V
V_5 Output Voltage	V_5	6V ≤ V_{LIN} ≤ 36V, no load on V_5		4.75	4.92	5.25	V
V_5 Load Regulation	ΔV_{5LDR}	V_{LIN} = 24V, 1mA < I_{LOAD} < 50mA			0.8	2	%
V_5 Line Regulation	ΔV_{5LNR}	6V ≤ V_{LIN} ≤ 36V, I_{LOAD} = 1mA			0.03	0.15	mV/V
V_5 Load Capacitance	C_{V5}	External capacitance on V_5		1			µF
DC CHARACTERISTICS / 3.3V LINEAR REGULATOR (V_{33})							
V_{33} Output Voltage	V_{33}	No load		3.1	3.17	3.3	V
V_{33} Load Regulation	ΔV_{33_LR}	1mA < I_{LOAD} < 30mA		0	0.35	1	%
V_{33} Load Capacitance	C_{V33}	External capacitance on V_{33}		1			µF

DC Electrical Characteristics (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS / C/Q, DO/DI DRIVER							
C/Q, DO/DI Driver High-Side On-Resistance	R_{CQOH}, R_{DOOH}	High-side enabled, CL[1:0] = 11, I_{LOAD} = +200mA (Note 3)			2.25	4.2	Ω
C/Q, DO/DI Driver Low-Side On-Resistance	R_{DOOL}, R_{DOOL}	Low-side enabled, CL[1:0] = 11, I_{LOAD} = -200mA (Note 3)			2.07	4.1	Ω
C/Q, DO/DI Driver Current Limit	I_{CQCL}, I_{DOCL}	V_{DROP} = 3V (Note 4)	CL[1:0] = 00	50	67	82	mA
			CL[1:0] = 01	100	120	140	
			CL[1:0] = 10	200	240	280	
			CL[1:0] = 11	250	300	350	
C/Q Leakage Current	I_{LEAK_CQ}	V_{24} = 24V, (V_{24} – 36V) ≤ $V_{C/Q}$ ≤ 36V, C/Q driver and C/Q receiver disabled		-40		+30	µA
DO/DI Leakage Current	I_{LEAK_DO}	V_{24} = 24V, (V_{24} – 36V) ≤ $V_{DO/DI}$ ≤ 36V, DO/DI driver disabled		-30		+17	µA
C/Q Output Reverse Current	I_{REV_CQ}	C/Q driver enabled and in push-pull, $V_{C/Q}$ = (V_{24}+ 5V) or (V_{GND} - 5V)		-100		+300	µA
DO/DI Output Reverse Current	$I_{REV\_DO/DI}$	DO/DI driver enabled and in push-pull, $V_{DO/DI}$ = (V_{24} + 5V) or (V_{GND} - 5V)		-100		+300	µA
C/Q, DO/DI Weak Pull-Down Current	I_{CQPD}, I_{DOPD}	Driver disabled, $V_{C/Q}$ = $V_{DO/DI}$ > 5V, CQ_PD = 1, CQ_PU = 0, DO_PD = 1, DO_PU = 0		-400	-300	-230	µA
C/Q, DO/DI Weak Pull-Up Current	I_{CQPU}, I_{DOPU}	Driver disabled, $V_{C/Q}$ = V_{DO} = (V_{24} - 5V), CQ_PD = 0, CQ_PU = 1, DO_PD = 0, DO_PU = 1		+230	+300	+400	µA
DC CHARACTERISTICS / C/Q, DO/DI RECEIVER							
C/Q, DO/DI Input Voltage Range	V_{CQIN}, V_{DIIN}	For valid RX/LI logic		V_{24} - 36V		36	V
C/Q, DO/DI Input Threshold High	V_{CQTH}, V_{DITH}	Driver disabled	V_{24} ≥ 18V	10.75		12.5	V
			V_{24} < 18V	53.1		84.4	%V_{24}
C/Q, DO/DI Input Threshold Low	V_{CQTL}, V_{DITL}	Driver disabled	V_{24} ≥ 18V	9		10.5	V
			V_{24} < 18V	43.75		72	%V_{24}
C/Q, DO/DI Input Hysteresis	V_{CQHYS}, V_{DIHYS}	Driver disabled	V_{24} ≥ 18V	1.45	1.9	2.15	V
			V_{24} < 18V	6.25	11.4	15.6	%V_{24}
C/Q Input Capacitance	C_{IN_CQ}	Driver disabled, CQ_PD = 0, CQ_PU = 0, f = 100kHz			35		pF
DO/DI Input Capacitance	C_{IN_DI}	Driver disabled, DO_PD = 0, DO_PU = 0, f = 100kHz			35		pF

DC Electrical Characteristics (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS / AUXILIARY INPUTS ($\overline{RESET}$, FREQ)						
$\overline{RESET}$Input Voltage Low	V_{RSTIL}				3.05	V
$\overline{RESET}$Input Voltage High	V_{RSTIH}		0.8			V
FREQ Input Voltage Low	V_{FREQIL}				3.05	V
FREQ Input Voltage High	V_{FREQIH}		0.8			V
$\overline{RESET}$Output Voltage Low	V_{POKLOW}	I_{LOAD} = 5mA			0.2	V
DC CHARACTERISTICS / LOGIC INPUTS ($\overline{SPI}$/I²C, $\overline{CS}$/A0, SCLK, SDI/A1, SDO/SDA, TX, TXEN, LO/LI)						
Logic Input Voltage Low	V_{IL}				0.2 x V_L	V
Logic Input Voltage High	V_{IH}		0.8 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
DC CHARACTERISTICS / LOGIC OUTPUTS ($\overline{WU}$, $\overline{IRQ}$, SDO/SDA, RX, LO/LI, MCLK)						
Logic Output Voltage Low	V_{OL}	$\overline{WU}$, SDO/SDA, RX, LO/LI, MCLK, I_{LOAD} = -5mA			0.2	V
Logic Output Voltage High	V_{OH}	$\overline{WU}$, SDO/SDA, RX, LO/LI, MCLK, I_{LOAD} = +5mA	V_L - 0.3V			V
$\overline{IRQ}$Open-Drain High Impedance Leakage Current	I_{LK_OD}	$\overline{IRQ}$not asserted	-1		+1	µA
SDO/SDA Leakage Current	I_{LK_SDO}	$\overline{SPI}$/I²C = low, $\overline{CS}$/A0 = high	-1		+1	µA
RX, LO/LI Leakage Current	I_{LK_RXLI}	RX = LO/LI = GND or V_L,DO_EN = 1	-1		+1	µA
DC CHARACTERISTICS / THERMAL CHARACTERISTICS						
C/Q or DO/DI Per-Driver Shutdown Temperature	T_{SHUT_DRV}	Driver temperature rising, C/Q or DO/DI driver fault bit is set and driver is disabled		+150		°C
C/Q or DO/DI Per-Driver Shutdown Hysteresis	T_{SHUT_DHYS}	Driver temperature falling, driver is automatically reenabled		8		°C
IC Thermal Warning Threshold	T_{WRN}	Die temperature rising, THERMW and THERMWINT bits are set		+147		°C
IC Thermal Warning Threshold Hysteresis	T_{WRN_HYS}	Die temperature falling, THERMW bit is cleared		9		°C
IC Thermal Shutdown Threshold	T_{SHUT_IC}	Die temperature rising		+170		°C
IC Thermal Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature		17		°C

AC Electrical Characteristics

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / C/Q, DO/DI DRIVER							
Driver Low-to-High Propagation Delay	t_{PDLH_PP}	CQLOSLEW[1:0] or DOLOSLEW[1:0] = 00, Figure 1	Push-pull or PNP mode		0.74	1	µs
	t_{PDLH_OC}		NPN mode		1		
Driver High-to-Low Propagation Delay	t_{PDHL_PP}	CQLOSLEW[1:0] or DOLOSLEW[1:0] = 00, Figure 1	Push-pull or NPN mode		0.99	1.4	µs
	t_{PDHL_OC}		PNP mode		1		
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, CQLOSLEW[1:0] or DOLOSLEW[1:0] = 00		-0.575		+0.1	µs
Driver Rise Time	t_{RISE}	Push-pull or PNP mode, V_{24}(max) = 30V, Figure 1	CQLOSLEW[1:0] or DOLOSLEW[1:0] = 00	0.1	0.2	0.325	µs
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 01		0.40		
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 10		1.22		
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 11		4.7		
Driver Fall Time	t_{FALL}	Push-pull or NPN mode, V_{24}(max) = 30V, Figure 1	CQLOSLEW[1:0] or DOLOSLEW[1:0] = 00	0.2	0.34	0.475	µs
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 01		0.66		
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 10		1.64		
			CQLOSLEW[1:0] or DOLOSLEW[1:0] = 11		7.1		
C/Q Driver Enable Time High	t_{ENH}	Push-pull or PNP mode, Figure 2			0.74	1.1	µs
C/Q Driver Enable Time Low	t_{ENL}	Push-pull or NPN mode, Figure 3			0.3	0.45	µs
C/Q Driver Disable Time High	t_{DISH}	Push-pull or PNP mode, Figure 2			1.8		µs
C/Q Driver Disable Time Low	t_{DISL}	Push-pull or NPN mode, Figure 3			1.8		µs

AC Electrical Characteristics (continued)

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / C/Q, DO/DI RECEIVER							
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH_CQ}	Figure 4	RXFILTER = 1	0.75	1.2	1.7	µs
			RXFILTER = 0	0.2	0.33	0.475	
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL_CQ}	Figure 4	RXFILTER = 1	0.7	1.13	1.65	µs
			RXFILTER = 0	0.125	0.25	0.375	
DO/DI Receiver Low-to-High Propagation Delay	t_{PRLH_DI}	Figure 4	DIFILTER = 1	1.3	2.1	2.9	µs
			DIFILTER = 0	0.7	1.2	1.65	
DO/DI Receiver High-to-Low Propagation Delay	t_{PRHL_DI}	Figure 4	DIFILTER = 1	1.1	1.8	2.55	µs
			DIFILTER = 0	0.55	0.91	1.3	
AC ELECTRICAL CHARACTERISTICS / WAKE-UP DETECTION (Figure 5)							
Wake-Up Input Minimum Pulse Width	t_{WUMIN}	C/Q load capacitance = 3nF		59.4	66	72.6	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}			85.5	95	104.5	µs
$\overline{WU}$ Output Low Time	t_{WUL}	Valid wake-up condition on C/Q		180	200	220	µs
AC ELECTRICAL CHARACTERISTICS / MCLK CLOCK							
MCLK Frequency	f_{MCLK}	CLKDIV[1:0] = 00		3.594	3.686	3.779	MHz
		CLKDIV[1:0] = 01		7.188	7.373	7.557	
		CLKDIV[1:0] = 10		14.377	14.746	15.114	
		CLKDIV[1:0] = 11		1.797	1.843	1.889	
AC ELECTRICAL CHARACTERISTICS / SPI TIMING ($\overline{CS}$/A0, SCLK, SDI/A1, SDO/SDA) (Figure 6)							
Maximum SCLK Frequency	f_{SPI_MAX}	Read/write				12	MHz
SCLK Clock Period	t_{CH+CL}	Read/write		80			ns
SCLK Pulse Width High	t_{CH}	Write only		20			ns
SCLK Pulse Width Low	t_{CL}	Write only		20			ns
$\overline{CS}$/A0 Fall to SCLK Rise Time	t_{CSS}			10			ns
SCLK Rise to $\overline{CS}$/A0 Rise Hold Time	t_{CSH}			10			ns
SDI/A1 Hold Time	t_{DH}			5			ns
SDI/A1 Setup Time	t_{DS}			5			ns
SDO/SDA Output Data Propagation Delay	t_{DO}					32	ns
SDO/SDA Rise and Fall Times	t_{FT}				1.5		ns
Minimum $\overline{CS}$/A0 Pulse	t_{CSW}				5		ns

AC Electrical Characteristics (continued)

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{DGND} = V_{SGND} = V_{GND} = 0V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / I²C COMPATIBLE TIMING SPECIFICATIONS (Figure 7)						
Maximum I²C Clock Frequency	f_{SCLK}				2	MHz
Maximum Clock Period	t_{SCL_MAX}		100			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.2			µs
START Condition Setup Time	$t_{SU:STA}$		0.1			µs
Repeat START Condition Setup Time	$t_{SU:STA}$	90% to 90%	0.1			µs
START Condition Hold Time	$t_{HD:STA}$	10% of SDA/SDO to 90% of SCLK	0.15			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCLK to 10% of SDA/SDO	0.1			µs
Clock Low Period	t_{LOW}	10% to 10%	0.1			µs
Clock High Period	t_{HIGH}	90% to 90%	0.15			µs
Data Valid to SCLK Rise Time	$t_{SU:DAT}$	Write setup time	50			ns
Data Hold Time	$t_{HD:DAT}$	Write hold time			0	ns
Maximum SDO/SDA Drive Low Time	t_{DATLOW}		1.0	1.1	1.2	ms
ESD AND EMC CHARACTERISTICS						
ESD Protection (C/Q, DO/DI, V_{24} Pins)		IEC 61000-4-2 Contact Discharge		±2		kV
		IEC 61000-4-2 Airgap Discharge		±3		
ESD Protection (All Other Pins)		Human Body Model		±2		kV
Surge Protection (C/Q, DO/DI, V_{24} Pins)	V_{SRG}	IEC 61000-4-5, 500Ω 8/20µs surge to ground		±1		kV

Note 2: All devices 100% productions tested at 25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: Not production tested. Guaranteed by design.
Note 4: V_{DROP} is measured as the voltage from the driver output to GND (V_{DRIVER} - V_{GND}) when measuring thelow-side driver current limit and as (V_{24} - V_{DRIVER}) when measuring the high-side driver current limit.

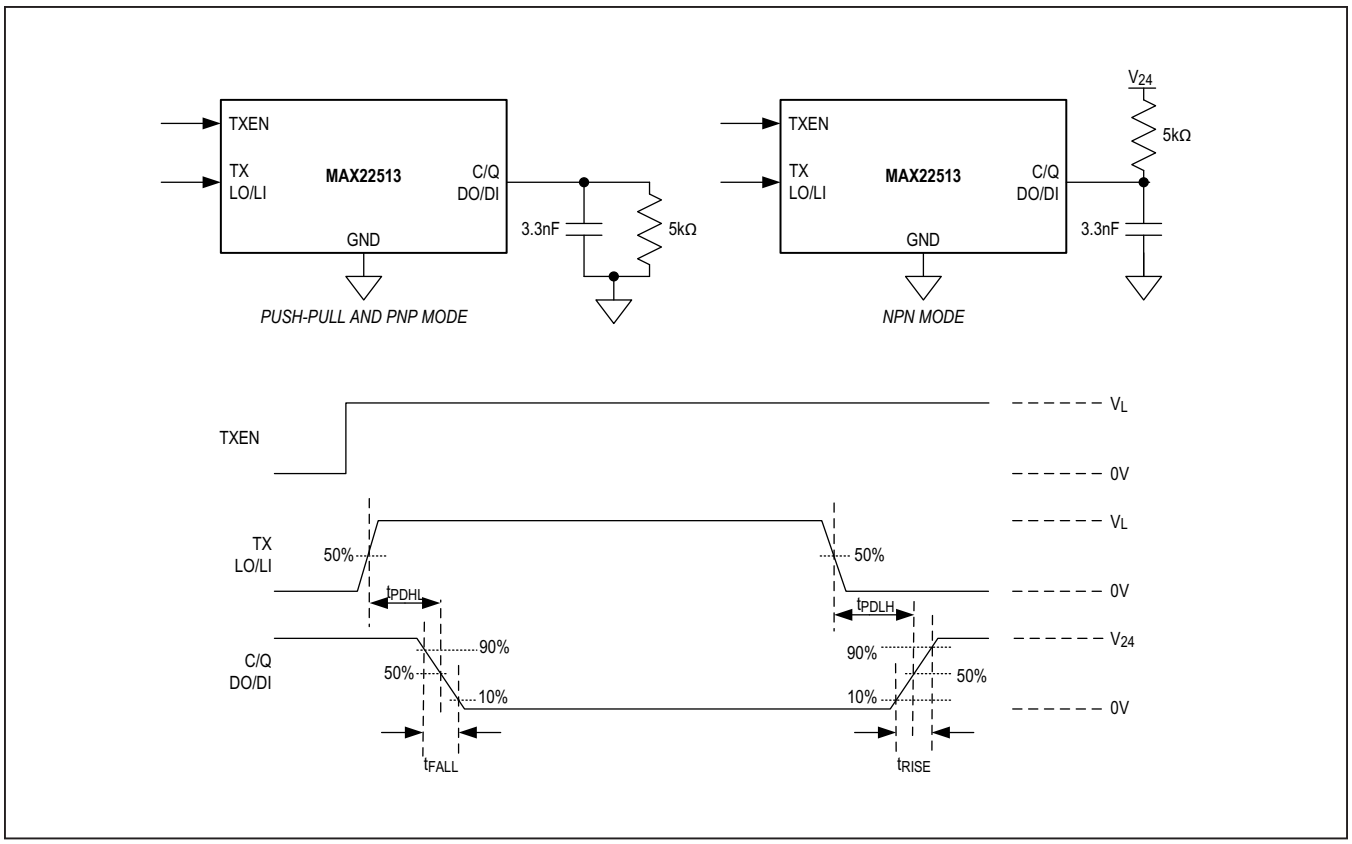


Figure 1. C/Q and DO/DI Driver Propagation Delays

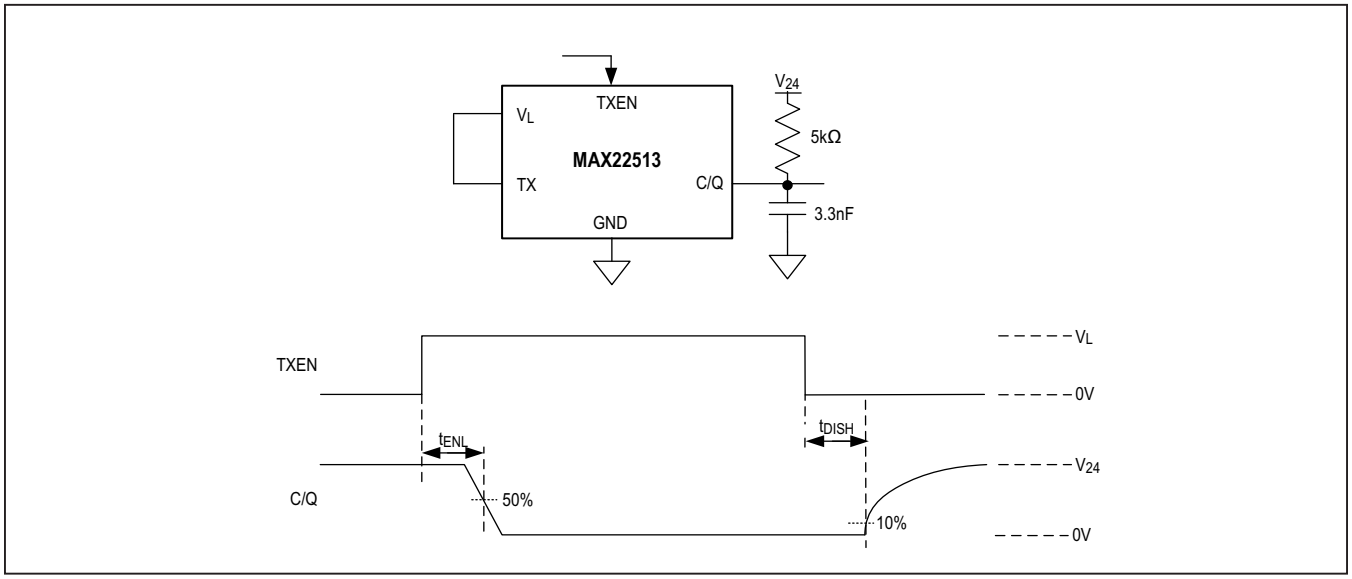


Figure 2. C/Q Driver Enable Low and Disable High Timing

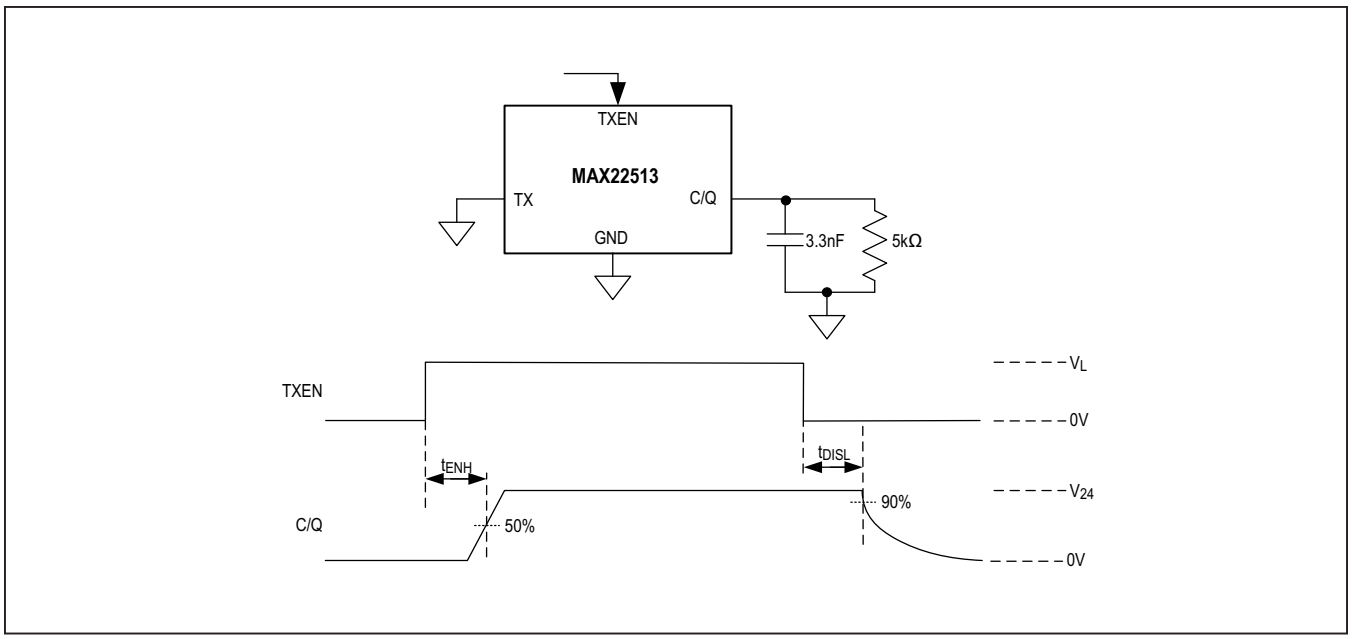


Figure 3. C/Q Driver Enable/Disable Timing

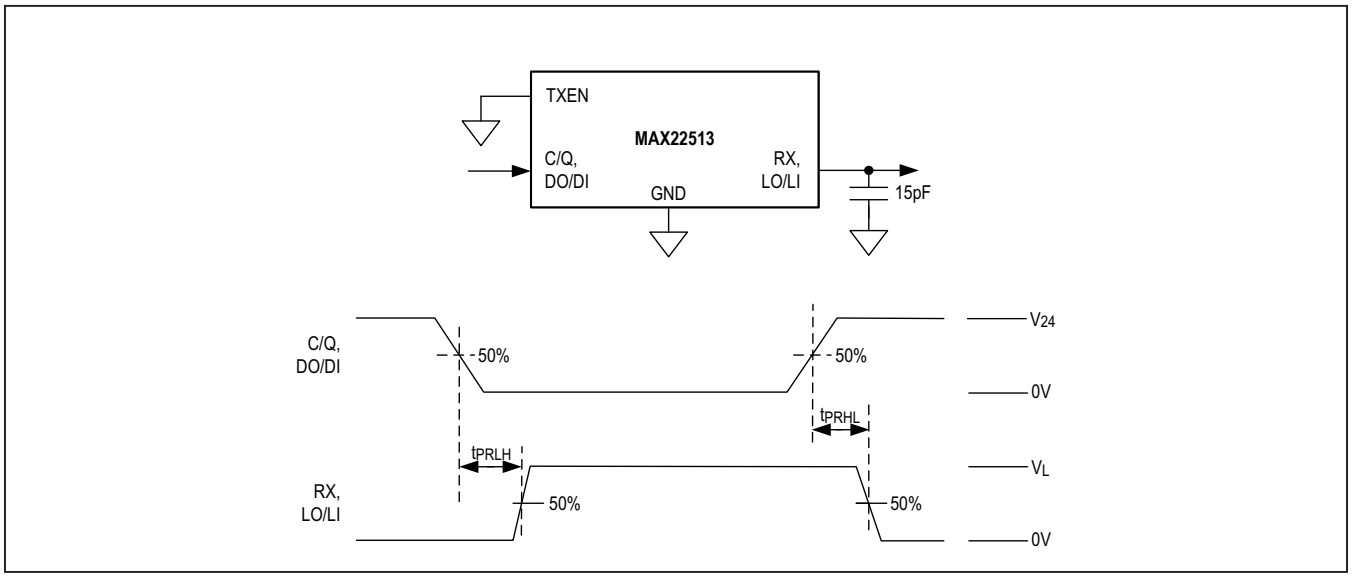


Figure 4. C/Q Receiver Timing

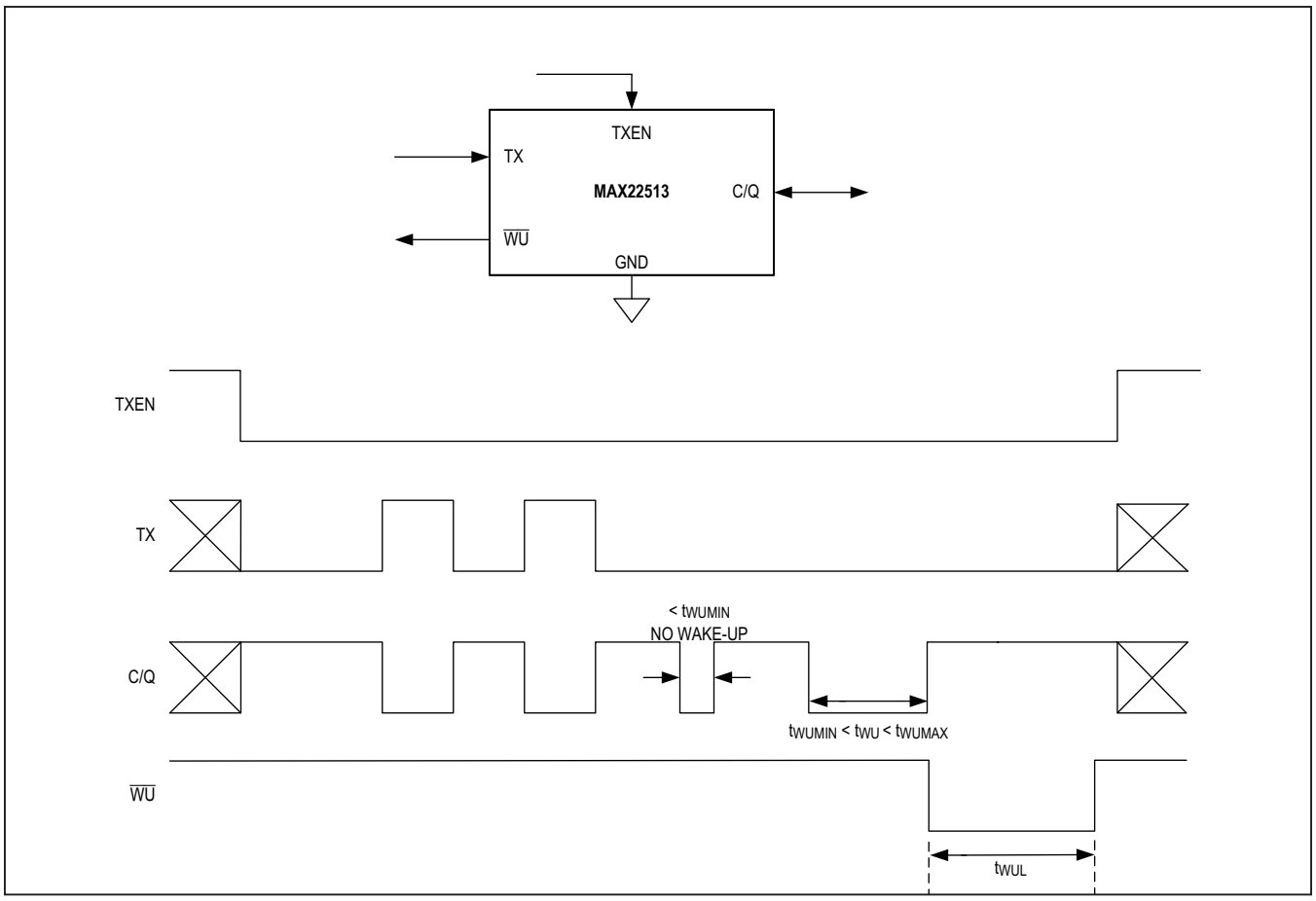


Figure 5. Wake-Up Timing

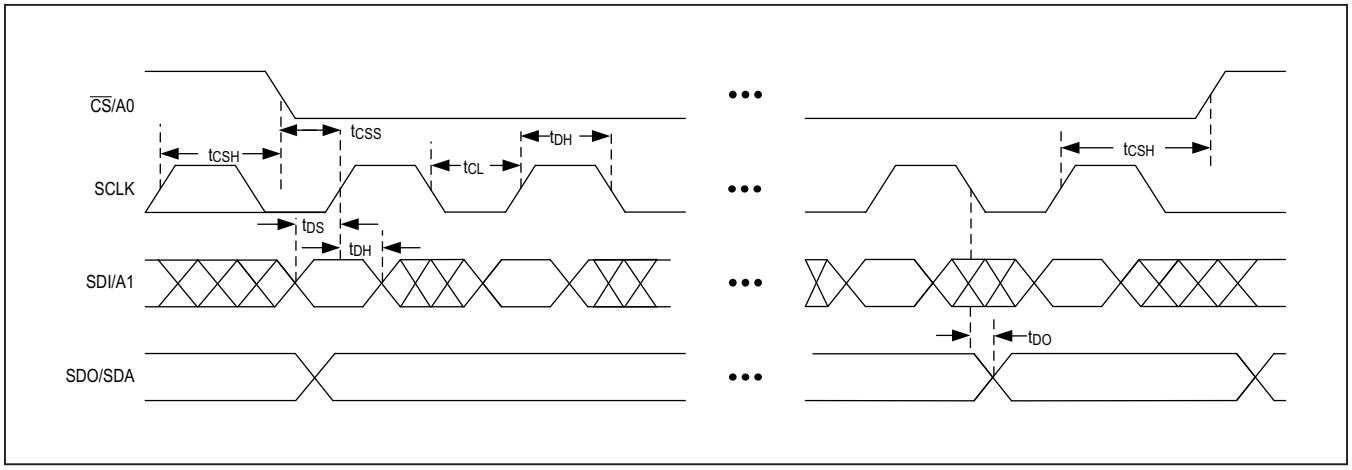


Figure 6. SPI Timing

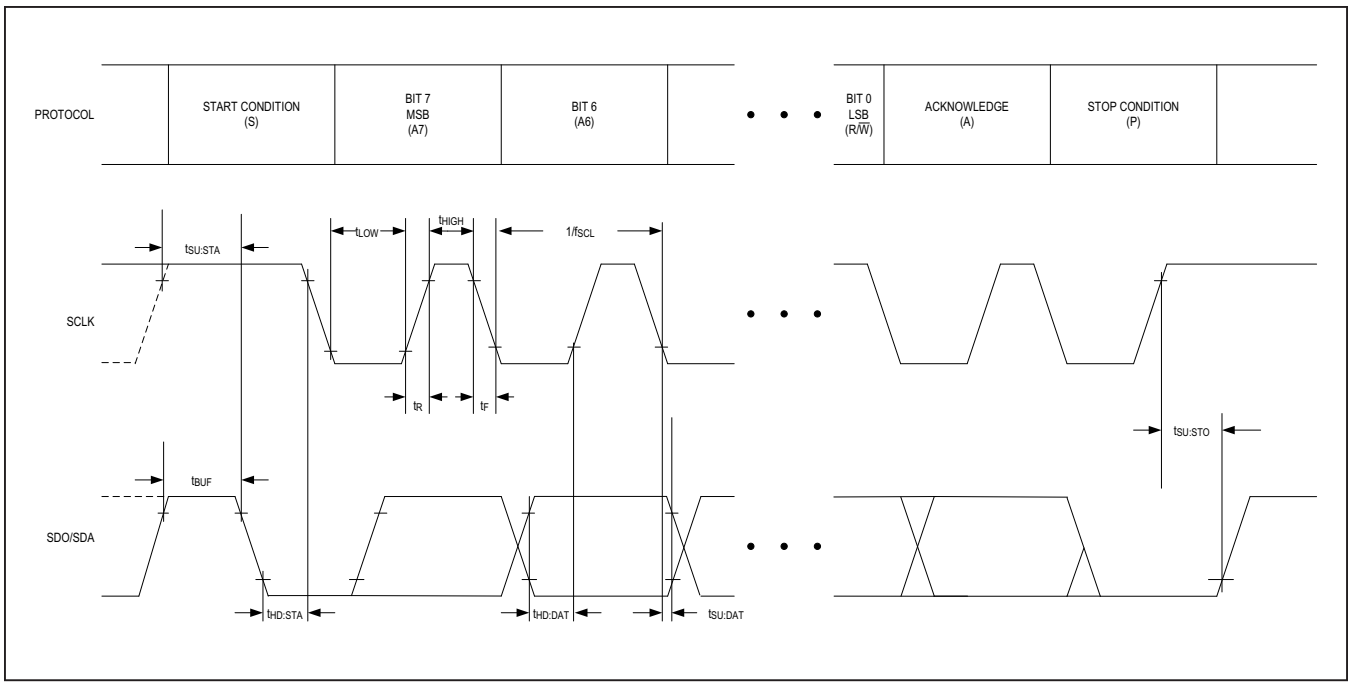
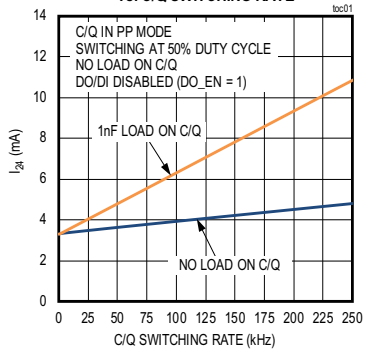


Figure 7. I2C Timing

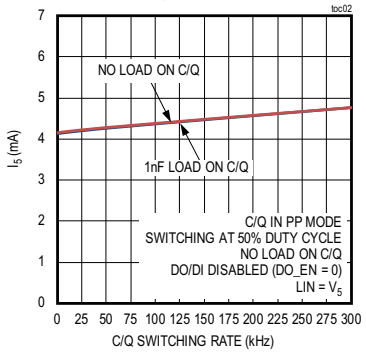
Typical Operating Characteristics

(V_{24} = 24V, V_5 = 5V, DC-DC regulator enabled, V_L = V_{33}, T_A = +25ºC, unless otherwise noted)

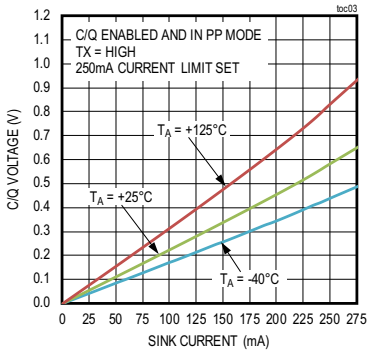
V_{24} SUPPLY CURRENT vs. C/Q SWITCHING RATE



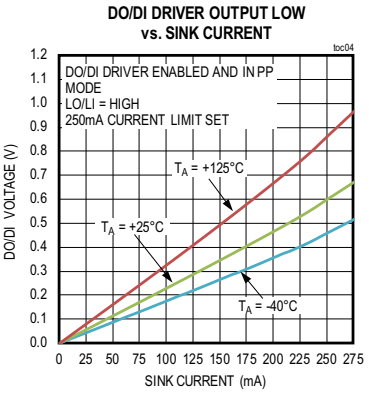
V_5 SUPPLY CURRENT vs. C/Q SWITCHING RATE



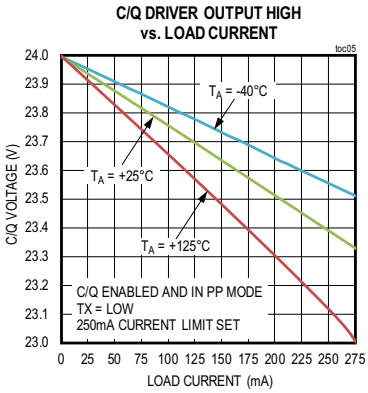
C/Q DRIVER OUTPUT LOW vs. SINK CURRENT



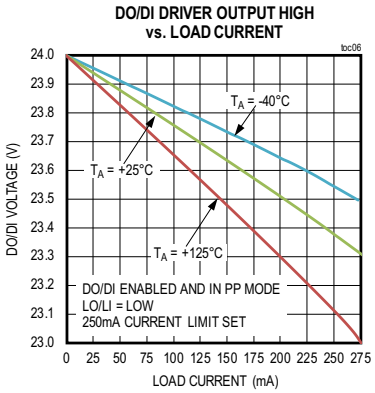
DO/DI DRIVER OUTPUT LOW vs. SINK CURRENT



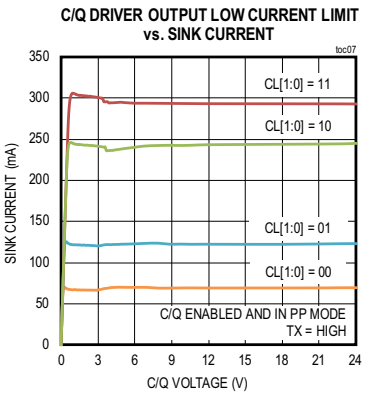
C/Q DRIVER OUTPUT HIGH vs. LOAD CURRENT



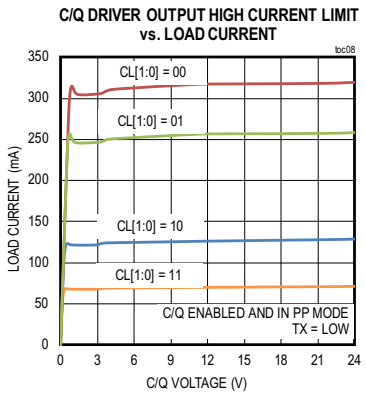
DO/DI DRIVER OUTPUT HIGH vs. LOAD CURRENT



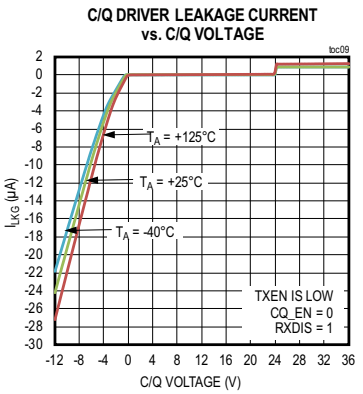
C/Q DRIVER OUTPUT LOW CURRENT LIMIT vs. SINK CURRENT



C/Q DRIVER OUTPUT HIGH CURRENT LIMIT vs. LOAD CURRENT



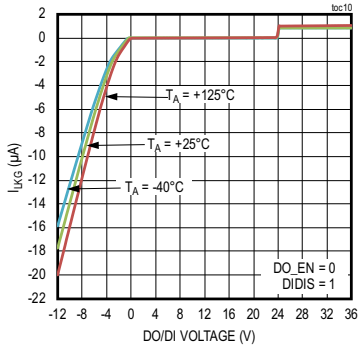
C/Q DRIVER LEAKAGE CURRENT vs. C/Q VOLTAGE



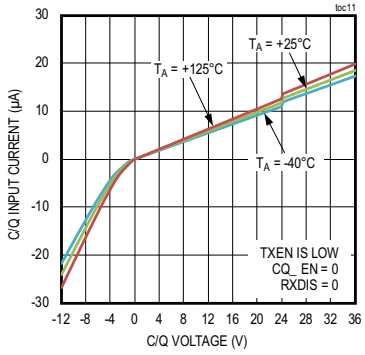
Typical Operating Characteristics (continued)

(V_{24} = 24V, V_5 = 5V, DC-DC regulator enabled, V_L = V_{33}, T_A = +25ºC, unless otherwise noted)

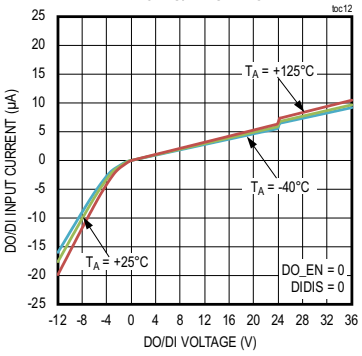
DO/DI DRIVER LEAKAGE CURRENT vs. DO/DI VOLTAGE



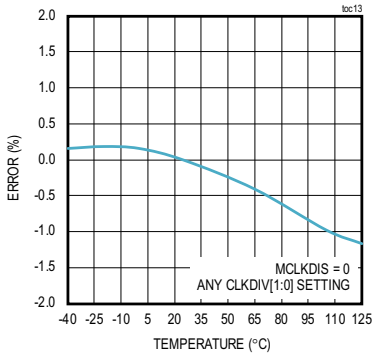
C/Q RECEIVER INPUT CURRENT vs. C/Q VOLTAGE



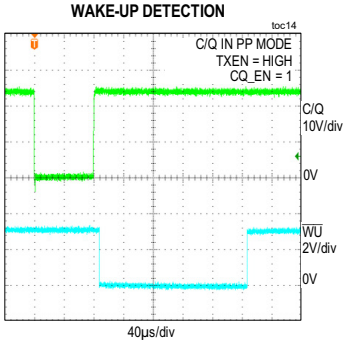
DO/DI RECEIVER INPUT CURRENT vs. DO/DI VOLTAGE



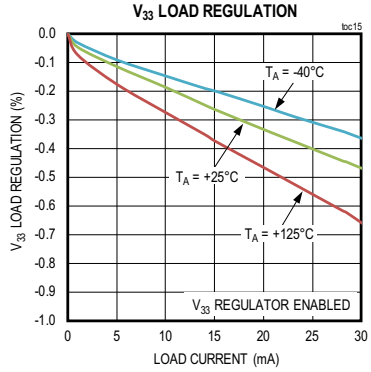
MCLK FREQUENCY ACCURACY vs. TEMPERATURE



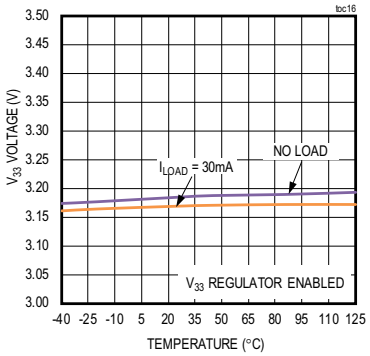
WAKE-UP DETECTION



V_{33} LOAD REGULATION

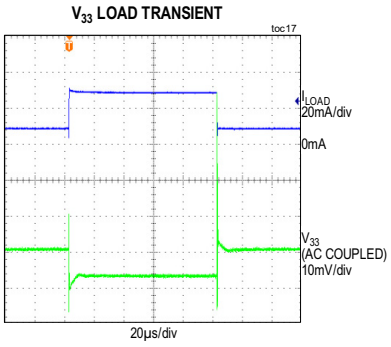


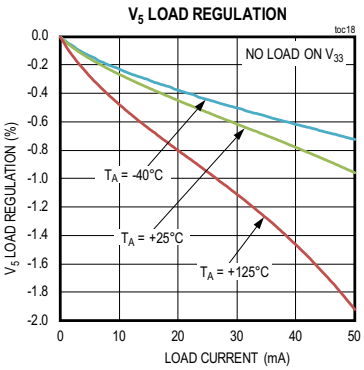
V_{33} OUTPUT VOLTAGE vs. TEMPERATURE

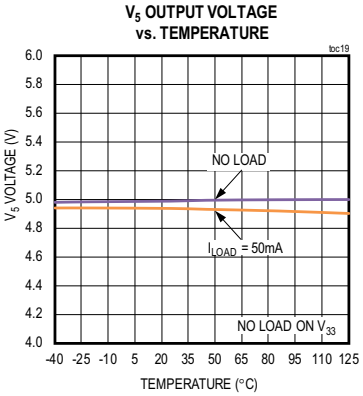


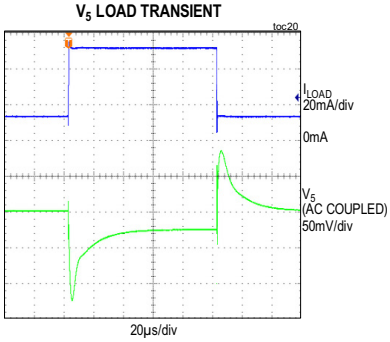
Typical Operating Characteristics (continued)

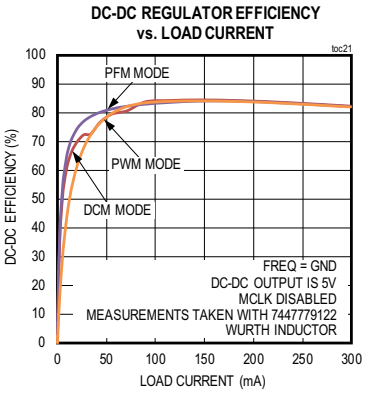
(V_{24} = 24V, V_5 = 5V, DC-DC regulator enabled, V_L = V_{33}, T_A = +25ºC, unless otherwise noted)

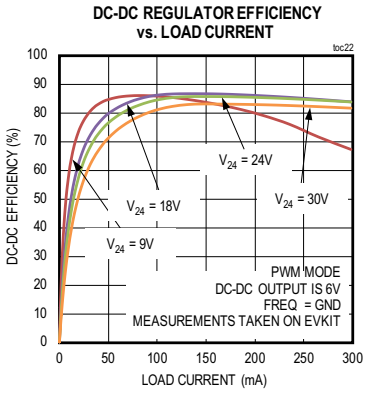


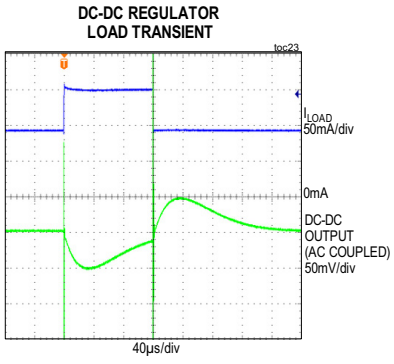




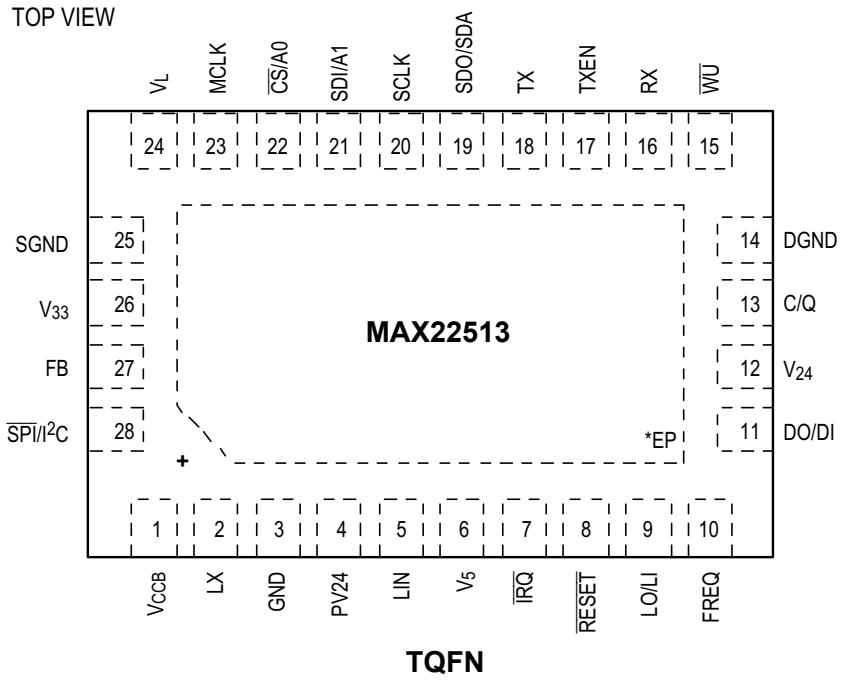




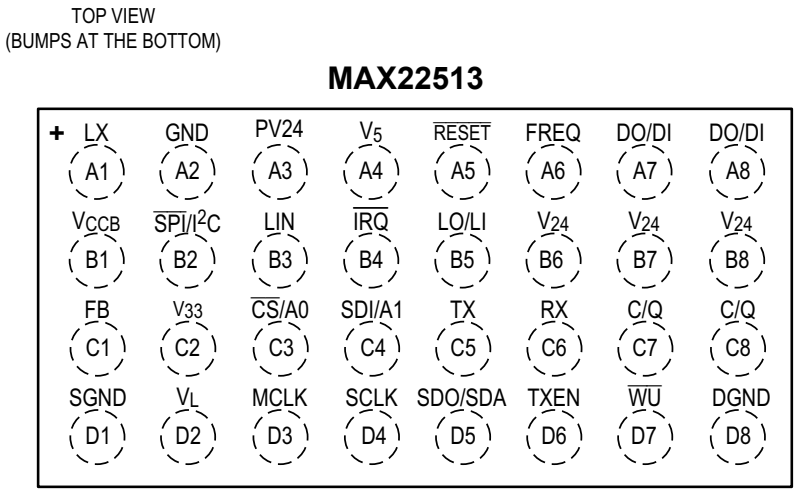




Pin Configurations



TQFN



WLP

Pin Description

PIN		NAME	FUNCTION
TQFN	WLP		
SUPPLY			
1	B1	V_{CCB}	Internal 5V Supply Regulator Output. Bypass V_{CCB} to GND with a 1µF capacitor as close to the device as possible. V_{CCB} can supply an external load up to 5mA.
3	A2	GND	Ground
4	A3	PV24	Active Diode Output and DC-DC Input. Bypass PV24 with an external 1µF capacitor as close to the device as possible.
5	B3	LIN	5V Linear Regulator Input. Connect LIN to the output of the DC-DC circuit, to the PV24 supply, or to an external supply between 6V and 36V. Bypass LIN to GND with a 1µF capacitor. Connect LIN to V_5 to disable the 5V linear regulator.
6	A4	V_5	5V Linear Regulator Output/Supply Input. V_5 is the output of the internal 5V linear regulator. Bypass V_5 to GND with a 1µF capacitor as close to the device as possible. To disable the 5V linear regulator, connect LIN to V_5. 5V is required on V_5 for normal operation. If the 5V regulator is disabled, apply an external 5V power supply to V_5.
12	B6, B7, B8	V_{24}	Supply Voltage Input. Apply a 24V (typ) supply to V_{24}. Bypass V_{24} to GND with a 10nF capacitor as close to the device as possible. When using the WLP package, connect all V_{24} bumps together.
14	D8	DGND	C/Q and DO/DI Driver IO-Link Ground. Connect DGND to the L-terminal of the IO-Link connector and to GND. See the *Layout and Grounding* section for more information.
24	D2	V_L	Logic Supply Input. Bypass V_L to GND with a 1µF capacitor as close to the device as possible. V_L sets the logic levels for all logic signals. Connect V_L to V_{33}, V_5, or to an external voltage between 2.5V and 5.5V.
25	D1	SGND	Signal Ground. Connect SGND to GND. See the *Layout and Grounding* section for more information.
26	C2	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND with a 1µF capacitor as close to the device as possible.
EP	-	EP	Exposed Pad. Connect EP to GND.
DC-DC REGULATOR			
2	A1	LX	Switching Output of the Integrated DC-DC Converter. Connect an inductor between LX and the output capacitor to generate a voltage with the DC-DC circuit. See the *Integrated DC-DC Regulator* section for more information.
10	A6	FREQ	DC-DC Buck Regulator Frequency Select Input. Connect FREQ to GND to operate the DC-DC regulator at a switching frequency of 921kHz (typ). Connect FREQ to V_{CCB} to operate the regulator at a switching frequency of 1.229MHz (typ).
27	C1	FB	DC-DC Buck Regulator Feedback Input. Connect FB to the tap of a resistor divider between the output of the DC-DC and GND. See Table 1 for recommended component values to set the DC-DC output between 2.5V and 12V. Connect FB to V_{CCB} if the DC-DC is not used.

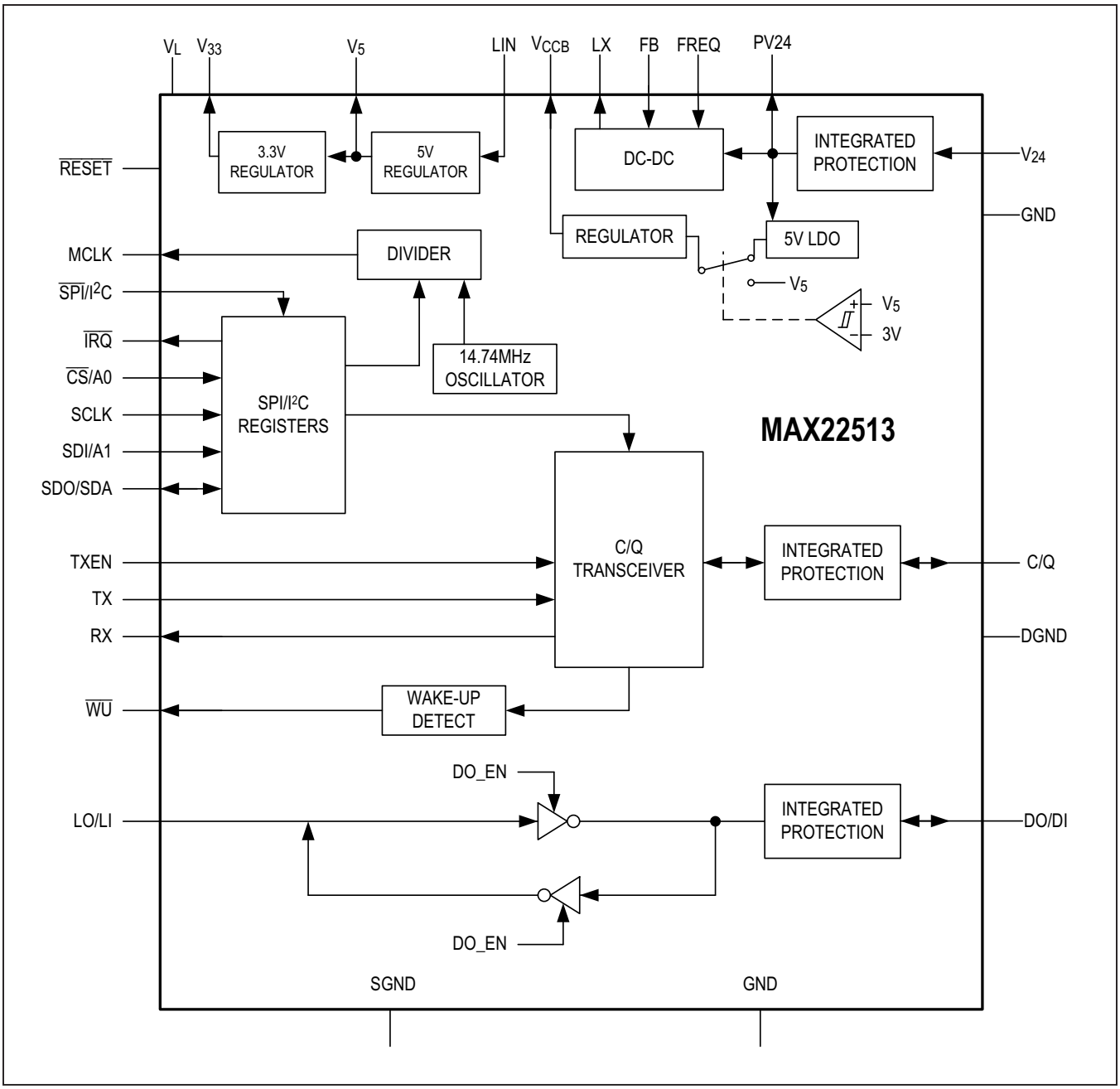
Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
24V LINE INTERFACE			
11	A7, A8	DO/DI	DO Auxiliary Driver Output/DI Auxiliary Digital Input. Use the register bits to select between digital output (DO) and digital input (DI) functionality for DO/DI. The DO/DI driver is disabled at started. When using the WLP package, only one of the DO/DI bumps need to be soldered. However, Maxim recommends connecting both bumps whenever possible.
13	C7, C8	C/Q	IO-Link Transceiver Input/Output. The C/Q driver is disabled at startup. Set CQ_EN = 1 and TXEN = high to enable the C/Q driver. When using the WLP package, only one of the C/Q bumps needs to be connected. However, Maxim recommends connecting both C/Q bumps whenever possible.
CONTROL INTERFACE			
7	B4	$\overline{IRQ}$	Active-Low Open-Drain Interrupt Request Output. $\overline{IRQ}$ asserts low when a bit is set in the INTERRUPT register. See the *Register Map* section for more information.
8	A5	$\overline{RESET}$	Dual Function Active-Low Reset Input and Open-Drain Power-OK (POK) Output. Drive $\overline{RESET}$ low to set the MAX22513 in reset mode. The C/Q and DO/DI outputs are disabled and all registers are reset to default values when $\overline{RESET}$ is driven low. The MAX22513 asserts $\overline{RESET}$ low when any of the V_{24}, V_5, or DC-DC output voltages are below their respective undervoltage lockout (UVLO) thresholds. Only V_5 is monitored when the DC-DC regulator is disabled. The MAX22513 deasserts $\overline{RESET}$ 4ms (typ) after the power supplies rise above their UVLO thresholds. Connect $\overline{RESET}$ to V_{CCB} or V_L with a 10kΩ (typ) resistor for normal operation.
9	B5	LO/LI	DO/DI Driver Logic Input/Receiver Logic Output. LO/LI is an output by default (DO_EN = 0 in the DOCONFIG register). In this configuration, LO/LI is inverted relative to the logic state of the DO/DI input. LO/LI is configured as an input when the DO/DI driver is enabled (DO_EN = 1 in the DOCONFIG register). In this configuration, DO/DI driver is inverted relative to the LO/LI logic state.
15	D7	$\overline{WU}$	IO-Link Wake-Up Request Output. $\overline{WU}$ asserts low for 200µs (typ) when a valid IO-Link wake-up pulse is detected on the C/Q line.
19	D5	SDO/SDA	Serial Data Output/Serial Data I/O. In SPI mode, SDO/SDA is the serial data output (MISO). SDO/SDA is high impedance when $\overline{CS}$/A0 is high. In I^2C mode, SDO/SDA operates as the serial data I/O line.
20	D4	SCLK	Serial Clock Input.
21	C4	SDI/A1	Serial Data Input/Address Select Input 1. In SPI mode, SDI/A1 operates as the serial data input (MOSI). In I^2C mode, connect SDA/A1 high or low to set the I^2C slave address for the device.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
22	C3	$\overline{CS}$/A0	SPI Chip-Select Input/I²C Address Input 0. In SPI mode, drive $\overline{CS}$/A0 low to start a read/write cycle. The cycle ends when $\overline{CS}$/A0 is driven high. In I²C mode, drive $\overline{CS}$/A0 high or low to set the I²C slave address.
28	B2	$\overline{SPI}$/I²C	$\overline{SPI}$ or I²C Control Interface Selection Input. Connect $\overline{SPI}$/I²C low for SPI operation. Connect $\overline{SPI}$/I²C high for I²C operation.
UART INTERFACE			
16	C6	RX	C/Q Receiver Logic Output. RX is inverted relative to the logic state of C/Q by default. Set the INVCQ bit in the CQCONFIG register to set RX to the same logic state as C/Q. Connect RX to the RX input of the UART for IO-Link communication.
17	D6	TXEN	C/Q Driver Enable Logic Input. Drive TXEN high and set the CQ_EN bit in the CONTROL register to enable the C/Q driver. Drive TXEN low to disable the C/Q driver. Connect TXEN to the RTS output of a microcontroller for IO-Link communication.
18	C5	TX	C/Q Driver Logic Input. TX is inverted relative to the logic state of C/Q by default. Set the INVCQ bit in the CQCONTROL register to set TX to the same logic state as C/Q. Connect TX to the TX output of the UART for IO-Link communication.
CLOCK OUTPUT			
23	D3	MCLK	Microcontroller Clock Output. Set the MCLK frequency by setting the CLKDIV bits in the CLKCONFIG register. The frequency of the MCLK signal can be trimmed by setting the CKTRIM bits in the CKTRIM register. Connect MCLK to an external microcontroller for comparison and trimming. The MCLK frequency is 3.686MHz by default but can be disabled or programmed to 14.74MHz, 7.37MHz, or 1.843MHz.

Functional Diagrams



Detailed Description

The MAX22513 industrial sensor output driver/IO-Link device transceiver integrates the high voltage functionality commonly found in sensors, including two 24V line drivers (C/Q and DO/DI), an integrated DC-DC buck regulator, 5V and 3.3V linear regulators, and a digital input (DO/DI). The MAX22513 can be configured and monitored with either an SPI or I^2C serial bus.

24V Interface (C/Q and DO/DI)

Overcurrent Limiting

The C/Q and DO/DI drivers feature a programmable current limit. Select the current limit for both drivers by setting the CL[1:0] bits in the CURRLIM register. Current limit thresholds can be set to 50mA (min), 100mA (min), 200mA (min), or 250mA (min). When the load attempts to draw more current than the current limit threshold setting, the C/Q and DO/DI driver actively limits the load current so a higher load current does not flow.

Continuous Current Limiting with Blanking Time

A programmable current limit blanking time allows the device to drive large capacitive or incandescent lamp loads without triggering a current limit fault. Select the blanking time by setting the CL_BL[1:0] bits in the CURRLIM register. Set the CL_BL[1:0] bits for a 128µs, 500µs, 1ms, or 5ms blanking time.

When the C/Q or DO/DI driver current exceeds the programmed current limit threshold for longer than the programmed blanking time, the associated driver fault bit (CQFAULTINT and/or DOFAULTINT) bit in the INTERRUPT register is set. If the interrupt is not masked, the $\overline{IRQ}$ output also asserts. If autoretry is enabled, the driver in overcurrent is disabled following the blanking time.

If autoretry is not enabled, the driver in overcurrent is not disabled after the blanking time. In this configuration, the CQFAULT and/or DOFAULT bit in the STATUS register are set and the drivers continue to operate until either the fault condition is removed or the driver in overcurrent enters thermal shutdown.

Autoretry

The MAX22513 features an autoretry function for applications where an overload condition might not be sustainable, or where power dissipation needs to be controlled. Set the AUTORETRYEN bit in the CURRLIM register to enable autoretry functionality. When autoretry is enabled, the MAX22513 automatically disables the driver after the current limit threshold has been exceeded for the selected blanking time. The driver is disabled for the programmed fixed off-time, and is then automatically reenabled. If the overcurrent condition is still present, the driver remains on for the blanking time and is then redisabled. The autoretry cycle continues until the overcurrent condition is removed.

Select the blanking time and fixed off-time by setting the CL_BL[1:0] bits and the TSHOFF[1:0] bits, respectively, in the CURRLIM register.

When charging large capacitive loads or incandescent lamps, ensure that the selected autoretry blanking time is long enough to charge the required load before the driver is disabled.

C/Q and DO/DI Driver Thermal Shutdown

The C/Q and DO/DI drivers are each independently disabled when the driver junction temperature exceeds the +150°C (typ) driver thermal shutdown temperature. The associated driver fault bits (CQFAULTINT and/or DOFAULTINT, CQFAULT and/or DOFAULT) in the INTERRUPT and STATUS registers are set. If the fault is not masked (CQFAULTM = 0 or DOFAULTM = 0 in the IRQMASK register), the $\overline{IRQ}$ is asserted after the programmed blanking time. Set the CL_BL[1:0] bits in the CURRLIM register to select the blanking time.

If autoretry is disabled, the driver is automatically reenabled when the driver junction temperature falls below 142°C (typ). If autorety is enabled (AUTORETRYEN = 1), the MAX22513 waits for the autoretry delay and reenables the driver.

Undervoltage Lockout Threshold (UVLO)

The C/Q and DO/DI drivers are turned off (high impedance) when any supply (V_{24}, V_5, or V_L) falls below its respective undervoltage lockout (UVLO) threshold.

If the registers were reset during the UVLO event, reenable the drivers when all supplies are above their UVLO thresholds.

Receiver Threshold

Although the IO-Link standard defines device/sensor operation for a supply ranging between 18V to 30V, industrial sensors in the field commonly operate with supply voltages as low as 9V. The MAX22513 operates with a supply voltage between 8V and 36V. When the V_{24} supply voltage is above 18V, the C/Q receiver on the MAX22513 supports the standard IO-Link receiver thresholds. When V_{24} is less than 18V, the MAX22513 scales the C/Q receiver thresholds, allowing receiver functionality down to the lowest supply voltage.

Wake-Up Detection

The IO-Link standard defines a wake-up condition as a combination of a current and a voltage event on the C/Q line when the driver is enabled in PNP, NPN, or push-pull mode. A wake-up event occurs when an IO-Link master forces a level on the C/Q line that is opposite to the set level of the C/Q driver level for 80µs (typ).

Wake-up detection on the MAX22513 is enabled by default. When a valid wake-up event is detected, the MAX22513 asserts the $\overline{WU}$ output for 200µs (typ). The WUINT bit in the INTERRUPT register is set and $\overline{IRQ}$ asserts if the wake-up interrupt is not masked (WUM = 0 in the IRQMASK register).

The MAX22513 automatically ignores false wake-up events that can sometimes occur as a consequence of driving large capacitive or lamp loads where the time constant of charge-up is in the range of about 80µs. No wake-up event is detected for the duration of the programmed blanking time after the C/Q driver changes logic state.

To disable wake-up detection, set the WUDIS bit in the CONTROL register.

V_{CCB} Output

The V_{CCB} output can supply an external supply current up to 5mA. V_{CCB} is the output of an internal regulator powered by V_{24} or V_5. V_{CCB} is powered by V_{24} until the V_5 voltage exceeds 3V. After which, V_{CCB} is powered by V_5. As V_5 is rising, V_{CCB} can drop below 5V until V_5 reaches its steady-state (5V).

$\overline{RESET}$ Input/Power OK (POK) Output

The $\overline{RESET}$ pin is a dual function open-drain logic input/output, functioning as a reset input and a power-OK (POK) output. Drive $\overline{RESET}$ low to put the MAX22513 in reset mode. The C/Q and DO/DI drivers are disabled and the registers are reset to their default state when $\overline{RESET}$ is driven low. Serial bus communication (SPI or I^2C) is available while $\overline{RESET}$ is low. If DC-DC is disabled in the registers (BUCKDIS = 1), the device deasserts $\overline{RESET}$ 4ms (typ) after $\overline{RESET}$ is released and all power supplies are valid. If the DC-DC is enabled, $\overline{RESET}$ deasserts immediately after being released.

The MAX22513 asserts $\overline{RESET}$ low when the V_{24} or V_5 voltage falls below their respective UVLO thresholds, or when the DC-DC output voltage falls below 95% of the set voltage (typ). $\overline{RESET}$ also asserts when the device enters thermal shutdown. The C/Q and DO/DI drivers are disabled and the registers are reset to their default state when $\overline{RESET}$ is low.

Connect a pullup resistor between $\overline{RESET}$ and V_L or V_{CCB} for normal operation. Connect $\overline{RESET}$ to the reset input of a microcontroller to use it as a reset signal.

Protection

Reverse Polarity Protection

The MAX22513 is internally protected against reverse polarity miswiring on the C/Q, DO/DI, V_{24} and GND pins. Any combination of these four pins can be connected to a voltage in the range of -36V to +36V. Shorts to these voltages results in a current flow of less than 500µA. Note that the maximum voltage between any pins cannot exceed *Absolute Maximum Ratings*.

High Temperature Warning

When the junction temperature of the die rises above the thermal warning threshold of 147°C, the THERMWINT bit in the INTERRUPT register and the TEMPW bit in the STATUS register are set. If not masked (THERMWM = 0), the $\overline{IRQ}$ output also asserts low. The MAX22513 continues to operate normally as long as the die temperature does not exceed the thermal shutdown threshold (+170°C, typ).

Thermal Shutdown

The MAX22513 enters thermal shutdown when the average die temperature exceeds the +170°C (typ) thermal shutdown threshold. The C/Q and DO/DI drivers and the internal regulators (including the DC-DC and linear regulators) are disabled when the device is in thermal shutdown. $\overline{RESET}$ asserts during thermal shutdown and the serial interface is disabled if an external 5V is applied to V_5 during thermal shutdown, the serial control interface remains operational.

When the average die temperature falls below the 153°C (typ) thermal shutdown hysteresis, all registers are reset and must be programmed when the serial interface becomes active after the device exits thermal shutdown.

POR and Register Corruption Check

The MAX22513 performs an on-going check of all register bits. A register is corrupted when the value is changed by an external event (for example, an ESD discharge, etc). When a corrupt register bit is detected, the CORR_REG bit in the STATUS register is set, the NOTREADY bit in the INTERRUPT register is set, and the MAX22513 asserts the $\overline{IRQ}$ output. The C/Q and DO/DI drivers are disabled when the NOTREADY bit is set.

The microcontroller must rewrite correct values to all of the registers after the CORR_REG bit has been set. The CORR_REG bit is automatically cleared when the serial interface control registers have been rewritten to their pre-event cycle values. Once the CORR_REG bit is cleared, read the INTERRUPT register to clear the NOTREADY bit and deassert $\overline{IRQ}$.

Integrated DC-DC Regulator

Overview

The MAX22513 features an integrated high-efficiency synchronous DC-DC buck regulator with active diode reverse protection, current overload protection, soft-start, a selectable switching frequency, spread spectrum operation, and an adjustable output voltage. The regulator operates in pulse-width modulation (PWM) mode, pulse frequency modulation (PFM) mode, or discontinuous conduction mode (DCM) during normal operation. Select the operating mode by setting the BUCKDCM or BUCKPFM mode bits in the MODE register. The regulator is enabled by default, but can be disabled through the serial interface.

The DC-DC regulator is supplied from the PV24 voltage to protect against supply inversion. Bypass PV24 to GND with a 1µF capacitor to ensure proper operation for the DC-DC.

Startup and Soft-Start

The MAX22513 DC-DC buck regulator features soft-start to slowly raise the output voltage when the device is powered up.

When the V_{24} voltage exceeds the 7.6V (typ) UVLO threshold, the DC-DC regulator is turned on, operating in DCM mode. The DCM mode allows the DC-DC output to soft-start whether the output voltage is unpowered or prebiased.

Internal circuitry slowly ramps the output voltage to 95% of the set voltage within 2.22ms (typ) of the V_{24} voltage exceeding the UVLO threshold, ending the soft-start sequence. Once soft-start has ended, the regulator switches from DCM mode to the selected mode for normal operation. By default, normal operation is PWM mode. Set the BUCKPFM and/or the BUCKDCM bits in the MODE register to select another operating mode of the DC-DC regulator.

Maximum DC-DC Output Current

The MAX22513 integrated DC-DC buck regulator can drive loads up to 300mA (typ).

The internal reverse-protection active diode between V_{24} and PV24 has a 200mA average current capability to supply the DC-DC input. Under certain conditions, the internal active diode between the V_{24} supply and PV24 can reduce the efficiency or reduce the maximum load current. If load currents are such that the current through the active diode exceeds 200mA, connect a Schottky diode between V_{24} and PV24 to bypass the internal active diode. When a Schottky diode is used, a TVS or varistor on V_{24} might be necessary to survive hot-plug events.

Setting up the DC-DC Regulator

Selecting the Mode of Operation

The MAX22513 features selectable switching modes for the integrated DC-DC regulator during normal operation. Available modes are pulse-width modulation (PWM), pulse frequency modulation (PFM), or discontinuous conduction mode (DCM). Set the BUCKDCM and BUCKPFM bits in the MODE register to select the normal operating mode.

Pulse Width Modulation (PWM)

A PWM DC-DC regulator switches at a fixed frequency, adjusting the duty cycle of the pulses depending on the output power requirements. The maximum duty cycle on the DC-DC regulator is near 100%. Switching noise is easily filtered in PWM mode.

The MAX22513 DC-DC regulator operates in PWM mode by default (BUCKDCM = 0 and BUCKPFM = 0 in the MODE register).

Pulse Frequeny Modulation (PFM)

In PFM mode, the DC-DC converter switches LX with a peak current set to be at least 200mA. LX stops switching when the output voltage exceeds 103% of set value and starts switching again when the DC-DC output voltage drops to 101% the set value.

Because the switching frequency changes in this mode, switching noise is more difficult to filter in PFM mode, typically resulting in a higher ripple on the output. PFM mode has the highest efficiency when driving low loads.

Set BUCKPFM = 1 and BUCKDCM = 0 in the MODE register to enable PFM mode on the DC-DC regulator.

Discontinuous Conduction Mode (DCM)

In DCM mode, the inductor current of the DC-DC regulator can reach zero for a short period during each switching cycle. In this mode, the output voltage is dependent on the input voltage, the inductance in the DC-DC regulator, the switching frequency, and the load. Use DCM mode for low output ripple and high efficiency under light load conditions.

The MAX22513 DC-DC regulator operates in DCM mode during soft-start. Set BUCKDCM = 1 in the MODE register (the BUCKPFM bit is ignored, in this case) to enable DCM functionality for normal operation.

Enabling/Disabling the DC-DC

The integrated DC-DC buck regulator on the MAX22513 is enabled by default, but can be disabled through the serial interface. Set the BUCKDIS bit in the MODE register to disable the DC-DC.

If the DC-DC regulator is not used, leave the LX unconnected and connect FB to V_{CCB}.

Setting the DC-DC Switching Frequency

The integrated DC-DC buck regulator operates with a fixed frequency during normal operation. The switching frequency is selectable by connecting the FREQ input high or low. Connect FREQ to GND to select a switching frequency of 921kHz (typ). Connect FREQ to V_{CCB} to select a 1.229MHz (typ) switching frequency.

Component Selection

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough to ensure that saturation cannot occur below the 860mA maximum current-limit value. Under lower load conditions, smaller inductors can be used.

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended to be used with the MAX22513 DC-DC regulator. The output capacitor has two functions: (1) it filters the square wave generated by the device along with the output inductor, and (2) it stabilizes the device's internal control loop. Capacitor selection depends on the operating conditions and the value of R_H, and can affect the stability of the DC-DC regulator.

Adjusting the Output Voltage

The output voltage of the DC-DC regulator can be programmed from 2.5V to 12V. Set the output voltage by connecting a resistor divider from the the output to FB to GND (see the *Typical Application Circuits*).

Calculate the output voltage using the following equation:

$$R_H = R_L \times (V_{OUT} / 0.9 - 1)$$

Ensure that $R_H \parallel R_L \leq 66k\Omega$ and use 1% resistors for best accuracy.

The R_H resistor controls the load regulation on the load step and can also affect the value of the output capacitor to ensure stability of the DC-DC regulator.

Typical External Components

Table 1 shows the recommended component values for the DC-DC buck regulator for a wide range of typical operating conditions. Recommended values in the table are designed for < ±3% load regulation on a 50% load current step and with minimum inductance. A ±30% tolerance on inductance and a ±20% tolerance on capacitance is expected due to C-V dependence. Note that the recommended standard capacitance shown in the table is a standard value and includes typical tolerance and voltage derating. For other configurations than shown in Table 1, please contact customer support.

Table 1. Recommended DC-DC Component Values

FREQ	OUTPUT VOLTAGE (V)	V_{24} (V)		MAXIMUM OUTPUT CURRENT (mA)	L (µH)	MINIMUM OUTPUT CAPACITANCE (µF)	MAXIMUM OUTPUT CAPACITANCE (µF)	RECOMMENDED STANDARD OUTPUT CAPACITOR (µF)	R_H (kΩ)	R_L (kΩ)
		MIN	MAX							
LOW	2.5	8	36	300	12	19.2	42.0	27	128	73.2
	3.0	8	36	300	12	9.1	49.0	12	154	66.5
	3.3	8	36	300	15	11.7	23.2	15	169	63.4
	5	8	36	300	22	5.2	18.0	6.8	261	56.2
	6	8	36	300	22	4.1	15.6	5.6	309	54.9
	7	8	36	260	27	2.7	12.0	3.9	422	61.9
	8	10	36	230	27	1.7	9.8	2.2	549	69.8
	9	12	36	200	33	1.2	8.3	1.8	665	73.2
	10	12	36	180	33	1.0	7.6	1.5	750	73.2
	11	12	36	160	33	0.8	7.0	1.2	825	73.2
	12	14	36	150	39	0.7	6.6	1	887	71.5
HIGH	3.3	8	36	300	10	11.5	23.7	15	169	63.4
	5	8	36	300	15	5.4	17.7	6.8	261	56.2
	6	8	36	300	18	4.4	15.3	5.6	309	54.9
	7	8	36	260	22	2.9	11.7	3.9	422	61.9
	8	10	36	230	22	1.8	9.5	2.7	549	69.8
	9	12	36	200	22	1.3	8.2	1.8	665	73.2
	10	12	36	180	27	1.1	7.4	1.5	750	73.2
	11	12	36	160	27	0.9	6.8	1.2	825	73.2
	12	14	36	150	27	0.8	6.5	1.2	887	71.5

DC-DC Spread-Spectrum

The DC-DC regulator uses an internal clock that is synchronized with the main on-board oscillator used to generate other signals and timing. To reduce EMC emission peaks and/or reduce interference between the DC-DC switching circuitry and analog circuitry, the MAX22513 features a selectable spread-spectrum functionality for the DC-DC clock. When enabled, the DC-DC clock is randomly changed with a maximum frequency deviation of ±10% (typ).

By default, DC-DC spread spectrum is disabled. Set the BUCKSS bit in the MODE register to enable spread spectrum for the DC-DC.

DC-DC Protection and Diagnostics

DC-DC Overcurrent and Runaway Protection

The DC-DC regulator includes integrated circuitry to protect the regulator during a current overload condition to avoid runaway. When the high-side current exceeds the 600mA (typ) high-side peak current limit (I_{DC_HSlim}), the high-side switch is disabled.

Low-side current protection is available. When the low-side current exceeds the 300mA (typ) low-side current limit threshold (I_{DC_LSmax}), the low-side switch is turned off and LX is unconnected until the next clock cycle and switching begins again.

Hiccup (Autoretry) Mode

The DC-DC regulator features an autoretry sequence (hiccup mode) to protect against fault conditions on the output.

After soft-start, if the output voltage of the DC-DC regulator falls below 64% (typ) of the set threshold, the regulator is disabled for 22ms (typ) and the BUCKFAULT bit in the STATUS2 register is set. Following the autoretry period, the DC-DC is restarted with soft-start.

If the fault on the output persists, the DC-DC is disabled and the autoretry sequence begins again. If the output voltage rises to 95% (typ) of the expected voltage, the DC-DC exits hiccup mode and operates normally.

DC-DC Power Diagnostics

The BUCKFAULT and BUCKOK bits in the STATUS2 register indicate the state of the DC-DC output. Use these bits to monitor the regulator during operation.

BUCKOK is set when the output voltage is above 95% (typ) of the set voltage and the regulator is operating normally. When the DC-DC output voltage falls below 95% (typ) of the set voltage, $\overline{RESET}$ asserts and the BUCKOK bit is 0.

BUCKFAULT is set when regulator is in a fault condition. Fault conditions include current overload, when the output voltage falls below 64% (typ) of the set threshold, or when the regulator is operating in hiccup mode. BUCKFAULT is cleared automatically when the regulator returns to normal operation.

SPI or I²C Controller Interface

Selecting the Controller Interface: SPI or I²C

The MAX22513 diagnostics and configuration registers are accessible through a serial interface. The MAX22513 supports both either SPI or I²C communication. All control and diagnostic registers are available in both SPI and I²C. Drive $\overline{SPI}$/I²C low to use the SPI control interface. Drive the $\overline{SPI}$/I²C input high to use the I²C control interface.

SPI Interface

The MAX22513 supports full- and half-duplex SPI communication at speeds up to 12MHz. At power-up, the SPI interface is configured for full-duplex communication. Set the SPIHDX bit in the MODE register to enable half-duplex SPI communication.

The master must generate clock and data signals in SPI MODE0 (clock polarity CPOL = 0 and clock phase CPHA = 0) to communicate with the MAX22513 in SPI mode. The SPI interface is not available when V_5 falls below 4.25V or when V_L is below 2.5V.

SPI Full-Duplex

SPI communication with the MAX22513 is full-duplex by default. Connect SCLK to the clock output of the microcontroller, $\overline{CS}$/A0 to the SS pin (or to a GPO), SDI/A1 to the MOSI output, and SDO/SDA to the MISO input in this mode. Figure 7 shows a single-cycle SPI write command and Figure 8 shows a single-cycle SPI read command in full-duplex mode.

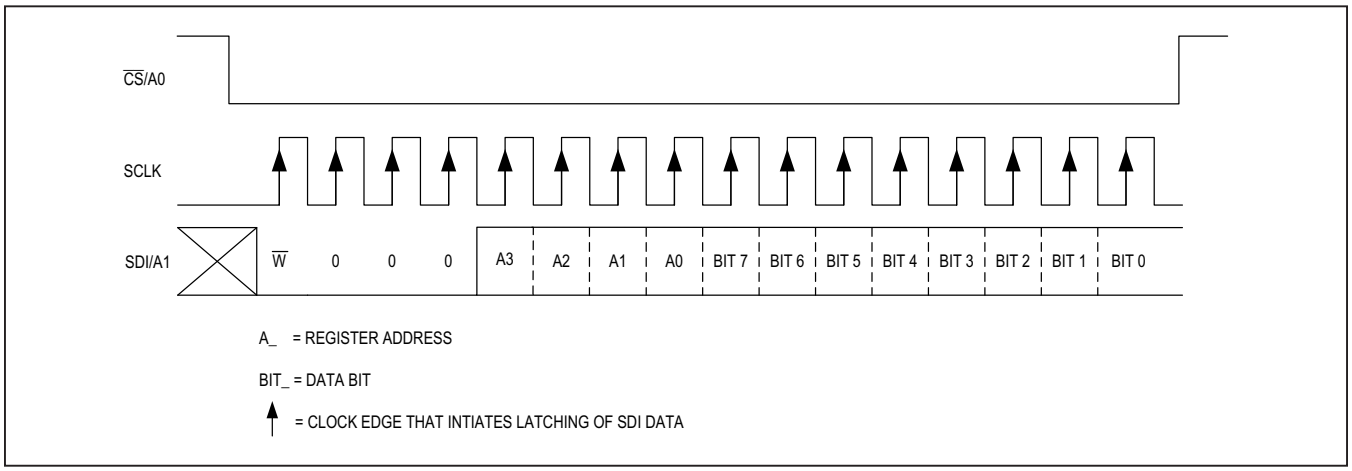


Figure 8. SPI Byte Write

Half-Duplex SPI Communication

Set the SPIHDX bit in the MODE register to enable half-duplex SPI communication. In this configuration, connect SDI/A1 to ground. Ensure that the SPI master supports half-duplex SPI. This commonly entails using open-drain outputs on MOSI.

A SPI half-duplex write byte command is the same as a full-duplex write command (Figure 8). In a read command, the master sends the read command and register address on the SDO/SDA line. The master then sends another 8 clock signals and reads the register information on the SDO/SDA line. Figure 10 shows a half-duplex read command.

I²C Interface

The MAX22513 includes an I²C-compatible interface for data communication with a host processor (SCLK and SDO/SDA). The interface supports Fast Mode Plus with a clock frequency up to 1MHz. SCLK and SDO/SDA require pullup resistors to V_L or V_{CCB} for I²C communication.

The MAX22513 supports both burst and single-byte read and write functionality.

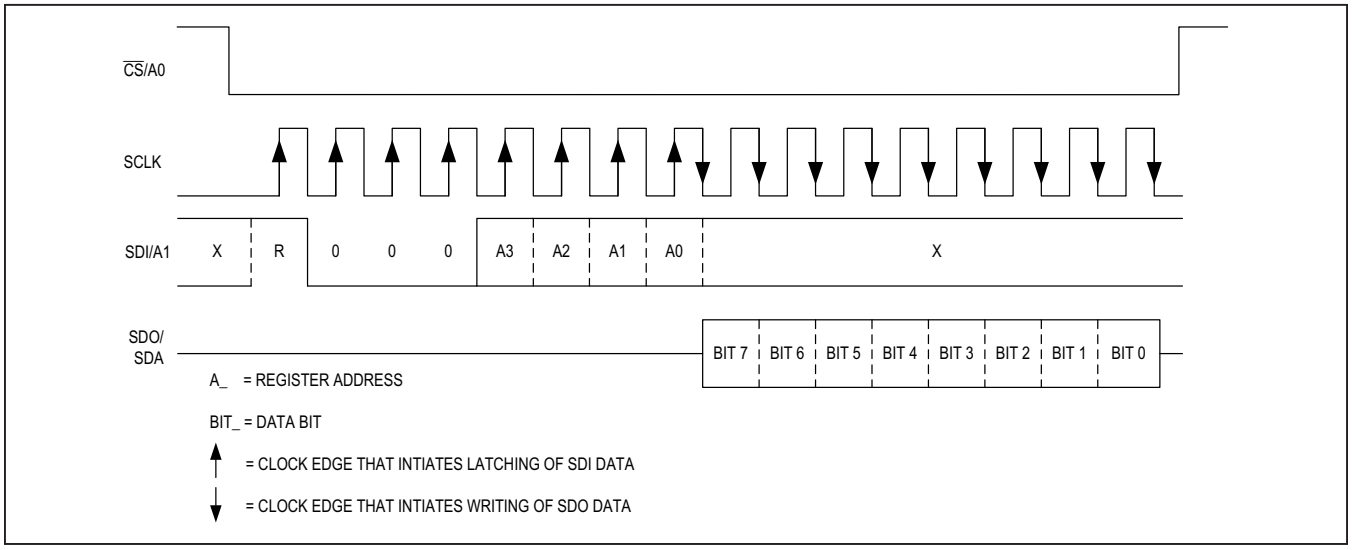


Figure 9. SPI Byte Read

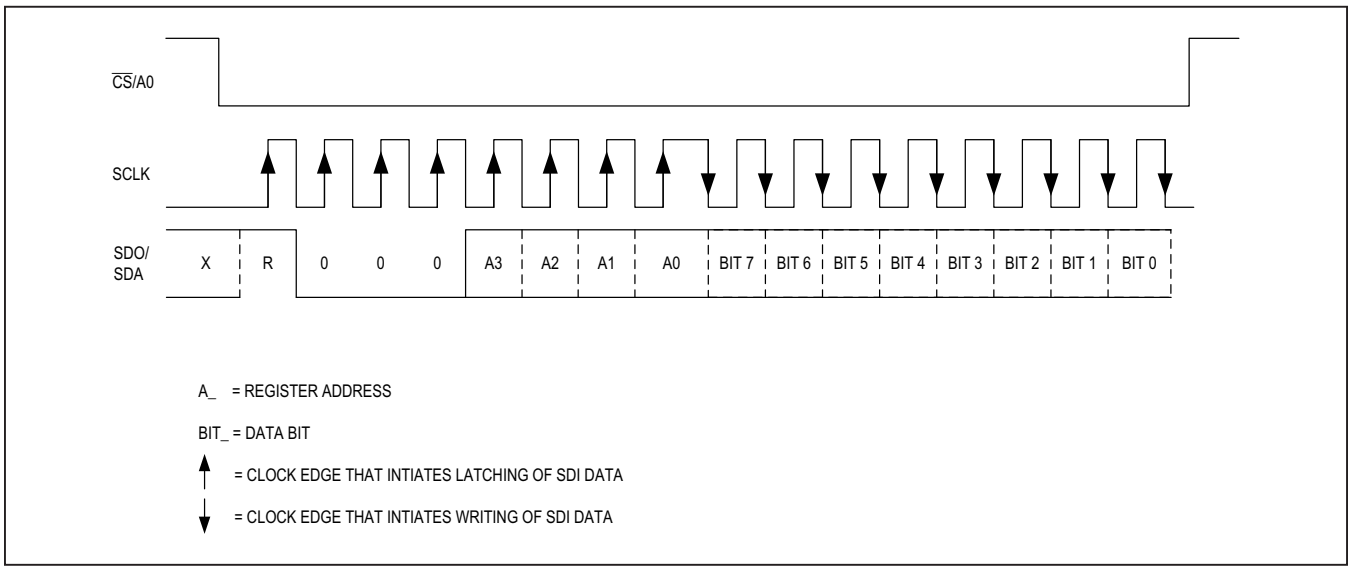


Figure 10. Half-Duplex SPI Byte Read

I²C Slave Address

The MAX22513 features two pins: SDI/A1 and $\overline{CS}$/A0 to set the 7-bit slave address for I²C communication. The first 5 bits (MSBs) of the slave address are factory-programmed and always 01101. Connect SDI/A1 and $\overline{CS}$/A0 to ground or V_L to set the I²C slave address (Table 2). The address is defined as the 7 MSBs followed by the read/write bit. Set the read/write bit to 1 to configure the MAX22513 to read mode. Set the read/write bit to 0 to configure the device for write mode. The address is the first byte of information sent to the device after the START condition.

I²C Byte Write

With this operation the master sends an address and 1 or 2 data bytes to the slave device (Figure 11). The write byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The active slave asserts an ACK on the data line only if the address is valid (NACK if not).
6) The master sends the 8-bit data byte.
7) The slave asserts an ACK on the data line.
8) The master generates a STOP condition.

Table 2. I²C Address Map

SDI/A1	$\overline{CS}$/A0	READ/WRITE	I²C ADDRESS
0	0	W	0x68
		R	0x69
0	1	W	0x6A
		R	0x6B
1	0	W	0x6C
		R	0x6D
1	1	W	0x6E
		R	0x6F

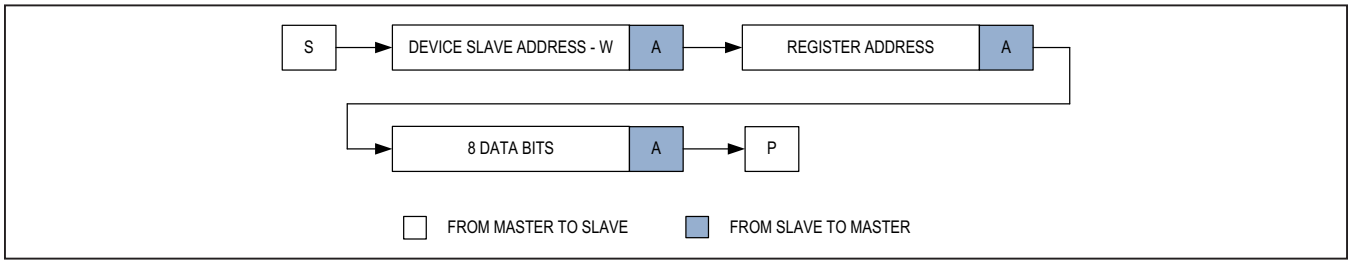


Figure 11. I²C Byte Write

I²C Byte Read

With this operation the master sends an address and receives 1 or 2 data bytes from the slave device (Figure 12). The read byte procedure is as follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends the 8-bit register address.
5) The active slave asserts an ACK on the data line only if the address is valid (NACK if not).
6) The master sends a repeated START (Sr).
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The slave asserts an ACK on the data line.
9) The slave sends 8 data bits.
10) The master asserts a NACK on the data line.
11) The master generates a STOP condition.

SDA Stuck Protection

A stuck bus occurs in I²C communication when a slave receives some communication, but does not receive a stop (P) or repeated start (Sr) that signals to the slave to release the bus. When this happens, the data line (SDO/SDA) is held low by the slave and no further communication can occur on the bus until it is released. The MAX22513 features an internal timer that monitors the SDO/SDA data line to protect against this situation. If SDO/SDA is held low for more than 1.1ms (typ), the MAX22513 releases the SDO/SDA line high, resuming normal communication. This bus protection limits the minimum I²C clock frequency to 10kHz.

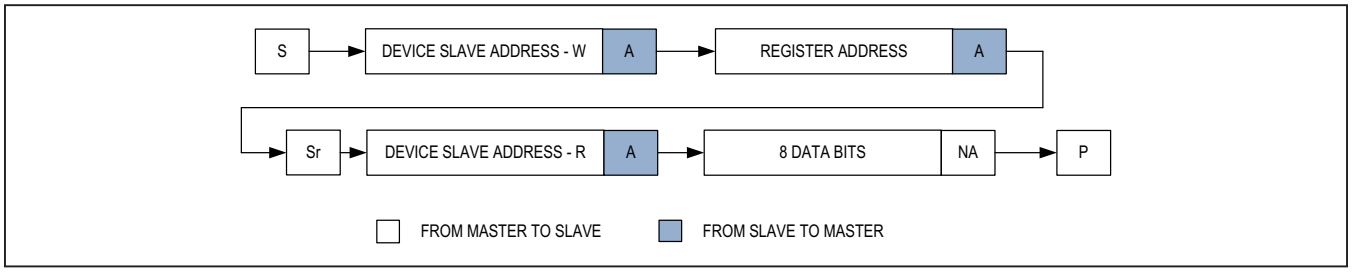


Figure 12. I²C Byte Read

Register Map

ADDRESS	NAME	TYPE	POR (DEFAULT)	7 (MSB)	6	5	4	3	2	1	0 (LSB)
0x00	INTERRUPT[7:0]	COR	80h	NOTREADY	WUINT	DOFAULTINT	CQFAULTINT	V24WINT	UV24INT	—	THERMWINT
0x01	IRQMASK[7:0]	RW	00h	–	WUM	DOFAULTM	CQFAULTM	V24WM	UV24M	—	THERMWM
0x02	STATUS[7:0]	R	00h	CQLVL	DILVL	DOFAULT	CQFAULT	V24WARN	UV24	—	TEMPW
0x03	STATUS2[7:0]	MIXED	01h	CORR_REG	–	–	–	–	–	BUCKFAULT	BUCKOK
0x04	MODE[7:0]	RW	00h	RST	SPIHDX	CQDOPAR	DO_AV	BUCKDCM	BUCKPFM	BUCKSS	BUCKDIS
0x05	CURRLIM[7:0]	RW	00h	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTO RETRYEN
0x06	CONTROL[7:0]	RW	00h	LDO33DIS	WUDIS	DIDIS	DIFILTER	RXDIS	RXFILTER	DO_Q	CQ_Q
0x07	CQCONFIG[7:0]	RW	00h	CQLOSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
0x08	DOCONFIG[7:0]	RW	00h	DOLOSLEW[1:0]		DO_PD	DO_PU	DO_NPN	DO_PP	INVDO	DO_EN
0x09	CLKCONFIG[7:0]	RW	00h	ENCLKTRIM	–	–	–	–	CLKDIV[1:0]		MCLKDIS
0x0A	CKTRIM[7:0]	RW	00h	–	–	CKTRIM[5:0]					
0x0C	CHIPID[7:0]	R	12h	CHIPID[7:0]							

"–" = *Unused and reserved for future use*
R = Read only.
RW = Read and Write
COR = Clear on Read
MIXED = Some bits are Write and Clear; others are Read and Write. See bit descriptions for details.

Register Details

INTERRUPT (0x00)

The $\overline{IRQ}$ output asserts when any of the bits in the INTERRUPT register are set and the interrupt is not masked. Read the INTERRUPT register to clear the bits and deassert $\overline{IRQ}$, once the fault condition has been removed.

BIT	7	6	5	4	3	2	1	0
Field	NOTREADY	WUINT	DOFAULTINT	CQFAULTINT	V24WINT	UV24INT	—	THERMWINT
Reset	1	0	0	0	0	0	0	0
Access Type	Clear on Read	Clear on Read	Clear on Read	Clear on Read	Clear on Read	Clear on Read	Clear on Read	Clear on Read

BITFIELD	BITS	DESCRIPTION
NOTREADY	7	0 = The MAX22513 is operating normally 1 = Any of the following conditions has occurred since the last INTERRUPT register read: • The V_5 supply voltage dropped below its UVLO and the registers were reset. • A power-up occurred and the registers have been reset. • At least one register has been corrupted due to an external event (not POR). The NOTREADY interrupt cannot be masked.
WUINT	6	0 = No wake-up condition has been detected. 1 = An IO-Link wake-up condition has been detected on the C/Q line since the last INTERRUPT register read.
DOFAULTINT	5	0 = DO/DI driver operating normally 1 = Overcurrent/overload condition or driver thermal shutdown has occurred on DO/DI driver since last INTERRUPT register read.
CQFAULTINT	4	0 = C/Q driver operating normally. 1 = Overcurrent/overload condition or driver thermal shutdown has occurred on the C/Q driver since the last INTERRUPT register read.
V24WINT	3	0 = V_{24} is above 16V (typ). 1 = V_{24} voltage has fallen below 16V (typ) since the last INTERRUPT register read.
UV24INT	2	0 = V_{24} is above the 7.6V (typ) undervoltage threshold (UVLO). 1 = The V_{24} voltage has fallen below the the 7.0V (typ) undervoltage threshold since the last INTERRUPT register read. Note that UV24INT is set only when the DC-DC is disabled (BUCKDIS = 1) and V_{24} is below the UVLO threshold. If BUCKDIS = 0 when V_{24} is below 7.0V (typ), $\overline{RESET}$ asserts and clears all registers.
THERMWINT	0	0 = The MAX22513 temperature has not risen above the warning temperature threshold. 1 = The MAX22513 temperature has risen above the warning temperature threshold since the last INTERRUPT register read.

IRQMASK (0x01)

Set the bits in the IRQMASK register to ignore selected events or fault notifications. $\overline{IRQ}$ does not assert when any of the masked bits in the INTERRUPT register is set. Bits in the INTERRUPT register are not affected by the bits in the IRQMASK register, and are set when the associated event or fault notification occurs.

BIT	7	6	5	4	3	2	1	0
Field	–	WUM	DOFAULTM	CQFAULTM	V24WM	UV24M	—	THERMWM
Reset	0	0	0	0	0	0	0	0
Access Type	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write

BITFIELD	BITS	DESCRIPTION
WUM	6	0 = $\overline{IRQ}$ asserts when the WUINT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the WUINT bit in the INTERRUPT register is set.
DOFAULTM	5	0 = $\overline{IRQ}$ asserts when the DOFAULT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the DOFAULT bit in the INTERRUPT register is set.
CQFAULTM	4	0 = $\overline{IRQ}$ asserts when the CQFAULT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the CQFAULT bit in the INTERRUPT register is set.
V24WM	3	0 = $\overline{IRQ}$ asserts when the V24WINT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the V24WINT bit in the INTERRUPT register is set.
UV24M	2	0 = $\overline{IRQ}$ asserts when the UV24INT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the UV24INT bit in the INTERRUPT register is masked.
THERMWM	0	0 = $\overline{IRQ}$ asserts when the THERMWINT bit in the INTERRUPT register is set. 1 = $\overline{IRQ}$ does not assert when the THERMWINT bit in the INTERRUPT register is set.

STATUS (0x02)

Bits in the STATUS register indicate the current status of the MAX22513. Bits in the STATUS register are set or cleared when an event occurs and are not cleared when the register is read.

BIT	7	6	5	4	3	2	1	0
Field	CQLVL	DILVL	DOFAULT	CQFAULT	V24WARN	UV24	—	TEMPW
Reset	0	0	0	0	0	0	0	0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CQLVL	7	0 = C/Q is high. 1 = C/Q is low.
DILVL	6	0 = DO/DI is high. 1 = DO/DI is low.
DOFAULT	5	0 = No fault on DO/DI driver. 1 = Overcurrent or thermal overload fault on DO/DI driver.
CQFAULT	4	0 = No fault on C/Q driver. 1 = Overcurrent or thermal overload fault on C/Q driver.
V24WARN	3	0 = V_{24} is above the 16V (typ) warning threshold. 1 = V_{24} is below the 16V (typ) warning threshold.
UV24	2	0 = V_{24} is above the 7.6V (typ) rising undervoltage lockout (UVLO) threshold. 1 = V_{24} is below the 7.0V (typ) falling UVLO threshold.
TEMPW	0	0 = The die temperature is below the 138°C (typ, falling) warning threshold temperature. 1 = The die temperature is above the 147°C (typ, rising) warning threshold temperature.

STATUS2 (0x03)

Bits in the STATUS2 register indicate the current status of the MAX22513 registers and the DC-DC regulator operation. Bits in the STATUS2 register are set or cleared when an event occurs and are not cleared when the register is read.

BIT	7	6	5	4	3	2	1	0
Field	CORR_ REG	–	–	–	–	–	BUCKFAULT	BUCKOK
Reset	0	–	–	–	–	–	0	1
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CORR_REG	7	0 = All register values are correct. 1 = Register values are corrupted. C/Q and DO/DI are disabled and RX and LO/LI are high impedance when CORR_REG = 1. V_{33} and DC-DC are also forced on and the signal at MCLK is enabled and switching at 3.686MHz.
BUCKFAULT	1	0 = DC-DC is operating normally. No fault conditions are present. 1 = Fault condition is present on the DC-DC regulator. Fault conditions include output overcurrent/overload, the output voltage falls below 70% of the set voltage, and when the regulator is in hiccup mode.
BUCKOK	0	0 = DC-DC regulator is not ready or has a fault condition. 1 = DC-DC regulator is operating normally in the steady-state condition and is ready to be used. BUCKOK = 1 when BUCKDIS = 1.

MODE (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RST	SPIHDX	CQDOPAR	DO_AV	BUCKDCM	BUCKPFM	BUCKSS	BUCKDIS
Reset	0	0	0	0	0	0	0	0
Access Type	Write and Clear*	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write

BITFIELD	BITS	DESCRIPTION
RST	7	0 = Registers are not in reset state. 1 = Set all registers to their default state. RST clears automatically.
SPIHDX	6	0 = SPI communication is full-duplex. 1 = Enable half-duplex SPI communication. In half-duplex SPI, the SDO output is not used.
CQDOPAR	5	0 = The DO/DI driver operates independently of C/Q. 1 = The DO/DI driver tracks the C/Q driver. In this configuration, both DO/DI and C/Q switch as a function of TX and/or the CQ_Q bit. CQDOPAR must be set when DO_AV = 1.
DO_AV	4	0 = Antivalent operation is not enabled. C/Q and DO/DI switch independently. 1 = Antivalent operation is enabled. C/Q and DO/DI drivers switch as a function of the TX input and/or the CQ_Q bit, but with opposite logic. CQDOPAR must be set to enable this functionality.
BUCKDCM	3	0 = The DC-DC regulator operates in PFM mode (BUCKPFM = 1) or PWM mode (BUCKPFM = 0) after soft-start is complete. See the BUCKPFM bit setting. 1 = The DC-DC regulator operates in DCM mode after soft-start is complete.
BUCKPFM	2	0 = The DC-DC regulator operates in PWM mode (BUCKDCM = 0) or DCM mode (BUCKDCM = 1). 1 = The DC-DC regulator operates in PFM mode.
BUCKSS	1	0 = Spread spectrum operation is not enabled on the DC-DC regulator. 1 = Spread spectrum operation is enabled on the DC-DC regulator.
BUCKDIS	0	0 = DC-DC regulator is enabled. 1 = DC-DC regulator is disabled. BUCKOK = 1 when BUCKDIS = 1.

**"Write Only" executes and clears all bits in all MAX22513 Registers to their default values, and sets the RST bit back to 0 in the MODE Register.*

CURRLIM (0x05)

BIT	7	6	5	4	3	2	1	0
Field	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTORETRYEN
Reset	00		0	00		00		0
Access Type	Read and Write		Read and Write	Read and Write		Read and Write		Read and Write

BITFIELD	BITS	DESCRIPTION
CL	7:6	CL[1:0] bits set the active current limit levels for the C/Q and DO/DI drivers when CLDIS = 0. 00 = 50mA (min) current limit 01 = 100mA (min) current limit 10 = 200mA (min) current limit 11 = 250mA (min) current limit
CLDIS	5	0 = C/Q and DO/DI driver current limits are enabled. Current limits are set by the CL[1:0] bits. 1 = C/Q and DO/DI driver current limits are disabled.
CL_BL	4:3	CL_BL[1:0] set the blanking time for the C/Q and DO/DI drivers. 00 = 128µs 01 = 500µs 10 = 1ms 11 = 5 ms
TAR	2:1	The TAR[1:0] bits set the fixed off-time for the C/Q and DO/DI drivers after a fault has been generated and auto-retry functionality is enabled (AUTORRETRYEN = 1). The driver is automatically re-enabled after the fixed off-delay. 00 = 50ms 01 = 100ms 10 = 200ms 11 = 500ms
AUTORETRYEN	0	0 = Autoretry is disabled on the C/Q and DO/DI drivers. 1 = Autoretry is enabled on the C/Q and DO/DI drivers. When a fault is signaled on the driver, the driver is disabled for the selected fixed off time and then automatically reenabled.

CONTROL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	LDO33DIS	WUDIS	DIDIS	DIFILTER	RXDIS	RXFILTER	DO_Q	CQ_Q
Reset	0	0	0	0	0	0	0	0
Access Type	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write

BITFIELD	BITS	DESCRIPTION
LDO33DIS	7	0 = V_{33} linear regulator is enabled. 1 = V_{33} linear regulator is disabled.
WUDIS	6	0 = IO-Link wake-up detection is enabled. 1 = IO-Link wake-up detection is disabled.
DIDIS	5	0 = DO/DI receiver is enabled. 1 = DO/DI receiver is disabled. LO/LI is low if DIDIS = 1. DO/DI input current is reduced when DIDIS = 1. DILVL = 0 when DIDIS = 1.
DIFILTER	4	0 = The 1µs (typ)glitch filter on the DO/DI receiver is disabled. 1 = The 1µs (typ) glitch filter on the DO/DI receiver is enabled.
RXDIS	3	0 = RX logic output is enabled. 1 = RX logic output is disabled. RX is high impedance. C/Q input current is reduced when RXDIS = 1. CQLVL = 0 when RXDIS = 1.
RXFILTER	2	0 = The 1µs (typ) glitch filter on the C/Q receiver is disabled. 1 = The 1µs (typ) glitch filter on the C/Q receiver is enabled.
DO_Q	1	Use the DO_Q bit to control the DO/DI driver output. See Table 3 for more information.
CQ_Q	0	Use the CQ_Q bit to control the C/Q driver output. See Table 4 for more information.

CQCONFIG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	CQLOSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
Reset	00		0	0	0	0	0	0
Access Type	Read and Write		Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write

BITFIELD	BITS	DESCRIPTION
CQLOSLEW	7:6	The CQLOSLEW[1:0] bits set the typical rising and falling slew rates on the C/Q driver. 00 = 250ns 01 = 500ns 10 = 1.25µs 11 = 5µs
CQ_PD	5	0 = The 300µA (typ) weak pull-down current sink on the C/Q driver is disabled. 1 = The 300µA (typ) weak pull-down current sink on the C/Q driver is enabled.
CQ_PU	4	0 = The 300µA (typ) weak pull-up current source on the C/Q driver is disabled. 1 = The 300µA (typ) weak pull-up current source on the C/Q driver is enabled.
CQ_NPN	3	0 = The C/Q driver is in PNP mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1). 1 = The C/Q driver is in NPN mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1).
CQ_PP	2	0 = The C/Q driver is in PNP mode (CQ_NPN = 0) or NPN mode (CQ_NPN = 1). 1 = The C/Q driver is in push-pull mode.
INVCQ	1	0 = C/Q logic is inverted compared to TX and RX. 1 = C/Q logic is the same as TX and RX.
CQ_EN	0	0 = C/Q driver is disabled. 1 = C/Q driver is enabled.

DOCONFIG (0x08)

BIT	7	6	5	4	3	2	1	0
Field	DOLOSLEW[1:0]		DO_PD	DO_PU	DO_NPN	DO_PP	INVDO	DO_EN
Reset	00		0	0	0	0	0	0
Access Type	Read and Write		Read and Write	Read and Write	Read and Write	Read and Write	Read and Write	Read and Write

BITFIELD	BITS	DESCRIPTION
DOLOSLEW	7:6	The DOLOSLEW[1:0] bits set the typical rising and falling slew rates on the DO/DI driver. 00 = 250ns 01 = 500ns 10 = 1.25µs 11 = 5µs
DO_PD	5	0 = The 300µA (typ) weak pulldown current sink on the DO/DI driver is disabled. 1 = The 300µA (typ) weak pulldown current sink on the DO/DI driver is enabled.
DO_PU	4	0 = The 300µA (typ) weak pullup current source on the DO/DI driver is disabled. 1 = The 300µA (typ) weak pullup current source on the DO/DI driver is enabled.
DO_NPN	3	0 = The DO/DI driver is in PNP mode (DO_PP = 0) or push-pull mode (DO_PP = 1). 1 = The DO/DI driver is in NPN mode (DO_PP = 0) or push-pull mode (DO_PP = 1).
DO_PP	2	0 = The DO/DI driver is in PNP mode (DO_NPN = 0) or NPN mode (DO_NPN = 1). 1 = The DO/DI driver is in push-pull mode.
INVDO	1	0 = DO/DI logic is inverted compared to LO/LI and the DO_Q bit. 1 = DO/DI logic is the same as LO/LI and the DO_Q bit.
DO_EN	0	0 = DO/DI driver is disabled. DO/DI receiver is enabled. LO/LI is an output. 1 = DO/DI driver is enabled. DO/DI receiver is disabled. LO/LI is an input.

CLKCONFIG (0x09)

BIT	7	6	5	4	3	2	1	0
Field	ENCLKTRIM	–	–	–	–	CLKDIV[1:0]		MCLKDIS
Reset	0	–	–	–	–	00		0
Access Type	Read and Write	–	–	–	–	Read and Write		Read and Write

BITFIELD	BITS	DESCRIPTION
ENCLKTRIM	7	0 =Fine trimming of the MCLK frequency is disabled. 1 = Fine trimming of the MCLK frequency is enabled. See the CKTRIM register.
CLKDIV	2:1	The CLKDIV[1:0] bits set the internal clock divider ratio. 00 = MCLK frequency is 3.686MHz 01 = MCLK frequency is 7.373MHz 10 = MCLK frequency is 14.74MHz 11 = MCLK frequency is 1.843MHz
MCLKDIS	0	0 = MCLK is enabled. 1 = MCLK is disabled. MCLK is not high impedance when MCLKDIS = 1.

CKTRIM (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CKTRIM[5:0]					
Reset			000000					
Access Type	Read and Write		Read and Write					

BITFIELD	BITS	DESCRIPTION
CKTRIM	5:0	The CKTRIM[5:0] bits are used to trim the internally generated clock frequency. The bits are binary coded, centered to 0. Range is from +0.7% for -32, 0% for 0, and -5.5% for +31.

CHIPID (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	CHIPID[7:0]							
Reset	0001 0010							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CHIPID	7:0	The CHIPID[7:0] bit identifies the revision of the MAX22513.

Applications Information

Table 3. DO/DI Control

DO_EN	LO/LI	DO_Q	DO/DI		
			NPN MODE	PNP MODE	PP MODE
0	OUTPUT	X	DO/DI DRIVER IS DISABLED. DO/DI IS CONFIGURED AS AN INPUT		
1	L	0	Z	H	H
		1	Z	H	H
	H	0	L	Z	L
		1	Z	H	H

Table 4. C/Q Control

CQ_EN	TXEN	TX	CQ_Q	C/Q		
				NPN MODE	PNP MODE	PP MODE
0	X	X	X	C/Q IS CONFIGURED AS A RECEIVER	Z	Z
1	L	X	X	Z	Z	Z
	H	L	0	Z	H	H
			1	Z	H	H
		H	0	L	Z	L
			1	Z	H	H

X = Don't Care, Z = High Impedance

MCLK Microcontroller Clocking

The MCLK output produces a clock suitable for IO-Link communication that can be used for UART clocking.

Select the frequency of the MCLK output by setting the CLKDIV[1:0] bits in the CLKCONFIG register. Available MCLK frequencies are 14.745MHz, 7.373MHz, 3.686MHz, or 1.843MHz.

The MCLK oscillator is enabled by default and the switching frequency is 3.686MHz. MCLK voltage output levels are referenced to the V_L logic supply.

Use the CKTRIM register to fine tune the MCLK frequency if needed.

EMC Protection

The MAX22513 features integrated surge protection of ±1kV/500Ω for 8µs/20µs surge line-to-line and line-to-ground on the C/Q, DO/DI, V_{24}, and GND pins.

External TVS diodes are required to meet higher levels of surge protection. Ensure that the TVS diode peak clamping voltage is within the *Absolute Maximum Ratings* voltage ratings.

Power Dissipation and Thermal Considerations

Ensure that the total power dissipation in the MAX22513 is less than the limit in the *Absolute Maximum Ratings*. Total power dissipation for the MAX22513 is calculated using the following equation:

$$P_{TOTAL} = P_Q + P_{V5} + P_{V33} + P_{C/Q} + P_{DO}$$

where:

P_Q = Quiescent power generated in MAX22513,

$P_{C/Q}$ = Power generated in the C/Q driver,

P_{DO} = Power dissipated by the DO/DI driver,

P_{V33} and P_{V5} = Power generated by the internal linear regulators

Quiescent power dissipated in the MAX22513 is calculated as:

$$P_Q = [I_{24} \times V_{24}(max)] + [I_5 \times V_5]$$

Power dissipated in the C/Q driver is calculated as:

$$P_{C/Q} = I_{C/Q}(max)^2 \times R_{ON}$$

$I_{C/Q}$ is the load current driven by the C/Q driver and R_{ON} is the driver on-resistance.

Power dissipated in the DO/DI driver is calculated as:

$$P_{DO} = I_{DO}(max)^2 \times R_{ON}$$

I_{DO} is the load current driven by the DO/DI driver and R_{ON} is the driver on-resistance.

Power dissipated in the 5V linear regulator (V_5) is calculated as:

$$P_{V5} = (V_{LIN} - V_5) \times I_{5LOAD}$$

I_{5LOAD} includes both the load current on the V_5 regulator and the 3.3V regulator.

Power dissipated in the 3.3V linear regulator (V_{33}) is calculated as:

$$P_{V33} = 1.7V \times I_{33LOAD}$$

I_{33LOAD} is the load on the 3.3V regulator.

Layout and Grounding

Layout for the MAX22513 is important to ensure that all parts operate normally and with minimal interference.

The MAX22513 features three ground pins: GND, DGND, and SGND.

Bypass all supply pins (V_5, V_L, and PV24) to the GND pin and connect directly to a ground plane. Bypass capacitors should be placed as close to the IC as possible.

Connect the SGND directly to the ground plane.

The V_{24}, C/Q, DO/DI and DGND pins are connected directly to the IO-Link connector. Connect all bypass capacitors and other components on this line directly to the DGND. Connect the DGND to the ground layer at the IC (at the exposed pad for the TQFN or under pad D8 on the WLP package).

Keep the component loop for the DC-DC buck regulator as small as possible. Ensure that the feedback resistor divider is not near the inductor. Connect the ground terminal of the DC-DC output capacitor to the ground plane with multiple vias.

Figure 13 shows an example of layout and grounding connections.

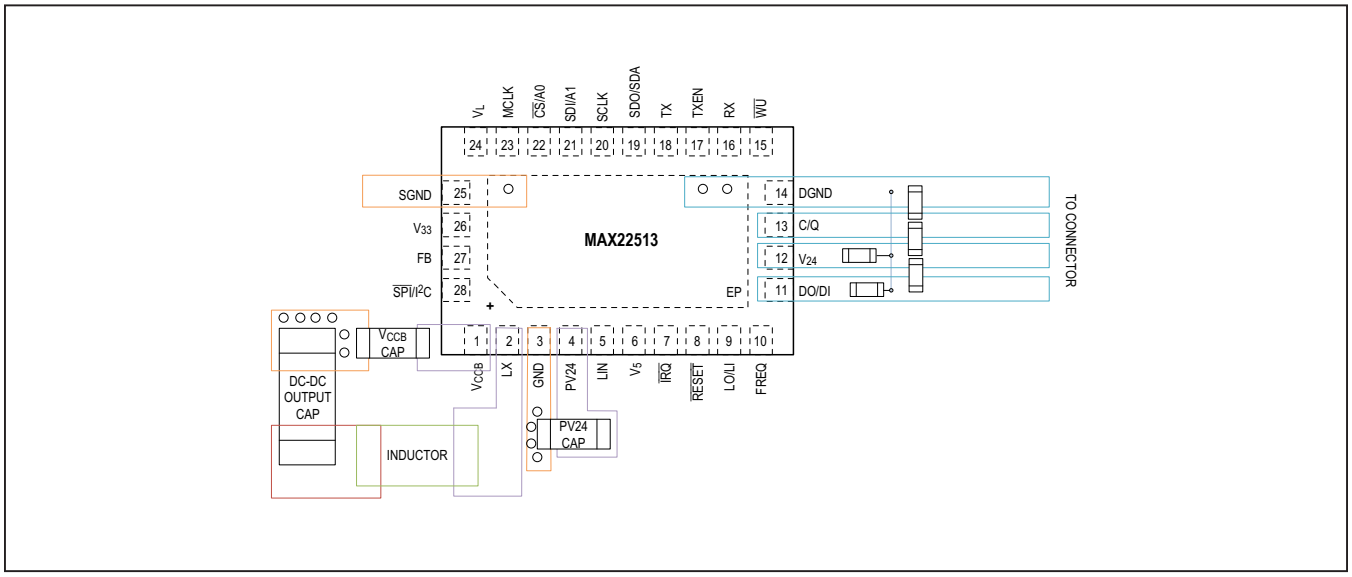
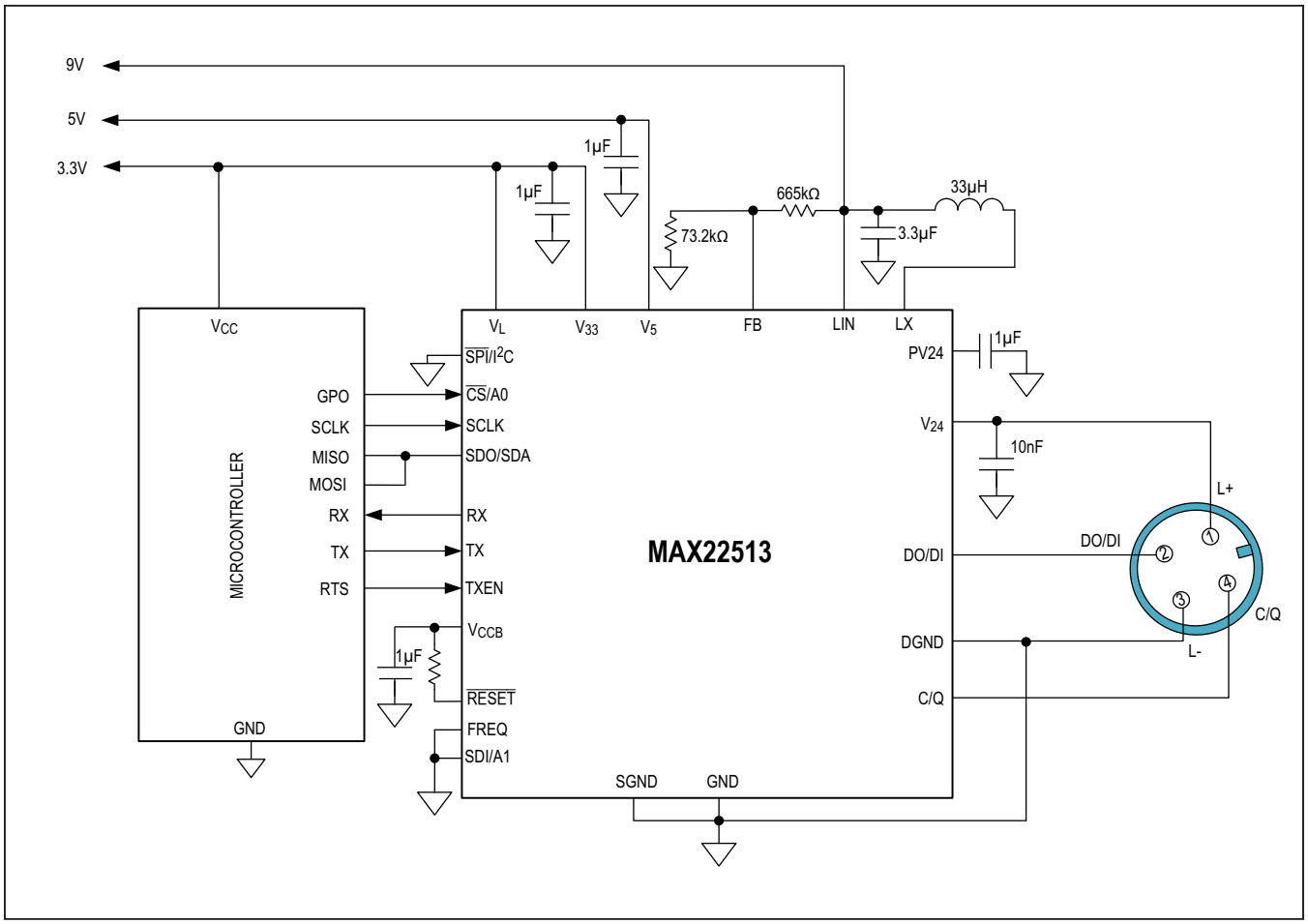


Figure 13. Sample Grounding Scheme (TQFN Package)

Typical Application Circuits

Half-Duplex SPI Interface Application with 9V/150mA DC-DC Output (12V, min Input)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	BALL PITCH
MAX22513ATI+	-40°C to +125°C	28 TQFN-EP*	—
MAX22513ATI+T	-40°C to +125°C	28 TQFN-EP*	—
MAX22513AWJ+	-40°C to +125°C	32 WLP	0.5mm
MAX22513AWJ+T	-40°C to +125°C	32 WLP	0.5mm

**EP = Exposed pad.*
T = Tape and reel.