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Surge Protected IO-Link Transceiver with DC-DC

MAX22514

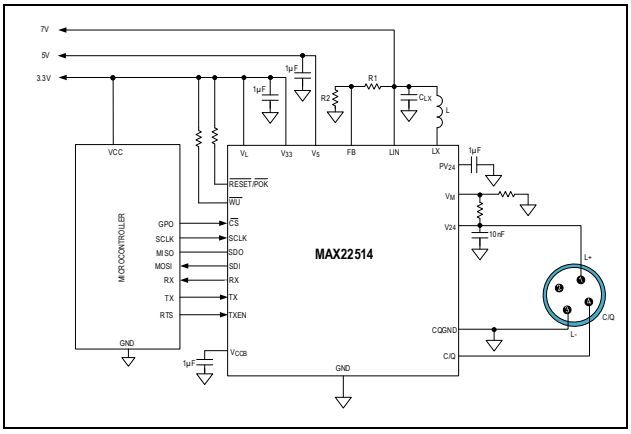
Product Highlights

- High Configurability and Integration
  - IO-Link Device and Master Applications
  - COM1, COM2, and COM3 Data Rates
  - Integrated High-Efficiency 200mA DC-DC Buck Regulator
  - 200µA/2mA/5mA Current Sinks/Sources
  - C/Q Receiver is Configurable for 5V TTL
  - Highly Configurable Driver Overload Handling
  - Four Selectable Driver Slew Rates
  - SPI Configuration and Monitoring
  - Integrated Temperature Sensor
  - Configurable C/Q Driver: PNP, NPN, and PP Modes
- Integrated Protection Enables Robust Systems
  - Integrated ±1kV/500Ω Surge Protection
  - Spread Spectrum DC-DC
  - Reverse Polarity Protection
  - Glitch Filter for Improved Burst Resilience
  - Hot-Plug Protection
- Optimized for Small Sensor Designs
  - Accurate Oscillator for IO-Link Communication
  - 2.4Ω (typ) Driver On-Resistance for Low Power Dissipation
  - 1.2MHz DC-DC Switching Rate
  - Integrated 3.3V and 5V Linear Regulators
  - Available in Tiny WLP (2.5mm x 2.6mm) and TQFN (4mm x 5mm) Packages

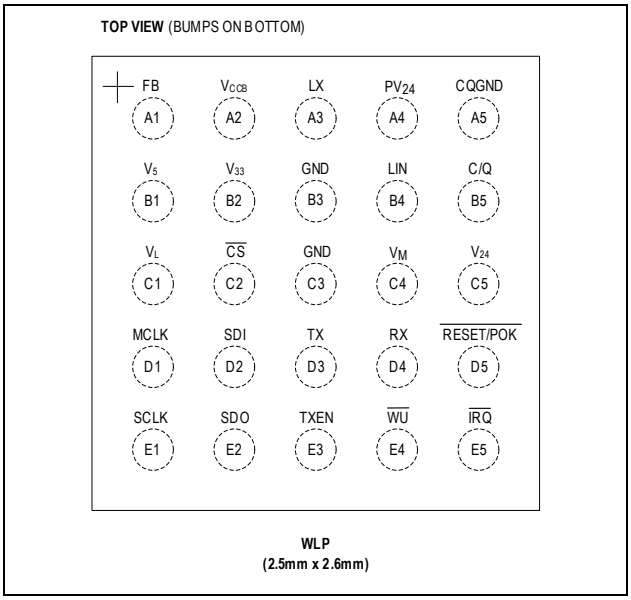
Key Applications

- IO-Link and Industrial Sensor and Actuator Devices
- The MAX22514 features a SPI interface for configuration and diagnostics. A high level of integration (including two linear regulators, a DC-DC buck regulator, and integrated surge protection, combined with low power dissipation and small packages) optimizes the MAX22514 for use in many different industrial and IO-Link small sensor applications.
- IO-Link Master Transceivers
  The MAX22514 is capable of being used in both IO-Link devices and IO-Link master applications. A SPI interface is used for extended configurability and diagnostics, and the transceiver is capable of operating at the COM1, COM2, and COM3 IO-Link data rates. The MAX22514 can be configured to enable the required 5mA pull-down/pull-up current on the C/Q line and generate a wake-up pulse.

Simplified Application Diagram



Pin Configuration



See more *Who should use this part.*

***Ordering Information* appears at end of data sheet.**

19-101287; Rev 1; 2/22

Absolute Maximum Ratings

All voltages referenced to GND, unless otherwise noted.

V_{24} (Continuous) ..... -36V to +36V

V_{24} (Peak, 100µs) ..... -52V to +65V

PV_{24} (Continuous) ..... -0.3V to +36V

PV_{24} (Peak, 100µs) MAX(-0.3V, V_{24} - 52V) to MIN(+52V, V_{24} + 52V)

LX ..... -0.3V to (PV_{24} + 0.3V)

LIN (Continuous) ..... MAX(-0.3V, V_5 - 0.3V) to +36V

LIN (Peak, 100µs) ..... MAX(-0.3V, V_5 - 0.3V) to +52V

C/Q (Continuous) MAX(-36V, V_{24} - 36V) to MIN(+36V, V_{24} + 36V)

C/Q (Peak, 100µs) MAX(-52V, V_{24} - 60V) to MIN(+52V, V_{24} + 60V)

V_M, FB, V_{CCB}, RESET/POK ..... -0.3V to +6V

V_5, V_L ..... -0.3V to +6V

V_{33} ..... -0.3V to (V_5 + 0.3V)

LOGIC INPUTS

CS, SCLK, SDI, TX, TXEN ..... -0.3V to (V_L + 0.3V)

LOGIC OUTPUTS

SDO, RX, MCLK ..... -0.3V to (V_L + 0.3V)

IRQ, WU ..... -0.3V to +6V

CQGND ..... -0.3V to +0.3V

Continuous Current into V_{24}, LX, GND, or CQGND ..... ±1A

Continuous Current into PV_{24} ..... ±200mA

Peak Current into PV_{24} (100µs) ..... ±1A

Continuous Current into C/Q ..... ±500mA

Continuous Current into Any Other Pin ..... ±50mA

Continuous Power Dissipation

24-pin TQFN (T_A = +70°C, derates at 28.6mW/°C above +70°C) 2285.7mW

25-bump WLP (T_A = +70°C, derates at 22.74mW/°C above +70°C) 1819mW

Operating Temperature Range ..... -40°C to +125°C

Maximum Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (Reflow) (TQFN only, soldering, 10 seconds) ..... +300°C

Bump Reflow Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN	
Package Code	T2445+2C
Outline Number	*21-0201*
Land Pattern Number	*90-0083*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	35°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.8°C/W

25 WLP	
Package Code	W252V2+1
Outline Number	*21-100546*
Land Pattern Number	Refer to *App Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	43.98°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
POWER SUPPLY							
V_{24} Supply Voltage	V_{24}			8		36	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising		7	7.5	8	V
		V_{24} falling		6.3	7	7.6	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}				500		mV
V_{24} Supply Current	I_{24}	No load on C/Q, V_5 powered externally, DC-DC disabled, MCLK disabled	C/Q disabled, V_{33} enabled		0.04	0.075	mA
			C/Q in push-pull, and is high or low		0.32	0.45	
		V_5 powered externally, DC-DC enabled, MCLK enabled	C/Q in push-pull and is high or low		1.95		
V_5 Supply Voltage	V_5	V_5 supplied externally		4.5		5.5	V
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 rising		3.98		4.26	V
		V_5 falling		3.92		4.19	
V_5 Supply Current	I_5	V_5 powered externally, DC-DC disabled, MCLK disabled, V_{33} enabled, no load on V_{33}	C/Q disabled		0.85	1.1	mA
		V_5 powered externally, DC-DC disabled, MCLK disabled, V_{33} enabled, no load on V_{33}	C/Q in push-pull mode, no load on C/Q		1.13	1.5	
		V_5 powered externally, DC-DC disabled, MCLK enabled and set to 29.48MHz, C/Q in push-pull and is high or low			3.0		
V_L Logic Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}			0.45		1.35	V
V_L Logic Level Supply Current	I_L	All logic inputs at GND or V_L, no load on any logic outputs, MCLK disabled			3	10	µA

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC SWITCHING REGULATOR						
Input Voltage Range	V_{24_DC}	V_{24} is the input to the DC-DC	8		36	V
DC-DC Turn-on Delay	t_{DC_ON}	Delay from V_{24} crossing V_{24UVLO} threshold until the DC-DC regulator finishes soft-start. RESET rises		10.2		ms
Switching Frequency	f_{DC_H}	BUCKSS = 0	1.198	1.229	1.260	MHz
	f_{DC_HSPRD}	BUCKSS = 1		1.229		
Spread Spectrum	Δf_{DC_SPRD}	FREQ = high, BUCKSS = 1		±10		%
Feedback (FB) Regulation Voltage	V_{DC_FB}			0.9		V
Output Voltage Accuracy	ACC_{DCFB}		-1.5	0	+1.5	%
Feedback (FB) OK Threshold	V_{DC_FBOK}	Voltage rising	92	95	98	$\%V_{DC\_FB}$
Feedback (FB) Low Threshold	$V_{DC\_FBTHLOW}$		61	65	70	$\%V_{DC\_FB}$
LX On-Resistance (High Side)	R_{DC_HS}	From PV_{24} to LX, LX is sinking current (Note 2)		2.2	3.9	Ω
LX On-Resistance (Low Side)	R_{DC_LS}	From LX to GND (Note 2)		1.3	2.8	Ω
Active Diode On-Resistance	R_{DC_ACT}	DC current (Note 2)		3	5.5	Ω
Maximum Peak Current into Active Diode	I_{DC_ACTMAX}		300			mA
Maximum LX Current Ripple	ΔI_{DC_LX}			100		%
High-Side Peak Current Limit	I_{DC_HSLIM}		+350	+400	+440	mA
Low-Side Current Limit	I_{DC_LSMAX}		-240	-200	-150	mA
DC-DC Autoretry Period	$T_{DCRETRY}$			30.6		ms
External Capacitance on PV_{24}	C_{DC_PV24}		1			µF
LX leakage	I_{LX_LKG}	$0V < V_{LX} < 36V$	-1		+1	µA
FB Input Bias	I_{FB_LKG}	$0 \le V_{FB} \le 1V$, T_A = 25°C	-100		+100	nA
LX Minimum On-Time	t_{LX_MINON}	(Note 2)		64	92	ns
LX Minimum Off-Time	t_{LX_MINOFF}	(Note 2)		32	60	ns
V_{CCB} LINEAR REGULATOR (V_{CCB})						

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CCB} Output Voltage	V_{CCB}	8V ≤ V_{PV24} ≤ 36V, 0mA ≤ I_{LOAD} ≤ 15mA		4.75	5	5.25	V
V_{CCB} Current Limit	I_{CCB_MAX}	V_{PV24} = 8V		30	55	90	mA
5V LINEAR REGULATOR (V_5)							
LIN Input Supply Voltage	V_{LIN}			6		36	V
V_5 Output Voltage	V_5	6V ≤ V_{LIN} ≤ 36V, no load on V_5		4.75	5	5.25	V
V_5 Load Regulation	$\Delta V5_{LDR}$	V_{LIN} = 24V, 1mA < I_{LOAD} < 50mA			0.85	2.4	%
V_5 Line Regulation	$\Delta V5_{LNR}$	6V ≤ V_{LIN} ≤ 36V, I_{LOAD} = 1mA			0.02	0.2	mV/V
V_5 Load Capacitance	C_{V5}	External capacitance on V_5		1			µF
3.3V LINEAR REGULATOR (V_{33})							
V_{33} Output Voltage	V_{33}	No load		3.1	3.3	3.5	V
V_{33} Load Regulation	ΔV_{33_LR}	1mA < I_{LOAD} < 50mA		0	0.18	1.2	%
V_{33} Load Capacitance	C_{V33}	External capacitance on V_{33}		1			µF
C/Q DRIVER							
C/Q Driver High-Side On-Resistance	R_{CQOH}	(Note 2)	High-side enabled, CL[1:0] = 11, I_{LOAD} = +150mA		2.4	4.4	Ω
C/Q Driver Low-Side On-Resistance	R_{CQOL}	(Note 2)	Low-side enabled, CL[1:0] = 11, I_{LOAD} = -150mA		2.0	4.0	Ω
C/Q Driver Current Limit	I_{CQCL}	V_{DROP} = 3V (Note 3)	CL[1:0] = 00	50	57	65	mA
			CL[1:0] = 01	100	114	130	
			CL[1:0] = 10	200	230	260	
			CL[1:0] = 11	250	290	325	
			WUGEN = 1	500			
C/Q Output Reverse Current	I_{REV_CQ}	CQ_EN = 1, CQ_PP = 1, CQ_PD = 0, CQ_PU = 0, $V_{C/Q}$ = (V_{24}+ 5V) or (V_{GND} - 5V)		-90		+375	µA
C/Q Leakage Current	I_{LEAK_CQ}	CQ_EN = 0, CQ_PD = 0, CQ_PU = 0, RX_DIS = 0, V_{24} = 24V, (V_{24} – 36V) ≤ $V_{C/Q}$ ≤ 36V		-35		+60	µA
C/Q CURRENT SINKS AND SOURCES							
C/Q Weak Pull-Down Current	I_{CQPD}	$V_{C/Q}$ > 5V, CQ_EN = 0, RX_DIS = 1, CQ_PD		-240	-200	-160	µA

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		= 1, CQ_PU = 0, CQPUD2MA = 0, CQPUD5MA = 0					
C/Q Weak Pull-Up Current	I_{CQPU}	$V_{C/Q}$ = (V_{24} - 5V), CQ_EN = 0, RX_DIS = 1, CQ_PD = 0, CQ_PU = 1, CQPUD2MA = 0, CQPUD5MA = 0		+160	+200	+240	µA
C/Q 2mA Pull-Down Current	I_{CQPD2}	$V_{C/Q}$ > 5V, CQ_EN = 0, RX_DIS = 1, CQ_PD = 1, CQ_PU = 0, CQPUD2MA = 1, CQPUD5MA = 0		-2.6	-2.2	-2.0	mA
C/Q 2mA Pull-Up Current	I_{CQPU2}	$V_{C/Q}$ = (V_{24} - 5V), CQ_EN = 0, RX_DIS = 1, CQ_PD = 0, CQ_PU = 1, CQPUD2MA = 1, CQPUD5MA = 0		+2.0	+2.2	+2.6	mA
C/Q 5mA Pull-Down Current	I_{CQPD5}	$V_{C/Q}$ > 5V, CQ_EN = 0, RX_DIS = 1, CQ_PD = 1, CQ_PU = 0, CQPUD2MA = 0, CQPUD5MA = 1		-6.5	-5.5	-5.0	mA
C/Q 5mA Pull-Up Current	I_{CQPU5}	$V_{C/Q}$ = (V_{24} - 5V), CQ_EN = 0, RX_DIS = 1, CQ_PD = 0, CQ_PU = 1, CQPUD2MA = 0, CQPUD5MA = 1		+5.0	+5.5	+6.5	mA
C/Q RECEIVER							
C/Q Input Voltage Range	V_{CQIN}	For valid RX logic		V_{24} - 36V		36	V
C/Q Input Threshold High	V_{CQTH}	TXEN = low and/or CQ_EN = 0, RXDIS = 0	V_{24} ≥ 18V	11		12.5	V
			V_{24} < 18V	54.4		78.8	%V_{24}
C/Q Input Threshold Low	V_{CQTL}	TXEN = low and/or CQ_EN = 0, RXDIS = 0	V_{24} ≥ 18V	9		10.5	V
			V_{24} < 18V	45		66.9	%V_{24}
C/Q Input Hysteresis	V_{CQHYS}	TXEN = low and/or CQ_EN = 0, RXDIS = 0	V_{24} ≥ 18V		2		V
			V_{24} < 18V		11		%V_{24}
C/Q Input Threshold High (TTL Mode)	$V_{CQTHTTL}$	TXEN = low and/or CQ_EN = 0, RXDIS = 0, RXTTL = 1	Rising	2.1		3.45	V
			Falling	1.1		1.85	
C/Q Input Hysteresis (TTL Mode)	$V_{CQHYSTTL}$	TXEN = low and/or CQ_EN = 0, RXDIS = 0, RXTTL = 1			1.3		V
C/Q Input Capacitance	C_{IN_CQ}	Driver disabled, CQ_PD = 0, CQ_PU = 0, f = 100kHz			35		pF
VOLTAGE MONITOR INPUT (V_M)							
V_M Voltage Range	V_M			0		5.5	V

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_M Threshold Voltage	V_{TH_M}	Rising	0.873	0.9	0.927	V
		Falling	0.832	0.858	0.883	
V_M Input Current	I_M		-1		+1	µA
RESET AND POWER-OK (RESET/POK**)**						
RESET/POK Input Voltage Low	V_{RSTIL}		0.4			V
RESET/POK Input Voltage High	V_{RSTIH}				1.3	V
RESET/POK Output Voltage Low	V_{POKLOW}	I_{LOAD} = -5mA			0.4	V
RESET/POK High Impedance Leakage Current	I_{RST_OD}	RESET/POK not asserted	-1		+1	µA
LOGIC INPUTS (CS**, SCLK, SDI, SDO, TX, TXEN)**						
Logic Input Voltage Low Threshold	V_{IL}				0.31 x V_L	V
Logic Input Voltage High Threshold	V_{IH}		0.68 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
LOGIC OUTPUTS (WU**,** IRQ**, SDO, RX, MCLK)**						
Logic Output Voltage Low	V_{OL}	IRQ, WU, SDO, RX, MCLK, I_{LOAD} = -5mA			0.4	V
Logic Output Voltage High	V_{OH}	SDO, RX, MCLK, I_{LOAD} = +5mA	V_L - 0.4			V
Open-Drain High Impedance Leakage Current	I_{LK_OD}	IRQ and WU, not asserted	-1		+1	µA
SDO Leakage Current	I_{LK_SDO}	CS = high	-1		+1	µA
RX Leakage Current	I_{LK_RX}	RX = GND or V_L	-1		+1	µA
THERMAL CHARACTERISTICS						
C/Q Driver Shutdown Temperature	T_{SHUT_DRV}	Driver temperature rising, C/Q driver fault bit is set and driver is disabled		+160		°C
C/Q Driver Shutdown Hysteresis	T_{SHUT_DHYS}	Driver temperature falling, driver is automatically reenabled, TSHOFFEN = 0		15		°C
IC Thermal Warning Threshold	T_{WRN}	Die temperature rising, THERMW and THERMWINT bits are set		+150		°C
IC Thermal Warning Threshold Hysteresis	T_{WRN_HYS}	Die temperature falling, THERMW bit is cleared		20		°C

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IC Thermal Shutdown Threshold	T_{SHUT_IC}	Die temperature rising, THSHUTD bit set			+170		°C
IC Thermal Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature falling, THSHUTD bit is cleared			20		°C
INTERNAL THERMAL SENSOR							
Programmable Thermal Warning Threshold Range	T_{WRN_RNG}	Typical range		-15		+174	°C
Programmable Thermal Warning Threshold Step	T_{WRN_LSB}	1 LSB			3		°C
Thermal ADC Resolution	T_{WRN_RES}				6		bit
Thermal ADC Accuracy	ΔT_{PREC_25C}	T_J = 27°C (Note 2)		-8	0	+8	°C
	ΔT_{PREC_85C}	T_J = 84°C			2		
	ΔT_{PREC_124C}	T_J = 126°C (Note 2)		-7	3	+12	
Thermal ADC Conversion Time	t_{ADC_CONV}				450		µs
AC ELECTRICAL CHARACTERISTICS							
C/Q DRIVER							
Driver Low-to-High Propagation Delay	t_{PDLH_PP}	CQLOSLEW[1:0] = 00, *Figure 1*	Push-pull or PNP mode		0.6	0.8	µs
	t_{PDLH_OC}	CQLOSLEW[1:0] = 00, *Figure 1*	NPN mode		1.8		
Driver High-to-Low Propagation Delay	t_{PDHL_PP}	CQLOSLEW[1:0] = 00, *Figure 1*	Push-pull or NPN mode		0.7	0.9	µs
	t_{PDHL_OC}	CQLOSLEW[1:0] = 00, *Figure 1*	PNP mode		2		
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, CQLOSLEW[1:0] = 00		-0.2		+0.2	µs
Driver Rise Time	t_{RISE}	Push-pull or PNP mode, V_{24}(max) = 30V, *Figure 1*	CQLOSLEW[1:0] = 00	0.2	0.37	0.565	µs
			CQLOSLEW[1:0] = 01	0.4	0.67	1.035	
			CQLOSLEW[1:0] = 10	0.8	1.56	2.55	
			CQLOSLEW[1:0] = 11	2.4	6.0	11.2	
Driver Fall Time	t_{FALL}	Push-pull or NPN mode, V_{24}(max) = 30V, *Figure 1*	CQLOSLEW[1:0] = 00	0.2	0.38	0.565	µs
			CQLOSLEW[1:0] = 01	0.45	0.76	1.08	

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			CQLOSLEW[1:0] = 10	1.2	1.87	2.7	
			CQLOSLEW[1:0] = 11	5	9	14	
C/Q Driver Enable Time High	t_{ENH}	Push-pull or PNP mode, *Figure 2*			0.59	0.935	µs
C/Q Driver Enable Time Low	t_{ENL}	Push-pull or NPN mode, *Figure 3*			0.45	0.7	µs
C/Q Driver Disable Time High	t_{DISH}	Push-pull or PNP mode, *Figure 2* (Note 2)			1.6	2.2	µs
C/Q Driver Disable Time Low	t_{DISL}	Push-pull or NPN mode, *Figure 3* (Note 2)			1.3	2.4	µs
C/Q RECEIVER							
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH_CQ}	*Figure 4*	RXFILTER = 1	0.825	1.22	1.6	µs
			RXFILTER = 0	0.24	0.28	0.43	
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL_CQ}	*Figure 4*	RXFILTER = 1	0.75	1.11	1.5	µs
			RXFILTER = 0	0.15	0.25	0.305	
WAKE-UP DETECTION (*Figure 5*)							
Wake-Up Input Minimum Pulse Width	t_{WUMIN}			62.2	64	65.8	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}			106	109	112	µs
$\overline{WU}$ Output Low Time	t_{WUL}	Valid wake-up condition on C/Q		150	200	250	µs
WAKE-UP GENERATION (*Figure 6*)							
Setup Time before Wake-Up	t_{SU_SU}				80		µs
Wake-up Pulse Duration	t_{WUGEN}	Wake-up pulse has the opposite polarity of the existing C/Q level		77.8	80	82.2	µs
On-Time after Wake-Up	t_{ON_WU}	C/Q driver enabled with original polarity after t_{WU}			2		µs
High Impedance Time after Wake-Up	t_{DIS_WU}	C/Q driver is high impedance after t_{ON_WU}			418		µs
MCLK CLOCK							
MCLK Frequency	f_{MCLK}	CLKDIV[2:0] = 000		3.594	3.686	3.779	MHz
		CLKDIV[2:0] = 001		7.189	7.373	7.557	
		CLKDIV[2:0] = 010		14.38	14.74	15.11	
		CLKDIV[2:0] = 011		28.75	29.49	30.23	
		CLKDIV[2:0] = 100		1.797	1.843	1.889	

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{CQGND} = V_{GND} = 0V, All logic inputs at V_L or GND, Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V and T_A = +25°C, unless otherwise noted (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING (CS, SCLK, SDI, SDO) (*Figure 7*)						
Maximum SCLK Frequency	f_{SPI_MAX}				12	MHz
SCLK Clock Period	t_{CH+CL}		35			ns
SCLK Pulse Width High	t_{CH}		5			ns
SCLK Pulse Width Low	t_{CL}		30			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}		7			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Hold Time	t_{DH}		3			ns
SDI Setup Time	t_{DS}		3			ns
SDO Output Data Propagation Delay	t_{DO}				23	ns
SDO Rise and Fall Times	t_{FT}			0.7		ns
Minimum $\overline{CS}$ Pulse	t_{CSW}			15		ns
EMC TOLERANCE						
ESD Protection (V_{24}, C/Q Pins)		IEC 61000-4-2 Contact Discharge		±2.5		kV
ESD Protection (All Other Pins)		Human Body Model		±1.5		kV
Surge Protection (V_{24}, C/Q Pins)	V_{SRG}	500Ω 8/20µs surge to ground		±1.2		kV

Note 1: All devices are 100% production tested at T_A = 25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Not production tested. Guaranteed by design.

Note 3: V_{DROP} is measured as the voltage from the driver output to GND (V_{DRIVER} - V_{GND}) when measuring the low-side driver current limit and as (V_{24} - V_{DRIVER}) when measuring the high-side current limit.

Timing Diagrams

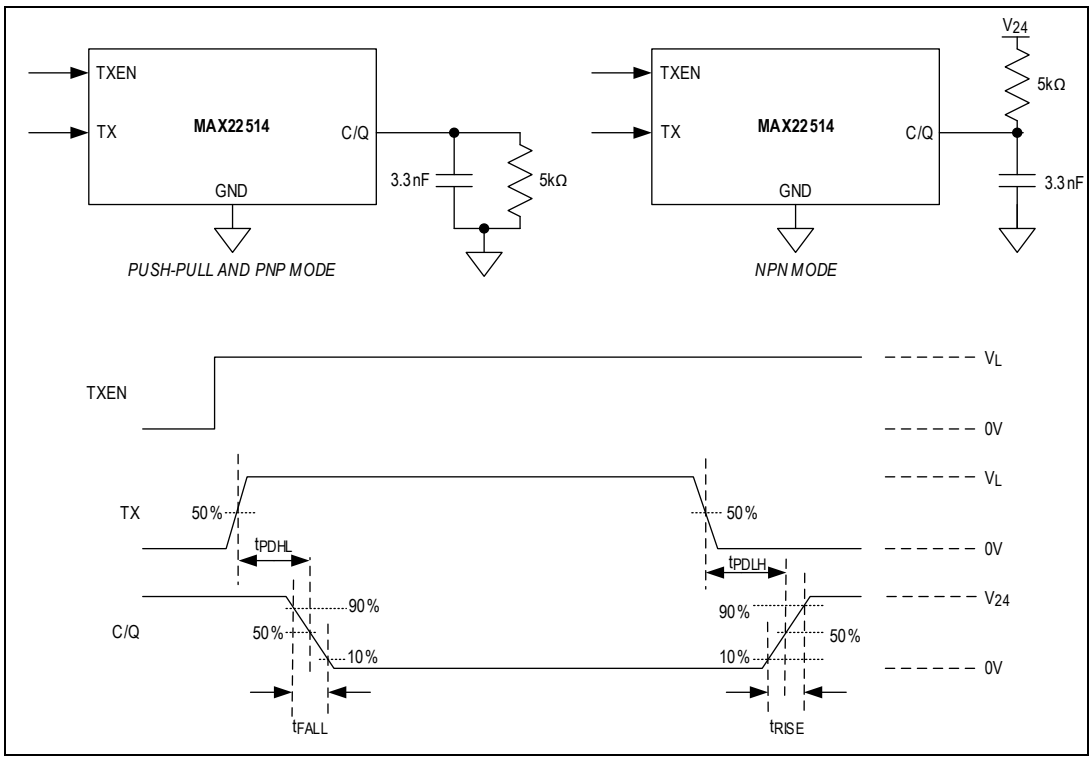


Figure 1. C/Q Driver Propagation Delays

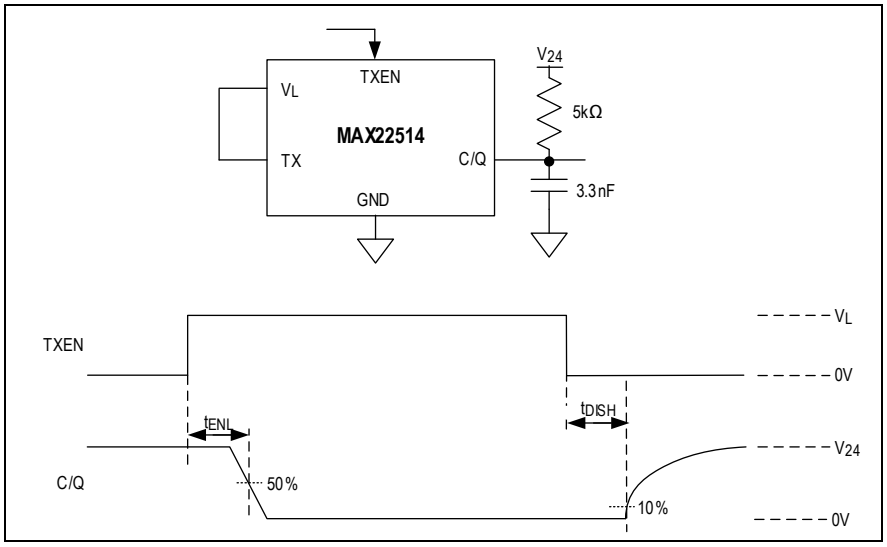


Figure 2. C/Q Driver Enable Low and Disable High Timing

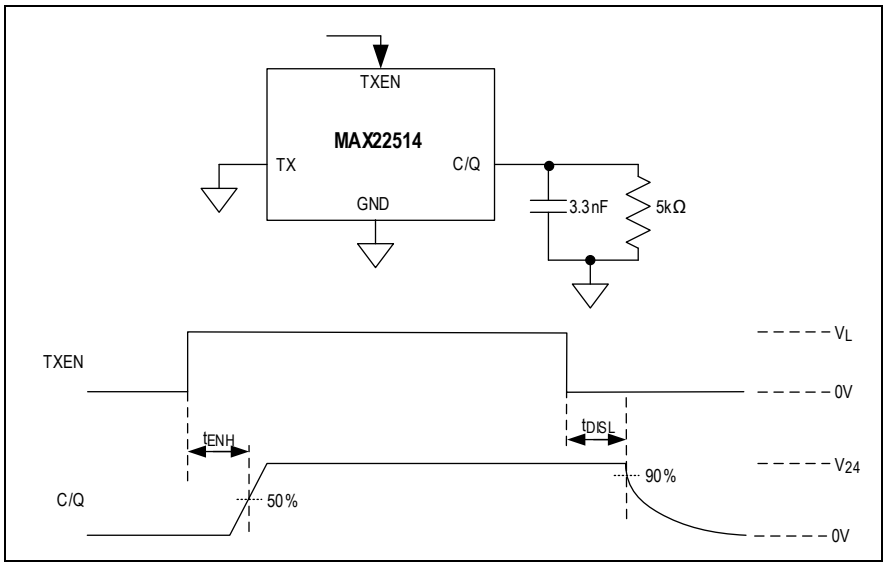


Figure 3. C/Q Driver Enable High and Disable Low Timing

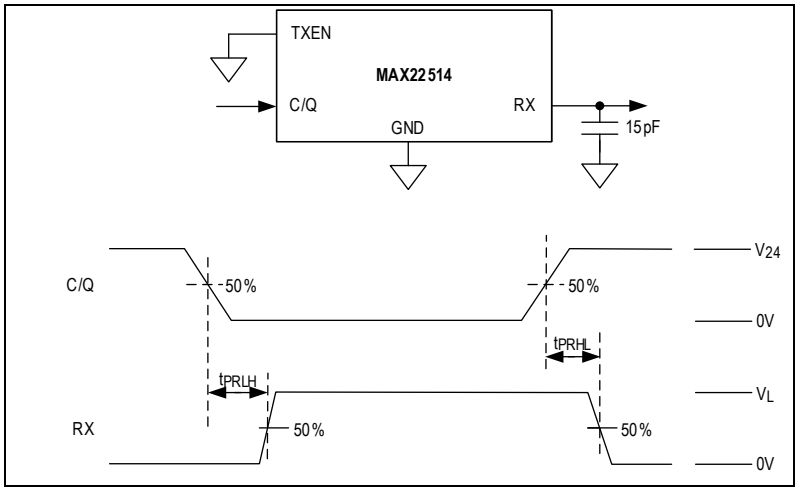


Figure 4. C/Q Receiver Timing

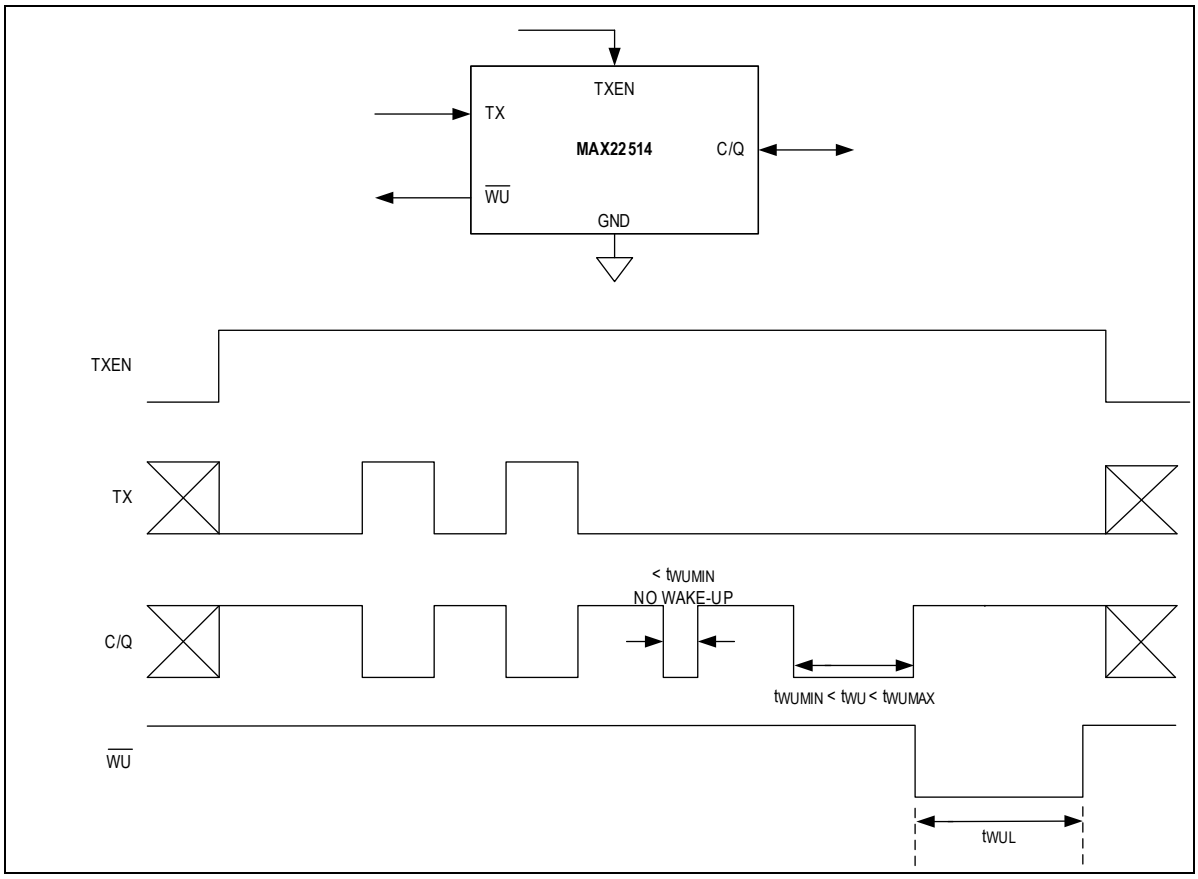


Figure 5. Wake-Up Detection Timing

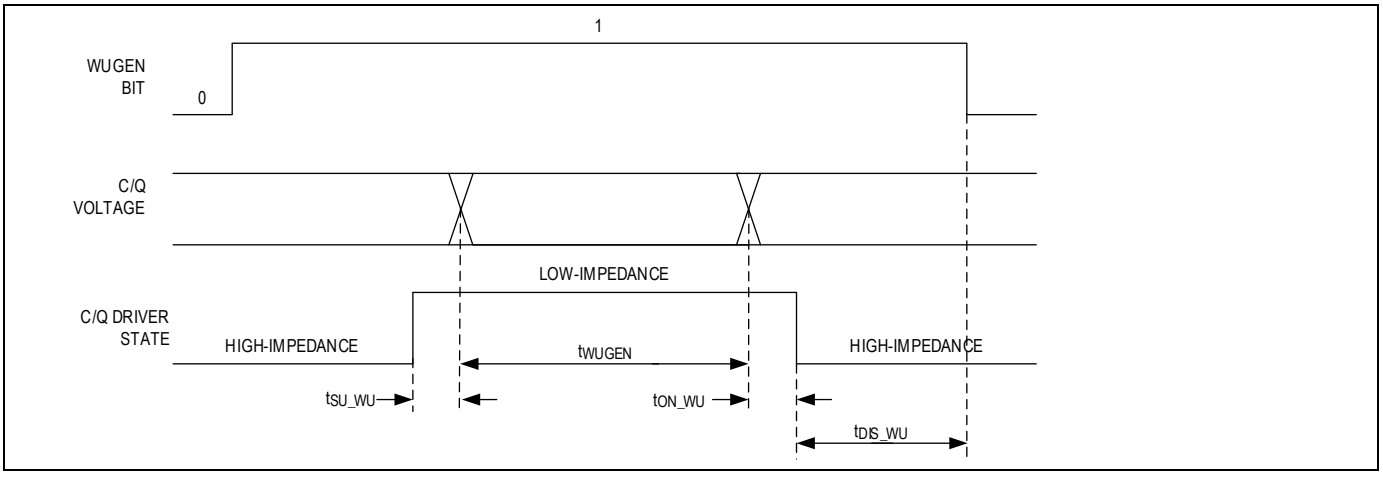


Figure 6. Wake-Up Generation

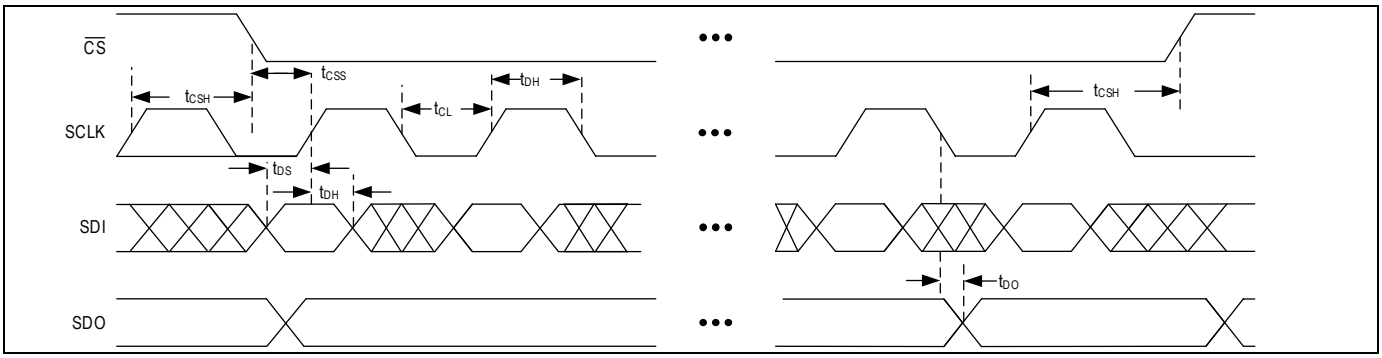
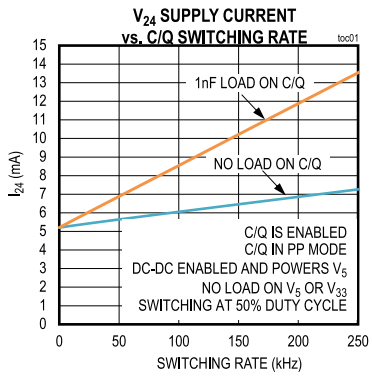
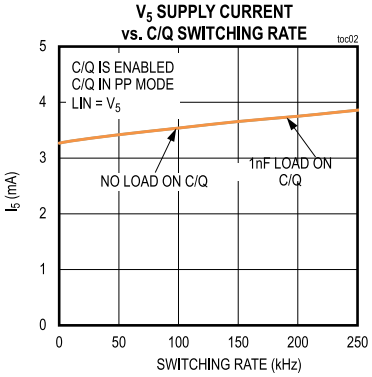


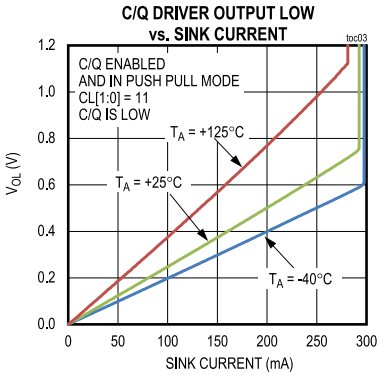
Figure 7. SPI Timing Diagram

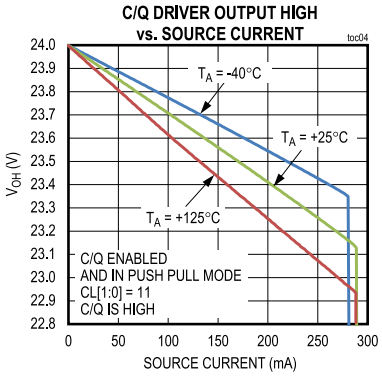
Typical Operating Characteristics

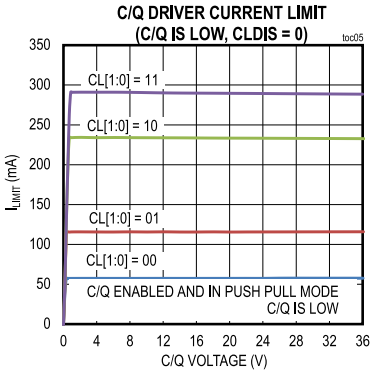
V_{24} = 24V, DC-DC regulator is enabled and connected to LIN, $V_L = V_{33}$, T_A = +25°C, unless otherwise noted.

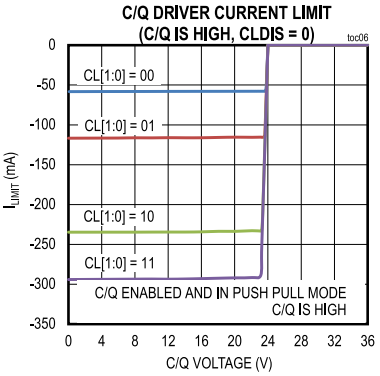


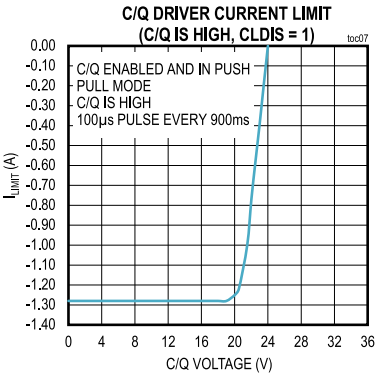


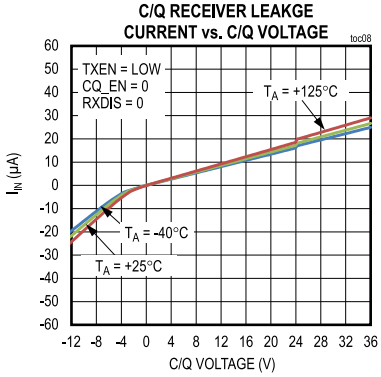


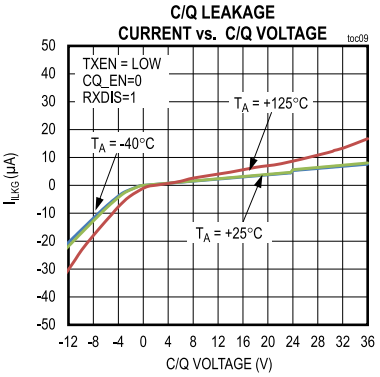






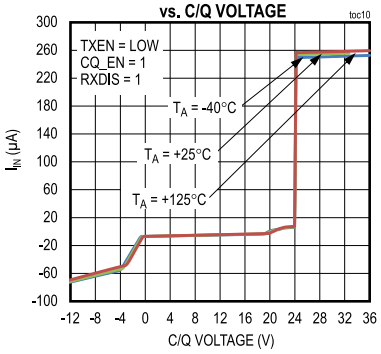




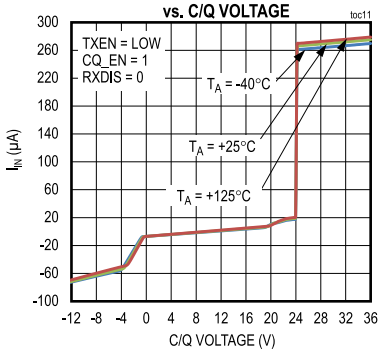


V_{24} = 24V, DC-DC regulator is enabled and connected to LIN, $V_L = V_{33}$, T_A = +25°C, unless otherwise noted.

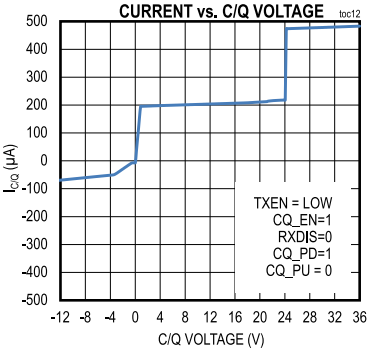
C/Q LEAKAGE CURRENT vs. C/Q VOLTAGE



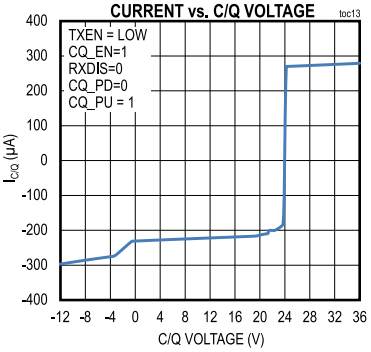
C/Q RECEIVER INPUT CURRENT vs. C/Q VOLTAGE



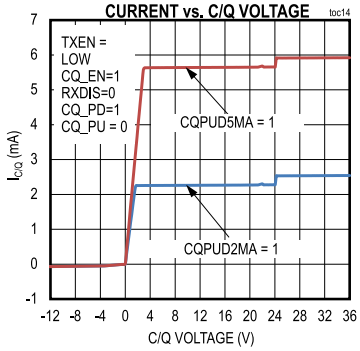
C/Q WEAK PULL-DOWN CURRENT vs. C/Q VOLTAGE



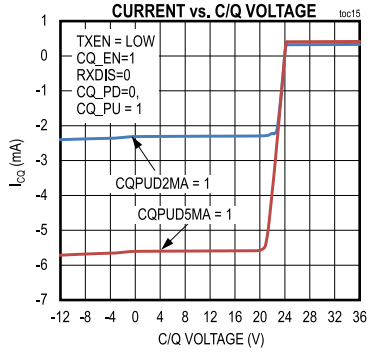
C/Q WEAK PULL-UP CURRENT vs. C/Q VOLTAGE



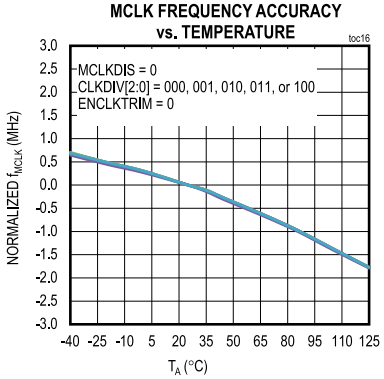
C/Q 2mA AND 5mA PULL-DOWN CURRENT vs. C/Q VOLTAGE



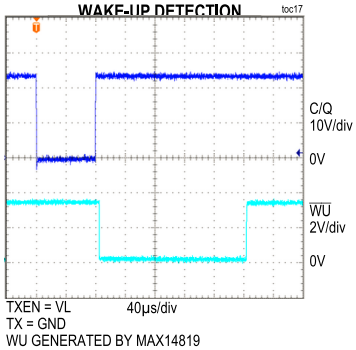
C/Q 2mA AND 5mA PULL-UP CURRENT vs. C/Q VOLTAGE



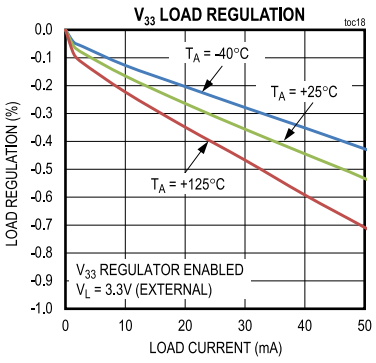
MCLK FREQUENCY ACCURACY vs. TEMPERATURE



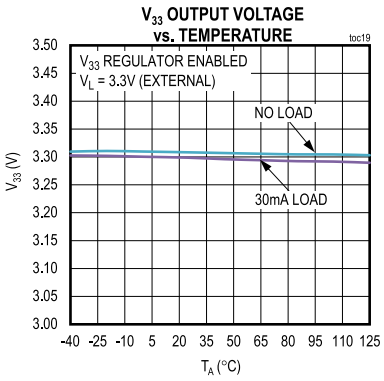
WAKE-UP DETECTION

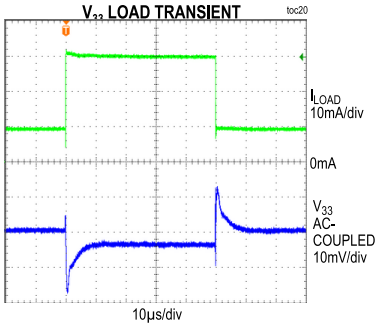


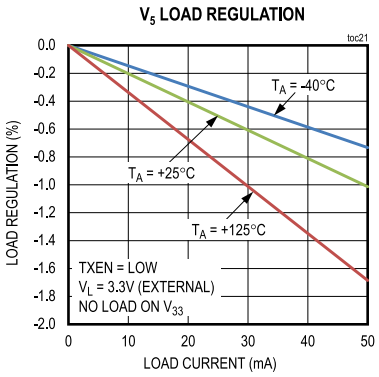
V_{33} LOAD REGULATION

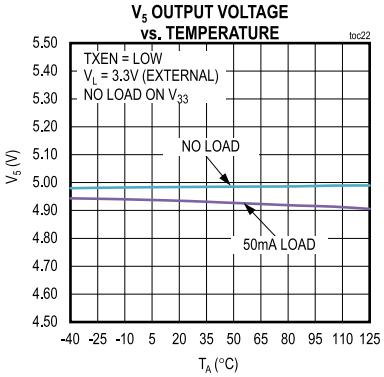


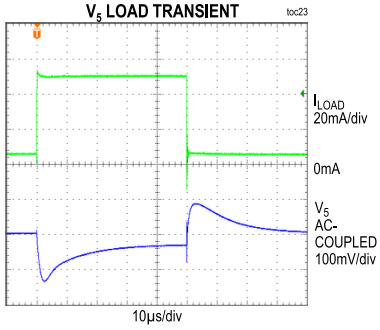
V_{24} = 24V, DC-DC regulator is enabled and connected to LIN, $V_L = V_{33}$, T_A = +25°C, unless otherwise noted.

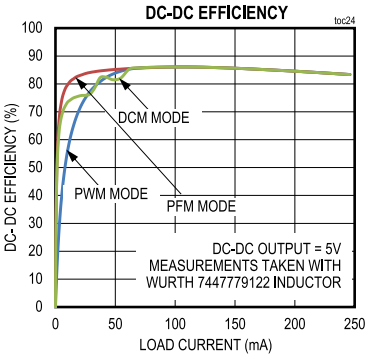


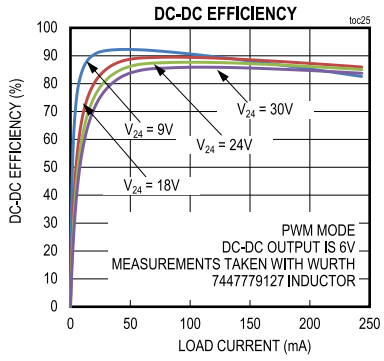


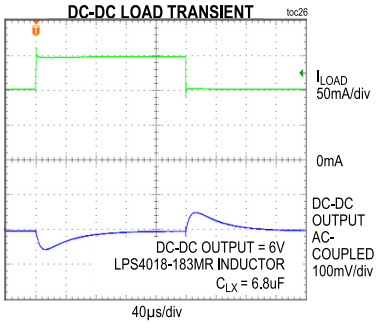


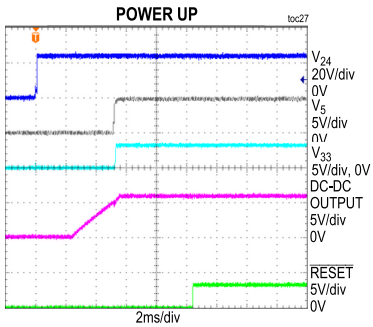




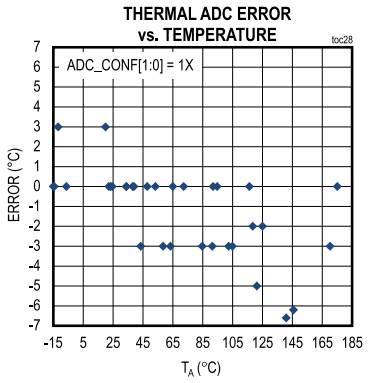




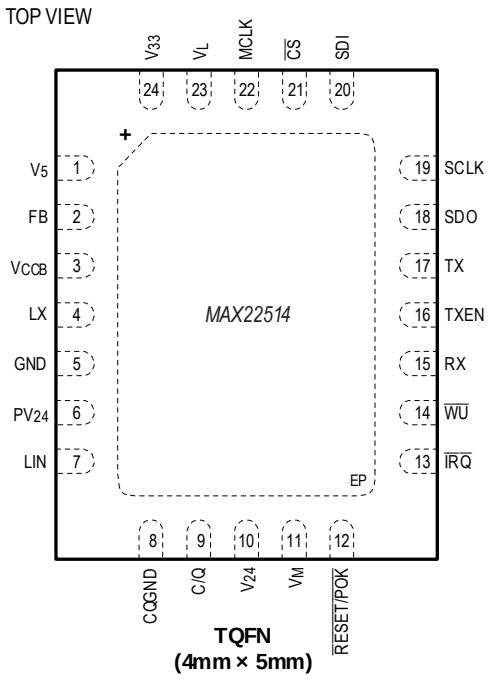




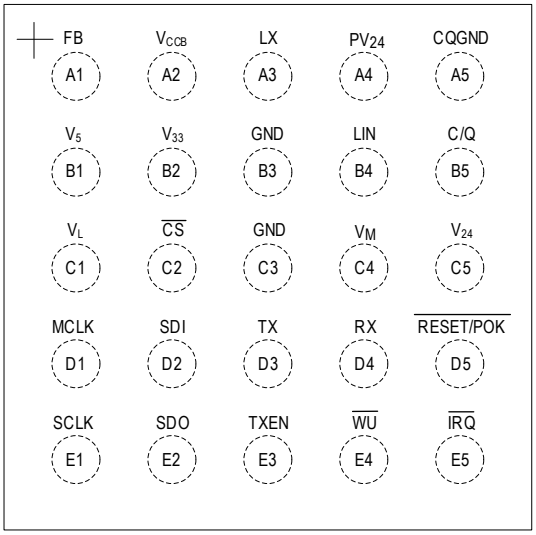
V_{24} = 24V, DC-DC regulator is enabled and connected to LIN, $V_L = V_{33}$, T_A = +25°C, unless otherwise noted.



Pin Configurations



TOP VIEW (BUMPS ON BOTTOM)



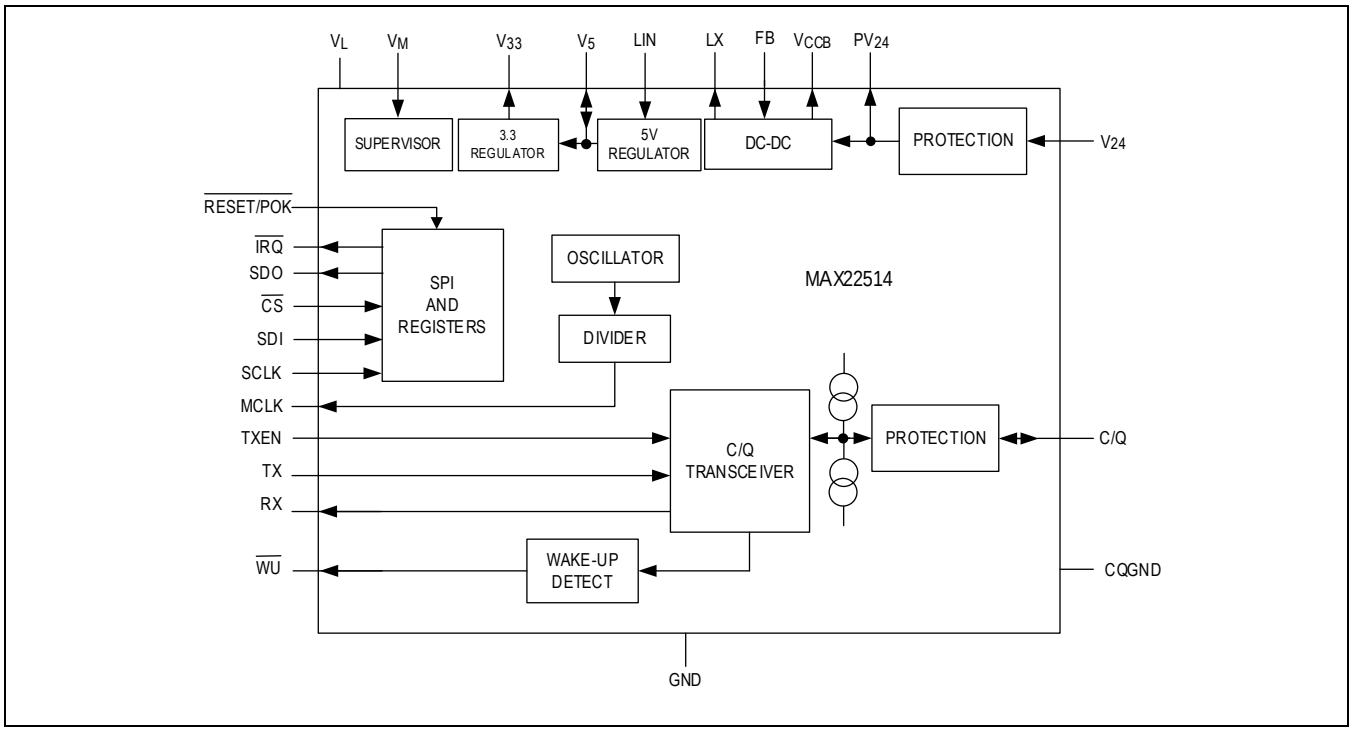
WLP
(2.5mm x 2.6mm)

Pin Descriptions

PIN		NAME	FUNCTION
TQFN	WLP		
SUPPLY			
3	A2	V_{CCB}	Internal 5V Supply Regulator Output. Bypass V_{CCB} to GND with a 1µF capacitor as close to the device as possible. V_{CCB} can supply an external load up to 5mA.
6	A4	PV_{24}	Active Diode Output and DC-DC Input. Bypass PV_{24} with an external 1µF capacitor as close to the device as possible.
7	B4	LIN	5V Linear Regulator Input. Connect LIN to the output of the DC-DC circuit, the PV_{24} supply, or an external supply between 6V and 36V. Bypass LIN to GND with a 1µF capacitor. Connect LIN to V_5 to disable the 5V linear regulator.
1	B1	V_5	5V Linear Regulator Output/ Supply Input. V_5 is the output of the internal 5V linear regulator. Bypass V_5 to GND with a 1µF capacitor as close to the device as possible. To disable the 5V linear regulator, connect LIN to V_5. 5V is required on V_5 for normal operation. If the 5V regulator is disabled, apply an external 5V power supply to V_5.
10	C5	V_{24}	Supply Voltage Input. Connect V_{24} to the L+ terminal of the IO-Link connector, or to an external supply. Bypass V_{24} to GND with a 10nF capacitor as close to the device as possible.
8	A5	CQGND	C/Q Driver IO-Link Ground. Connect CQGND to the L- terminal of the IO-Link connector and to GND. See the *Layout and Grounding* section for more information.
23	C1	V_L	Logic Supply Input. Bypass V_L to GND with a 1µF capacitor as close to the device as possible. V_L sets the logic levels for all logic signals. Connect V_L to V_{33}, V_5, or to an external voltage between 2.5V and 5.5V.
5	B3, C3	GND	Ground. Connect GND to CQGND. See the *Layout and Grounding* section for more information.
24	B2	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND with a 1µF capacitor as close to the device as possible.
EP	-	EP	Exposed Pad. Connect EP to GND. See the *Layout and Grounding* section for more information.
DC-DC REGULATOR			
4	A3	LX	Switching Output of the Integrated DC-DC Converter. Connect an inductor between LX and the output capacitor to generate a voltage with the DC-DC circuit. See the *DC-DC Component Selection* section for more information.
2	A1	FB	DC-DC Buck Regulator Feedback Input. Connect FB to the tap of a resistor divider between the output of the DC-DC and GND. See *Table 4* for recommended component values to set the DC-DC output between 2.5V and 12V. Connect FB to V_{CCB} if the DC-DC is not used.
24V LINE INTERFACE			
9	B5	C/Q	IO-Link Transceiver Input/ Output. The C/Q driver is disabled at startup. Set CQ_EN = 1 and TXEN = high to enable the C/Q driver.
CONTROL INTERFACE			
11	C4	V_M	Voltage Monitor Input. Connect a resistor divider between the monitored supply voltage (e.g. V_{24} or PV_{24}) and GND to define the power-OK threshold voltage for the monitored supply voltage. See the *Voltage Monitor Input (VM)* section for more information.

12	D5	RESET/POK	Dual Function Active-Low Reset Input and Open-Drain Power-OK (POK) Output. Drive RESET/POK low to set the MAX22514 in reset mode. The C/Q output is disabled and all registers are reset to default values when RESET/POK is driven low. The MAX22514 asserts RESET/POK low when any of the V_{24}, V_5, or DC-DC output voltages are below their respective undervoltage lockout (UVLO) thresholds. Only V_5 is monitored when the DC-DC regulator is disabled. The MAX22514 deasserts RESET/POK 4ms (typ) after the power supplies rise above their UVLO thresholds. Connect RESET/POK to V_{CCB} or V_L with a 10kΩ (typ) resistor for normal operation.
14	E4	WU	Open-Drain IO-Link Wake-Up Request Output. WU asserts low for 200µs (typ) when a valid IO-Link wake-up pulse is detected on the C/Q line.
13	E5	IRQ	Active-Low Open-Drain Interrupt Request Output. IRQ asserts low when a bit is set in the INTERRUPT register. See the Register Details section for more information.
18	E2	SDO	Serial Data Output. Connect SDO on the MAX22514 to the MISO input on the SPI master. SDO is high impedance when CS is high.
19	E1	SCLK	Serial Clock Input
20	D2	SDI	Serial Data Input. Connect SDI on the MAX22514 to the MOSI output on the SPI master.
21	C2	CS	SPI Chip-Select Input. Drive CS low to start a read/write cycle. The cycle ends when CS is driven high.
UART INTERFACE			
15	D4	RX	C/Q Receiver Logic Output. RX is inverted, relative to the logic state of C/Q, by default. Set the INVCQ bit in the CQCONFIG register to set RX to the same logic state as C/Q. Connect RX to the RX input of the UART for IO-Link communication.
16	E3	TXEN	C/Q Driver Enable Logic Input. Drive TXEN high and set the CQ_EN bit in the CQCONFIG register to enable the C/Q driver. Drive TXEN low to disable the C/Q driver. Connect TXEN to the RTS output of a microcontroller for IO-Link communication.
17	D3	TX	C/Q Driver Logic Input. TX is inverted, relative to the logic state of C/Q, by default. Set the INVCQ bit in the CQCONFIG register to set TX to the same logic state as C/Q. Connect TX to the TX output of the UART for IO-Link communication.
CLOCK OUTPUT			
22	D1	MCLK	Microcontroller Clock Output. Set the MCLK frequency by setting the CLKDIV bits in the CLKCONFIG register. Connect MCLK to an external microcontroller for comparison and trimming. The MCLK frequency is 3.686MHz (typ) by default, but can be disabled or programmed to 3.686MHz, 7.373MHz, 14.74MHz, 29.49MHz, or 1.843MHz.

Functional Diagrams



Detailed Description

The MAX22514 IO-Link transceiver integrates high voltage functionality, including one 24V line driver, an integrated DC-DC buck regulator, and 5V and 3.3V linear regulators. The MAX22514 is targeted for IO-Link devices, masters, and industrial switching sensor applications, and can be configured and monitored using a standard SPI interface.

24V Interface I/O (C/Q)

The MAX22514 features an IO-Link transceiver interface capable of operating with voltages up to 36V. This is the industrial standard 24V interface and includes the C/Q input/output, the V24 supply, and ground. The C/Q switching driver is programmable for PNP, NPN, or push-pull mode, features a programmable current limit, slew rate, and pull-up/pull-down currents, and operates over all of the COM1, COM2, and COM3 IO-Link data rates.

The C/Q driver is enabled when TXEN is high and the CQ_EN = 1 in the CQCONFIG register. Toggle the TX input to switch the C/Q output. Alternatively, set the CQ_Q bit in the CONTROL register to set C/Q high or low. See *Table 1* and *Table 2*. C/Q is the logic inverse of the TX input, by default. Set the INVCQ = 1 in the CQCONFIG register to align the TX, C/Q, and RX logic states.

Table 1. C/Q Driver Control (CQINV = 0)

INPUTS				C/Q OUTPUT		
CQ_EN	TXEN	TX	CQ_Q	NPN MODE	PNP MODE	PP MODE
0	X	X	X	C/Q Driver Disabled		
1	L	X	X	HIGH Z	HIGH Z	HIGH Z
	H	L	0	HIGH Z	HIGH	HIGH
			1	HIGH Z	HIGH	HIGH
		H	0	LOW	HIGH Z	LOW
			1	HIGH Z	HIGH	HIGH

X = Don’t care

Table 2. C/Q Receiver Logic

INPUTS				OUTPUT
RXDIS	CQ_EN	CQINV	C/Q	RX
0	X	0	L	H
			H	L
		1	L	L
			H	H
1	X	X	X	HIGH Z

X = Don’t care

Overcurrent Limiting

The C/Q driver features a programmable current limit. Select the current limit by setting the CL[1:0] bits in the CURRLIM register. Current limit thresholds can be set to 50mA (min), 100mA (min), 200mA (min), and 250mA (min). When the load attempts to draw more current than the current limit threshold setting, the C/Q driver actively limits the load current so a higher load current does not flow.

Setting CLDIS = 1 disables active current limiting, resulting in higher load currents. Setting CLDIS = 1 should only be done in PNP mode. Setting CLDIS = 1 in NPN or push-pull modes can damage the device.

Autoretry

The MAX22514 features an autoretry function to mange and limit heating and power dissipation during driver overload conditions.

Set the AUTORETRYEN bit (AUTORETRYEN = 1) in the CURRLIM register to enable autoretry functionality. When autoretry is enabled, the MAX22514 disables the driver after the current limit threshold has been exceeded for the selected blanking time. The driver is disabled for the programmed fixed off-time and is then automatically reenabled. If the overcurrent condition persists, the driver remains on for the blanking time and is then redisabled. This autoretry cycle continues until the overcurrent condition is removed.

Select the blanking time and fixed off-time by setting the CL_BL[1:0] bits and the TAR[1:0] bits respectively in the CURRLIM register.

When charging large capacitive loads or incandescent lamps, ensure that the selected autoretry blanking time is long enough to charge the required load before the driver is disabled.

C/Q Driver Thermal Shutdown

The C/Q driver is turned off when the driver junction temperature exceeds the +160ºC (typ) driver thermal shutdown temperature. The associated driver fault bits (CQFAULTINT, CQFAULT) in the INTERRUPT and STATUS registers (respectively) are set. If the fault is not masked (CQFAULTM = 0 in the IRQMASK register), IRQ is asserted after the programmed blanking time. Set the CL_BL[1:0] bits in the CURRLIM register to select the blanking time. The driver is automatically reenabled when the driver junction temperature falls below 145ºC (typ).

C/Q Receiver Threshold

Although the IO-Link standard defines operation for a supply ranging between 18V to 30V, industrial controllers and sensors in the field commonly operate with supply voltages as low as 9V. The MAX22514 operates with a supply voltage between 8V and 36V. When the V24 supply voltage is above 18V, the C/Q receiver on the MAX22514 supports the standard IO-Link receiver thresholds. When V24 is less than 18V, the MAX22514 scales the C/Q receiver thresholds, allowing receiver functionality down to the lowest supply voltage.

The C/Q receiver can also be configured to detect 5V TTL signal levels. Set the RXTTL bit (RXTTL = 1) in the CQMASTER register to enable TTL thresholds on the C/Q receiver. RXTTL is not set by default.

Current Sink and Source on C/Q

The MAX22514 features six different pull-up/pull-down current sources/sinks that can be enabled on the C/Q line: a 200µA (typ) weak pull-up and/or pull-down current, a 2mA (min) pull-up or pull-down current, and a 5mA (min) pull-up or pull-down current. Configure and enable the current on C/Q by setting the CQ_PD and CQ_PU bits in the CQCONFIG register and by setting the CQPUD5MA and CQPUD2MA bits in the CQMASTER register. See *Table 3*.

Table 3. Pull-Up/Pull-Down Current Settings on C/Q

CQ_PU	CQ_PD	CQPUD5MA	CQPUD2MA	C/Q OUTPUT
0	0	X	X	No pull-up or pull-down current enabled
0	1	0	0	Weak pull-down current enabled
		1	X	5mA pull-down current enabled
		0	1	2mA pull-down current enabled
1	0	0	0	Weak pull-up current enabled
		1	X	5mA pull-up current enabled
		0	1	2mA pull-up current enabled

X = Don’t care

Wake-Up Detection

A wake-up event occurs when an IO-Link master forces a level on the C/Q line that is opposite to the set level of the C/Q driver level for 80µs (typ). WU pulses low for 200µs (typ) when the device detects a wake-up pulse on C/Q (*Figure 5*).

Wake-up detection on the MAX22514 is enabled by default. When a valid wake-up event is detected and the interrupt is not disabled (WUM = 0 in the IRQMASK register), the MAX22514 generates an interrupt and asserts IRQ.

To disable wake-up detection, set the WUDIS bit in the CONTROL register. When WUDIS = 1, the WUINT bit is not set when a wake-up pulse is detected.

The MAX22514 automatically ignores false wake-up events that can sometimes occur as a consequence of driving large capacitive or lamp loads where the time constant of charging is around 80µs. No wake-up event is detected for the duration of the programmed blanking time after the C/Q driver changes logic state.

Wake-Up Pulse Generation

The MAX22514 can generate an IO-Link master wake-up pulse. To prepare the transceiver to generate a wake-up pulse, set the C/Q driver in receive mode (TXEN = low) and set the TX input high. Set the WUGEN bit in the CQMASTER register to generate the wake-up pulse.

When WUGEN = 1, the MAX22514 samples the voltage level on the C/Q receiver. The device then enables the C/Q driver and pulls the C/Q line to the opposite polarity of the sampled voltage for 80µs (typ). The driver remains enabled and the line is driven back to the original polarity after the wake-up pulse duration. Following the on-time after wake-up delay (tON_WU), the driver is set to high impedance. The MAX22514 continues to ignore signals on TX and TXEN and holds the driver in a high impedance state for the high-impedance time after wake-up delay (t_{DIS_WU}), after which the microcontroller can initiate the EstablishCOM IO-Link communication sequence. See *Figure 6*.

While the MAX22514 is generating the wake-up pulse, the current limit is automatically set above 500mA and the C/Q slew rates are automatically set to the highest rate. Register settings are not changed during wake-up generation, and programmed current limit and slew rate settings operate normally after the wake-up pulse is generated. These settings do not need to be reprogrammed after a wake-up is generated.

V_{CCB} Output

V_{CCB} is the output of an internal regulator powered by V_{24} or V_5. V_{CCB} is powered by V_{24} until the V_5 voltage exceeds 3.92V (min). After which, V_{CCB} is powered by V_5. As V_5 is rising, and V_{CCB} can drop below 5V until V_5 reaches its steady state voltage. V_{CCB} can be used to drive a small (≤ 10mA) external load.

Reset Input/ Power OK Output (RESET/POK)

The RESET/POK pin is a dual function open-drain logic input/output, functioning as a reset input and a power-OK (POK) output.

Drive RESET/POK low to put the MAX22514 in reset mode. The C/Q driver is disabled and the registers are reset to their default state when RESET/POK is driven low. Serial bus communication is available while RESET/POK is low. If the DC-DC has been disabled in the registers (BUCKDIS = 1), the device deasserts RESET/POK 4ms (typ) after RESET/POK is released and all power supplies are valid. If the DC-DC has been enabled, RESET/POK deasserts immediately after being released.

The MAX22514 asserts RESET/POK low when V_{24} or V_5 voltage falls below their respective UVLO thresholds, or when the DC-DC output voltage falls below 95% of the set voltage (typ). The C/Q driver is disabled and the registers are reset to their default state when RESET/POK is low. Serial bus communication is available while RESET/POK is low. The MAX22514 deasserts RESET/POK 4ms (typ) after all power supplies are valid.

Connect a pull-up resistor between RESET/POK and V_L or V_{CCB} for normal operation. Connect RESET/POK to the reset input of a microcontroller to use it as a reset signal.

Voltage Monitor Input (VM)

The MAX22514 features a flexible voltage comparator. This comparator monitors the voltage at the V_M input. When the V_M input voltage is below the 858mV (typ) threshold, the VMINT bit in INTERRUPT register is set and IRQ is asserted if not masked (VMINTM = 0 in the IRQMASK register). Note that the VMINT interrupt bit is not cleared when the INTERRUPT register is read while the V_M voltage is below the comparator threshold. This bit is cleared only if the V_M voltage exceeds the threshold voltage during the INTERRUPT read.

V_M can be used to supervise the voltage on V_{24}, PV_{24}, or any other pin.

For example, to monitor the PV_{24} use a resistor divider between PV_{24}, V_M, and GND to set the minimum PV_{24} voltage threshold (*Figure 8*). Calculate the monitored voltage power-OK threshold (V_{POK}) as:

$$V_{POK} = V_{TH\_M} \times [(R_1 + R_2) / R_2]$$

Select the resistor values to ensure that V_M does not exceed the 5.5V maximum voltage.

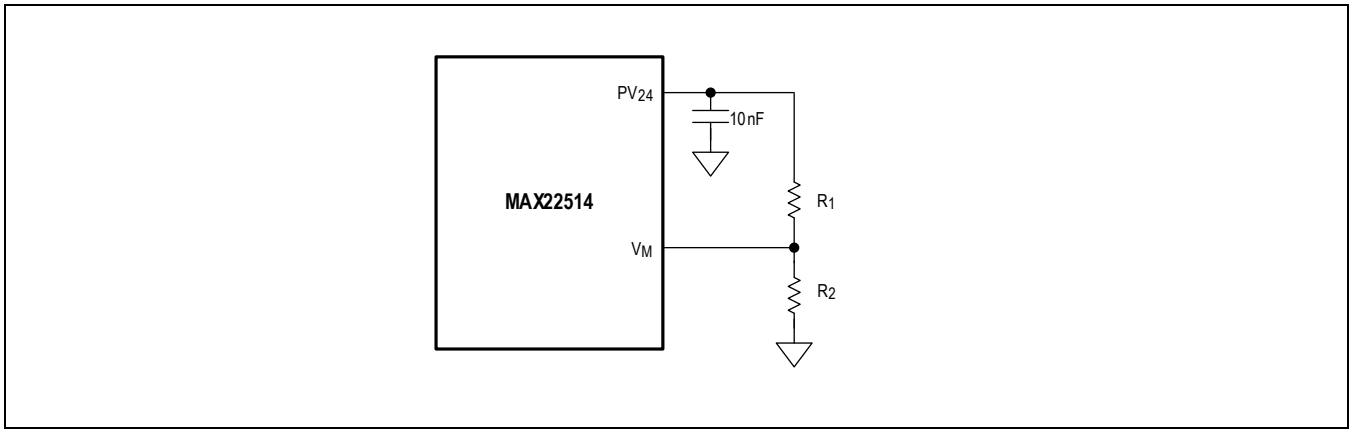


Figure 8. VM input used to monitor the PV24 supply

Integrated DC-DC Regulator

Overview

The MAX22514 features an integrated high-efficiency synchronous DC-DC buck regulator with active diode reverse protection, current overload protection, soft start, spread spectrum operation, and an adjustable output voltage. The DC-DC regulator operates with a fixed 1.229MHz (typ) frequency during normal operation. The regulator can be configured to operate in pulse-width modulation (PWM) mode, pulse frequency modulation (PFM) mode, or discontinuous conduction mode (DCM) during normal operation. Select the operating mode by setting the BUCKDCM or BUCKPFM mode bits in the MODE register. The regulator is enabled by default but can be disabled through the serial interface. The DC-DC regulator is supplied from the PV24 voltage to protect against supply inversion. Bypass PV24 to GND with a 1µF capacitor to ensure proper operation for the DC-DC.

Startup and Soft Start

The MAX22514 DC-DC buck regulator features soft-start to slowly raise the output voltage when the device is powered up. When the V_{24} voltage exceeds the 7.5V (typ) UVLO threshold, the DC-DC regulator is turned on, operating in DCM mode. DCM mode allows the DC-DC output to soft-start whether the output voltage is unpowered or prebiased. Internal circuitry slowly ramps the output voltage to 95% of the set voltage within 3.3ms (typ) of the V_{24} voltage exceeding the UVLO threshold, ending the soft-start sequence. Once soft-start has ended, the regulator switches from DCM mode to the selected mode for normal operation. By default, normal operation is PWM mode. Set the BUCKPFM and/or the BUCKDCM bits in the MODE register to select another operating mode of the DC-DC regulator.

Maximum DC-DC Output Current

The MAX22514 integrated DC-DC buck regulator can supply loads up to 200mA (typ). The internal reverse-protection active diode between V_{24} and PV_{24} has a 200mA average current capability to supply the DC-DC input. Under certain conditions, the internal active diode between the V_{24} supply and PV_{24} can reduce the efficiency or reduce the maximum load current. If load currents are such that the current through the active diode exceeds 300mA, connect a Schottky diode between V_{24} and PV_{24} to bypass the internal active diode. When a Schottky diode is used, a TVS or varistor on V_{24} might be necessary to survive hot-plug events.

Selecting the Mode of Operation

Pulse Width Modulation Mode

A Pulse Width Modulation Mode (PWM) DC-DC regulator switches at a fixed frequency, adjusting the duty cycle of the pulses depending on the output power requirements. The maximum duty cycle on the DC-DC regulator is near 100%. Switching noise is easily filtered in PWM mode. The MAX22514 DC-DC regulator operates in PWM mode by default (BUCKDCM = 0 and BUCKPFM = 0 in the MODE register).

Pulse Frequency Modulation Mode

In Pulse Frequency Modulation Mode (PFM), the DC-DC converter switches LX with a peak current set to be at least 200mA (typ). LX stops switching when the output voltage exceeds 103% of the set value and starts switching again when the DC-DC output voltage drops to 101% of the set value. Because the switching frequency changes in PFM mode, switching noise is more difficult to filter in PFM mode typically resulting in a higher ripple on the output. PFM mode has the highest efficiency when driving low loads. Set BUCKPFM = 1 and BUCKDCM = 0 in the MODE register to enable PFM mode on the DC-DC regulator.

Discontinuous Conduction Mode

In Discontinuous Conduction Mode (DCM), the inductor current of the DC-DC regulator can reach zero for a short period during each switching cycle. In this mode, the output voltage is dependent on the input voltage, the inductance in the DC-DC regulator, the switching frequency, and the load. Use DCM mode for low output ripple and high efficiency under light load conditions. The MAX22514 DC-DC regulator operates in DCM mode during soft-start. Set BUCKDCM = 1 in the MODE register (the BUCKPFM bit is ignored, in this case) to enable DCM functionality for normal operation.

Enabling/Disabling the DC-DC

The integrated DC-DC buck regulator on the MAX22514 is enabled by default but can be disabled through the serial interface. Set the BUCKDIS bit in the MODE register to disable the DC-DC. If the DC-DC regulator is not used, leave the LX unconnected and connect FB to VCCB.

DC-DC Component Selection

Setting the Output Voltage

The output voltage of the DC-DC regulator can be programmed from 2.5V to 12V. Set the output voltage by connecting a resistor divider from the output to FB to GND (*Figure 9*).

Calculate the output voltage using the following equation:

$$R_1 = R_2 \times (V_{OUT} / 0.9 - 1)$$

Ensure that $R_1 \parallel R_2 \leq 46k\Omega$ and use ±1% resistors for best accuracy.

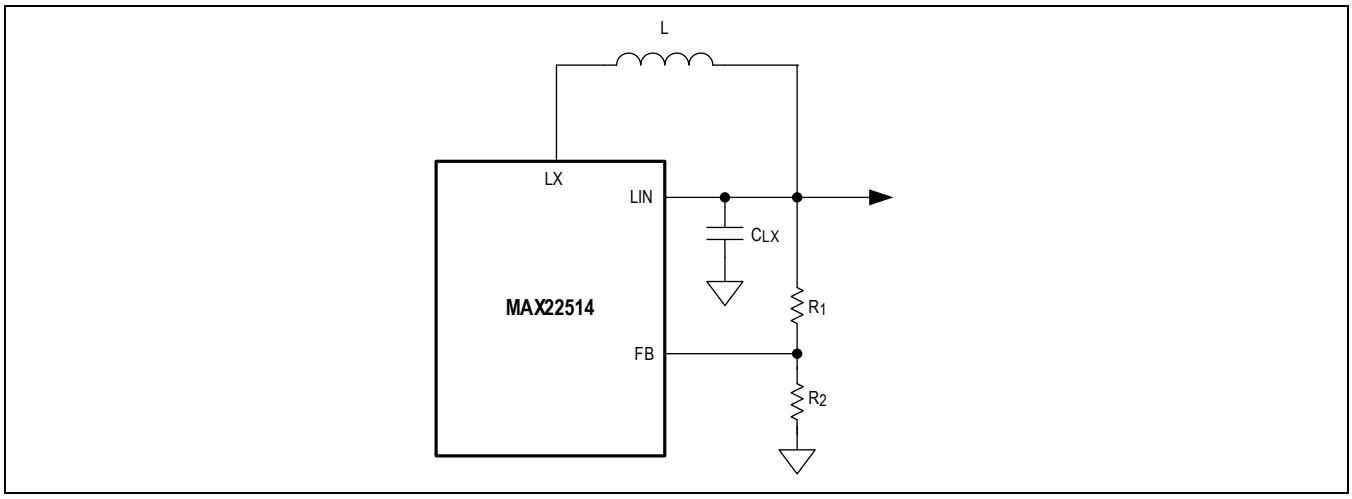


Figure 9. Setting the DC-DC Output Voltage

The R_1 resistor controls the load regulation on the load step and can also affect the value of the output capacitor to ensure stability of the DC-DC regulator. See *Table 4* for R_1 and R_2 values for common DC-DC output voltage settings.

Inductor Selection

A low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough ensure that saturation cannot occur below the 440mA maximum current-limit value. Under lower load conditions, smaller inductors can be used.

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended to use with the MAX22514 DC-DC regulator. The output capacitor has two functions: filter the square wave generated by the device along with the output inductor and stabilize the device's internal control loop. Capacitor selection depends on the operating conditions and the value of R1 and can affect the stability of the DC-DC regulator.

Typical External Components

Table 4 shows the recommended component values for the DC-DC buck regulator for a wide range of typical operating conditions (see the *Simplified Application Diagram*). Recommended values in the table are designed for <±3% load regulation on a 50% load current step and with minimum inductance. A ±30% tolerance on inductance and a ±20% tolerance on capacitance is expected due to C-V dependence.

Table 4. Typical DC-DC Component Selection

V24 (V)		OUTPUT VOLTAGE (V)	MAXIMUM OUTPUT CURRENT (mA)	L [µH]	MINIMUM C_{LX} OUTPUT CAPACITANCE [µF]	MAXIMUM C_{LX} OUTPUT CAPACITANCE [µF]	R1 [kΩ]	R2 [kΩ]
MIN	MAX							
8	36	3.3	200	15	4.7	27	226	84.5
8	36	5	200	22	3.3	17	348	75
8	36	6	200	27	3.3	14	412	73.2
9	36	7	190	33	2.7	12	499	73.2
10	36	8	190	33	2.2	11	562	71.5
10	36	9	170	33	1.8	9	634	69.8
12	36	10	180	39	1.8	8	698	69.8
12	36	11	160	39	1.5	8	768	68.1
14	36	12	180	39	1.2	7	845	68.1

DC-DC Spread Spectrum

The DC-DC regulator uses an internal clock synchronized with the main on-board oscillator that is used to generate other signals and timing. To reduce EMC emission peaks and/or reduce interference between the DC-DC switching circuitry and analog circuitry, the MAX22514 features selectable spread-spectrum functionality for the DC-DC clock. When enabled, the DC-DC clock is randomly changed with a maximum frequency deviation of ±10% (typ).

By default, DC-DC spread spectrum is disabled. Set the BUCKSS bit in the MODE register to enable spread spectrum for the DC-DC.

DC-DC Protection and Diagnostics

DC-DC Overcurrent and Runaway Protection

The DC-DC regulator includes integrated circuitry to protect the regulator during a current overload condition to avoid runaway. When the high-side current exceeds the 400mA (typ) high-side peak current limit (I_{DC_HSLIM}), the high-side switch is disabled. Similarly, when the low-side current exceeds the 200mA (typ) low-side current limit threshold (I_{DC_LSMAX}), the low-side switch is turned off and LX is floating until the next clock cycle, when switching begins again.

Hiccup Mode (Autoretry)

The DC-DC regulator features an autoretry sequence (hiccup mode) to protect against fault conditions on the output. After soft-start, if the output voltage of the DC-DC regulator falls below 70% of the set threshold, the regulator is disabled for 22ms (typ) and the BUCKFAULT bit in the STATUS2 register is set. Following the autoretry period, the DC-DC is restarted with soft-start.

If the fault on the output persists, the DC-DC is disabled and the autoretry sequence begins again. If the output voltage rises to 95% of the expected voltage, the DC-DC exits hiccup mode and operates normally.

DC-DC Power Diagnostics

The BUCKFAULT and BUCKOK bits in the STATUS2 register indicate the state of the DC-DC output. Use these bits to monitor the regulator during operation.

The BUCKOK bit is set when the output voltage is above 95% of the set voltage and the regulator is operating normally. When the DC-DC output voltage falls below 95% of the set voltage, RESET/POK asserts and the BUCKOK bit is 0.

The BUCKFAULT bit is set when regulator is in a fault condition. Fault conditions include current overload, when the output voltage falls below 70% of the set threshold, and/or when the regulator is operating in hiccup mode. The BUCKFAULT bit is cleared automatically when the regulator returns to normal operation.

Integrated Temperature Sensing

The MAX22514 monitors the die temperature during normal operation. This temperature can be read through the SPI interface and can be configured to generate a high temperature warning when the temperature rises above a set threshold. This threshold is user programmable.

The MAX22514 uses the same thermal sense circuitry to monitor the die temperature for the default thermal warning and when the programmable thermal warning methods are used. The default thermal warning system features a reduced precision, but faster response times. The programmable thermal ADC features a higher precision but slower functionality.

The high temperature warning can be disabled completely by setting the ADC_CONF bits in the THADC_CFG register.

High Temperature Warning

To protect against thermal damage, the MAX22514 monitors the die temperature during operation. The MAX22514 compares the die temperature to two different thresholds: the warning threshold and the thermal shutdown threshold. By default, the high temperature warning threshold is 150°C.

Programmable Thermal Warning

Enable the programmable thermal warning threshold by setting the ADC_CONF[1:0] bits in the THADC_CFG register to 01. Program the warning threshold by setting the THWRN[5:0] bits in the THADC_THD register. Bits in the THWRN[5:0] bits are binary-coded, with 1 LSB = 3°C and THWARN = 0 at -15°C (typ). See *Table 5*.

Table 5. Thermal ADC Conversion

Die temperature (°C)	THWARN[5:0]
0	000101 (5d)
27	001110 (14d)
84	100001 (33d)
126	101111 (47d)

The THERMWINT bit in the INTERRUPT register and the TEMPW bit in the STATUS register are set when the die temperature exceeds the thermal warning threshold. If not masked (THERMWM = 0 in the IRQMASK register), IRQ asserts when the THERWINT bit is set. THERMWINT is cleared when the INTERRUPT register is read, but THERMW is not cleared until the temperature is below the thermal warning threshold hysteresis. No hysteresis is available for the programmable warning threshold mode.

Thermal ADC

Set the ADC_CONF[1:0] bits in the THAD_CNG register to 10 or 11 to enable ADC thermal monitoring to allow the die temperature to be read over the SPI interface.

Set the ADC_START bit in the THADC_CFG register to start the thermal ADC measurement. The ADC_START bit is cleared and the ADC_EOC bit in the THADC_RES register is set after the manual ADC thermal measurement is completed after 450µs (typ). Measurement results are stored in the THVAL[5:0] bits in the THADC_RES register. Measurements are binary-coded, 1 LSB = 3°C (typ) and THVAL = 0 at -15°C (typ). Thermal ADC measurements range from -15°C to 174°C. See *Table 5*.

Thermal warning functionality is disabled when manual ADC thermal monitoring is enabled. Ignore the THERMW bit in the STATUS register and mask the thermal warning interrupt (THERMWINT in the INTERRUPT register) by setting the THERMWM = 1 in the IRQMASK register.

Protection

Reverse Polarity Protection

The MAX22514 is internally protected against reverse polarity miswiring on the V_{24}, C/Q, and GND pins. Any combination of these pins can be connected to a DC voltage in the range of -36V to +36V. Shorts to these voltages result in a current flow of less than 500µA. Note that the maximum voltage between any pins should not exceed the Absolute Maximum Ratings.

Thermal Shutdown

The MAX22514 enters thermal shutdown when the average die temperature exceeds the +170°C (typ) thermal shutdown threshold. The C/Q driver, the DC-DC regulator, and the V_5 and V_{33} regulators are disabled when the device is in thermal shutdown. The MAX22514 exits thermal shutdown when the average die temperature falls below the 20°C (typ) thermal shutdown hysteresis. Thermal shutdown is present regardless of the method of high temperature warning utilized and cannot be disabled.

Register Corruption Check

The MAX22514 performs an ongoing check of all register bits. A register is corrupted when the value is changed by an external event (for example, an ESD discharge, etc). When a corrupt register bit is detected, the CORR_REG bit in the STATUS register is set, the NOTREADY bit in the INTERRUPT register is set, and the MAX22514 asserts the IRQ output. The C/Q driver is disabled when the NOTREADY bit is set.

The microcontroller must rewrite correct values to all of the registers after the CORR_REG bit has been set. The CORR_REG bit is automatically cleared when the serial interface control registers have been rewritten to their pre-event cycle values. Once the CORR_REG bit is cleared, read the INTERRUPT register to clear the NOTREADY bit and deassert IRQ.

SPI Controller Interface

The MAX22514 supports full-duplex SPI communication at speeds up to 12MHz. The master must generate clock and data signals in SPI MODE0 (clock polarity CPOL = 0 and clock phase CPHA = 0) to communicate with the MAX22514. The SPI interface is not available when V_5 falls below 4.26V or when V_L is below 2.5V.

Figure 10 shows a single-cycle WPI write command and *Figure 11* shows a single-cycle SPI read command.

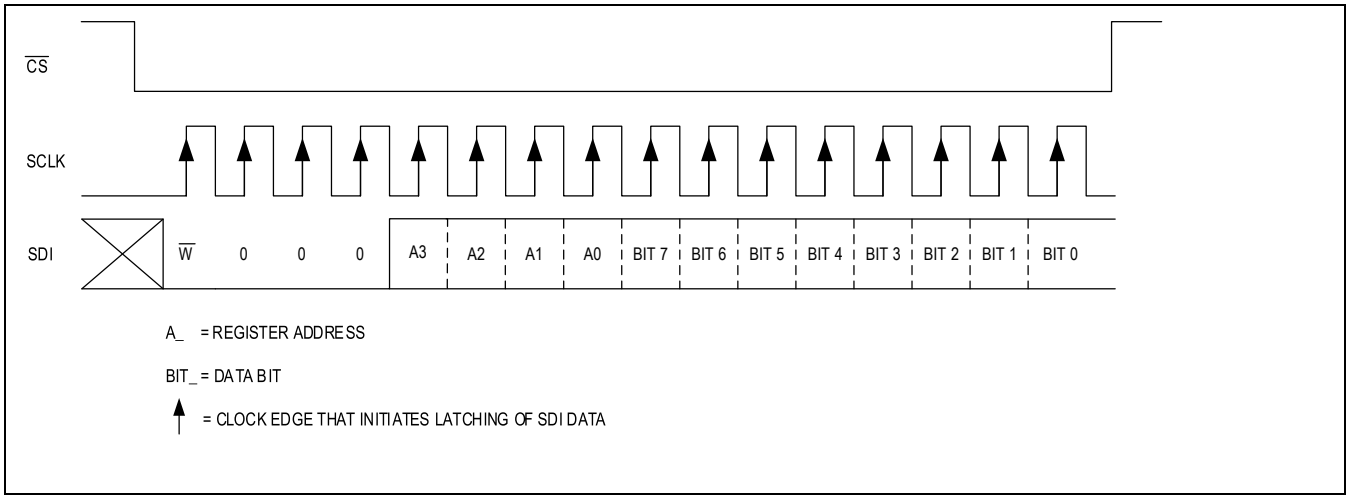


Figure 10. SPI Write Byte

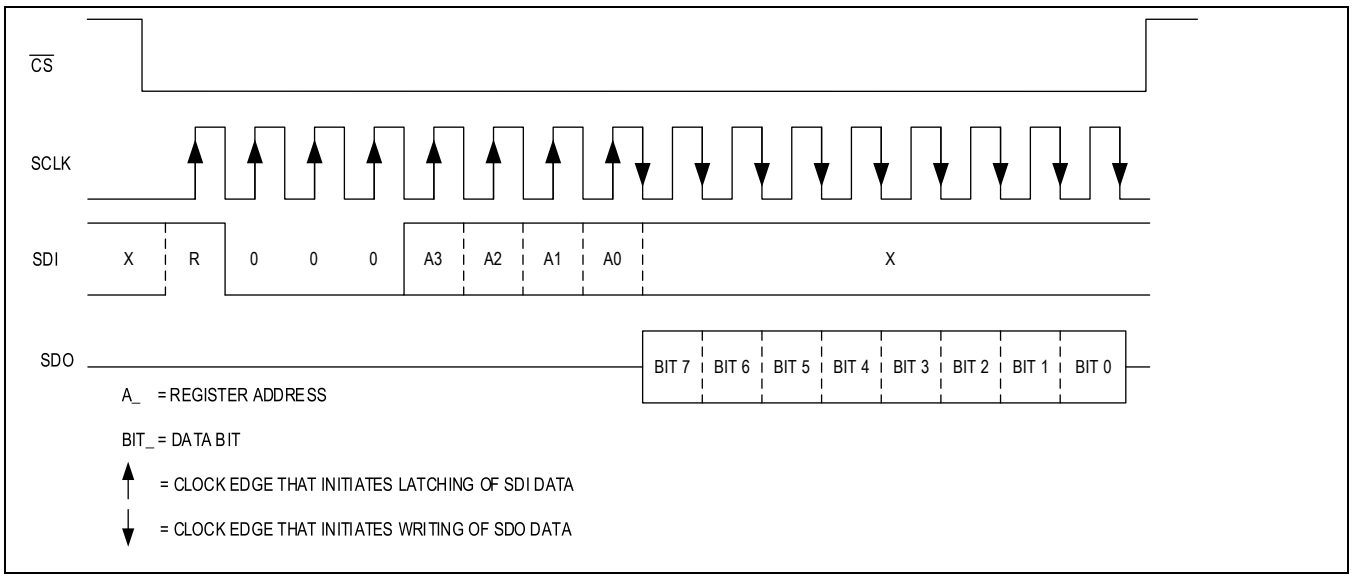


Figure 11. SPI Read Byte

Register Map

REGISTER MAP

ADDRESS	NAME	MSB							LSB
SPI User									
0x00	INTERRUPT[7:0]	NOTREADY	WUINT	THADCINT	CQFAULTINT	VMINT	UV24INT	-	THERMWINT
0x01	IRQMASK[7:0]	–	WUM	THADCM	CQFAULTM	VMINTM	UV24M	-	THERMWM
0x02	STATUS[7:0]	CQLVL	–	–	CQFAULT	VMWARN	UV24	-	THERMW
0x03	STATUS2[7:0]	CORR_REG	–	–	–	–	–	BUCKFAULT	BUCKOK
0x04	MODE[7:0]	RST	–	–	–	BUCKDCM	BUCKPFM	BUCKSS	BUCKDIS
0x05	CURRLIM[7:0]	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTORETRYEN
0x06	CONTROL[7:0]	LDO33DIS	WUDIS	–	–	RXDIS	RXFILTER	–	CQ_Q
0x07	CQCONFIG[7:0]	CQLOSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
0x09	CLKCONFIG[7:0]	ENCKTRIM	–	–	–	CLKDIV[2:0]			MCLKDIS
0x0A	CKTRIM[7:0]	–	–	CKTRIM[5:0]					
0x0B	CQMASTER[7:0]	WUGEN	–	–	RXTTL	–	–	CQPUD5MA	CQPUD2MA
0x0C	CHIPID[7:0]	CHIPID[7:0]							
0x0D	THADC_CFG[7:0]	ADC_START	–	–	–	–	–	ADC_CONF[1:0]	
0x0E	THADC_THD[7:0]	–	–	THWRN[5:0]					
0x0F	THADC_RES[7:0]	ADC_EOC	–	THVAL[5:0]					

Register Details

INTERRUPT (0x0)

The IRQ output asserts when any of the bits in the INTERRUPT register are set and the interrupt is not masked. Read the INTERRUPT register to clear the bits and deassert IRQ, once the fault condition has been removed.

BIT	7	6	5	4	3	2	1	0
Field	NOTREADY	WUINT	THADCINT	CQFAULTINT	VMINT	UV24INT	-	THERMWINT
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read, Ext	Read, Ext	Read, Ext	Read Clears All	Read, Ext

BITFIELD	BITS	DESCRIPTION
NOTREADY	7	0 = The MAX22514 is operating normally 1 = Any of the following conditions has occurred since the last INTERRUPT register read: • The V_5 supply voltage dropped below its UVLO and the registers were reset. • A power-up occurred and the registers have been reset. • At least one register has been corrupted due to an external event (not POR). The NOTREADY interrupt cannot be masked.
WUINT	6	0 = No wake-up condition has been detected. 1 = An IO-Link wake-up condition has been detected on the C/Q line since the last INTERRUPT register read.
THADCINT	5	0 = No thermal conversion has been completed. 1 = A thermal ADC conversion has been completed since the last INTERRUPT register read.
CQFAULTINT	4	0 = C/Q driver operating normally. 1 = Overcurrent/overload condition on the C/Q driver since the last INTERRUPT register read. Note that CQFAULT is only cleared if the overload condition has been removed when INTERRUPT the register is read.
VMINT	3	0 = V_M is above 900mV (typ) 1 = V_M voltage is below 858mV (typ). V_M is level sensitive. VMINT is only cleared when the V_M voltage is higher than the 900mV threshold during the INTERRUPT read.
UV24INT	2	0 = V_{24} is above the 7.5V (typ) undervoltage threshold (UVLO). 1 = The V_{24} voltage is below the the 7V (typ) undervoltage threshold. V_{24} is level sensitive. UV24INT is only cleared when the V_{24} voltage is higher than the 7.5V (typ) threshold during the INTERRUPT read.
-	1	Not used
THERMWINT	0	0 = The die temperature has not risen above the warning temperature threshold. 1 = The die temperature has risen above the warning temperature threshold since the

BITFIELD	BITS	DESCRIPTION
		last INTERRUPT register read. THWINT is only cleared if the die temperature is below the warning threshold when the INTERRUPT register is read. This bit should be ignored when manual ADC thermal conversion is enabled.

IRQMASK (0x1)

Set the bits in the IRQMASK register to ignore selected events or fault notifications. IRQ does not assert when any of the masked bits in the INTERRUPT register are set. Bits in the INTERRUPT register are not affected by the bits in the IRQMASK register, and are set when the associated event or fault notification occurs.

BIT	7	6	5	4	3	2	1	0
Field	–	WUM	THADCM	CQFAULTM	VMINTM	UV24M	-	THERMWM
Reset	–	0b0	0x0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
WUM	6	0 = IRQ asserts when the WUINT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the WUINT bit in the INTERRUPT register is set.
THADCM	5	0 = IRQ asserts when the THADCINT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the THADCINT bit in the INTERRUPT register is set.
CQFAULTM	4	0 = IRQ asserts when the CQFAULT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the CQFAULT bit in the INTERRUPT register is set.
VMINTM	3	0 = IRQ asserts when the VMINT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the VMINT bit in the INTERRUPT register is set.
UV24M	2	0 = IRQ asserts when the UV24INT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the UV24INT bit in the INTERRUPT register is masked.
-	1	Not used
THERMWM	0	0 = IRQ asserts when the THERMWINT bit in the INTERRUPT register is set. 1 = IRQ does not assert when the THERMWINT bit in the INTERRUPT register is set. Set this bit when when manual ADC thermal conversion is enabled (ADC_CONF[1:0] = 10 or 11).

STATUS (0x2)

Bits in the STATUS register indicate the current status of the MAX22514. Bits in the STATUS register are set or cleared when an event occurs and are not cleared when the register is read.

BIT	7	6	5	4	3	2	1	0

Field	CQLVL	–	–	CQFAULT	VMWARN	UV24	-	THERMW
Reset	0b0	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CQLVL	7	0 = C/Q is high. 1 = C/Q is low.
CQFAULT	4	0 = No fault on C/Q driver. 1 = Overcurrent or thermal overload fault on C/Q driver.
VMWARN	3	0 = V_M is above the 900mV (typ) threshold. 1 = V_M is below the 858mV (typ) threshold.
UV24	2	0 = V_{24} is above the 7.5V (typ) rising undervoltage lockout (UVLO) threshold. 1 = V_{24} is below the 7V (typ) falling UVLO threshold.
-	1	Not used
THERMW	0	0 = The die temperature is below the 130°C (typ, falling) warning threshold temperature. 1 = The die temperature is above the 150°C (typ, rising) warning threshold temperature. This bit should be ignored when manual ADC thermal conversion is enabled (ADC_CONF[1:0] = 10 or 11).

STATUS2 (0x3)

Bits in the STATUS2 register indicate the current status of the MAX22514 registers and the DC-DC regulator operation. Bits in the STATUS2 register are set or cleared when an event occurs and are not cleared when the register is read.

BIT	7	6	5	4	3	2	1	0
Field	CORR_REG	–	–	–	–	–	BUCKFAULT	BUCKOK
Reset	0b0	–	–	–	–	–	0b0	0b1
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CORR_REG	7	0 = All register values are correct. 1 = Register values are corrupted. C/Q is disabled and RX is high impedance when CORR_REG = 1. V_{33} and DC-DC are also forced on and the signal at MCLK is enabled and switching at 3.686MHz (typ).
BUCKFAULT	1	0 = The DC-DC is operating normally. No fault conditions are present. 1 = A fault condition is present on the DC-DC regulator. Fault conditions include output

BITFIELD	BITS	DESCRIPTION
		overcurrent/overload, the output voltage falls below 70% of the set voltage, and when the regulator is in hiccup mode.
BUCKOK	0	0 = The DC-DC regulator is not ready or has a fault condition. 1 = The DC-DC regulator is operating normally in the steady state condition and is ready to be used.

MODE (0x4)

BIT	7	6	5	4	3	2	1	0
Field	RST	–	–	–	BUCKDCM	BUCKPFM	BUCKSS	BUCKDIS
Reset	0b0	–	–	–	0b0	0b0	0b0	0b0
Access Type	Write Only Clears All	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RST	7	0 = Registers are not in reset state. 1 = Set all registers to their default state. RST clears automatically.
BUCKDCM	3	0 = The DC-DC regulator operates in PFM mode (BUCKPFM = 1) or PWM mode (BUCKPFM = 0) after soft-start is complete. See the BUCKPFM bit setting. 1 = The DC-DC regulator operates in DCM mode after soft-start is complete.
BUCKPFM	2	0 = The DC-DC regulator operates in PWM mode (BUCKDCM = 0) or DCM mode (BUCKDCM = 1). 1 = The DC-DC regulator operates in PFM mode.
BUCKSS	1	0 = Spread spectrum operation is not enabled on the DC-DC regulator. 1 = Spread spectrum operation is enabled on the DC-DC regulator.
BUCKDIS	0	0 = DC-DC regulator is enabled. 1 = DC-DC regulator is disabled.

CURRLIM (0x5)

BIT	7	6	5	4	3	2	1	0
Field	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTORETRY EN
Reset	0b00		0b0	0b00		0b00		0b0
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
CL	7:6	CL[1:0] bits set the active current limit levels for the C/Q driver when CLDIS = 0. 00 = 50mA (min) current limit 01 = 100mA (min) current limit 10 = 200mA (min) current limit 11 = 250mA (min) current limit
CLDIS	5	0 = C/Q driver current limits are enabled. Current limits are set by the CL[1:0] bits. The C/Q rising/falling slew rates are set by the CQLOSLEW bits. 1 = C/Q driver current limits are disabled. The C/Q rising/falling slew rate is set to 380ns (typ).
CL_BL	4:3	Set the CL_BL[1:0] to program the blanking time for the C/Q driver: 00 = 175µs (typ) 01 = 500µs (typ) 10 = 1ms (typ) 11 = 5ms (typ)
TAR	2:1	Set the TAR[1:0] bits to select the fixed off-time for the C/Q driver after a fault has been generated and autoretry functionality is enabled (AUTORETRYEN = 1). 00 = 50ms (typ) 01 = 100ms (typ) 10 = 200ms (typ) 11 = 500ms (typ) The driver is automatically reenabled after the fixed off-delay.
AUTORETRYEN	0	0 = Autoretry is disabled on the C/Q driver. 1 = Autoretry is enabled on the C/Q driver. When a fault is signaled on the driver, the driver is disabled for the selected fixed off time and then automatically reenabled.

CONTROL (0x6)

BIT	7	6	5	4	3	2	1	0
Field	LDO33DIS	WUDIS	–	–	RXDIS	RXFILTER	–	CQ_Q
Reset	0b0	0b0	–	–	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	–	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO33DIS	7	0 = V_{33} linear regulator is enabled. 1 = V_{33} linear regulator is disabled.

BITFIELD	BITS	DESCRIPTION
WUDIS	6	0 = IO-Link wake-up detection is enabled. 1 = IO-Link wake-up detection is disabled.
RXDIS	3	0 = RX logic output is enabled. 1 = RX logic output is disabled. RX is high impedance. The C/Q input current is reduced when RXDIS = 1.
RXFILTER	2	0 = The 1µs (typ) glitch filter on the C/Q receiver is disabled. 1 = The 1µs (typ) glitch filter on the C/Q receiver is enabled.
CQ_Q	0	Use the CQ_Q bit to control the C/Q driver output. See Table 1 for more information.

CQCONFIG (0x7)

BIT	7	6	5	4	3	2	1	0
Field	CQLOSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
Reset	0b00		0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CQLOSLEW	7:6	Set the CQLOSLEW[1:0] bits to program the typical rising and falling slew rates on the C/Q driver. 00 = 380ns (typ) 01 = 700ns (typ) 10 = 1.7µs (typ) 11 = 7.5µs (typ) CQLOSLEW is ignored when the CLDIS bit is set.
CQ_PD	5	0 = The pull-down current on the C/Q driver is disabled. 1 = Enable the pull-down current on the C/Q driver. See Table 3 for more information.
CQ_PU	4	0 = The pull-up current on the C/Q driver is disabled. 1 = Enable the pull-up current on the C/Q driver. See Table 3 for more information.
CQ_NPN	3	0 = The C/Q driver is in PNP mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1). 1 = The C/Q driver is in NPN mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1).
CQ_PP	2	0 = The C/Q driver is in PNP mode (CQ_NPN = 0) or NPN mode (CQ_NPN = 1). 1 = The C/Q driver is in push-pull mode.

BITFIELD	BITS	DESCRIPTION
INVCQ	1	0 = C/Q logic is inverted compared to TX and RX. 1 = C/Q logic is the same as TX and RX.
CQ_EN	0	0 = C/Q driver is disabled. 1 = C/Q driver is enabled.

CLKCONFIG (0x9)

BIT	7	6	5	4	3	2	1	0
Field	ENCKTRIM	–	–	–	CLKDIV[2:0]			MCLKDIS
Reset	0b0	–	–	–	0b000			0b0
Access Type	Write, Read	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION
ENCKTRIM	7	0 = Fine trimming of the MCLK frequency is disabled. 1 = Fine trimming of the MCLK frequency is enabled. See the CKTRIM register.
CLKDIV	3:1	Set the CLKDIV[1:0] bits to select the internal clock divider ratio and MCLK switching frequency: 000 = MCLK frequency is 3.686MHz (typ) (default) 001 = MCLK frequency is 7.373MHz (typ) 010 = MCLK frequency is 14.74MHz (typ) 011 = MCLK frequency is 29.49MHz (typ) 100 = MCLK frequency is 1.843MHz (typ) MCLK switches at 3.686MHz (typ) at power-up.
MCLKDIS	0	0 = MCLK is enabled. 1 = MCLK is disabled. MCLK is high when disabled.

CKTRIM (0xA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CKTRIM[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
CKTRIM	5:0	The CKTRIM[5:0] bits are used to trim the internally generated clock frequency. The bits are binary coded, centered to 0 from -5% for -32 to +6.7% for +31.

CQMASTER (0xB)

BIT	7	6	5	4	3	2	1	0
Field	WUGEN	–	–	RXTTL	–	–	CQPUD5MA	CQPUD2MA
Reset	0x0	–	–	0x0	–	–	0x0	0x0
Access Type	Write, Read	–	–	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
WUGEN	7	0 = No wake-up pulse is generated on C/Q 1 = Generate a 80µs (typ) wake-up pulse on C/Q. Program C/Q to push-pull mode and set CQ_EN = 0 and TXEN = low before setting WUGEN = 1. WUGEN is automatically reset after the wake-up pulse is generated.
RXTTL	4	0 = IO-Link receiver thresholds enabled for C/Q receiver 1 = TTL receiver thresholds enabled for C/Q receiver
CQPUD5MA	1	0 = The 5mA (min) current on C/Q is disabled. 1 = Enables the 5mA (min) current on the C/Q driver.
CQPUD2MA	0	0 = The 2mA (min) current on C/Q is disabled. 1 = Enables the 2mA (min) current on the C/Q driver.

CHIPID (0xC)

BIT	7	6	5	4	3	2	1	0
Field	CHIPID[7:0]							
Reset	0x13							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CHIPID	7:0	The CHIPID register identifies the revision of the MAX22514.

THADC_CFG (0xD)

BIT	7	6	5	4	3	2	1	0
Field	ADC_START	–	–	–	–	–	ADC_CONF[1:0]	
Reset	0b0	–	–	–	–	–	0b00	
Access Type	Write, Read	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
ADC_START	7	0 = No manual thermal ADC conversion. 1 = Start a new manual thermal ADC conversion. Set ADC_CONF[1:0] = 10 or 11 to enable manual thermal ADC conversion. Results of the thermal conversion are stored in the THADC_RES register when the conversion is complete. This bit is automatically cleared when the manual ADC conversion is complete.
ADC_CONF	1:0	00 = Internal/Default thermal warning threshold and response time is enabled. 01 = Programmable thermal warning threshold is enabled. 1x = Manual thermal ADC is enabled. Thermal warning is disabled in this mode.

THADC_THD (0xE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	THWRN[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
THWRN	5:0	Set ADC_CONF[1:0] = 01 to enable the programmable thermal warning threshold. Program the THWRN[5:0] bits to set the thermal warning threshold. Scaling is the same as for the THVAL[5:0] bits in the THADC_RES register. The THERMWINT and THERMW bits are set when the die temperature exceeds this threshold. There is no hysteresis when the programmable thermal warning threshold is enabled.

THADC_RES (0xF)

BIT	7	6	5	4	3	2	1	0

Field	ADC_EOC	–	THVAL[5:0]
Reset	0b0	–	0b000000
Access Type	Read Only	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ADC_EOC	7	Set the ADC_CONF[1:0] bits to 10 or 11 to enable manual thermal ADC conversion. 0 = Thermal ADC conversion is complete and THVAL[5:0] bits hold the latest thermal ADC conversion value 1 = Thermal ADC conversion is running. Value in THVAL[5:0] bits is not valid.
THVAL	5:0	This register holds the results of the latest thermal conversion. Bits are binary coded with 1LSB = 3°C and THVAL = 0 at -15°C (typ). See Table 5.

Applications Information

MCLK Microcontroller Clocking

The MCLK output produces a clock that can be used for microcontroller/IO-Link UART clocking.

Select the frequency of the MCLK output by setting the CLKDIV[2:0] bits in the CLKCONFIG register. Available MCLK frequencies are 1.843MHz (typ), 3.686MHz (typ), 7.373MHz (typ), 14.74MHz (typ), and 29.49MHz (typ). The MCLK frequency can be finely adjusted by setting the ENCKTRIM bit in the CLKCONFIG register to 1 and writing the CKTRIM bits in the CKTRIM register. The CKTRIM bits are used to trim the internally generated clock frequency. The bits are binary coded and centered to 0 from -5% for -32, and to +6.7% for +31.

MCLK is enabled by default at power up and the switching frequency is 3.686MHz (typ). MCLK voltage output levels are referenced to the V_L logic supply.

EMC Protection

The MAX22514 features integrated surge protection of ±1kV/500Ω for 8µs/20µs surge on the C/Q and V_{24} pins. External TVS diodes are required to meet higher levels of surge and ESD protection. Ensure that the TVS diode peak clamping voltage is within the Absolute Maximum voltage ratings.

Power Dissipation and Thermal Considerations

Ensure that the total power dissipation in the MAX22514 is less than the limit in the Absolute Maximum Ratings. Total power dissipation for the MAX22514 is calculated using the following equation:

$$P_{TOTAL} = P_Q + PV_5 + PV_{33} + P_{C/Q}$$

where:

P_Q = Quiescent power generated in MAX22514,

$P_{C/Q}$ = Power generated in the C/Q driver,

PV_{33} and PV_5 = Power generated by the internal linear regulators

Quiescent power dissipated in the MAX22514 is calculated as:

$$P_Q = [I_{24} \times V_{24}(max)] + [I_5 \times V_5]$$

Power dissipated in the C/Q driver is calculated as:

$$P_{C/Q} = I_{C/Q}(max)^2 \times R_{ON}$$

$I_{C/Q}$ is the load current driven by the C/Q driver and R_{ON} is the driver on-resistance.

Power dissipated in the 5V linear regulator (V_5) is calculated as:

$$P_{V5} = (V_{LIN} - V_5) \times I_{5LOAD}$$

I_{5LOAD} includes both the load current on the V_5 regulator and the 3.3V regulator.

Power dissipated in the 3.3V linear regulator (V_{33}) is calculated as:

$$P_{V33} = 1.7V \times I_{33LOAD}$$

I_{33LOAD} is the load on the 3.3V regulator

Layout and Grounding

Layout for the MAX22514 is important to ensure that all parts operate normally and with minimal interference.

The MAX22514 features two ground pins: GND, CQGND.

Bypass all supply pins (V_5, V_L, and PV_{24}) to the GND pin and connect directly to a ground plane. Bypass capacitors should be placed as close to the IC as possible.

The V_{24}, C/Q, and CQGND pins are connected directly to the IO-Link connector. Connect all bypass capacitors and other components on this line directly to the CQGND. Connect the CQGND to the ground layer at the IC (at the exposed pad for the TQFN or under pad D8 on the WLP package).

Keep the component loop for the DC-DC buck regulator as small as possible. Ensure that the feedback resistor divider is not near the inductor. Connect the ground terminal of the DC-DC output capacitor to the ground plane with multiple vias.

Figure 12 shows an example of layout and grounding connections.

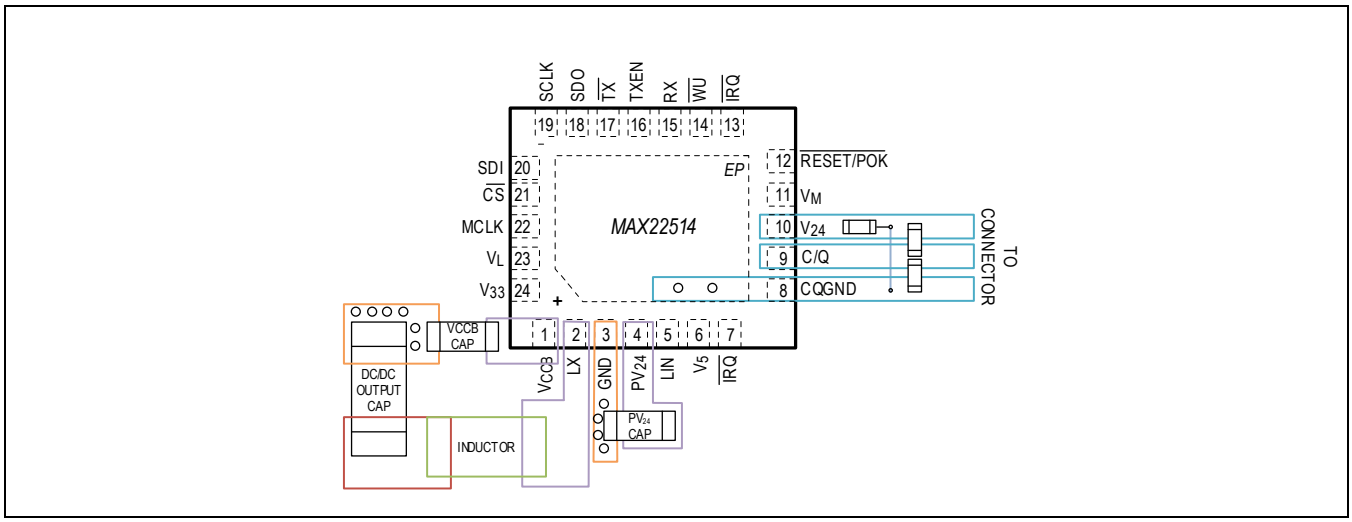


Figure 12. Sample Grounding Scheme (TQFN Package)

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	BALL PITCH
MAX22514ATG+	-40°C to +125°C	24 TQFN-EP*	—
MAX22514ATG+T	-40°C to +125°C	24 TQFN-EP*	—
MAX22514AWA+	-40°C to +125°C	25 WLP	0.5
MAX22514AWA+T	-40°C to +125°C	25 WLP	0.5

+Denotes a lead(pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS