*Click **here** for production status of specific part numbers.*

MAX22520

One-Time Programmable (OTP) Industrial Sensor Output Driver

General Description

The MAX22520 24V line driver for industrial sensors incorporates a one-time programmable (OTP) analog interface for signal conditioning of binary switching sensors. Sensor calibration and configuration settings can be permanently programmed with the inline data interface using one-time programming (OTP). Additionally, an accurate integrated linear regulator provides a programmable (3.3V or 5V) low-noise supply for analog signal sensing circuitry.

The driver output (DO) is configurable using the Maxim® 1-Wire® protocol and an OTP interface to permanently operate in a normally-open or normally-closed state and in a high-side (PNP), low-side (NPN), or push-pull configuration. The maximum driver load current can be programmed to 100mA (min) or 200mA (min).

Configuration and OTP programming are done using V_{CC}, DO, and GND. This use of the standard three-wire interface pins simplifies programming at the end-of-line, when the sensor is already in its final housing.

The MAX22520 also features a programmable comparator, PWM oscillator, and digital potentiometer. These integrated functions further support sensor calibration for analog sensing circuitry. Additionally, an on-board LED driver provides visual feedback of the logic state of the sensor DO output.

Robust protection enables the MAX22520 to function in harsh industrial environments. DO, V_{CC}, and GND are all protected against hot-plug events, ±1kV/500Ω surge events, reverse-polarity, short circuits, and ESD strikes.

The MAX22520 operates from a wide 4.75V/8V to 36V supply and is available in a 20-bump wafer-level package (WLP) (2mm x 2.5mm, 0.5mm pitch). The device operates over the -40°C to +105°C temperature range.

Applications

- Industrial Binary Sensors
- Proximity Switches
- Inductive and Magnetic Sensors

Benefits and Features

- High Configurability Supports a Wide Range of Sensor Designs
  - Programmable Driver Configuration: High-Side (PNP), Low-Side (NPN), or Push-Pull
  - Programmable Driver Current Limit: 100mA (min), 200mA (min)
  - Programmable Linear Regulator Voltage: 3.3V (typ), 5V (typ)
  - Input Comparator with Programmable Thresholds
  - Digital Potentiometer with Programmable 6-bit Tap
  - PWM Oscillator with Programmable Duty Cycles
  - 4.75V/8V (min) to +36V Supply Voltage
  - Integrated LED Driver for Visual Feedback
- Robust Design for Harsh Industrial Environments
  - Reverse Polarity Protection on DO, V_{CC}, and GND
  - Short Circuit Protection on DO
  - Thermal Shutdown Protection
  - ±6kV IEC 61000-4-2 Air-Gap ESD Protection
  - ±6kV IEC 61000-4-2 Contact Discharge ESD Protection
  - ±1kV/500Ω IEC 61000-4-5 Surge Protection
  - -40°C to +105°C Operating Temperature Range
  - 1µF Capacitive Load Drive Capability
  - Fast Demagnetization of Inductive Loads
- Small Form Factor for Compact Designs
  - Ultra-Small (2mm x 2.5mm) 20-bump WLP

***Ordering Information** appears at end of data sheet.*

19-100601; Rev 1; 12/19

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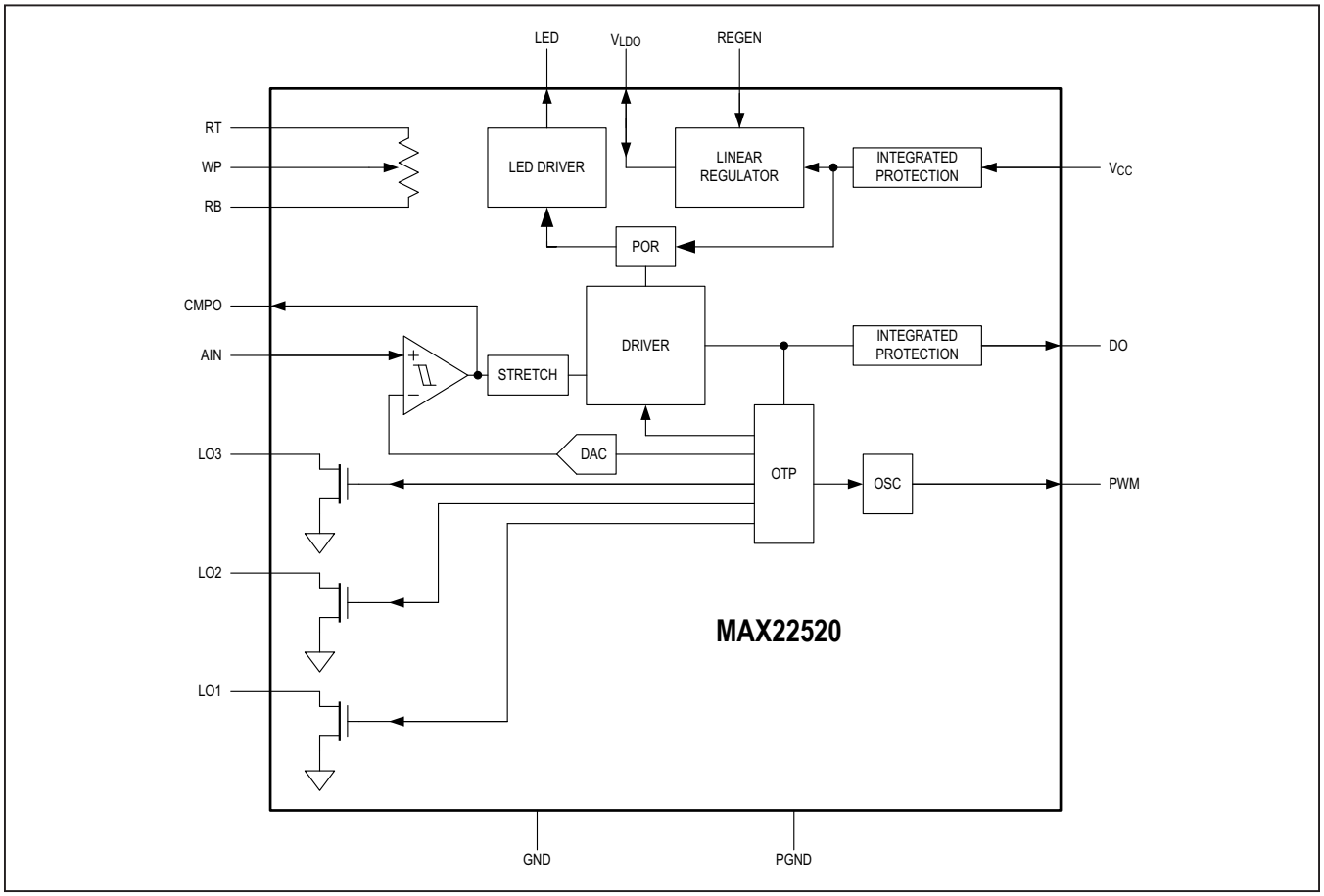
Simplified Block Diagram



Absolute Maximum Ratings

All voltages referenced to GND unless otherwise specified.

V_{CC} ..... -36V to +36V
PGND ..... -0.3V to +0.3V
DO ..... max[(V_{CC} – 36V), -36V] to min[(V_{CC} + 36V), +36V]
REGEN ..... -0.3V to min[(V_{CC} + 0.3V), +6V]
V_{LDO} ..... -0.3V to min[(V_{CC} + 0.3V), +6V]
LO1, LO2, LO3, CMPO, AIN, PWM, LED ..... -0.3V to (V_{LDO} + 0.3V)
RT, RB, WP ..... -0.3V to (V_{LDO} + 0.3V)
Continuous Current into V_{CC} and GND ..... ±1A
Continuous Current into DO ..... ±500mA
Continuous Current into Any Other Pin ..... ±50mA
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate at 21mW/°C above +70°C) 1500mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: WLP20	
Package Code	W201K2+1
Outline Number	**21-1000314**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	47.6°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to 36V, GND = 0V, C_{LDO} = 0.1µF to 1.2µF, C_{LOAD} on DO = 1nF, REGEN is unconnected, all logic inputs at V_{LDO} or GND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY (V_{CC})							
Supply Voltage	V_{CC}	V_{LDO} = 3.3V		4.75		36	V
		V_{LDO} = 5V		8		36	
V_{CC} Undervoltage Lockout (UVLO) Threshold	V_{TH}	V_{CC} rising, DO active	V_{LDO} = 3.3V	4.1		4.7	V
			V_{LDO} = 5V	6.0		7.0	
V_{CC} UVLO Threshold Hysteresis	V_{HTH}	V_{LDO} = 3.3V or 5V			0.5		V
V_{CC} UVLO Debounce Filter	t_{UVLO_FLT}	V_{CC} rising		50	64	80	µs
V_{CC} Supply Current	I_{CC}	V_{CC} = 24V, no external load on V_{LDO}, LED is off, RT, WP, and RB are unconnected, no load on DO	Normal operation, PWM enabled, DO in NPN or push-pull mode		2.2	3.5	mA
			Slave mode operation, PWM disabled, DO is in PNP mode		1.3	2.2	
OTP PROGRAMMING MODE (V_{CC}, DO)							
V_{CC} Supply in 1-Wire Access Mode	V_{CC_OA}			3.5		4.1	V
I_{CC} Supply Current in 1-Wire Access Mode	I_{CC_OA}					3	mA
V_{CC} Supply 1-Wire RAM Mode	V_{CC_OWA}			3.5		36	V
I_{CC} Supply Current in 1-Wire RAM Mode	I_{CC_OWA}	3.8V ≤ V_{CC} ≤ 36V				5	mA
V_{CC} Supply During OTP Burn	V_{CC_OB}			12		34	V
I_{CC} Supply Current in OTP Burn	I_{CC_OB}	V_{CC} = V_{CC_OB}			24		mA
DO Receiver Rising Input Threshold	$V_{DO\_RX\_R}$	1-Wire OTP access and 1-Wire RAM			1.2	2	V
DO Receiver Falling Input Threshold	$V_{DO\_RX\_F}$	1-Wire OTP access and 1-Wire RAM		0.6	1.1		V
Required External Pullup Voltage on DO During 1-Wire Communication	V_{DO_PU}	1-Wire OTP access and 1-Wire RAM				5.5	V
DO Output Low Voltage During 1-Wire Communication	V_{OL}	100Ω pullup between DO and V_{CC}, V_{CC} = V_{DO_PU}				0.3	V

Electrical Characteristics (continued)

(V_{CC} = $V_{CC(MIN)}$ to 36V, GND = 0V, C_{LDO} = 0.1µF to 1.2µF, C_{LOAD} on DO = 1nF, REGEN is unconnected, all logic inputs at V_{LDO} or GND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR (V_{LDO}, REGEN)							
LDO Output Voltage	V_{LDO}	REGEN is unconnected, $V_{CC(MIN)}$ ≤ V_{CC} ≤ 36V, I_{LOAD} = 30mA	LDOVSET = 0	3.17	3.30	3.43	V
			LDOVSET = 1	4.8	5.0	5.2	
External V_{LDO} Supply Power-OK Threshold	V_{LDO_OK}	REGEN = GND, $V_{CC(MIN)}$ ≤ V_{CC} ≤ 36V (Note 2)	LDOVSET = 0	2.3	2.47	2.7	V
			LDOVSET = 1	3.6	3.75	3.9	
External V_{LDO} Supply Undervoltage Lockout Threshold Voltage	V_{LDO_UVLO}	REGEN = GND, $V_{CC(MIN)}$ ≤ V_{CC} ≤ 36V (Note 2)	LDOVSET = 0	1.9	2.07	2.2	V
			LDOVSET = 1	3.2	3.35	3.5	
LDO Short Circuit Current Limit	I_{LDO_SC}	V_{LDO} shorted to GND		35			mA
V_{LDO} Change Over Temperature	ΔV_{LDO}	I_{LOAD} = 1mA, -40°C ≤ T_A ≤ 105°C	V_{LDO} = 3.3V		5.6		mV
			V_{LDO} = 5V		7.5		
V_{LDO} Line Regulation		8V ≤ V_{CC} ≤ 36V, I_{LOAD} = 1mA			1		mV
V_{LDO} Load Regulation		V_{LDO} = 3.3V or 5V, 1mA ≤ I_{LOAD} ≤ 30mA			6		mV
LDO Power Supply Rejection Ratio	PSRR	I_{LOAD} = 10mA, f = 100Hz, 500mV_{PP}			60		µV
DRIVER (DO)							
DO High-Side On-Resistance	R_{ON_H}	I_{SOURCE} = 200mA			2	4.2	Ω
DO Low-Side On-Resistance	R_{ON_L}	I_{SINK} = 200mA			2	4.2	Ω
DO Current Limit	$\|I_{DO\_CL}\|$	DO enabled	DOILIM = 0	110	132	159	mA
			DOILIM = 1	220	264	317	
DO Leakage Current	$I_{LKG\_DO\_PP}$	DO in push-pull mode and high impedance, 0V ≤ V_{DO} ≤ V_{CC} (Note 3)		-12		+12	µA
DO Weak Pulldown	$I_{LKG\_DO\_HS}$	DO in PNP mode and high impedance, 0V ≤ V_{DO} ≤ V_{CC}, DOPUPD[1:0] = 10		+150	+347	+450	µA
DO Weak Pullup	$I_{LKG\_DO\_LS}$	DO in NPN mode and high impedance, 0V ≤ V_{DO} ≤ V_{CC}, DOPUPD[1:0] = 01		-450	-320	-150	µA
DO Output Negative Clamp Voltage	V_{CLN}	DO in PNP mode, 200mA clamp current flowing into DO			V_{CC}-42V	V_{CC}-36V	V
DO Output Positive Clamp Voltage	V_{CLP}	DO in NPN mode, 200mA clamp current flowing out of DO		36	42		V

Electrical Characteristics (continued)

(V_{CC} = $V_{CC(MIN)}$ to 36V, GND = 0V, C_{LDO} = 0.1µF to 1.2µF, C_{LOAD} on DO = 1nF, REGEN is unconnected, all logic inputs at V_{LDO} or GND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS (LO1, LO2, LO3, CMPO, PWM, LED)						
Logic Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
Logic Output High Voltage	V_{OH}	LED, CMPO, PWM in push-pull, I_{SOURCE} = 5mA	V_{LDO}- 0.4			V
Open-Drain Leakage	I_{LEAK_LO}	LO1, LO2, LO3, PWM in open-drain, output is high impedance, V_{OUT} = V_{LDO} or GND	-1		+1	µA
COMPARATOR (AIN)						
Number of OTP Programmable Thresholds	NV_{TH}	V_{T1}, V_{T2} (Note 4)		2		
Comparator Threshold Range	V_{TH_R}		0		V_{LDO} - 0.9	V
Comparator Threshold Resolution in OTP	V_{TH_RES}			6		Bits
Comparator Threshold Differential Nonlinearity (DNL)	V_{TH_DNL}		-0.9		+0.9	LSB
Comparator Threshold Temperature Variation	ΔV_{TH}	Includes comparator and DAC, REGEN = GND, 3.1V ≤ V_{LDO} ≤ 5.2V (Note 5)	-9		+9	mV
PWM OSCILLATOR (PWM)						
Number of OTP Programmable Duty Cycles	$NPWM_{DC}$	(Note 6)		2		
Number of Programmable PWM Duty Cycle Steps	DC_{STEPS}	High-to-low/Open-to-closed ratio		512		
PWM Duty Cycle Range	DC_{RNG}	High-to-low/Open-to-closed ratio	0		99.8	%
PWM Duty Cycle Variation Over Temperature	ΔDC_{TMPCO}		0		0	%
DIGIPOT (RT, RB, WP)						
End-to-End Resistance	R_{EE}	RT to RB, WP unconnected	6.5	10	13.5	kΩ
End-to-End Temperature Coefficient	TC_{EE}	RT to RB, WP unconnected, -40°C ≤ T_A ≤ +105°C		-25		ppm/°C
Wiper Output Impedance	R_{WP}	RT = V_{LDO}, RB = GND; V_{LDO} = 3.3V			7.6	kΩ
		RT = V_{LDO}, RB = GND; V_{LDO} = 5V			9	kΩ
Wiper Output Impedance Temperature Variation	R_{WP_TC}	RT = V_{LDO}, RB = GND, I_{LOAD} = 1µA on WP		0.18		%/°C

Electrical Characteristics (continued)

(V_{CC} = $V_{CC(MIN)}$ to 36V, GND = 0V, C_{LDO} = 0.1µF to 1.2µF, C_{LOAD} on DO = 1nF, REGEN is unconnected, all logic inputs at V_{LDO} or GND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Number of Programmable Digipot Wiper Steps	WP_{STEPS}	Linear			64		
Wiper Setting Minimum Value	S_{MIN}	DIGIPOTSET[5:0] = 000000			0		%
Wiper Setting Maximum Value	S_{MAX}	DIGIPOTSET[5:0] = 111111			100		%
Wiper Setting Differential Nonlinearity (DNL)	RES_{DNL}			-0.5		+0.5	LSB
PROTECTION							
Thermal Shutdown	T_{SHDN}	Junction temperature rising			+150		°C
Thermal Shutdown Hysteresis	T_{SH_HYS}				15		°C
Reverse Polarity Current	I_{RP}	Any combination of V_{CC}, DO, and GND			±0.55		mA
ESD Protection (V_{CC}, DO)		IEC 61000-4-2 Contact Discharge, C_{LOAD} = 1nF on DO			±6		kV
		IEC 61000-4-2 Airgap Discharge, C_{LOAD} = 1nF on DO			±6		
ESD Protection (All Other Pins)		Human Body Model			±2		kV
SWITCHING CHARACTERISTICS / POWER ON RESET (POR) TIMING							
DO, LED POR Delay	t_{PU_DO}	Delay after V_{CC} rises above V_{TH} until DO and LED are active	PORDLY[1:0] = 00	6	8	10	ms
			PORDLY[1:0] = 01	9	12	15	
			PORDLY[1:0] = 10	12	16	20	
			PORDLY[1:0] = 11	30	40	50	
POR Delay (All Other Pins)	t_{PU_O}					1	ms
SWITCHING CHARACTERISTICS / DO DRIVER TIMING							
Low-to-High Driver Propagation Delay	t_{PLH}	AIN to DO, V_{CC} = 24V, C_L = 4nF, R_L = 5kΩ, to 50%, Push-pull or PNP mode, Figure 1			9	16.5	µs
High-to-Low Driver Propagation Delay	t_{PHL}	AIN to DO, V_{CC} = 24V, C_L = 4nF, R_L = 5kΩ, to 50%, Push-pull or NPN mode, Figure 1			9	16.5	µs
DO Output Rise Time	t_{RISE}	V_{CC} = 24V, C_L = 4nF, R_L = 5 kΩ, 10% to 90%, Push-pull mode, Figure 1			6	12	µs
DO Output Fall Time	t_{FALL}	V_{CC} = 24V, C_L = 4nF, R_L = 5 kΩ, 90% to 10%, Push-pull mode, Figure 1			6	12	µs

Electrical Characteristics (continued)

(V_{CC} = $V_{CC(MIN)}$ to 36V, GND = 0V, C_{LDO} = 0.1µF to 1.2µF, C_{LOAD} on DO = 1nF, REGEN is unconnected, all logic inputs at V_{LDO} or GND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS / DO DRIVER PULSE STRETCH TIMING						
DO Stretched Pulse Length	t_{PS}	DO pulse stretching enabled (PLSTEN = 1), AIN positive input pulse length < t_{PS}.	3.5	4.0	4.5	ms
SWITCHING CHARACTERISTICS / COMPARATOR TIMING (AIN, CMPO)						
Comparator AIN to CMPO Propagation Delay	t_{COM_PD}	AIN to CMPO	0.5	0.65	0.9	µs
AIN Rejected Input Pulse	t_{PR}		0		200	ns
SWITCHING CHARACTERISTICS / DO DRIVER OVERCURRENT AUTORETRY TIMING						
DO Overcurrent Detection Time	$t_{ILIMDET}$			500		µs
DO Overcurrent Turn-off Time	$t_{ILIMOFF}$			50		ms
SWITCHING CHARACTERISTICS / PWM OSCILLATOR TIMING						
PWM Oscillator Start-up Time	t_{PWM}	V_{CC} rises above V_{TH} to PWM active		64		µs
PWM Oscillator Center Frequency	f_{PWM_C}		28	34	40	kHz
PWM Duty Cycle Switching Delay	t_{PWM_SW}	Duty cycle switches after comparator logic output change		50		µs

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Program the LDOVSET bit in the OTP registers to set the UVLO threshold for V_{LDO} when the internal regulator is disabled (REGEN = GND) and an external supply is connected to V_{LDO}.

Note 3: DO driver cannot be disabled during normal operation. When in push-pull configuration, the DO driver is in a high impedance state during thermal shutdown or during the power-on-reset (POR) delay.

Note 4: Up to two comparator thresholds (V_{T1} and V_{T2}) can be programmed in the OTP registers. If only one threshold is needed, set V_{T1} = V_{T2}. See the *Input Comparator (AIN, CMPO)* section for more information.

Note 5: Not production tested. Guaranteed by design.

Note 6: Up to two duty cycles (DC1 and DC2) can be programmed for the PWM output in the OTP registers. If only one duty cycle is needed, set DC1 = DC2. See the *PWM Oscillator* section for more information.

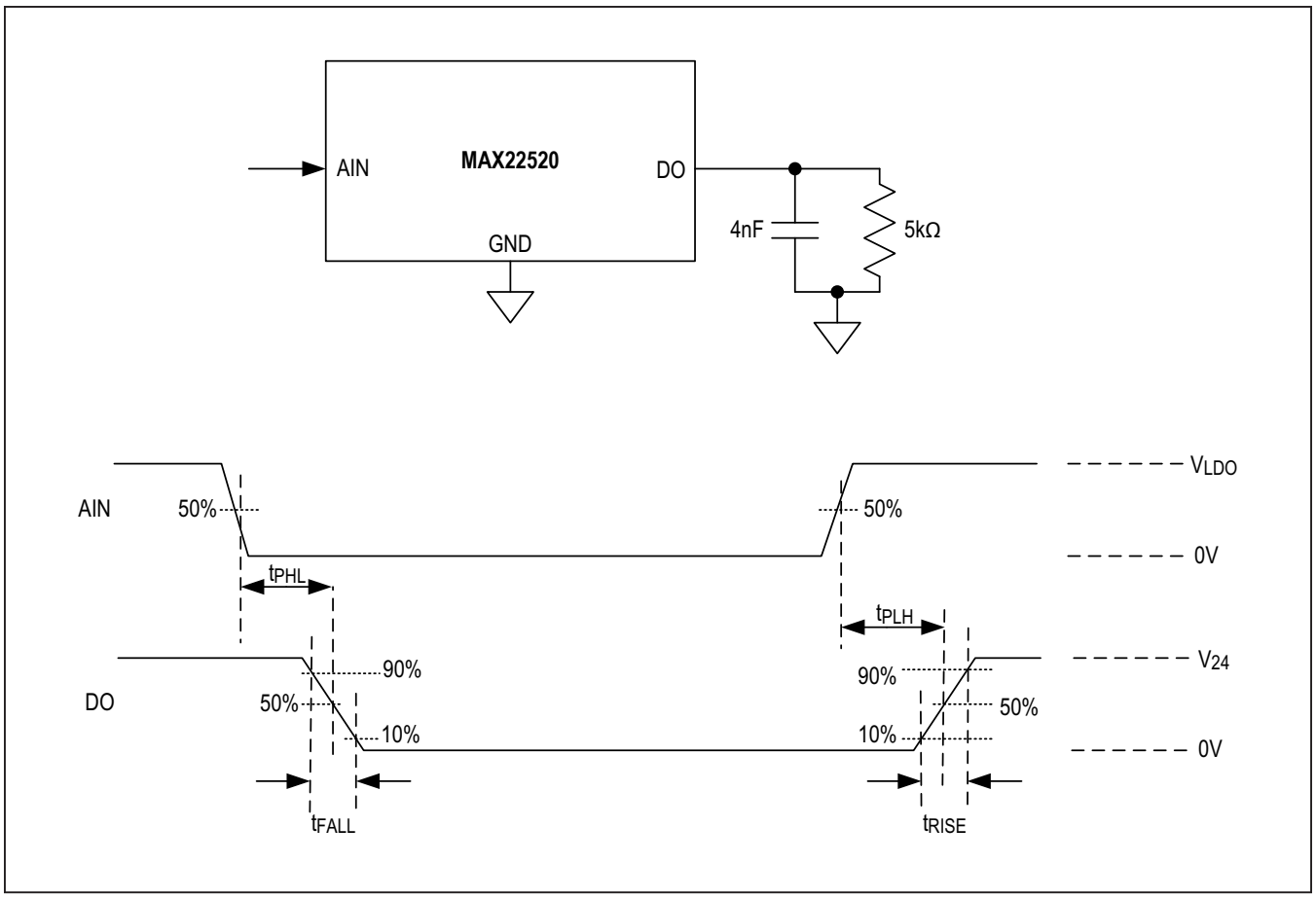
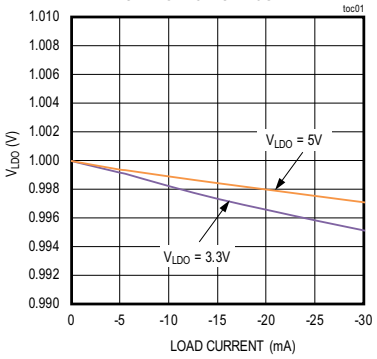


Figure 1. DO Driver Propagation Delays (Push-Pull Mode)

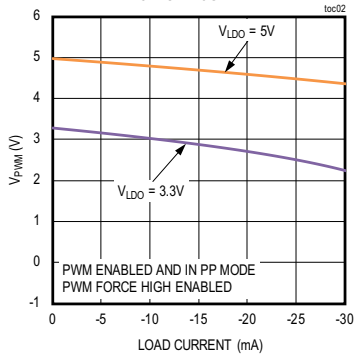
Typical Operating Characteristics

(V_{CC} = 24V, T_A=+25°C, V_{LDO} unloaded)

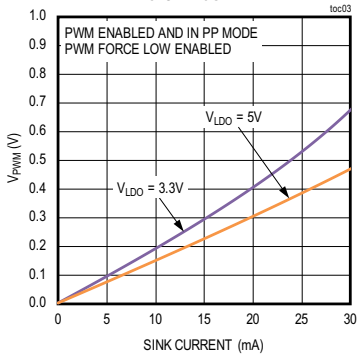
NORMALIZED LDO OUTPUT VOLTAGE vs. LOAD CURRENT



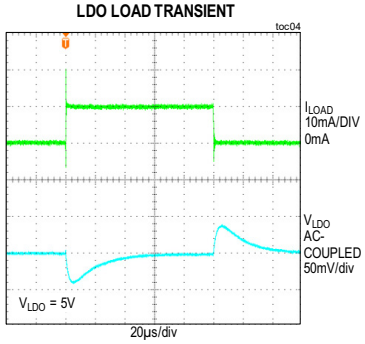
LOGIC VOLTAGE OUTPUT HIGH vs. LOAD CURRENT



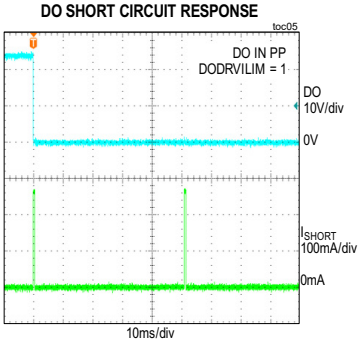
LOGIC VOLTAGE OUTPUT LOW vs. SINK CURRENT



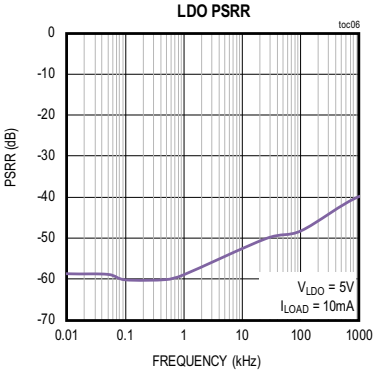
LDO LOAD TRANSIENT



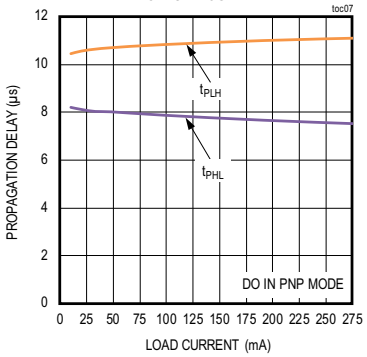
DO SHORT CIRCUIT RESPONSE



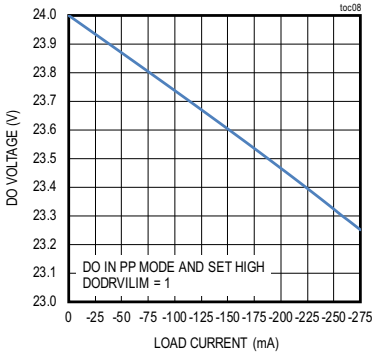
LDO PSRR



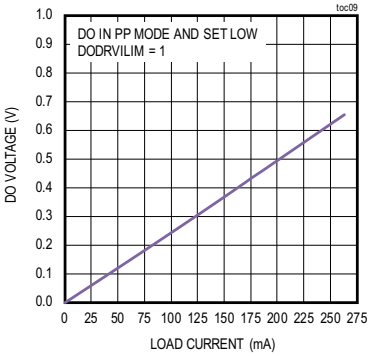
DO PROPAGATION DELAY vs. LOAD CURRENT



DO OUTPUT VOLTAGE HIGH vs. LOAD CURRENT



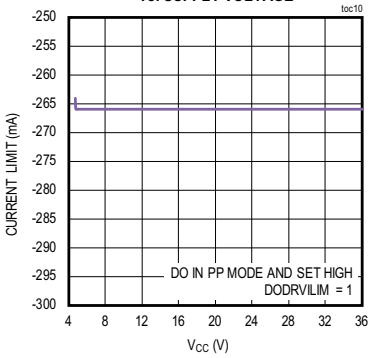
DO OUTPUT VOLTAGE LOW vs. SINK CURRENT



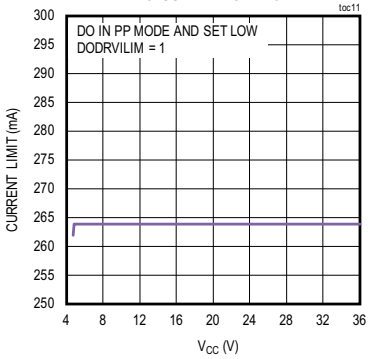
Typical Operating Characteristics (continued)

(V_{CC} = 24V, T_A=+25°C, V_{LDO} unloaded)

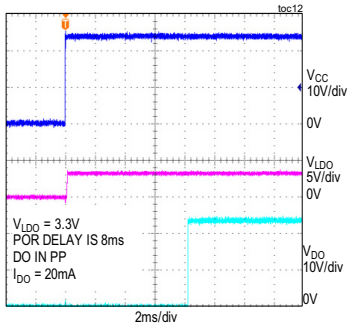
DO HIGH-SIDE CURRENT LIMIT vs. SUPPLY VOLTAGE



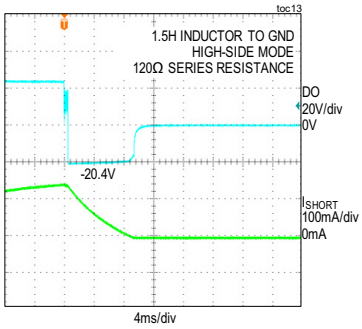
DO LOW-SIDE CURRENT LIMIT vs. SUPPLY VOLTAGE



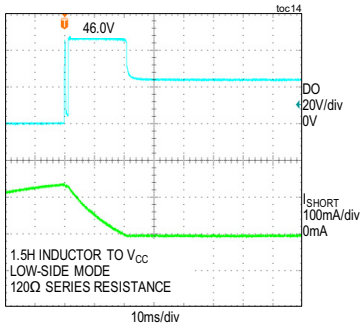
POR DELAY



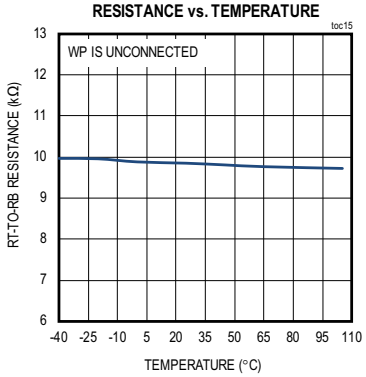
INDUCTIVE DEMAG RESPONSE



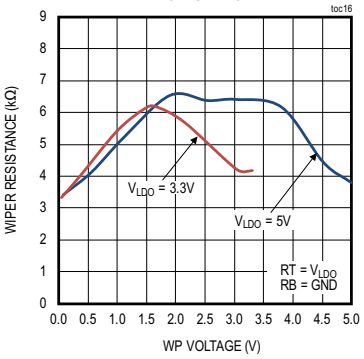
INDUCTIVE DEMAG RESPONSE



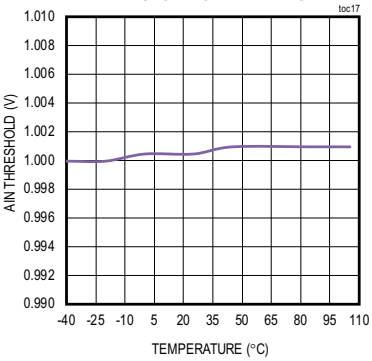
DIGITPOT RT TO RB RESISTANCE vs. TEMPERATURE



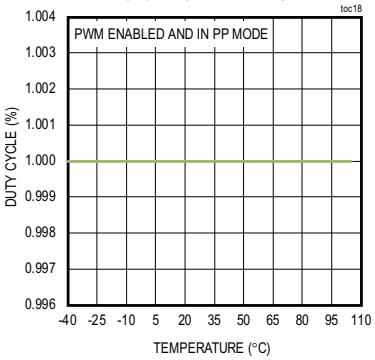
WIPER OUTPUT RESISTANCE vs. VOLTAGE



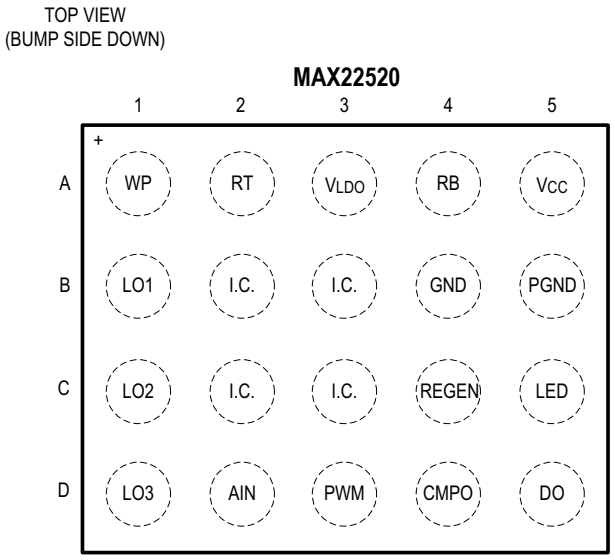
NORMALIZED COMPARATOR INPUT THRESHOLD vs. TEMPERATURE



NORMALIZED PWM DUTY CYCLE vs. TEMPERATURE



Pin Configuration



WLP
2mm × 2.5mm

Pin Description

PIN	NAME	FUNCTION
POWER		
A5	V_{CC}	Supply Voltage. Bypass V_{CC} to GND with a 10nF capacitor as close to the pin as possible.
B4	GND	Ground.
B5	PGND	Power Ground. Connect PGND to GND.
LINEAR REGULATOR		
A3	V_{LDO}	LDO Supply Input/Linear Regulator Output. Bypass V_{LDO} to GND with a 1µF capacitor. Leave REGEN unconnected to enable the internal regulator. V_{LDO} can be 3.3V (typ) or 5V (typ) when the part is powered up and the part is not OTP programmed. Program the LDOVSET bit in the OTP registers to set V_{LDO} to 3.3V (typ) or 5V (typ) when the internal regulator is enabled. Connect REGEN to GND to disable the internal regulator. Connect an external supply of 3.3V or 5V to V_{LDO} when the internal regulator is disabled. Program the LDOVSET bit in the OTP registers to set the UVLO threshold for V_{LDO} when the internal linear regulator is disabled and an external supply is connected to V_{LDO}.
C4	REGEN	Linear Regulator Enable. Leave REGEN unconnected to enable the V_{LDO} linear regulator. Do not apply an external voltage to REGEN. Connect REGEN to GND to disable the internal linear regulator. Apply an external 3.3V or 5V supply to V_{LDO} when the internal regulator is disabled.

Pin Description (continued)

PIN	NAME	FUNCTION
DRIVER		
D5	DO	Driver Output. DO is configurable in the OTP registers for PNP, NPN, push-pull, normally-open, or normally-closed operation. See the *Table 2. Logic Truth Table* and *OTP Register Map* for more information. DO is the 1-Wire I/O when programming OTP registers or when the device is in OTP-transparent RAM mode. See the *One-Time Programming (OTP)* section for more information.
COMPARATOR		
D2	AIN	Analog Input of the Internal Comparator. Program up to two comparator thresholds (V_{T1}, V_{T2}) in the OTP registers. See the *Table 2. Logic Truth Table* and *OTP Register Map* for more information.
D4	CMPO	Comparator Logic Output.
LED DRIVER		
C5	LED	Push-pull Logic LED Driver Output. Connect an LED and current limiting resistor between LED and GND. See the *Table 2. Logic Truth Table* for more information.
DIGIPOT		
A1	WP	Digipot Wiper. Set the internal digipot resistance at WP by programming the DIGIPOTSET[5:0] bits in OTP. See the *OTP Register Map* for more information.
A2	RT	Digipot Top Terminal. Connect RT to V_{LDO} or another external voltage.
A4	RB	Digipot Bottom Terminal. Connect RB to a voltage between GND and V_{RT}.
LOGIC OUTPUTS		
B1	LO1	Open-drain Logic Output 1. Set the LO1CFG[1:0] bits in the OTP registers to configure LO1 operation. See the *OTP Register Map* for more information.
C1	LO2	Open-drain Logic Output 2. Set the LO2CFG[2:0] bits in the OTP registers to configure LO2 operation. See the *OTP Register Map* for more information.
D1	LO3	Open-drain Logic Output 3. Set the LO3CFG bit in the OTP registers to configure LO3 operation. See the *OTP Register Map* for more information.
D3	PWM	Internal PWM Oscillator Output. Program the OTP registers to configure the PWM output for open-drain or push-pull operation and to set the duty cycle(s). See the *OTP Register Map* for more information.
B2, B3, C2, C3	I.C.	Internally Connected. Do not connect.

Detailed Description

The MAX22520 24V driver is optimized for use in 3-wire sensors operated in harsh industrial environments. Integrated analog interface I/Os are included to support sensor signal generation and signal conditioning for sensing circuitry.

This device is configurable through one-time programming (OTP) using a 1-Wire interface with the V_{CC}, DO, and GND pins. OTP programming can be done at the end-of-line, during sensor calibration and test. The 1-Wire interface allows the user to set analog and logic parameters (PWM duty cycles, comparator thresholds, and an integrated digipot). During programming, the comparator output (CMPO) logic state is available, providing a logic-level representation of the binary sensor output, allowing on-board calibration.

OTP Configurable Functions

Table 1 shows the OTP configurable functions in the MAX22520. Two OTP banks are available to configure the device. Note that each OTP bank must be burnt individually, in a separate burn step. See the *One-Time Programming (OTP)* section for more information.

LDO Linear Regulator (V_{LDO})

The MAX22520 includes an integrated programmable 3.3V/5V linear regulator output, V_{LDO}. Leave REGEN unconnected to enable the internal regulator. Set the LDOVSET bit in the OTP registers to 0 to set V_{LDO} = 3.3V (typ). Set LDOVSET = 1 to set V_{LDO} = 5V (typ).

V_{LDO} can be 3.3V (typ) or 5V (typ) when the part is powered up and the part is not OTP programmed.

Connect REGEN to GND to disable the internal regulator. Apply an external voltage of 3.3V or 5V to V_{LDO} when the internal regulator is disabled. A voltage must be present on V_{LDO} when REGEN = GND for normal operation. Program the LDOVSET bit in the OTP registers to set the UVLO threshold for V_{LDO} when the internal regulator is disabled and an external supply is connected to V_{LDO}.

The logic outputs (LO1, LO2, LO3, PWM, and CMPO) and the internal comparator are referenced to V_{LDO} and GND.

Table 1. OTP Configurable Functions

FUNCTION	PROGRAMMABLE OPTIONS	OTP BANK
V_{LDO} Linear Regulator Output Voltage	3.3V 5V	1
AIN Comparator	VT1, VT2 Thresholds Output Polarity	1
DO Pulse Stretching	Enable/Disable Pulse Polarity	1
PWM Configuration	Enable/Disable Configuration Normal Operation	1
Digipot Resistance	0kΩ to 10kΩ Dependencies	1
LO1 Open-Drain Logic Output	Static Low Static High Dependencies	1
POR Delay	8ms 12ms 16ms 40ms	1
PWM Duty Cycle	DC1, DC2 Switching Dependencies	2
LO2 Open-Drain Logic Output	Static Low Static High Fault Output Dependencies	2
LO3 Open-Drain Logic Output	Static Low Static High	2
DO Driver Configuration	NPN PNP Push-Pull	2
DO Driver Operating State	Normally-Open Normally-Closed	2
DO Driver Weak Pullup/Pulldown	Disabled Weak Pullup Weak Pulldown	2
DO Driver Current Limit	100mA 200mA	2

Input Comparator (AIN, CMPO)

A configurable integrated comparator provides the input signal that drives the DO driver output. The PWM output, digipot wiper position, and the logic states of the LO1 and LO2 outputs can also be configured to be dependent on the comparator output.

AIN is the input of the comparator. Two comparator thresholds (V_{T1}, V_{T2}) can be programmed in the OTP registers to define the switching hysteresis.

CMPO is a logic-level comparator output. CMPO can be programmed in the OTP registers to be in-phase or inverted compared to AIN.

Comparator Threshold Voltages (V_{T1}, V_{T2})

Two threshold voltages (V_{T1}, V_{T2}) can be programmed for the internal comparator, each with a 6-bit resolution relative to V_{LDO}. Set the thresholds by programming the VT1SET[5:0] and VT2SET[5:0] bits in the OTP registers. Calculate the programmed threshold voltages using the following equation::

$$V_{T\_} = \frac{VT\_SET[5:0]}{63} \times V_{LDO}$$

VT_SET are the 6-bit words programmed into the C1_ OTP2 and C1_OTP3 registers. The V_{T1} and V_{T2} thresholds must be in the range of the 0V to (V_{LDO} - 0.9V). If V_{T1} and V_{T2} are not the same, ensure that the V_{T1} threshold is greater than the V_{T2} threshold ($V_{T1} \geq V_{T2}$).

Multiple functions can be configured to depend on the AIN, V_{T1}, and V_{T2} voltages including the CMPO output, the state of the DO driver, and the PWM duty cycle. Figure 2 shows an example of the CMPO output operation when a comparator threshold and hysteresis are programmed.

To disable hysteresis, or if only one threshold is needed, set $V_{T2} = V_{T1}$.

Pulse Stretching

When enabled in the OTP registers (PLSTEN = 1), positive or negative pulses received at AIN that are shorter than 4ms are stretched to 4ms (typ) at the output of the pulse stretcher circuitry. Pulses on DO are lengthened to match this output.

Select the AIN pulse polarity to be stretched at DO by setting the PLSTPOL bit in the OTP registers. Set PLSTPOL to 0 to stretch positive pulses on DO (PLSTEN = 1), as shown in Figure 3. Set PLSTPOL to 1 to stretch negative DO pulses on DO (PLSTEN = 1).

Very short pulses on AIN (< 200ns, max) are filtered out by the glitch filter that precedes the pulse stretcher and are not stretched when pulse stretching is enabled.

CMPO pulses are not stretched when pulse stretch is enabled.

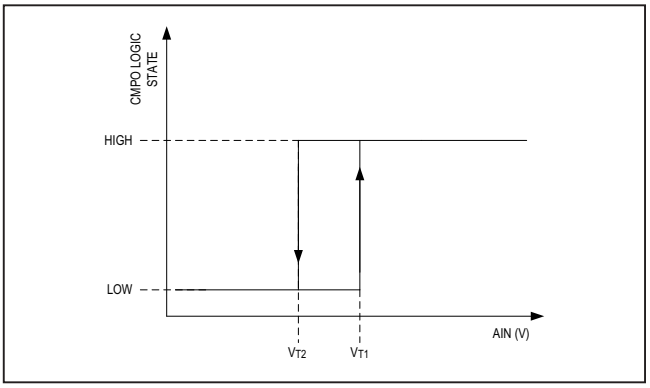


Figure 2. Comparator Operation with Hysteresis

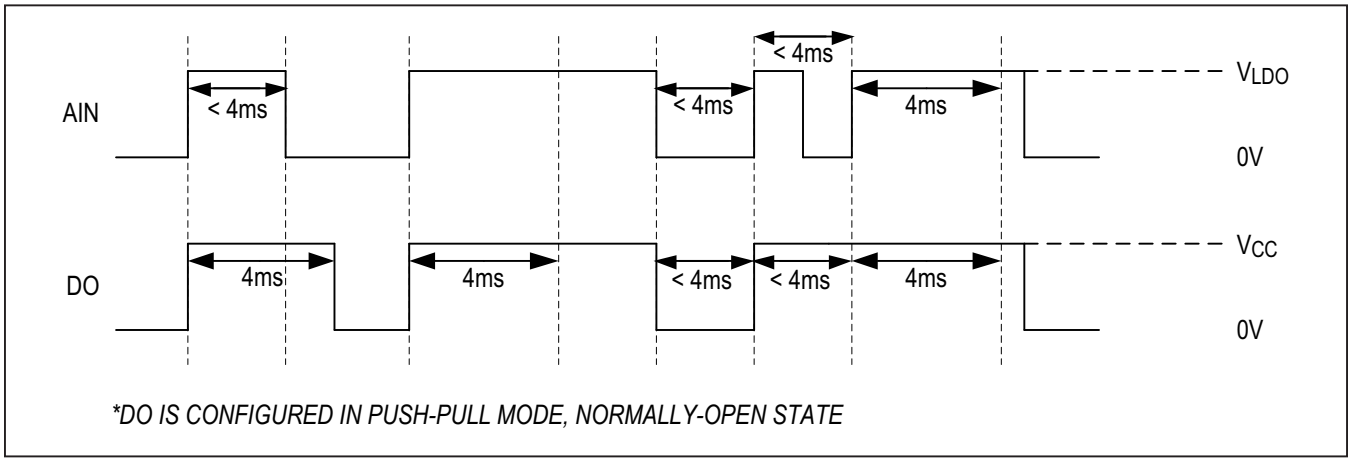


Figure 3. Sample Waveform with Positive Pulse Stretching

Driver Output (DO)

The DO driver output is configurable for high-side operation (PNP), low-side operation (NPN), or push-pull operation in a normally-open (NO) or normally-closed (NC) state in the OTP registers. An integrated LED output provides visual feedback of the state of DO at all times. See Table 2.

DO Short Circuit Protection

When the DO driver load current exceeds the programmed current limit threshold for longer than 500µs (typ), DO is disabled and the device enters autoretry mode. In autoretry mode, the driver is disabled for 50ms and then reenabled. If the fault condition is still present, the MAX22520 waits for 500µs (typ) and disables the driver again. The MAX22520 remains in autoretry mode until the fault condition is removed. The DO driver remains enabled and operates normally after the fault condition has been removed.

Select the DO driver current limit threshold to 100mA (min) or 200mA (min) by setting the DOILIM bit in the OTP registers.

Table 2. Logic Truth Table

AIN VOLTAGE	DO CONFIGURATION				LED
	NO/NC	PNP	NPN	PUSH-PULL	
L	NO	HIGH-Z	HIGH-Z	L	OFF
	NC	H	L	H	ON
H	NO	H	L	H	ON
	NC	HIGH-Z	HIGH-Z	L	OFF

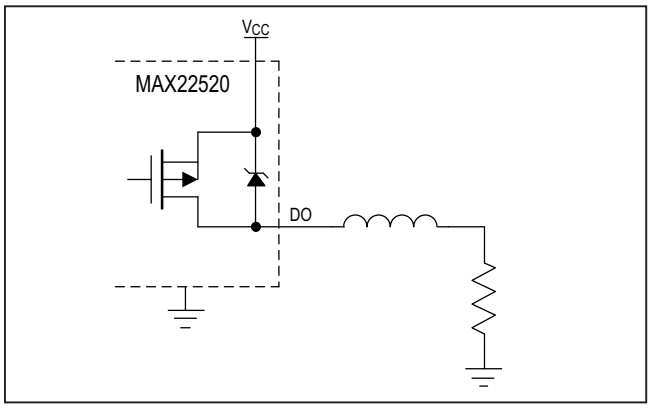


Figure 4. High-Side Mode with Ground-Connected Load

Driving Inductive Loads

Inductive loads can be turned-off/demagnetized by the MAX22520 in NPN, PNP, and push-pull modes. The internal clamps on DO turn off both GND-connected and 24V-connected inductive loads fast due to their 42V (typ) positive clamping voltage and (V_{CC} – 42V) (typ) negative clamping voltage. Inductive loads of up to 1.2H, with up to 200mA load current, can be turned off safely with supply voltages up to +36V.

Integrated Digipot (RT, RB, WP)

The MAX22520 features an integrated 10kΩ (typ) linear digital potentiometer that can be used for on-board sensor calibration. Connect the top of the digital potentiometer (RT) to V_{LDO} or to another external voltage up to V_{LDO}. Connect the bottom of the digital potentiometer (RB) to a voltage between ground and RT.

Set the wiper position by programming the DIGIPOTSET[7:2] bits in the OTP registers. Calculate the voltage at WP using the following equation:

$$V_{WP} = \frac{DIGIPOTSET[5:0]}{64} \times (V_{RT} - V_{RB})$$

LED Output

The MAX22520 includes an integrated LED output for visual feedback on the state of the DO driver. The LED current source is on, when the DO driver is on (in PNP or NPN mode) or when DO is driven high in push-pull mode. See the *Table 2. Logic Truth Table*. The LED might turn on during power up while $V_{CC} \le V_{CC\_OA}$. The LED is guaranteed to be off for the power-on-reset POR delay (t_{PU_DO}) once V_{CC} rises above the V_{CC_OA}.

PWM Oscillator

The MAX22520 features an internal 34kHz (typ) oscillator output, PWM. The PWM output is configurable in the OTP registers and is disabled by default.

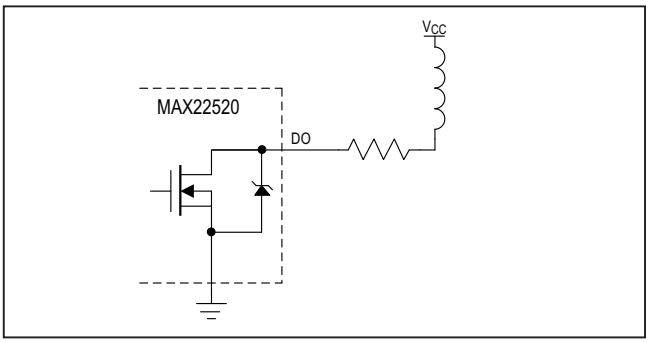


Figure 5. Low-Side Mode with Supply-Connected Load

Configuring the PWM Output

The PWM oscillator is disabled by default but can be enabled and configured in the OTP registers. Set PWMEN to 1 to enable the PWM output. Set the PWMCFG bit to configure PWM as an open-drain or push-pull output. Set the PWM output permanently high, permanently low, or as a switching output by setting the PWMFH and PWMFL bits.

PWM Duty Cycle

The PWM output can be configured with up to two duty cycles (DC1 and DC2). Duty cycles can vary from 0% (min) to 99.8% (max) and have a 9-bit resolution. Calculate the duty cycle using the the following equation:

$$DC\_ = \frac{PMWD\_[8:0]}{512} \times 100\%$$

During normal operation, the PWM duty cycle is determined by the state of the comparator AIN input voltage and programmed input voltage hysteresis (Figure 6). Set the V_{T1} and V_{T2} thresholds in the C1_OTP2 and C1_OTP3 registers.

Set DC1 = DC2, if only one duty cycle is required.

Use the following procedure to set the DC1 and DC2 duty cycles when the MAX22520 is in OTP-transparent RAM mode:

1) Write bit values to the C2_OTP1 (0x1A) and/or C2_OTP2 (0x1B) registers to set the PWMD1[7:0] and/ or PWMD2[7:0] duty cycle bits.
2) Write bit values to the C2_OTP0 (0x19) register.

Note that the C2_OTP0 (0x19) register must be written to after setting PWMD1[7:0] and/or PWMD2[7:0], even if the PWMD1[8] and/or PWMD2[8] bit values do not change. PWM duty cycles are not updated if step (2) is skipped.

Voltage Transients

Short-duration voltage transients that rise above the absolute maximum rating of the V_{CC} pin occurs during ESD, surge, and hot plug events. With a 10nF bypass capacitor on the V_{CC} line, the device is not damaged. Transients due to inductive kickback on DO when driving inductive loads up to 1.5H at 200mA or less may also bring the DO voltage above the absolute maximum rating, yet the device is not damaged. The absolute maximum ratings for V_{CC} and DO should not be violated for any length of time by external sources.

Thermal Protection

Integrated circuitry protects the MAX22520 from thermal overload conditions. When the die temperature rises above 150°C (typ), the MAX22520 enters thermal shutdown and the DO driver, the LED driver, and the internal linear regulator (V_{LDO}) are disabled. DO, LED, and V_{LDO} are reenabled when the die temperatures fall below the 15°C thermal shutdown hysteresis to 135°C (typ).

One-Time Programming (OTP)

The MAX22520 features a high level of configurability through one-time programmable (OTP) registers. The state of the OTP bits are unknown if the part is powered up and has not been programmed. Once programmed, the selected functionality cannot be reprogrammed. Program the configurable options using the sensor interface pins (V_{CC}, DO, and GND) and the 1-Wire interface protocol. For protocol information on the 1-Wire interface, refer to the design resources section on the **1-Wire Devices** page and the **1-Wire tutorial video**. The MAX22520 is only compatible with standard 1-Wire mode and requires a MSB-first data exchange.

Two OTP banks are provided for all of the configurable options. Each OTP bank must be burnt individually, in a separate OTP burn. The flow charts in Figure 9 and Figure 10 outline the automatic OTP burn procedure.

Registers in the MAX22520 can be configured and verified by entering OTP-transparent mode before OTP is burned, or after. In this mode, all of the functionality, except DO, is available for programming. OTP registers return to their burned values (if already burned), or the default values (if not burned), when the V_{CC} supply is cycled.

1-Wire Interface

Enable the 1-Wire interface for the MAX22520 by cycling the V_{CC} power supply to 0V and then raising V_{CC} to 3.8V (typ).

A 1-Wire access cycle is always initiated by the master controller sending a command byte that contains the access type (read or write) and the register address. The MAX22520 reads/writes the MSB first.

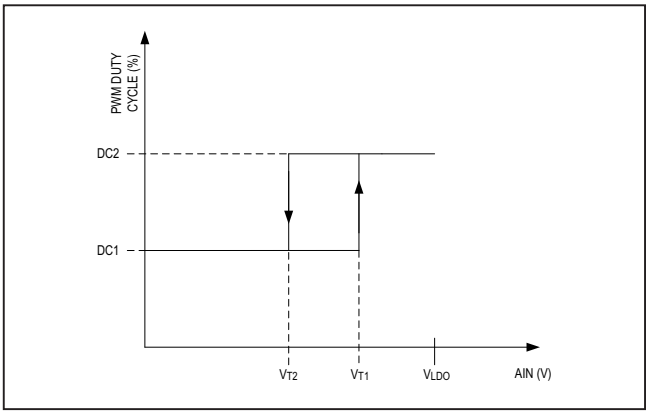


Figure 6. PWM Duty Cycle Hysteresis, Dependent on Comparator Thresholds

1-Wire Write Byte

The first bit of the command byte is always 0 and is used by the MAX22520 as a START bit. Set the R/$\overline{W}$ bit to 0 for write access. Send an 8-bit data byte after the command byte is sent (Figure 7).

1-Wire Read Byte

1-Wire access is always initiated by the master controller. The first bit of the command byte is 0 and is used by the MAX22520 as a START bit. Set the R/$\overline{W}$ bit to 1 for read access. The following bits in the command byte are the OTP register address.

The MAX22520 sends an 8-bit data byte to the master controller after the read command byte is received (Figure 8). The master must time the read slots during a read cycle.

Entering OTP Mode

To enter OTP mode, ensure the die temperature is at room temperature (25°C) and follow these steps:

1) Power cycle the MAX22520 and set the V_{CC} voltage between 3.5V and 4.1V. This enables the 1-Wire interface on the DO pin.
2) Using the 1-Wire interface, write the RAM mode enable code (0x3C) to the 0x2A register. This write enables 1-Wire RAM mode, but the device does not yet enter RAM mode.
3) Write the RAM mode latch code (0x96) to the 0x36 register to enter RAM mode. At this point, the MAX22520 is set into RAM mode and V_{CC} can be set to the normal operating voltage.
4) Verify that the bank C1LOCK or C2LOCK bit is not set (indicating that the OTP has not been burned).
5) Enter 1-Wire RAM mode to set the OTP register values and verify operation before OTP burn.
6) Enable OTP autoburn functionality and send the command to start OTP burn.

The MAX22520 includes two OTP banks that must be burned individually, in separate burn steps, and the V_{CC} supply must be cycled after each burn. Figure 9 shows the burn sequence for the C1 OTP bank. Figure 10 shows the burn sequence for the C2 OTP bank.

COMMAND BYTE (MASTER-TO-SLAVE)							
MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
START	R/$\overline{W}$	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

DATA BYTE (MASTER-TO-SLAVE)							
MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 7. 1-Wire Write Byte

COMMAND BYTE (MASTER-TO-SLAVE)							
MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
START	R/$\overline{W}$	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

DATA BYTE (SLAVE-TO-MASTER)							
MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 8. 1-Wire Read Byte

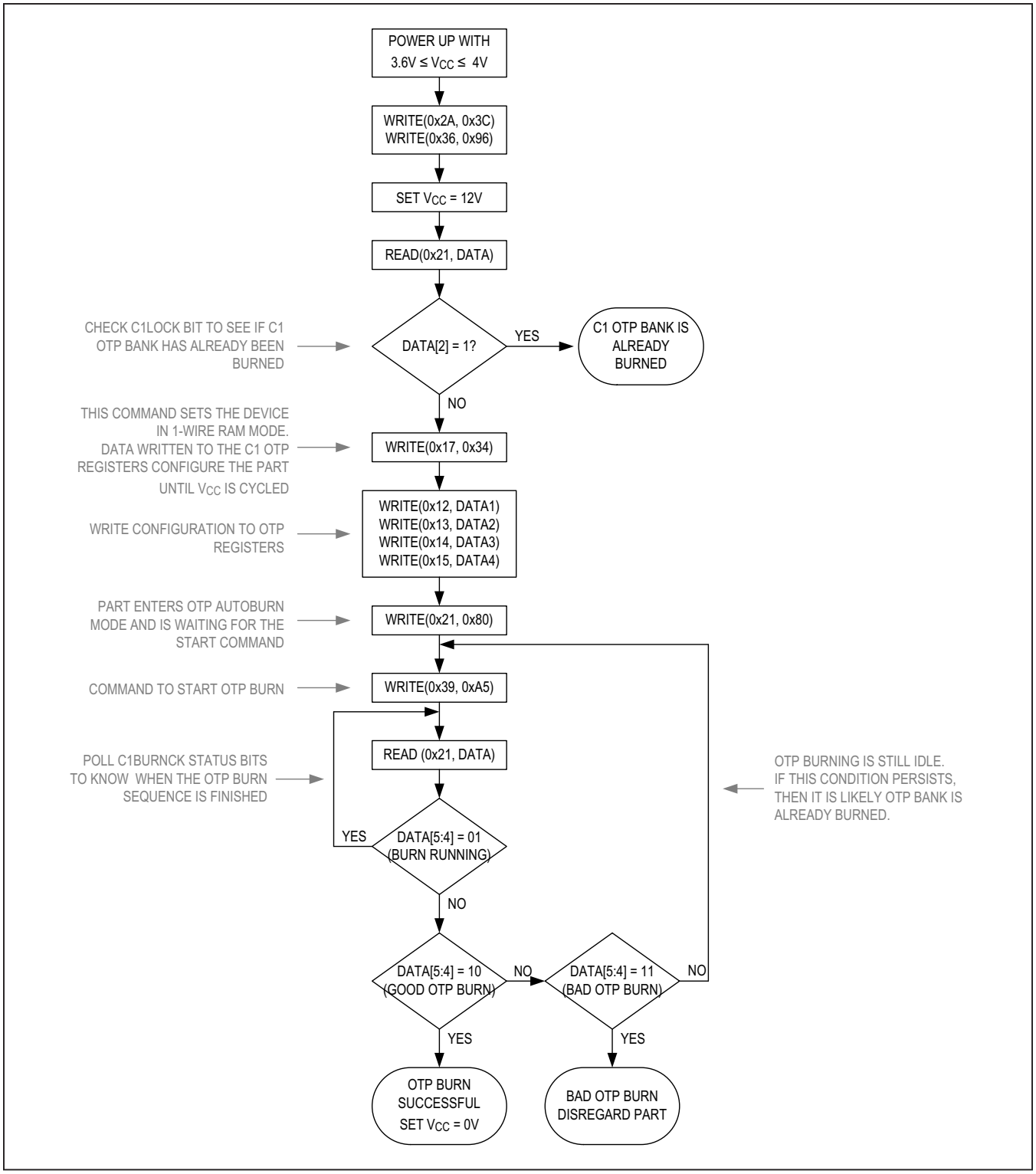


Figure 9. Bank 1 OTP Configuration Flow Chart

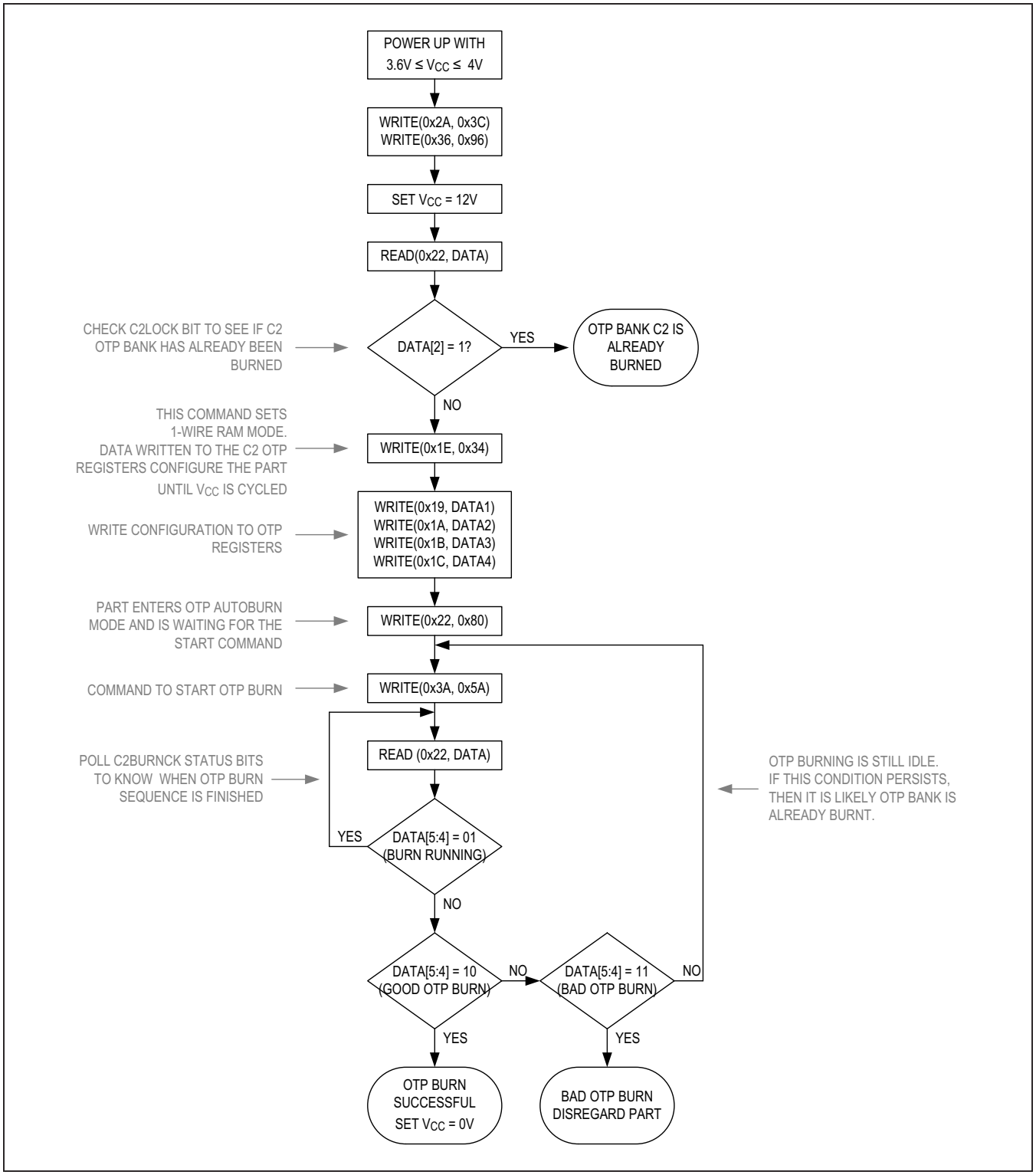


Figure 10. Bank 2 OTP Configuration Flow Chart

Verify OTP Burn

Once OTP burn is complete for the C1 or C2 banks, verify that the registers in the bank have been correctly programmed as shown in the Figure 11 and Figure 12 flow charts.

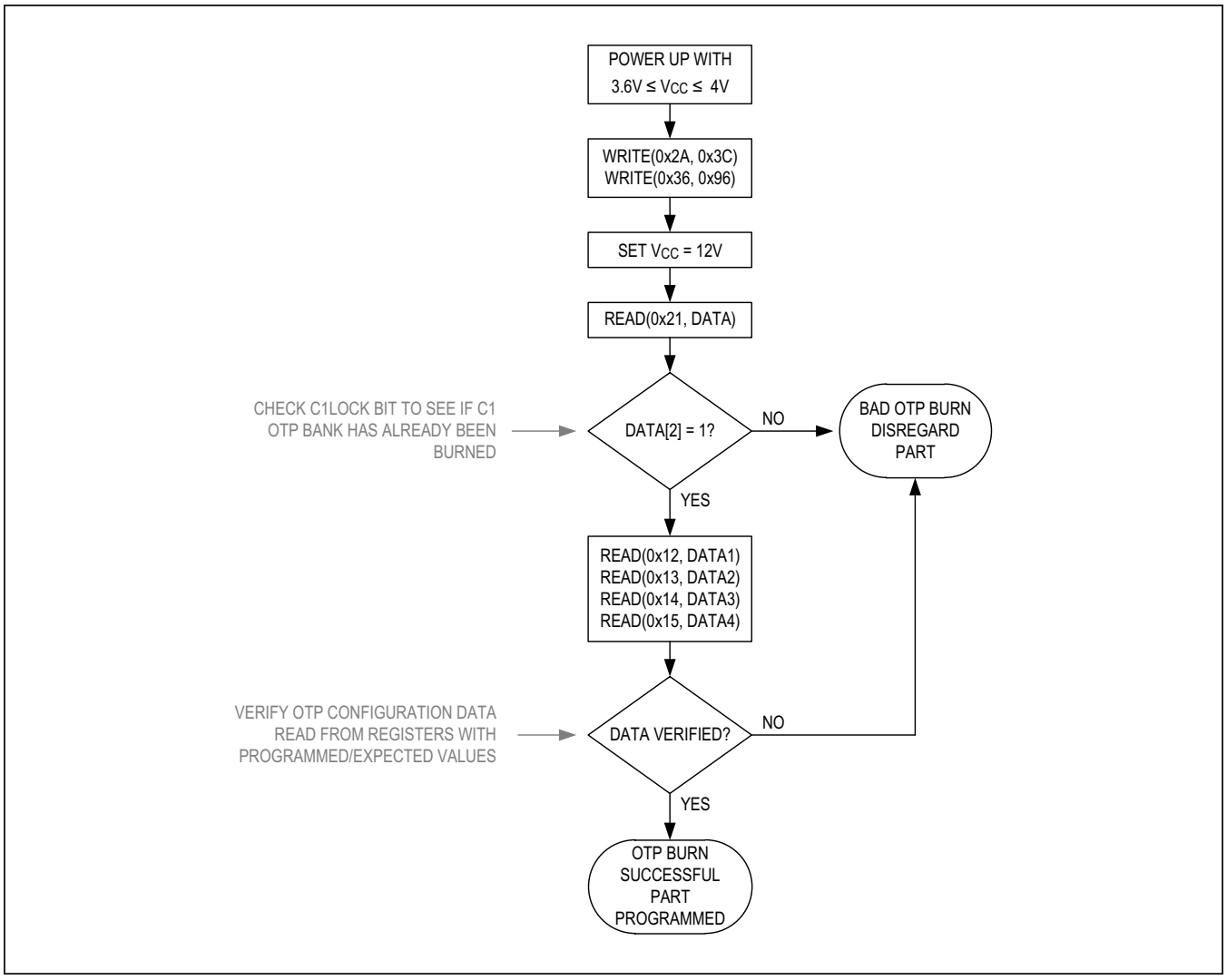


Figure 11. Bank C1 OTP Configuration Check

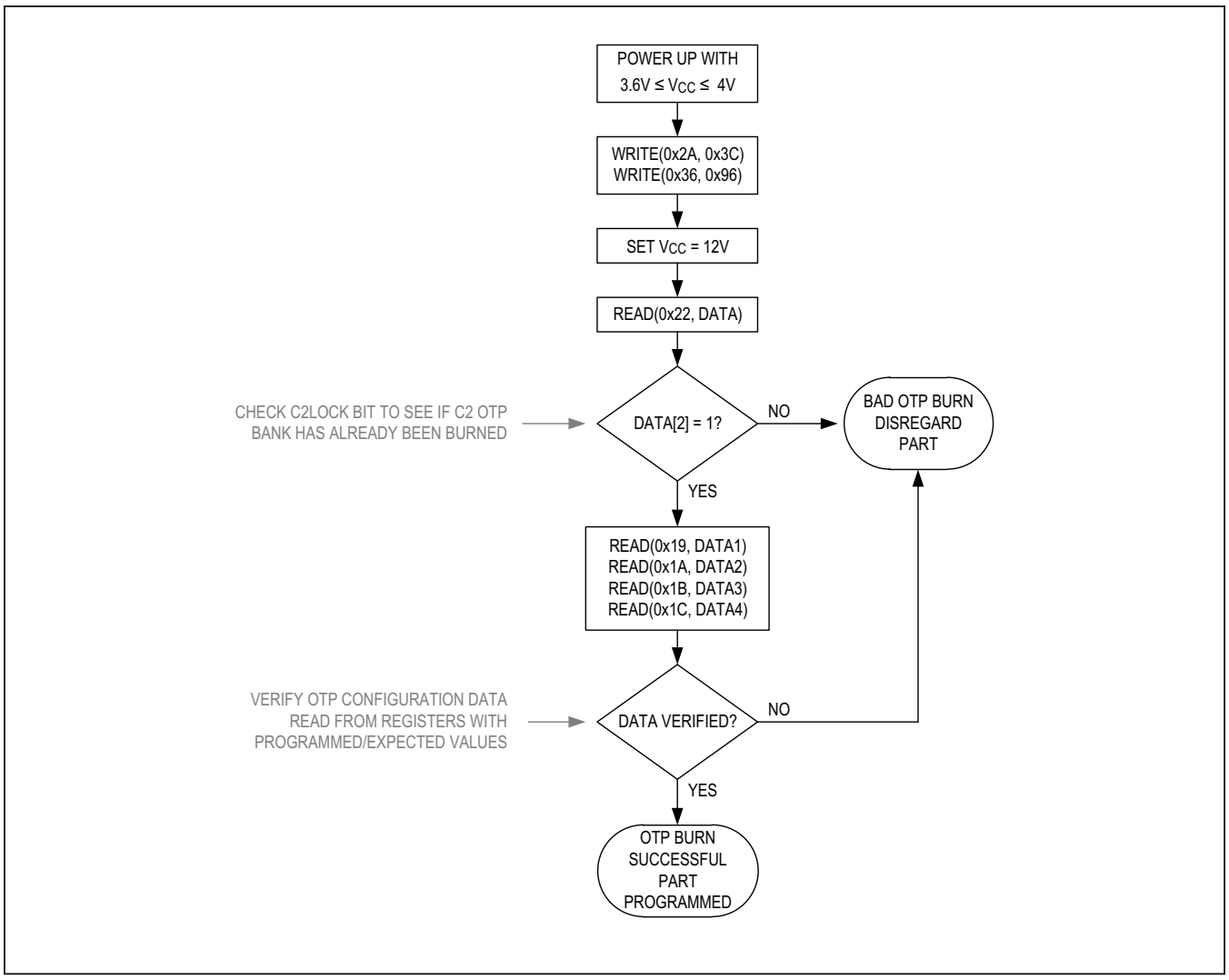


Figure 12. Bank C2 OTP Configuration Check

Register Map

OTP Register Map

ADDRESS	NAME	MSB							LSB
OTP BANK1/BANK2									
0x00	REV_ID[7:0]	REVID[7:0]							
0x12	C1_OTP0[7:0]	DIGIPOTSET[5:0]						PLSTEN	LDOV-SET
0x13	C1_OTP1[7:0]	PORDLY[1:0]		L01CFG[1:0]		PWM-CFG	PWMFH	PWMFL	PWMEN
0x14	C1_OTP2[7:0]	–	–	VT1SET[5:0]					
0x15	C1_OTP3[7:0]	CMPO POL	PLST-POL	VT2SET[5:0]					
0x17	C1RAMEN[7:0]	C1RAMMODE[7:0]							
0x19	C2_OTP0[7:0]	PWMD2 [8]	PWMD1 [8]	DOILIM	DOPUPD[1:0]		DOST	DOCFG[1:0]	
0x1A	C2_OTP1[7:0]	PWMD1[7:0]							
0x1B	C2_OTP2[7:0]	PWMD2[7:0]							
0x1C	C2_OTP3[7:0]	–	–	–	–	LO3CFG	LO2CFG[2:0]		
0x1E	C2RAMEN[7:0]	C2RAMMODE[7:0]							
0x21	C1_CHK[7:0]	C1AU-TOBURN	AINC-MPOUT	C1BURNCK[1:0]		–	C1LOCK	–	–
0x22	C2_CHK[7:0]	C2AU-TOBURN	AINC-MPOUT	C2BURNCK[1:0]		–	C2LOCK	–	–
0x2A	RAMMODEEN[7:0]	RAMEN[7:0]							
0x36	RAMMODEVAL[7:0]	RAMVAL[7:0]							
0x39	C1_OTP_BURN[7:0]	C1BURN[7:0]							
0x3A	C2_OTP_BURN[7:0]	C2BURN[7:0]							

Register Details

REV_ID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	REVID[7:0]							
Reset	0x02							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
REVID	7:0	Chip Revision

C1_OTP0 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	DIGIPOTSET[5:0]						PLSTEN	LDOVSET
Reset	00000						0	0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DIGIPOTSET	7:2	Digipot Wiper Set Bits. Set the DIGIPOTSET[5:0] bits to set the resistance at WP. See the *Integrated Digipot (RT, RB, WP)* section for more information.
PLSTEN	1	DO Pulse Stretch Enable 0 = Pulse stretching is disabled. 1 = Pulse stretching is enabled.
LDOVSET	0	Set the V_{LDO} Output Voltage 0 = V_{LDO} is 3.3V (typ) 1 = V_{LDO} is 5V (typ)

C1_OTP1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	PORDLY[1:0]		L01CFG[1:0]		PWMCFG	PWMFH	PWMFL	PWMEN
Reset	0		00		0	0	0	0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
PORDLY	7:6	Power-On Reset Delay Select 00 = 8ms 01 = 12ms 10 = 16ms 11 = 40ms
L01CFG	5:4	L01 Open-Drain Logic Output Configuration 00 = Static low 01 = Static open 10 = L01 is set by the comparator output: Comparator Output High: L01 is ON Comparator Output Low: L01 is OFF 11 = L01 is set by the comparator output: Comparator Output High: L01 is OFF Comparator Output Low: L01 is ON
PWMCFG	3	PWM Output Configuration 0 = Push-pull 1 = Open-drain
PWMFH	2	PWM Output Force High Enable Set PWMEN = 1. This bit is ignored when PWMEN = 0. 0 = Disabled 1 = PWM output is forced high. PWMFL must be 0.
PWMFL	1	PWM Output Force Low Enable Set PWMEN = 1. This bit is ignored when PWMEN = 0. 0 = Disabled 1 = PWM output is forced low. PWMFH must be 0.
PWMEN	0	PWM Output Enable 0 = PWM output is disabled. 1 = PWM output is enabled.

C1_OTP2 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VT1SET[5:0]					
Reset	–	–	00 0000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VT1SET	5:0	Comparator Threshold Voltage 1 (V_{T1}). See the *Comparator Threshold Voltages (VT1, VT2)* section for more information.

C1_OTP3 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	CMPOPOL	PLSTPOL	VT2SET[5:0]					
Reset	0	0	00 0000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
CMPOPOL	7	CMPO Output Polarity Select 0 = Normal 1 = Inverted
PLSTPOL	6	DO Pulse Stretch Polarity 0 = Positive pulses are stretched. 1 = Negative pulses are stretched.
VT2SET	5:0	Comparator Threshold Voltage 2 (V_{T2}). See the *Comparator Threshold Voltages (VT1, VT2)* section for more information.

C1RAMEN (0x17)

BIT	7	6	5	4	3	2	1	0
Field	C1RAMMODE[7:0]							
Reset	0x35							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
C1RAMMODE	7:0	C1 1-Wire Access Enable. Write 0x34 to C1RAMMODE[7:0] to access the C1 OTP bank when in 1-Wire RAM mode.

C2_OTP0 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	PWMD2[8]	PWMD1[8]	DOILIM	DOPUPD[1:0]		DOST	DOCFG[1:0]	
Reset	0	0	0	00		0	00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
PWMD2[8]	7	MSB of the PWM Output Duty Cycle 2 PWMD2[8:0] bits. See the *PWM Duty Cycle* section for more information.
PWMD1[8]	6	MSB of the PWM Output Duty Cycle 1 PWMD1[8:0] bits. See the *PWM Duty Cycle* section for more information.
DOILIM	5	DO Driver Current Limit 0 = 100mA (min) 1 = 200mA (min)
DOPUPD	4:3	DO Driver Pullup/Pulldown Configuration 00 = Disabled 01 = Weak pullup enabled 10 = Weak pulldown enabled 11 = Reserved
DOST	2	DO Driver State 0 = Normally-open 1 = Normally-closed See the *Table 2. Logic Truth Table* for more information.
DOCFG	1:0	DO Driver Configuration 00 = PNP 01 = NPN 10 = Push-pull 11 = Reserved

C2_OTP1 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	PWMD1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PWMD1	7:0	PWM Output Duty Cycle 1. See the *PWM Duty Cycle* section for more information.

C2_OTP2 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	PWMD2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PWMD2	7:0	PWM Output Duty Cycle 2. See the *PWM Duty Cycle* section for more information.

C2_OTP3 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LO3CFG	LO2CFG[2:0]		
Reset	–	–	–	–	0	000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
LO3CFG	3	LO3 Open-Drain Logic Output 0 = Static low 1 = Static high
LO2CFG	2:0	LO2 Open-Drain Logic Output 000 = Static low 001 = Static open 010 = Dependent on the comparator output. Comparator Output High: L02 is ON Comparator Output Low: L02 is OFF 011 = Dependent on the comparator output. Comparator Output High: L02 is OFF Comparator Output Low: L02 is ON 100 = DO fault output. LO2 asserts low when DO goes high impedance due to an overcurrent or thermal overload fault.

C2RAMEN (0x1E)

BIT	7	6	5	4	3	2	1	0
Field	C2RAMMODE[7:0]							
Reset	0x35							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
C2RAMMODE	7:0	C2 1-Wire Access Enable. Write 0x34 to C2RAMMODE[7:0] to access the C2 OTP bank when in 1-Wire RAM mode.

C1_CHK (0x21)

BIT	7	6	5	4	3	2	1	0
Field	C1AUTO BURN	AINC MPOUT	C1BURNCK[1:0]		–	C1LOCK	–	–
Reset	0	0	00		–	0	–	–
Access Type	Write, Read	Read Only	Read Only		–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION
C1AUTOBURN	7	C1 OTP Bank Autoburn Mode Enable 0 = OTP autoburn mode is disabled. 1 = OTP autoburn mode is enabled.
AINCMPOUT	6	AIN Comparator Output 0 = CMPO is low. 1 = CMPO is high.
C1BURNCK	5:4	C1 OTP Bank Self-Burn Results 00 = OTP burn process is idle. 01 = OTP burn process is ongoing. 10 = OTP burn process is completed with GOOD. 11 = OTP burn process completed with FAIL.
C1LOCK	2	C1 OTP Bank Lock Bit: 0 = C1 OTP bank is not burned. 1 = C1 OTP bank is burned.

C2_CHK (0x22)

BIT	7	6	5	4	3	2	1	0
Field	C2AUTO BURN	AINC MPOUT	C2BURNCK[1:0]		–	C2LOCK	–	–
Reset	0	0	00		–	0	–	–
Access Type	Write, Read	Read Only	Read Only		–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION
C2AUTOBURN	7	C2 OTP Bank Autoburn Mode Enable 0 = OTP autoburn mode is disabled. 1 = OTP autoburn mode is enabled.
AINCMPOUT	6	AIN Comparator Output 0 = CMPO is low. 1 = CMPO is high.
C2BURNCK	5:4	C2 OTP Bank Self-Burn Results: 00 = OTP burn process is idle 01 = OTP burn process is ongoing 10 = OTP burn process is completed with GOOD. 11 = OTP burn process completed with FAIL.
C2LOCK	2	C2 OTP Bank Lock Bit: 0 = C2 OTP bank is not burned. 1 = C2 OTP bank is burned.

RAMMODEEN (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	RAMEN[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
RAMEN	7:0	1-Wire RAM Mode Enable. Write 0x3C to this register to enable 1-Wire RAM mode.

RAMMODEVAL (0x36)

BIT	7	6	5	4	3	2	1	0
Field	RAMVAL[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
RAMVAL	7:0	1-Wire RAM Mode Latch. Wite 0x96 to this register to latch the MAX22520 in 1-Wire RAM mode. V_{CC} can be raised above 4V after this write is complete and the MAX22520 stays in 1-Wire RAM mode.

C1_OTP_BURN (0x39)

BIT	7	6	5	4	3	2	1	0
Field	C1BURN[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
C1BURN	7:0	C1 OTP Bank Burn Mode Write 0xA5 to start burning C1 OTP bank. C1AUTOBURN must be set to 1.

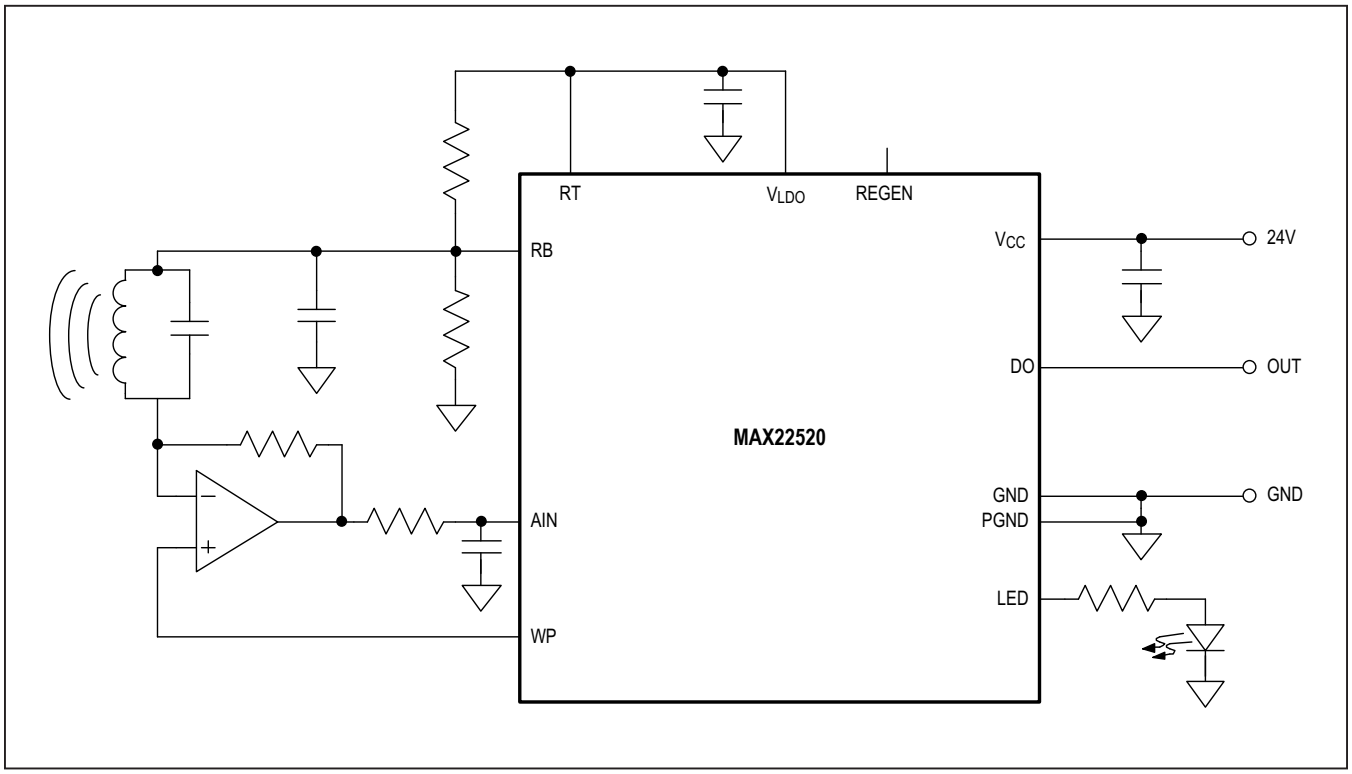
C2_OTP_BURN (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	C2BURN[7:0]							
Reset	0x00							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
C2BURN	7:0	C2 OTP Bank Burn Mode Write 0x5A to start burning C2 OTP bank. C2AUTOBURN must be set to 1.

Typical Application Circuits

Inductive Sensor



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	BALL PITCH
MAX22520GWP+	-40°C to +105°C	20 WLP	0.5mm
MAX22520GWP+T	-40°C to +105°C	20 WLP	0.5mm

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = tape and reel.