MAX2981

Integrated Powerline Communication Analog Front-End Transceiver and Line Driver

General Description

The MAX2981 powerline communication analog frontend (AFE) and line-driver IC is a state-of-the-art CMOS device that delivers high performance at low cost. This highly integrated design combines an analog-to-digital converter (ADC), digital-to-analog converter (DAC), adaptive gain control (AGC), filters, and line driver on a single chip. The MAX2981 substantially reduces previously required system components and complies with the HomePlug® 1.0 standard.

Combined with Maxim's integrated PHY/MAC digital baseband, the device delivers the most flexible and cost-effective solution. The advanced design of the MAX2981 allows operation without external control, enabling simplified connection to a variety of HomePlug 1.0 digital PHY ICs.

The MAX2981 is specified over the -40°C to +105°C automotive temperature range and is offered in a 64-pin lead-free LQFP package. The device is qualified to the AEC-Q100 Rev F automotive standard.

Applications

- Local Area Networking (LAN)
- Broadband-over-Powerline (BPL)
- Remote Monitoring and Control
- Energy Management
- Industrial Automation
- Building Automation
- IPTV Distribution

Typical Operating Circuit appears at end of data sheet.

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Features

- HomePlug 1.0 Compliant
- Fully Integrated AFE and Line Driver
- Fully Compatible with the MAX2982/MAX2986
- Pin-to-Pin Compatible with the MAX2980
- Seamless Interface to Third-Party PHY ICs
- Fully Integrated, 10-Bit, 50Msps ADC and DAC
- 56dB Adaptive Gain Control
- Line Impedance Drive Capability as Low as 10Ω
- Line-Driver Bypass Mode
- 220mA in Rx Mode and 150mA in Tx Mode at 3.3V
- -40°C to +105°C Operating Temperature Range
- AEC-Q100 Rev F (Automotive) Qualified
- 64-Pin LQFP Package

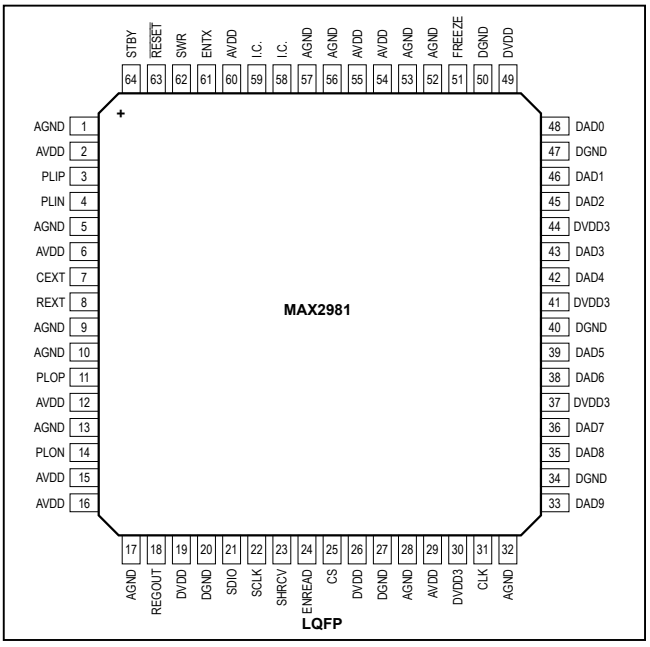
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2981GCB/V+	-40°C to +105°C	64 LQFP

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant part.

Pin Configuration



maxim integrated™

Absolute Maximum Ratings

AVDD to AGND .....-0.3V to +3.9V
DVDD3 to DGND.....-0.3V to +3.9V
DVDD to DGND.....-0.3V to +2.8V
AGND to DGND.....-0.3V to +0.3V
All Other Pins.....-0.3V to (V_{DD} + 0.3V)
Current into Any Pin.....±100mA
Short-Circuit Duration (V_{REGOUT} to AGND) 10ms

Continuous Power Dissipation (T_A = +70°C)
64-Pin LQFP (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

Electrical Characteristics

(V_{AVDD} = V_{DVDD3} = +3.3V, DVDD = REGOUT, V_{AGND} = V_{DGND} = V_{SHRCV} = 0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{AVDD}		3.0		3.6	V
Digital Supply Voltage	V_{DVDD3}		3.0		3.6	V
Digital Supply Voltage	V_{DVDD}	(Note 2)		2.4		V
Quiescent Supply Current	I_{AVDD}	Receive mode, transmitter disabled, no signal applied		220		mA
		Transmit mode, receiver disabled, no signal and no load applied		150		
Standby Supply Current		No clock			6	mA
Regulator Output	V_{REGOUT}			2.4		V
Output-Voltage High	V_{OH}	I_{SOURCE} = 5mA	2.4			V
Output-Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
LOGIC INPUT						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IH}	V_{IH} = V_{DVDD}			+5	µA
	I_{IL}	V_{IL} = 0V	-5			
ANALOG-TO-DIGITAL CONVERTER (ADC)						
Resolution	N	(Note 3)		10		Bits
Integral Nonlinearity	INL			2.3		LSB
Differential Nonlinearity	DNL			0.8		LSB
Two-Tone 3rd-Order Distortion	IM3	Two tones at 17MHz and 18MHz at input $1V_{P-P}$ differential voltage		-51.5		dBc
DIGITAL-TO-ANALOG CONVERTER (DAC)						
Resolution	N	(Note 3)		10		Bits
Integral Nonlinearity	INL			0.5		LSB
Differential Nonlinearity	DNL			0.4		LSB
Two-Tone 3rd-Order Distortion	IM3	Two tones at 17MHz and 18MHz at output $1V_{P-P}$ differential voltage		-54		dBc

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD3} = +3.3V, DVDD = REGOUT, V_{AGND} = V_{DGND} = V_{SHRCV} = 0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER						
Common-Mode Voltage				1.6		V
Input Impedance	Z_{IN}	Between PLIP or PLIN and 0V at 12MHz (Note 3)		875		Ω
Two-Tone 3rd-Order Distortion	IM3	Two tones at 17MHz and 18MHz at input 1V_{P-P} differential voltage		-52		dBc
Receiver Gain Range	Rx			56		dB
Lowpass Filter -3dB Corner Frequency		(Note 3)		23		MHz
Lowpass Filter Ripple		(Note 3)		2.6		dB
Highpass Filter -3dB Corner Frequency		(Note 3)		2.4		MHz
TRANSMITTER						
Common-Mode Voltage				1.6		V
Output Impedance	Z_{OUT}	Between PLOP/PLON and 0V at 12.5MHz (Note 3)		3		Ω
Output Voltage Swing		Predriver gain = -6dB at 12.5MHz, V_{P-P} at 10Ω single-ended output load		1.4		V_{P-P}
		Predriver gain = 3dB at 12.5MHz, V_{P-P} at 10Ω single-ended output load		4		
Predriver Output Voltage Swing		Line driver in bypass mode, predriver gain = 3dB; at 50Ω single-ended output load		1.4		V_{P-P}
Two-Tone 3rd-Order Distortion	IM3	Two tones at 17MHz and 18MHz		-50	-35	dBc
Lowpass Filter -3dB Corner Frequency		(Note 3)		23		MHz
Lowpass Filter Ripple		(Note 3)		2.6		dB
Minimum Line Impedance Drive Capability		Single-ended output		10		Ω
Predriver Line Impedance Capability		Line driver is in bypass mode, single-ended output		50		Ω
TIMING CHARACTERISTICS						
CLK Frequency				50		MHz
CLK Fall to ADC Data Output Valid Time	t_{ADCO}			2		ns
CLK Fall to DAC Data Latch Time	t_{DACI}			3		ns

Note 1: Min and max values are guaranteed by design and characterization at T_A = -40°C and production tested at T_A = +25°C and +105°C. Typical values are tested functionally at T_A = +25°C.

Note 2: Bypass internal 2.4V regulator with 0.1µF capacitor to DGND.

Note 3: Typical values are guaranteed by design at T_A = +25°C.

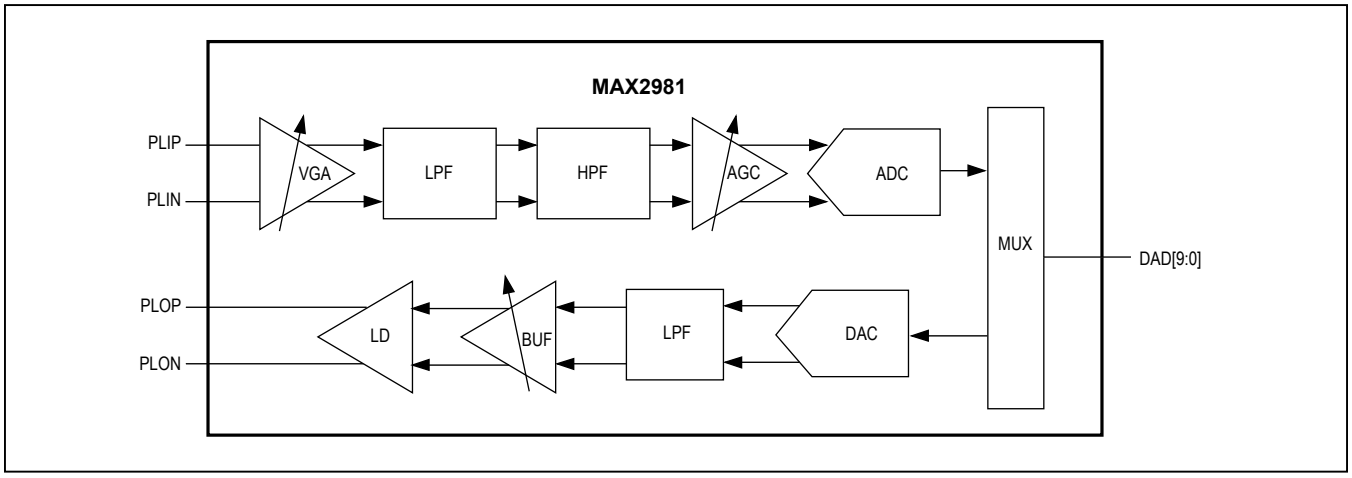
Pin Description

PIN	NAME	FUNCTION
1, 5, 9, 10, 13, 17, 28, 32, 52, 53, 56, 57	AGND	Analog Ground
2, 6, 12, 15, 16, 29, 54, 55, 60	AVDD	Analog Power-Supply Voltage. AVDD supply range is 3.0V to 3.6V. Bypass AVDD with a 0.1µF capacitor to AGND.
3	PLIP	AC Powerline Positive Input
4	PLIN	AC Powerline Negative Input
7	CEXT	External Capacitor Connection. Connect a 10nF capacitor from C_{EXT} to AGND.
8	REXT	External Resistor Connection. Connect a 25kΩ resistor from R_{EXT} to AGND.
11	PLOP	AC Powerline Positive Output
14	PLON	AC Powerline Negative Output
18	REGOUT	Voltage Regulator Output. Connect REGOUT to DVDD for normal operation.
19, 26, 49	DVDD	Digital 2.4V Voltage Input. Connect DVDD to REGOUT for normal operation.
20, 27, 34, 40, 47, 50	DGND	Digital Ground
21	SDIO	Serial Data Input/Output
22	SCLK	Serial Clock Input
23	SHRCV	Receiver Shutdown Control. Drive SHRCV high to power down the receiver. Drive low for normal operation.
24	ENREAD	Read-Mode Enable Control. Drive ENREAD high to place the DAD[9:0] bidirectional buffers in read mode. Data is transferred from the digital PHY to the AFE DAC. ENREAD signal frames the transmission.
25	CS	Active-High Carrier-Select Input. Drive CS high to initiate the internal timer.
30, 37, 41, 44	DVDD3	Digital Power-Supply Voltage. DVDD3 supply range is 3.0V to 3.6V. Bypass DVDD3 to DGND with a 0.1µF capacitor as close as possible to the pin.
31	CLK	50MHz System Clock Input
33	DAD9	DAC/ADC Input/Output MSB Data Bit. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
35	DAD8	DAC/ADC Input/Output Data Bit 8. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.

Pin Description (continued)

PIN	NAME	FUNCTION
36	DAD7	DAC/ADC Input/Output Data Bit 7. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
38	DAD6	DAC/ADC Input/Output Data Bit 6. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
39	DAD5	DAC/ADC Input/Output Data Bit 5. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
42	DAD4	DAC/ADC Input/Output Data Bit 4. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
43	DAD3	DAC/ADC Input/Output Data Bit 3. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
45	DAD2	DAC/ADC Input/Output Data Bit 2. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
46	DAD1	DAC/ADC Input/Output Data Bit 1. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
48	DAD0	DAC/ADC Input/Output LSB Data Bit. Input/output of 10-bit, 50MHz bidirectional digital-to-analog and analog-to-digital converter. Data is in binary format.
51	FREEZE	Active-High Freeze-Mode Enable. Drive FREEZE high to place the adaptive gain control (AGC) in freeze mode. Drive FREEZE low if the the signal is not available for the companion baseband chip.
58, 59	I.C.	Internally Connected. Leave these pins unconnected.
61	ENTX	Active-High Transmit Enable. Drive ENTX high to enable the transmitter. Drive ENTX low to place the transmitter in three-state.
62	SWR	Active-High Register Write Enable. Drive SWR high to place the registers in write mode.
63	$\overline{\text{RESET}}$	Active-Low Reset Input. Drive $\overline{\text{RESET}}$ low to place the MAX2981 in reset mode. Set CLK in free-running mode during a reset. The minimum reset pulse width is 100ns.
64	STBY	Active-High Standby Input. Drive STBY high to place the MAX2981 in standby mode. Drive low for normal operation.

Functional Diagram



Detailed Description

The MAX2981 powerline communication AFE and line-driver IC is a state-of-the-art CMOS device that delivers high performance at low cost. This highly integrated design combines an ADC, DAC, AGC, filters, and line driver on a single chip as shown in the *Functional Diagram*. The MAX2981 substantially reduces previously required system components and complies with the HomePlug 1.0 standard.

Combined with Maxim's integrated PHY/MAC digital baseband, the device delivers the most flexible and cost-effective solution. The advanced design of the MAX2981 allows operation without external control, enabling simplified connection to a variety of HomePlug 1.0 digital PHY ICs.

Receive Channel

The receiver analog front-end consists of a variablegain amplifier (VGA), a lowpass filter (LPF), a highpass filter (HPF), and an AGC circuit. An ADC block samples the AGC output. The ADC communicates to the digital PHY chip through a mux block.

The VGA reduces the receive channel input-referred noise by providing some signal gain to the AFE input.

The filter blocks remove unwanted noise, and provide the anti-aliasing required by the ADC for accurate sampling.

The AGC scales the signal for conversion from analog to digital. The scaling maintains the optimum signal level at the ADC input and keeps the AGC amplifiers out of saturation.

The 10-bit ADC samples the analog signal at 50Msps and converts it to a 10-bit digital stream. The block fully integrates reference voltages and biasing for the input differential signal.

Transmit Channel

The transmit channel consists of a 10-bit DAC, a LPF, and an adjustable-gain transmitter buffer and line driver. The DAC receives the data stream from the digital PHY IC through the mux block.

The 50MHz, 10-bit DAC provides the complementary function to the receive channel. The DAC converts the 10-bit digital stream to an analog voltage at a 50MHz rate.

The LPF removes spurs and harmonics adjacent to the desired passband to help reduce the out-of-band transmitted frequencies and energy from the DAC output.

The transmit buffer and line-driver blocks allow the output level of the LPF to obtain a level necessary to connect directly to the powerline medium, without the use of external amplifiers and buffers. The output level is adjustable from $1.4V_{P-P}$ to $4.0V_{P-P}$ differential. The line driver can drive resistive loads as low as 10Ω singleended.

Line Driver Bypass

Use register R6B[2:1] to bypass the line driver. With the line driver bypassed, the output can drive a 50Ω single-ended external load.

Digital Interface

The digital interface is composed of control signals and a 10-bit bidirectional data bus for the DAC and ADC. The control signals include a reset line, a transmit request, an I/O direction request, and a receiver shutdown control.

Control Signals

Transmit Enable (ENTX)

The ENTX line enables the transmitter of the MAX2981 AFE circuit. With ENTX and ENREAD driven high, data sent to the DAC through DAD[9:0] is conditioned and delivered onto the power line.

Read Enable (ENREAD)

The ENREAD line sets the direction of the data bus DAD[9:0]. With ENREAD high, data is sent from the digital PHY to the DAC in the MAX2981 AFE. A low on ENREAD sends data from the ADC to the digital PHY.

Receiver Power-Down (SHRCV)

The SHRCV line provides receiver shutdown control. A logic-high on SHRCV powers down the receiver section of the MAX2981 whenever the device is transmitting. The MAX2981 also features a transmit power-saving mode, which reduces supply current from 350mA to 150mA. To enter the transmit power-saving mode, drive SHRCV high 0.1µs prior to the end of transmission. Connect SHRCV to ENTX and ENREAD for normal operation.

Digital-to-Analog and Analog-to-Digital Converter Input/Output (DAD[9:0])

DAD[9:0] is the 10-bit bidirectional bus connecting the digital PHY to the MAX2981 DAC and ADC. The bus direction is controlled by ENREAD, as described in the *Read Enable (ENREAD)* section.

AGC Control Signal (CS)

The CS signal controls the AGC circuit of the receive path in the MAX2981. A logic-low on CS sets the gain circuit on the input signal to continuously adapt for maximum sensitivity. A valid preamble detected by the digital PHY raises CS to high. While CS is high, the AGC continues to adapt for an additional 8µs; then the AGC locks the currently adapted level on the incoming signal. The digital PHY holds CS high while receiving a transmission, and then lowers CS for continuous adaptation for maximum sensitivity of other incoming signals.

AGC Freeze Mode (FREEZE)

Use the FREEZE signal to instantly lock the AGC gain.

Clock (CLK)

The CLK signal provides all timing for the MAX2981. Apply a 50MHz clock to this input. See the timing diagram (Figure 1) for more information.

Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ signal provides reset control for the MAX2981. To perform a reset, set CLK in free-running mode and drive $\overline{\text{RESET}}$ low for a minimum of 100ns. Always perform a reset at power-up.

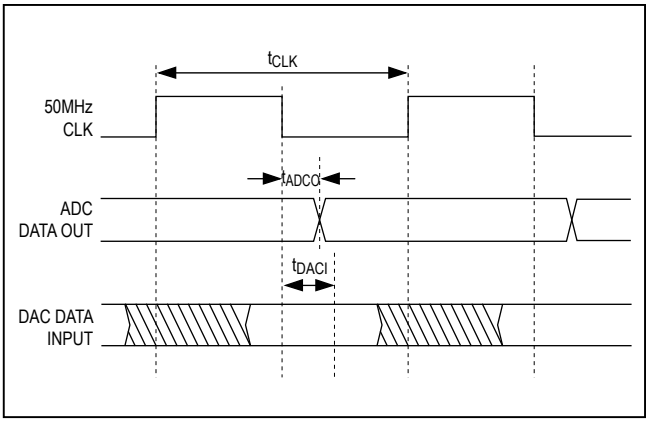


Figure 1. ADC and DAC Timing Diagram

Standby Control (STBY)

The MAX2981 features a low-power, shutdown mode that is activated by STBY. Drive STBY high to place the MAX2981 in standby mode. In standby, the MAX2981 consumes only 20mA with a clock and 5mA without a clock.

MAX2981 Control Registers

MAX2981 Serial Interface

The 3-wire serial interface controls the MAX2981 operation mode. The SCLK is the serial clock line for register programming. The SDIO is the I/O serial data input and output for register writing or reading. The SWR signal controls the write/read mode of the serial interface.

If SWR is high, the serial interface is in write mode and a new value can be written into the MAX2981 registers. Following SWR low-to-high transitions, data is shifted synchronously (LSB first) to registers on the falling edge of the serial clock (SCLK) as illustrated in Figure 2. Note that one extra clock (WR_CLK) is required to write the content of holding the buffer to the appropriate register bank.

If SWR is low, the serial interface is in read mode and the value of the current register can be read. The read operation to a specific register must be followed immediately after writing to the same register. Following SWR high-to-low transitions, data is shifted synchronously (LSB first) to registers on the falling edge of the serial clock (SCLK) as illustrated in Figure 3.

The MAX2981 has a set of six read/write registers; bits A2, A1, A0 are the register address bits.

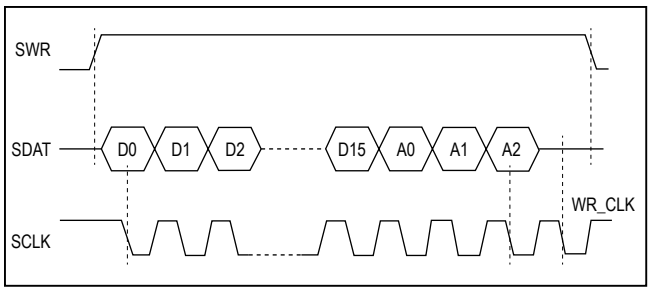


Figure 2. Writing Mode Register Timing Diagram

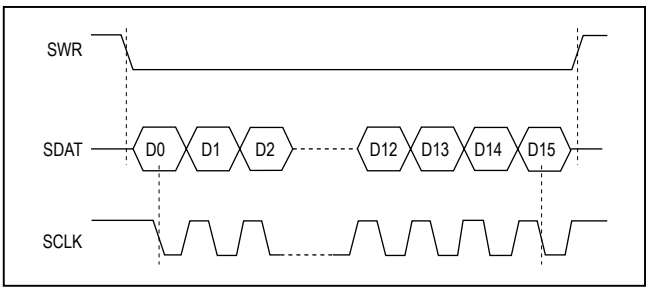


Figure 3. Reading Mode Register Timing Diagram

Table 1. Register Addresses

REGISTER	A2	A1	A0
R1 (R/W)	0	0	0
R2 (R/W)	0	0	1
R3 (R/W)	0	1	0
R4 (R/W)	0	1	1
R5 (R/W)	1	0	0
R6 (R/W)	1	0	1

MAX2981 AFE Register Maps

Table 2. Register R1 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R1B0	High	Active high, powers down the receiver when in transmit mode.
R1B1	High	Active high, powers down the transmitter when in receive mode.
R1B2	Low	Active high, powers down the DAC when in receive mode.
R1B3	Low	Active high, powers down the entire device.
R1B4	Low	Reserved.
R1B5	Low	Reserved.
R1B6	Low	Reserved.
R1B7	Low	Reserved.
R1B8	Low	Reserved.
R1B9	Low	Reserved.
R1B10	Low	Reserved.
R1B11	Low	Reserved.
R1B12	Low	Reserved.
R1B13	Low	Reserved.
R1B14	Low	Reserved.
R1B15	Low	Reserved.

Table 3. Register R2 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R2B0	Low	Reserved.
R2B1	Low	Reserved.
R2B2	Low	Reserved.
R2B3	High	Reserved.
R2B4	Low	Reserved.
R2B5	Low	Reserved.
R2B6	Low	Reserved.
R2B7	Low	Reserved.
R2B8	Low	Reserved.
R2B9	Low	Reserved.
R2B10	Low	Reserved.
R2B11	Low	Reserved.
R2B12	Low	Reserved.
R2B13	Low	Reserved.
R2B14	Low	Reserved.
R2B15	Low	Active high, bypass the receive LPF.

Table 4. Register R3 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R3B0	Low	Reserved.
R3B1	Low	
R3B2	Low	These set the predriver gain as follows setting 000 to 111: 3dB, 2dB, 1dB, 0dB, -1dB, -2dB, -3dB, -6dB R3B2 is the LSB.
R3B3	Low	
R3B4	Low	
R3B5	Low	Reserved.
R3B6	Low	
R3B7	Low	
R3B8	Low	
R3B9	Low	
R3B10	Low	
R3B11	High	Active high, place process tune in continuous mode. Otherwise active only during reset.
R3B[15:12]	0111	Reserved.

Table 5. Register R4 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R4B0	Low	Reserved.
R4B1	High	Reserved.
R4B2	High	Reserved.
R4B3	High	Reserved.
R4B4	Low	Reserved.
R4B5	Low	Reserved.
R4B[10:6]	01011	Reserved.
R4B11	High	Reserved.
R4B12	High	Reserved.
R4B13	High	Reserved.
R4B14	High	Reserved.
R4B15	Low	Reserved.

Table 6. Register R5 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R5B[6:0]	Low	Reserved.
R5B[12:7]	Low	Reserved.
R5B13	Low	Reserved.
R5B14	Low	Reserved.
R5B15	Low	Reserved.

Table 7. Register R6 Map

REGISTER BIT NO.	DEFAULT	COMMENT
R6B0	Low	Reserved.
R6B[2:1]	00	00 internal LD active; 01 internal LD bypassed external load up to 1kΩ and predriver current consumption 21mA; 11 internal LD bypassed external load 50Ω and predriver current consumption 42mA.
R6B3	Low	Reserved.
R6B4	Low	Active high, allow bypass of transmit LPF.
R6B[6:5]	00	Reserved.
R6B7	Low	
R6B8	Low	
R6B9	Low	
R6B[11:10]	10	
R6B[13:12]	00	
R6B14	High	Disable receiver highpass filter.
R6B15	High	Reserved.

Applications Information

Interfacing to Digital PHY Circuit

The MAX2981 interfaces to the MAX2982/MAX2986 digital baseband IC using a bidirectional bus to pass the digital data to and from the DAC and ADC. Handshake lines help accomplish the data transfer and operation of the MAX2981. The application circuit diagram of Figure 4 shows the connection of the MAX2981 to the MAX2982/MAX2986 digital baseband chip.

Layout Considerations

A properly designed PCB is an essential part of any high-speed circuit. Use controlled-impedance lines on all frequency inputs and outputs. Use low-inductance connections to ground on all ground pins and wherever the components are connected to ground. Place decoupling capacitors close to all V_{DD} connections. For proper operation, connect the metal exposed paddle at the back of the IC to the PCB ground plane with multiple vias.

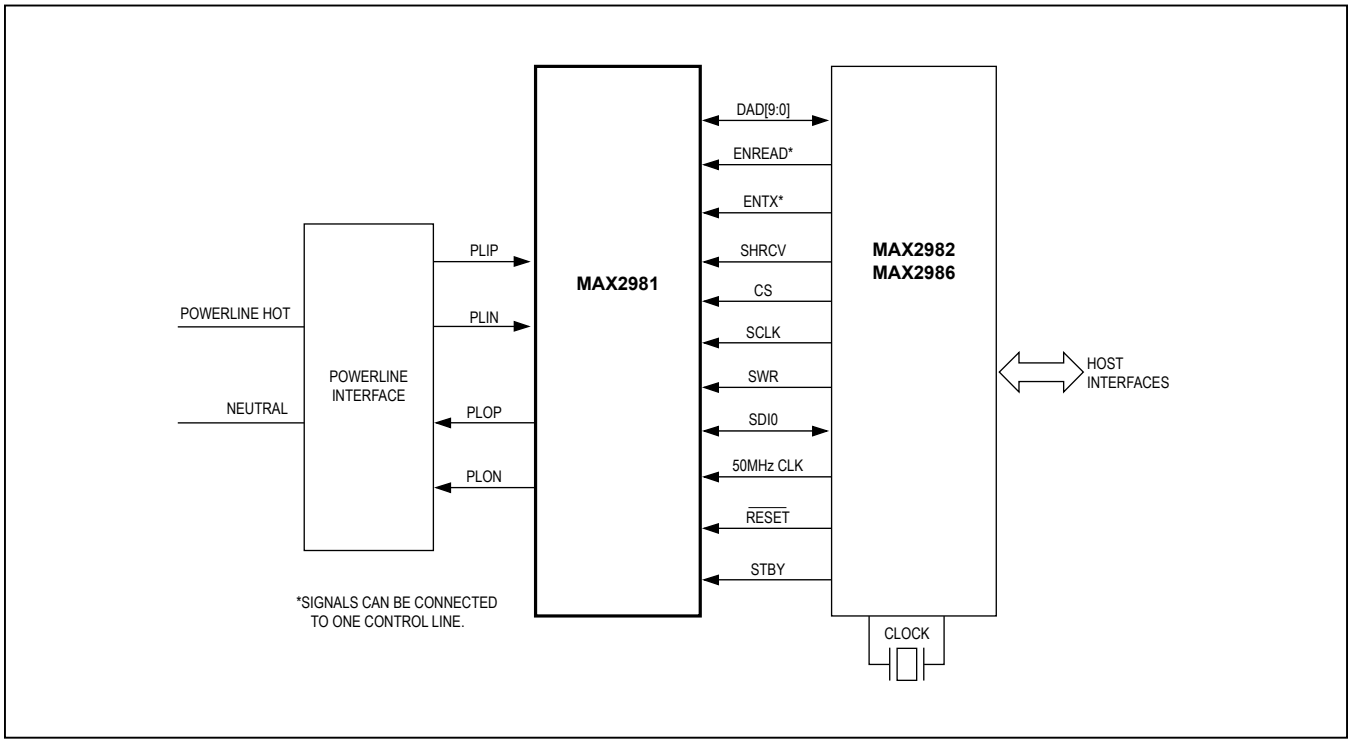


Figure 4. Interfacing the MAX2981 to the MAX2982/MAX2986