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Low-Current, Real-Time Clock with I²C, Power Management, and Integrated Crystal

MAX31329

General Description

The MAX31329 low-current, real-time clock (RTC) is a timekeeping device that provides timekeeping current in nanoamperes, thus extending battery life. The MAX31329 incorporates an integrated 32.768kHz crystal, which eliminates the need for an external crystal. This device is accessed through an I²C serial interface. The MAX31329 features one digital Schmitt trigger input (DIN) and generates an interrupt output on a falling or rising edge of this digital input. An integrated power-on reset function ensures deterministic default register status upon power-up. Other features include two time-of-day alarms, interrupt outputs, a programmable square-wave output, and a serial bus timeout mechanism.

The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either 24-hour or 12-hour format. The MAX31329 also includes a clock input for synchronization. When a reference clock (e.g., 32kHz, 50Hz/60Hz power line, GPS 1pps) is present at the CLKIN pin and the enable external clock input bit (ENCLKIN) is set to 1, the MAX31329 RTC is frequency-locked to the external clock and the clock accuracy is determined by the external source.

The device is available in a lead (Pb)-free/RoHS-compliant, 10-pin, 5mm x 5mm LGA package. The device supports the -40°C to +85°C extended temperature range.

Applications

- Industrial Equipment
- Test and Measurement Equipment
- Energy Meters
- Medical Devices
- Portable Instruments
- Factory Automation
- IoT Devices
- Surveillance Cameras
- Servers

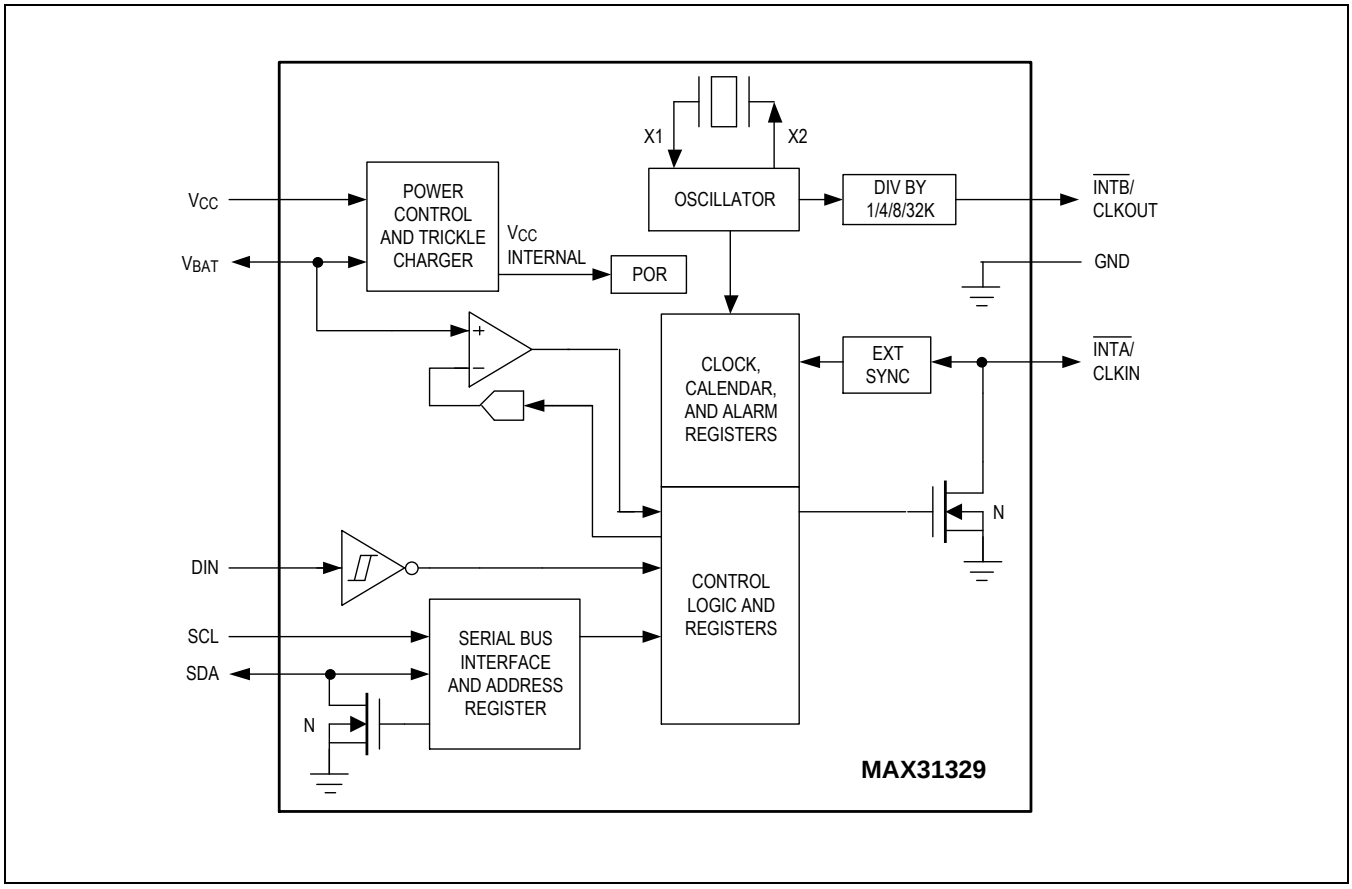
Benefits and Features

- Increases Battery Life
  - 240nA Timekeeping Current
  - Trickle Charger for External Supercapacitor or Rechargeable Battery
- Provides Flexible Configurability
  - A Schmitt Trigger Input for Event Detection
  - Programmable Square-Wave Output for Clock Monitoring
  - Two Interrupt Pins for Multiple Wakeup Configurations
  - Clock Input Pin for External Clock Synchronization
- Saves Board Space
  - Integrated Crystal and Load Capacitors Tuned to ±5ppm Typical Clock Accuracy
  - 5mm x 5mm, 10-Pin LGA Package
- Value-Added Features for Ease-of-Use
  - +1.6V to +5.5V Operating Voltage Range
  - Two Time-of-Day Alarms
  - Countdown Timer with Repeat and Pause Functions
  - 64-Byte RAM for User Data Storage
- Integrated Protection
  - Power-on Reset for Default Configuration
  - Automatic Switchover to Backup Battery or Supercapacitor on Power-Fail
  - Lockup-Free Operation with Bus Timeout

***Ordering Information* appears at end of data sheet.**

19-100992; Rev 1; 12/21

Simplified Block Diagram



Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground .....-0.3V to +6V

Continuous Power Dissipation (Multilayer Board (T_A = +70°C, derate 6.88mW/°C above +70°C) 550.02mW

Operating Temperature Range..... -40°C to +85°C

Junction Temperature .....+125°C

Storage Temperature Range.....-55°C to +85°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	L1055M+2C
Outline Number	*21-100481*
Land Pattern Number	*90-100169*
Thermal Resistance, Multilayer Board:	
Junction to Ambient (θ_{JA})	145.45°C/W
Junction to Case (θ_{JC})	66.67°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = +1.6V to +5.5V = typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Operating Voltage Range	V_{CC}	Full operation (*Note 2*)		1.6		5.5	V
Timekeeping Current	I_{CCT}	CLKIN = GND or CLKIN = V_{CC}	V_{CC} = +1.6V (*Note 3*)		200	500	nA
			V_{CC} = +3.0V		240	550	
			V_{CC} = +5.5V		300	700	
Data Retention Current	I_{BATDR}	(Oscillator stopped and I²C enabled)			5		nA
Maximum Supply Power-Up Slew Rate	T_{VCCR}				5		V/ms
Maximum Supply Switchover Slew Rate	T_{VCCF}				1.4		V/ms
BATTERY BACKUP AND THRESHOLD							
Backup Supply Voltage	V_{BAT}			1.6		5.5	V
Power-Fail Threshold Voltage	V_{PF}	V_{TH1}			1.8		V
		V_{TH2}			2.0		
		V_{TH3}			2.4		
Trickle-Charge Current-Limiting Resistance	R1	Measured at V_{BAT} = 0V			3.3		kΩ
	R2	Measured at V_{BAT} = 0V			6.4		

(V_{CC} = +1.6V to +5.5V = typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	R3	Measured at V_{BAT} = 0V		11.3		
SCHMITT TRIGGER INPUT (DIN)						
Rising Input Threshold Voltage	V_{T+}	V_{CC} = 5.5V		2.8	3.2	V
		V_{CC} = 3.0V		1.65	2	
		V_{CC} = 1.6V		0.9	1.25	
Falling Input Threshold Voltage	V_{T-}	V_{CC} = 5.5V	1.1	1.6		V
		V_{CC} = 3.0V	0.7	0.9		
		V_{CC} = 1.6V	0.35	0.6		
Input Leakage	I_{LI}		-0.1		+0.1	µA
LOGIC INPUTS AND OUTPUTS						
Logic 1 Input	V_{IH}	V_{CC} = 1.6V (Note 1, Note 2)	0.75 x V_{CC}		V_{CC} + 0.3	V
		V_{CC} = 3.01V (Note 1, Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	
		V_{CC} = 5.5V (Note 1, Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	
Logic 0 Input	V_{IL}	(Note 1, Note 2)	-0.3		0.3 x V_{CC}	V
Input Leakage (SCL, INTA/CLKIN)	I_{IL}	Input clock enabled	-0.1		+0.1	µA
Output Leakage (INTA/CLKIN, INTB/CLKOUT)	I_O	Input clock disabled	-1		+1	µA
Output Logic 1 (INTB/CLKOUT)	I_{OH}	V_{OH} = +1.0V, V_{CC} ≥ 1.6V	-0.6			mA
Output Logic 0 (SDA, INTA/CLKIN, INTB/CLKOUT)	I_{OL}	V_{OL} = +0.4V, V_{CC} ≥ 1.6V	2			mA
AC CHARACTERISTICS						
SCL Clock Frequency	f_{SCL}	(Note 4)	10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 5)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 6, Note 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	V_{CC} = 3.0V (Note 8)	100			ns
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Minimum Rise Time of Both SDA and SCL Signals	t_{RMIN}	(Note 9)		20 + 0.1C_B		ns

(V_{CC} = +1.6V to +5.5V = typical values at V_{CC} = +3.0V, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Rise Time of Both SDA and SCL Signals	t_{RMAX}			300		ns
Minimum Fall Time for Both SDA and SCL Signals	t_{FMIN}	(*Note 9*)		20 + 0.1C_B		ns
Maximum Fall Time for Both SDA and SCL Signals	t_{FMAX}			300		ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Maximum Capacitive Load for Each Bus Line	C_B	(*Note 9*)		400		pF
I/O Capacitance	$C_{I/O}$	(*Note 10*)		10		pF
SCL Spike Suppression	t_{SP}	(*Note 10*)		37		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(*Note 11*)		30	150	ms
Timeout Interval	$t_{TIMEOUT}$	(*Note 12*)	25		35	ms
Nominal Frequency	f_O			32.768		kHz
Frequency Accuracy	$\Delta f/f_O$	V_{CC} = 3.0V, T_A = +25°C		±5		ppm

Note 1: Limits at -40°C and +85°C are guaranteed by design; not production tested.

Note 2: Voltage referenced to ground.

Note 3: Specified with I²C bus inactive. Oscillator operational. (ENCLKO = 0, ENCLKIN = 0).

Note 4: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.

Note 5: After this period, the first clock pulse is generated.

Note 6: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 7: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 8: A fast-mode (400kHz) device can be used in a standard-mode (100kHz) system, but the requirement $t_{SU:DAT} \geq$ 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.

Note 9: C_B is the total capacitance of one bus line, including all connected devices, in pF.

Note 10: Guaranteed by design; not 100% production tested.

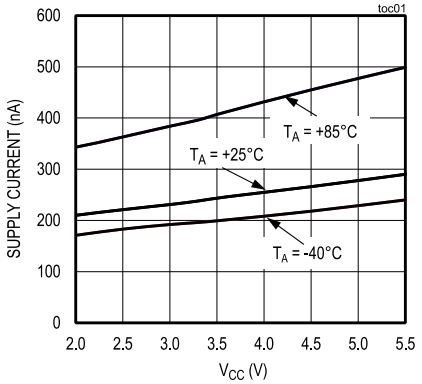
Note 11: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over V_{CC} range.

Note 12: The device I²C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the device detects this condition, the SDA output is released. The oscillator must be running for this function to work.

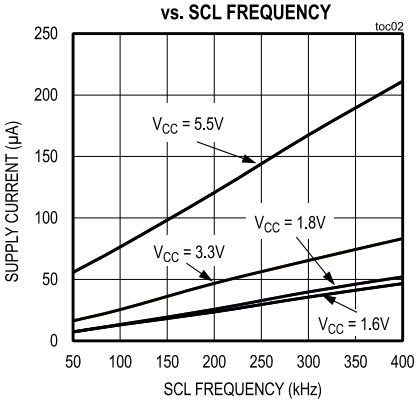
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

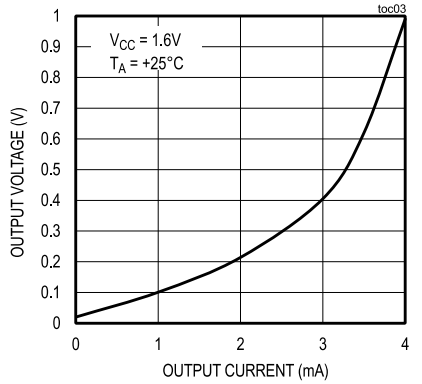
TIMEKEEPING SUPPLY CURRENT vs. SUPPLY VOLTAGE



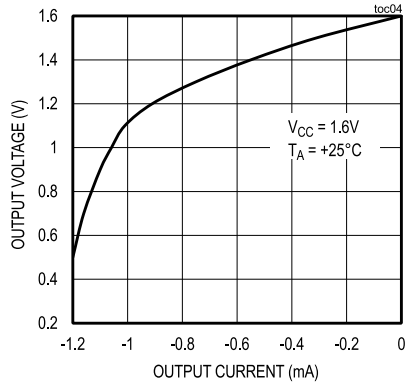
SUPPLY CURRENT vs. SCL FREQUENCY



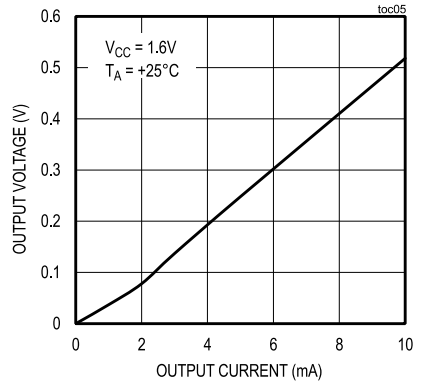
CLKOUT/$\overline{INTB}$ OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



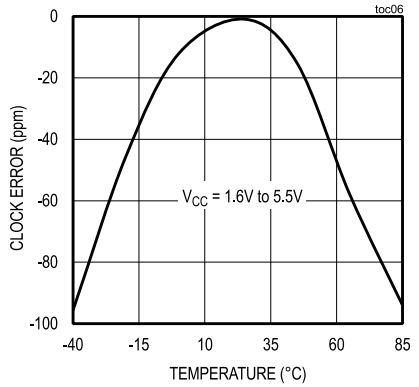
CLKOUT/$\overline{INTB}$ OUTPUT VOLTAGE HIGH vs. OUTPUT CURRENT



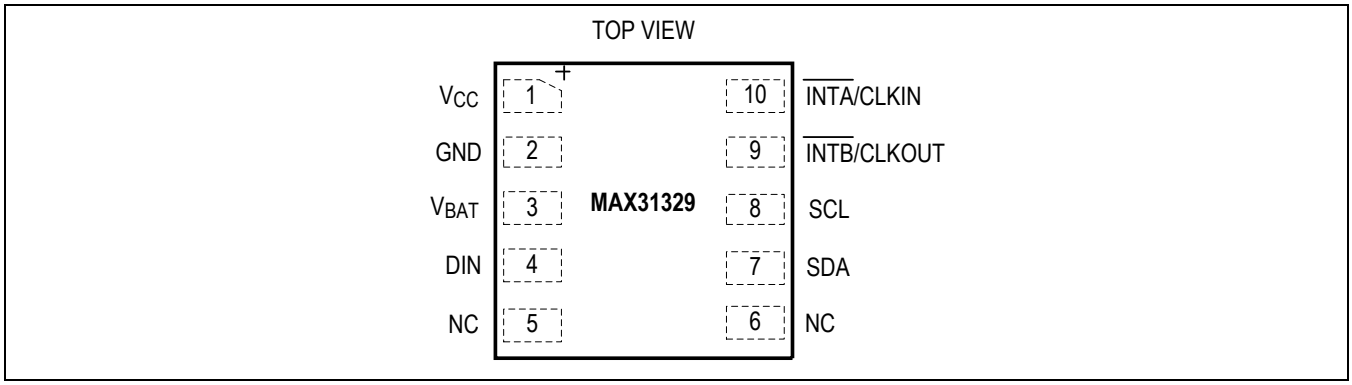
CLKIN/$\overline{INTA}$ OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



CLOCK ERROR vs. TEMPERATURE



Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage
2	GND	Ground Connection
3	V_{BAT}	Backup Battery Input and Trickle Charger Output. Connect to GND when backup battery is not used.
4	DIN	Digital Schmitt Trigger (Event Detection) Input
5, 6	NC	Not Connected
7	SDA	Serial-Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is open-drain and requires an external pullup resistor.
8	SCL	Serial-Clock Input. SCL is used to synchronize data movement on the serial interface.
9	INTB/CLKOUT	Square-Wave Clock or Active-Low Interrupt Output. This pin is used to output a programmable square wave or an alarm interrupt signal. This is a CMOS push-pull output and does not require an external pullup resistor. If not used, this pin can be left unconnected. See *Table 2*.
10	INTA/CLKIN	Clock Input/Active-Low Interrupt Output. This I/O pin is used to output an alarm interrupt or accept an external clock input to drive the RTC counter. In the output mode, this is an open-drain and requires an external pullup resistor. If not used, connect this pin to ground. See *Table 2*.

Detailed Description

The MAX31329 low-current, real-time clock (RTC) is a timekeeping device that provides nanoamperes timekeeping current, extending battery life. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for each month, including corrections for leap year through 2199. The clock operates in either 24-hour or 12-hour format.

The MAX31329 is accessed through an I²C serial interface. The device features one digital Schmitt trigger input and generates an interrupt output on a falling or rising edge of this input (DIN). An integrated power-on reset function ensures deterministic default register status upon power-up. Soft reset is required after a brownout or brief blackout. Other features include two time-of-day alarms, two interrupts, a programmable square-wave output, a countdown timer, and a bus timeout mechanism that resets the I²C bus if it remains inactive for a minimum of $t_{TIMEOUT}$. The MAX31329 uses an integrated 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. The MAX31329 also accepts an external clock reference for synchronization. The external clock can be a 32.768kHz, 50Hz, 60Hz, or 1Hz source. When the enable oscillator bit (ENOSC) is set to 1, the MAX31329 uses the oscillator for timekeeping. If the enable external clock input bit (ENCLKIN) is set to 1, the time base derived from the oscillator is compared to the 1Hz signal that is derived from the CLKIN signal. The conditioned signal drives the RTC time and date counters. When the external clock is lost or when the frequency differs more than ±0.8% from the crystal frequency, the loss-of-sync (LOS) flag is asserted.

Address and data are transferred serially through an I²C serial interface.

Clock/Calendar

The time and calendar information are obtained by reading the appropriate I²C registers. The time and calendar data are set or initialized by writing to the appropriate time/date registers. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The century bit (bit 7 of the Month register) is toggled when the Year register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the secondary buffers are synchronized to the internal registers on any I²C START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

I²C Interface

The I²C interface is guaranteed to operate when V_{CC} is between 1.6V and 5.5V. The I²C interface is accessible whenever V_{CC} is at a valid level. To prevent invalid device operation, the I²C interface should not be accessed when V_{CC} is below +1.6V. The slave address is defined as the 7 most significant bits (MSbs) sent by the master after a START condition. The address is 0xD0 (left justified with LSb set to 0). The 8th bit is used to define a write or read operation. If a microcontroller connected to the MAX31329 resets during I²C communication, it is possible that the microcontroller and the MAX31329 could become unsynchronized. When the microcontroller resets, the MAX31329 I²C interface can be placed into a known state by holding SCL low for $t_{TIMEOUT}$. Doing so limits the minimum frequency at which the I²C interface can be operated. If data is being written to the device when the interface timeout is exceeded, prior to the acknowledge, the incomplete byte of data is not written.

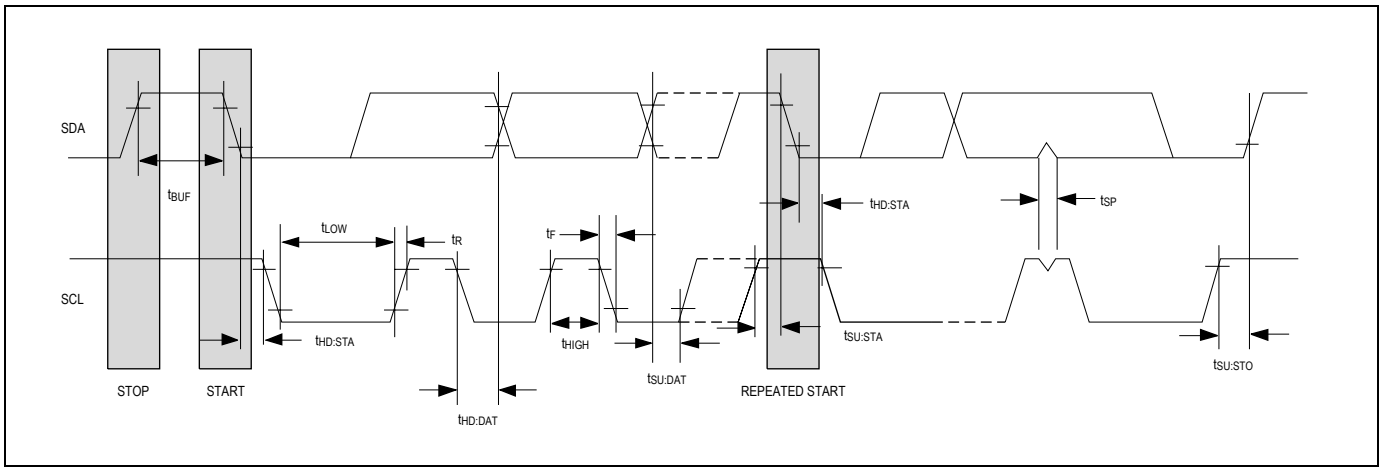


Figure 1. Data Transfer on I²C Serial Bus

Burst Mode

Burst read/write allows the controller to read/write multiple consecutive bytes from a device. It is initiated in the same manner as the byte read/write operation, but instead of terminating the read/write cycle after the first data byte is transferred, the controller can read/write to the whole register array. In burst write operation, after the receipt of each byte, the device responds with an acknowledge, and the address is internally incremented by one. When the address pointer reaches the end of the register address list, it goes back to the first register address. In burst read mode, the controller responds with an acknowledge, indicating it is waiting for additional data. The device continues to output data for each acknowledge received. The controller terminates the read operation by not responding with an acknowledge and issuing a STOP condition.

Oscillator Circuit

The MAX31329 uses an integrated 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. After the oscillator is enabled, the startup time of the oscillator circuit is usually less than 1 second.

Power Management

The MAX31329 has a power-management function which monitors supply voltage on V_{CC} and backup battery voltage on V_{BAT}, and then determines which source to use as internal supply. There is a PFAIL interrupt flag status bit in the register map to indicate the power-fail condition. In power-management mode, the V_{BAT} pin should be connected to the backup battery. If there is no backup battery, V_{BAT} should be tied to ground. Power-management control bits Pwr_mgmt[3:2] (register 0x18h) are used as follows: For the Power-Management Auto and Trickle Charger mode, specify a “power-fail voltage” with the register Pwr_mgmt[3:2]. Pwr_mgmt[3:2] = 01b sets the power-fail voltage to V_{TH1}. Pwr_mgmt[3:2] = 10b sets the power-fail voltage to V_{TH2}. Pwr_mgmt[3:2] = 11b sets the power-fail voltage to V_{TH3}. See the values of V_{TH1}, V_{TH2}, and V_{TH3} in the *Electrical Characteristics* table. Note that Pwr_mgmt[3:2] = 00b, V_{TH1} is not a valid power-fail voltage. Once the power-fail voltage is set, the MAX31329 switches backup battery to the internal power supply if and only if main supply V_{CC} is lower than both the power-fail voltage and the backup battery voltage. Otherwise, V_{CC} remains as the main supply. There is an PFAIL interrupt flag status bit in the status reg (00h) register that can be used as a power-fail flag. The PFAIL interrupt flag monitors the V_{CC} supply and is set when V_{CC} falls below the power-fail threshold voltage set through PFVT in the Pwr_mgmt (18h) register or when power-fail threshold voltage is adjusted to cross above V_{CC}.

Table 1. Power Management

D_TRKCHG_EN	D_VBACK_SEL	D_MAN_SEL	MODE OF OPERATION	
1	x	0	Power-Management Auto and Trickle Charger On	
			Supply Condition	**Active Supply**
			$V_{CC} < V_{TH}$, $V_{CC} < V_{BAT}$	V_{BAT}
			$V_{CC} < V_{TH}$, $V_{CC} > V_{BAT}$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} < V_{BAT}$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} > V_{BAT}$	V_{CC}
1	0	1	Power-Management Manual and Trickle Charger On Active Supply = V_{CC}	
1	1	1	Power-Management Manual and Trickle Charger On Active Supply = V_{BAT} for $V_{BAT} \geq V_{CC}$	
0	x	0	Power-Management Auto and Trickle Charger Off	
			Supply Condition	**Active Supply**
			$V_{CC} < V_{TH}$, $V_{CC} < V_{BAT}$	V_{BAT}
			$V_{CC} < V_{TH}$, $V_{CC} > V_{BAT}$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} < V_{BAT}$	V_{CC}
			$V_{CC} > V_{TH}$, $V_{CC} > V_{BAT}$	V_{CC}
0	0	1	Power-Management Manual and Trickle Charger Off Active Supply = V_{CC}	
0	1	1	Power-Management Manual and Trickle Charger Off Active Supply = V_{BAT} for $V_{BAT} \geq V_{CC}$	

Trickle Charger

The trickle charger is for charging an external supercapacitor or a rechargeable battery. The maximum charging current can be calculated as follows:

$I_{MAX} = (V_{CC} - V_D - V_{BAT})/R$

Where V_D is the diode voltage drop, V_{BAT} is the voltage of the battery being charged, and R is the resistance selected in the charging path. As the battery charges, the battery voltage increases and the voltage across the charging path decreases. Therefore, the charging current also decreases.

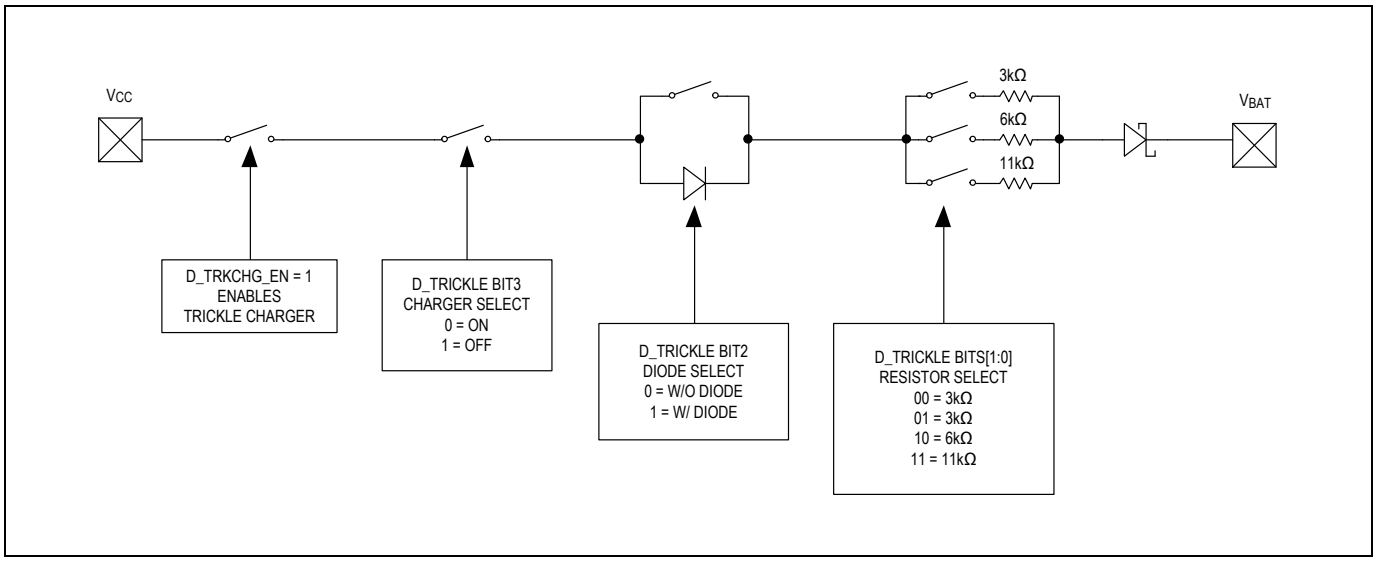


Figure 2. Trickle Charger Register (19h)

Interrupt Status and Outputs

When an interrupt is asserted, a corresponding status bit in Int_status_reg (xxh) becomes “1”, and an interrupt output transitions from high to low. The interrupt status bit and output can be cleared by reading Int_status_reg. See *Table 2* for interrupt configurations.

Table 2. Interrupt Modes

ENCLKO	**ENCLKIN**	INTA/**CLKIN**	INTB/**CLKOUT**
0	0	INTA: Alarm1, Timer, Power-Fail (PFAIL), Digital Interrupt (DIN)	INTB: Alarm2
0	1	CLKIN	INTB: Alarm1, Alarm2, Timer, PFAIL, DIN
1	0	INTA: Alarm1, Alarm2, Timer, PFAIL, DIN	CLKOUT
1	1	CLKIN	CLKOUT

Data Retention Mode

The MAX31329 features a Data Retention mode wherein the device shuts down its internal functional blocks (including the oscillator) except the I²C interface. The device consumes 5nA (typ) in this mode. It retains all of the register contents, including the last valid date and time values. Exit Data Retention mode to resume counting. User data can be preserved in this mode as long as the active supply is present. To enter the Data Retention mode, write "1" to DATA_RET in the RTC_config1(03h) register. To exit the Data Retention mode, write "0" to DATA_RET in the RTC_config1(03h) register.

Alarms

The MAX31329 contains two time-of-day/date alarms. Alarm1 can be set by writing to registers 0Dh–12h. Alarm2 can be set by writing to registers 13h–15h. See *Table 3* and *Table 4*. The alarms can be programmed by the A1IE and A2IE bits in Int_en register to activate the INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers and bit 6 of Alm1_mon register are mask bits (*Table 2*). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day, date, month, and year alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. *Table 3* and *Table 4* show the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0–5 of that register represents the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

Table 3. Alarm1 Modes

DY/DT	ALARM1 REGISTER MASK BITS (BIT 7)						ALARM RATE
	A1M6	A1M5	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	1	1	Alarm once a second
X	1	1	1	1	1	0	Alarm when seconds match
X	1	1	1	1	0	0	Alarm when minutes and seconds match
X	1	1	1	0	0	0	Alarm when hours, minutes, and seconds match
0	1	1	0	0	0	0	Alarm when dates, hours, minutes, and seconds match
0	1	0	0	0	0	0	Alarm when months, dates, hours, minutes, and seconds match
0	0	0	0	0	0	0	Alarm when years, months, dates, hours, minutes, and seconds match
1	1	1	0	0	0	0	Alarm when days, hours, minutes, and seconds match

Table 4. Alarm2 Modes

DY/DT	ALARM2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	Alarm once per minute (00 seconds of every minute)
X	1	1	1	Alarm when minutes match
X	1	1	0	Alarm when hours and minutes match
X	1	0	0	Alarm when dates, hours, and minutes match
0	0	0	0	Alarm when days, hours, and minutes match
1	0	0	0	Alarm when days, hours, and minutes match

Countdown Timer

The MAX31329 features a countdown timer with a pause function. The timer can be configured by writing into registers Timer_config (05h) and Timer_init (17h). The Timer_init register should be loaded with the initial value from which the timer would start counting down. The Timer_config register allows these configuration options:

- Select the frequency of the timer using the TFS[1:0] field.
- Start/stop the timer using the TE (Timer Enable) bit.
- Enable/disable the timer repeat function using the TRPT bit. This function reloads and restarts the timer with the same init value once it counts down to 0.
- Pause/resume the countdown at any time when the timer is enabled using the TPAUSE bit (explained below).

The timer can be programmed to assert the INT output (see *Table 2*) whenever it counts down to 0. This can be enabled/disabled using the TIE bit in register Int_en register (01h).

The TPAUSE bit is only valid when TE = 1. This bit must be reset to 0 whenever TE is reset to 0.

Table 5 highlights the steps to be used for various use cases involving TE and TPAUSE.

Typical use cases:

- Countdown timer without pause: Step 1 -> Step 2 -> Step 1, and so on
- Countdown timer with pause: Step 1 -> Step 2 -> Step 3a -> Step 3b -> Step 1, and so on

Table 5. Countdown Timer Sequence

SEQUENCE	TE	TPAUSE	ACTION
Step 1	0	0	Countdown timer is reset, and ready for next countdown operation. Timer_init can be programmed in this state.
Step 2	1	0	Countdown timer starts counting down from the value programmed in Timer_init.
Step 3a (Optional)	1	1	Countdown timer is paused and is ready to start counting down when TPAUSE is programmed back to ‘0’. Contents of the countdown timer are preserved in this state.
Step 3b If 3a is true	1	0	Countdown timer is brought out of pause state and starts counting down from the paused value.
	0	1	Not allowed

Applications Information

Power Supply Decoupling

To achieve the best results when using the device, decouple the V_{CC} and/or V_{BAT} power supplies with 0.1µF and/or 1.0µF capacitors. Use a high-quality, ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance and ceramic capacitors tend to have adequate high-frequency response for decoupling applications. If communications during battery operation are not required, the V_{BAT} decoupling capacitor can be omitted.

Using Open-Drain Outputs

The INTA output is open-drain and, therefore, requires external pullup resistor to realize logic-high output levels. Pullup resistor values around 10kΩ are typical.

Battery Leakage Current

When the MAX31329 switches from V_{CC} to V_{BAT} supply, all of the I/O buffers internally operate on a V_{BAT} supply rail. If these pins are externally connected to an intermediate voltage level (between 0.7V and V_{BAT} - 0.7V), there will be a high leakage current (tens of microamperes) on the V_{BAT} supply. This scenario can occur when the system V_{CC} rail is discharging and the MAX31329 has switched to V_{BAT} supply, but the I/O pins are pulled up to the V_{CC} rail. Set EN_IO = 0 in RTC_Config1 register (03h) to ensure that all of the open-drain I/O pins (SDA, SCL, INTA/CLKIN) are disabled before switching the main supply to V_{BAT} to minimize the leakage current. These pins will be automatically enabled when the MAX31329 switches back to the V_{CC} supply.

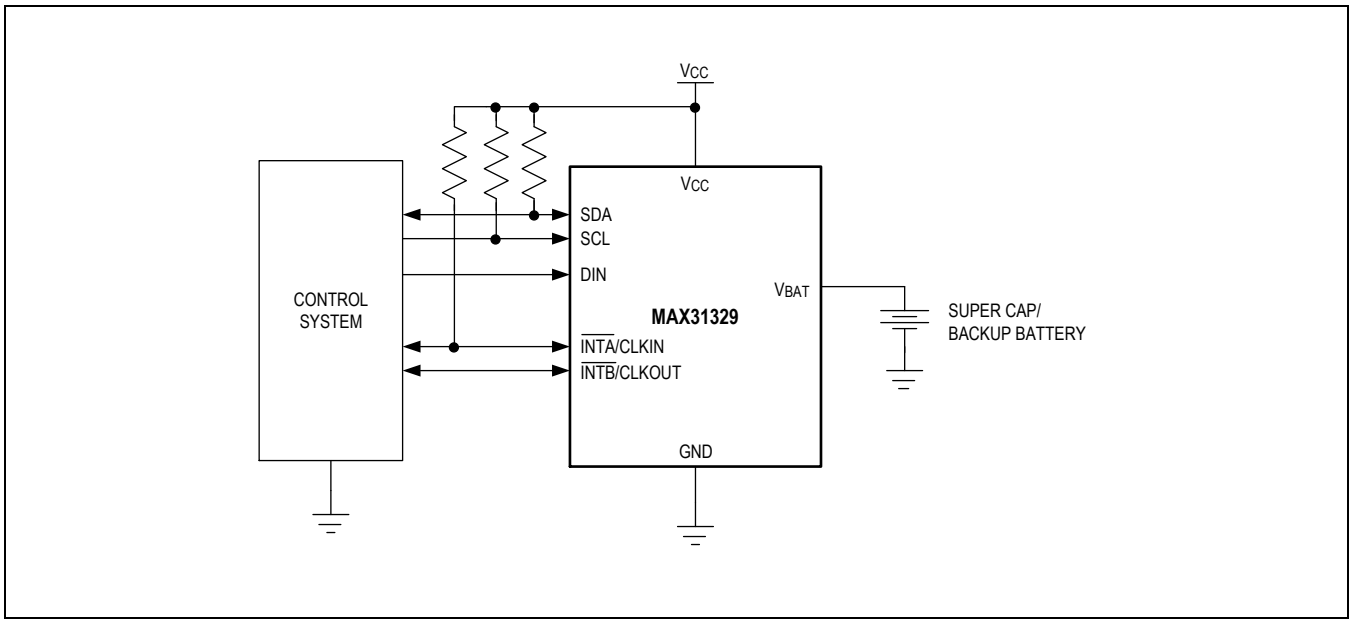
SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high level. Because the device does not use clock cycle stretching, a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Handling

The MAX31329 package contains an integrated resonator. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the resonator.

Typical Application Circuit



Register Map

REGS

ADDRESS	NAME	MSB							LSB
REGBLK									
0x00	STATUS[7:0]	PSDECT	OSF	PFAIL	LOS	DIF	TIF	A2F	A1F
0x01	INT_EN[7:0]	–	DOSF	PFAILE	–	DIE	TIE	A2IE	A1IE
0x02	RTC_RESET[7:0]	–	–	–	–	–	–	–	SWRST
0x03	RTC_CONFIG1[7:0]	–	–	–	–	EN_IO	DATA_RET	I2C_TIMEOUT	ENOSC
0x04	RTC_CONFIG2[7:0]	ENCLKO	CLKO_HZ[1:0]		–	DIP	ENCLKIN	CLKIN_HZ[1:0]	
0x05	TIMER_CONFIG[7:0]	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
0x06	SECONDS[7:0]	–	SEC_10[2:0]			SECONDS[3:0]			
0x07	MINUTES[7:0]	–	MIN_10[2:0]			MINUTES[3:0]			
0x08	HOURS[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x09	DAY[7:0]	–	–	–	–	–	DAY[2:0]		
0x0A	DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x0B	MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x0C	YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x0D	ALM1_SEC[7:0]	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
0x0E	ALM1_MIN[7:0]	A1M2	A1_MIN_10[2:0]			A1_MINUTES[3:0]			
0x0F	ALM1_HRS[7:0]	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]			
0x10	ALM1_DAY_DATE[7:0]	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
0x11	ALM1_MON[7:0]	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			
0x12	ALM1_YEAR[7:0]	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
0x13	ALM2_MIN[7:0]	A2M2	A2_MIN_10[2:0]			A2_MINUTES[3:0]			

ADDRESS	NAME	MSB							LSB
0x14	ALM2_HRS[7:0]	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
0x15	ALM2_DAY_DATE[7:0]	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
0x16	TIMER_COUNT[7:0]	TIMER_COUNT[7:0]							
0x17	TIMER_INIT[7:0]	TIMER_INIT[7:0]							
0x18	PWR_MGMT[7:0]	–	–	–	–	PFVT[1:0]		D_VBACK_SEL	D_MAN_SEL
0x19	TRICKLE_REG[7:0]	D_TRKCHG_EN	–	–	–	D_TRICKLE[3:0]			
RAM_REG									
0x22	Ram_reg 0[7:0]	DATA[7:0]							
0x23	Ram_reg 1[7:0]	DATA[7:0]							
0x24	Ram_reg 2[7:0]	DATA[7:0]							
0x25	Ram_reg 3[7:0]	DATA[7:0]							
0x26	Ram_reg 4[7:0]	DATA[7:0]							
0x27	Ram_reg 5[7:0]	DATA[7:0]							
0x28	Ram_reg 6[7:0]	DATA[7:0]							
0x29	Ram_reg 7[7:0]	DATA[7:0]							
0x2A	Ram_reg 8[7:0]	DATA[7:0]							
0x2B	Ram_reg 9[7:0]	DATA[7:0]							
0x2C	Ram_reg 10[7:0]	DATA[7:0]							
0x2D	Ram_reg 11[7:0]	DATA[7:0]							
0x2E	Ram_reg 12[7:0]	DATA[7:0]							
0x2F	Ram_reg 13[7:0]	DATA[7:0]							
0x30	Ram_reg 14[7:0]	DATA[7:0]							
0x31	Ram_reg 15[7:0]	DATA[7:0]							
0x32	Ram_reg 16[7:0]	DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x33	Ram_reg 17[7:0]	DATA[7:0]							
0x34	Ram_reg 18[7:0]	DATA[7:0]							
0x35	Ram_reg 19[7:0]	DATA[7:0]							
0x36	Ram_reg 20[7:0]	DATA[7:0]							
0x37	Ram_reg 21[7:0]	DATA[7:0]							
0x38	Ram_reg 22[7:0]	DATA[7:0]							
0x39	Ram_reg 23[7:0]	DATA[7:0]							
0x3A	Ram_reg 24[7:0]	DATA[7:0]							
0x3B	Ram_reg 25[7:0]	DATA[7:0]							
0x3C	Ram_reg 26[7:0]	DATA[7:0]							
0x3D	Ram_reg 27[7:0]	DATA[7:0]							
0x3E	Ram_reg 28[7:0]	DATA[7:0]							
0x3F	Ram_reg 29[7:0]	DATA[7:0]							
0x40	Ram_reg 30[7:0]	DATA[7:0]							
0x41	Ram_reg 31[7:0]	DATA[7:0]							
0x42	Ram_reg 32[7:0]	DATA[7:0]							
0x43	Ram_reg 33[7:0]	DATA[7:0]							
0x44	Ram_reg 34[7:0]	DATA[7:0]							
0x45	Ram_reg 35[7:0]	DATA[7:0]							
0x46	Ram_reg 36[7:0]	DATA[7:0]							
0x47	Ram_reg 37[7:0]	DATA[7:0]							
0x48	Ram_reg 38[7:0]	DATA[7:0]							
0x49	Ram_reg 39[7:0]	DATA[7:0]							
0x4A	Ram_reg 40[7:0]	DATA[7:0]							
0x4B	Ram_reg 41[7:0]	DATA[7:0]							
0x4C	Ram_reg 42[7:0]	DATA[7:0]							

ADDRESS	NAME	MSB							LSB
0x4D	Ram_reg 43[7:0]	DATA[7:0]							
0x4E	Ram_reg 44[7:0]	DATA[7:0]							
0x4F	Ram_reg 45[7:0]	DATA[7:0]							
0x50	Ram_reg 46[7:0]	DATA[7:0]							
0x51	Ram_reg 47[7:0]	DATA[7:0]							
0x52	Ram_reg 48[7:0]	DATA[7:0]							
0x53	Ram_reg 49[7:0]	DATA[7:0]							
0x54	Ram_reg 50[7:0]	DATA[7:0]							
0x55	Ram_reg 51[7:0]	DATA[7:0]							
0x56	Ram_reg 52[7:0]	DATA[7:0]							
0x57	Ram_reg 53[7:0]	DATA[7:0]							
0x58	Ram_reg 54[7:0]	DATA[7:0]							
0x59	Ram_reg 55[7:0]	DATA[7:0]							
0x5A	Ram_reg 56[7:0]	DATA[7:0]							
0x5B	Ram_reg 57[7:0]	DATA[7:0]							
0x5C	Ram_reg 58[7:0]	DATA[7:0]							
0x5D	Ram_reg 59[7:0]	DATA[7:0]							
0x5E	Ram_reg 60[7:0]	DATA[7:0]							
0x5F	Ram_reg 61[7:0]	DATA[7:0]							
0x60	Ram_reg 62[7:0]	DATA[7:0]							
0x61	Ram_reg 63[7:0]	DATA[7:0]							

Register Details

STATUS (0x0)

Interrupt Status Register

BIT	7	6	5	4	3	2	1	0
Field	PSDECT	OSF	PFAIL	LOS	DIF	TIF	A2F	A1F

Reset	0b0	0b1	0b0	0x0	0b0	0b0	0b0	0b0
Access Type	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
PSDECT	7	Main Supply Source Indication	0x0: Part is running on V_{CC} 0x1: Part is running on V_{BAT}
OSF	6	Oscillator Stop Flag	0x0: Set to 0 when oscillator is running or when DOSF = 1. 0x1: Set to 1 when oscillator has stopped. An interrupt will not be generated on interrupt pins.
PFAIL	5	Power-Fail Flag	0x0: Set to zero when there is no power-fail condition on V_{CC}. 0x1: Set to 1 when there is a power-fail condition on V_{CC}. When this is set to '1', and PFAILE = 1, an interrupt will be generated on pin INTAb/INTBb. After an initial power-fail condition occurs, if the condition does not persist, this bit can only be cleared by reading the Status register.
LOS	4	Loss of Signal. Valid only for external clock modes. (ENCLKIN = 1)	0x0: Oscillator clock frequency is within 0.8% of the external clock frequency. 0x1: Oscillator clock frequency differs more than 0.8% from the external clock frequency.
DIF	3	Digital (DIN) Interrupt Flag	0x0: Set to zero if DIN interrupt is not triggered. 0x1: Set to 1 when DIN interrupt is triggered. When this is set to '1', and DIE = 1, an interrupt will be generated on pin INTAb/INTBb.
TIF	2	Timer Interrupt Flag	0x0: Set to zero when countdown timer is not zero. 0x1: Set to 1 when countdown timer reaches to zero. When this is set to '1', and TIE = 1, an interrupt will be generated on pin INTAb/INTBb.
A2F	1	Alarm2 Interrupt Flag	0x0: Set to 0 when RTC time does not match the alarm2 register. 0x1: Set to 1 when RTC time matches the alarm2 register. When this bit is set, and A2IE = 1, an interrupt will be generated on INTAb/INTBb.
A1F	0	Alarm1 Interrupt Flag	0x0: Set to zero when RTC time doesn't match to alarm1 register. 0x1: Set to 1 when RTC time matches the alarm1 register. When this is set to 1, and A1IE=1, an interrupt will be generated on pin INTAb/INTBb.

INT_EN (0x1)

Interrupt Enable Register

BIT	7	6	5	4	3	2	1	0
Field	–	DOSF	PFAILE	–	DIE	TIE	A2IE	A1IE
Reset	–	0b0	0b0	–	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DOSF	6	Disable Oscillator Flag	0x0: Allow the OSF to indicate the oscillator status. 0x1: Disable the oscillator flag, irrespective of the oscillator status.

BITFIELD	BITS	DESCRIPTION	DECODE
PFAILE	5	Power-Fail Interrupt Enable	0x0: When set to 0, power-fail interrupt function is disabled. 0x1: When set to 1, power-fail interrupt function is enabled.
DIE	3	Digital (DIN) Interrupt Enable	0x0: Disable DIN interrupt function 0x1: Enable DIN interrupt function
TIE	2	Timer Interrupt Enable	0x0: Disable timer interrupt function 0x1: Enable timer interrupt function
A2IE	1	Alarm2 Interrupt Enable	0x0: Disable alarm2 interrupt function 0x1: Enable alarm2 interrupt function
A1IE	0	Alarm1 Interrupt Enable	0x0: Disable alarm1 interrupt function 0x1: Enable alarm1 interrupt function

RTC_RESET (0x2)

RTC Software Reset Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWRST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
SWRST	0	Active-High Software Reset Bit. To exit the reset state, this bit must be cleared.	0x0: When set to 0, the device is in normal working mode. 0x1: When set to 1, resets the digital block and the I²C-programmable registers, except for RAM registers and RTC_reset.SWRST. Oscillator is disabled.

RTC_CONFIG1 (0x3)

RTC Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_IO	DATA_RET	I2C_TIMEOUT	ENOSC
Reset	–	–	–	–	0b1	0b0	0b1	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_IO	3	Disables All Open-Drain I/Os (SDA, SCL, INTAb/CLKIN) when running on V_{BAT}. No effect when running on V_{CC}.	0x0: Disables all open-drain I/Os when running on V_{BAT}. 0x1: Enables all open-drain I/Os when running on V_{BAT}.

BITFIELD	BITS	DESCRIPTION	DECODE
DATA_RET	2	Data Retention Mode Enable/Disable	0x0: Normal operation mode 0x1: Data Retention mode
I2C_TIMEOUT	1	I²C Timeout Enable	0x0: Disables I²C timeout 0x1: Enables I²C timeout
ENOSC	0	Active-High Enable for Oscillator	0x0: Disable oscillator 0x1: Enable oscillator

RTC_CONFIG2 (0x4)

RTC Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	ENCLKO	CLKO_HZ[1:0]		–	DIP	ENCLKIN	CLKIN_HZ[1:0]	
Reset	0b0	0b00		–	0x0	0x0	0b00	
Access Type	Write, Read	Write, Read		–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ENCLKO	7	CLKO Enable	0x0: Sets INTBb/CLKOUT pin as INTBb (interrupt). 0x1: Sets INTBb/CLKOUT pin as CLKO (clock output).
CLKO_HZ	6:5	Set Output Clock Frequency on INTB/CLKOUT	0x0: 1Hz 0x1: 4.096kHz 0x2: 8.192kHz 0x3: 32.768kHz
DIP	3	Digital (DIN) Interrupt Polarity	0x0: Interrupt triggers on falling edge of DIN input. 0x1: Interrupt triggers on rising edge of DIN input.
ENCLKIN	2	CLKIN Enable	0x0: Sets INTAb/CLKIN pin as INTAb (interrupt). 0x1: Sets INTAb/CLKIN pin as CLKIN (clock input).
CLKIN_HZ	1:0	Set Input Clock Frequency on INTA/CLKIN	0x0: 1Hz 0x1: 50Hz 0x2: 60Hz 0x3: 32.768kHz

TIMER_CONFIG (0x5)

Countdown Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
Reset	–	–	–	0b0	0b0	0b1	0b00	
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TE	4	Timer Enable	0x0: Timer is reset when set to 0. New timer countdown value (Timer_Init) can be programmed in this state. Note: In this state, ensure TPAUSE is also programmed to

BITFIELD	BITS	DESCRIPTION	DECODE
		Also see the TPAUSE field for additional information.	0 if TPAUSE was set to 1 earlier. 0x1: Timer starts counting down from the value programmed in Timer_Init.
TPAUSE	3	Timer Pause. This field is valid only when TE = 1. When TE will be programmed to 0, this field must also be reset to 0. Details about Timer Pause are explained in detail in another section of the data sheet.	0x0: Timer continues to count down from the paused count value as per programming. 0x1: Timer is paused, however, the count value is retained. When this bit is reset back to 0, the countdown continues from the paused value.
TRPT	2	Timer Repeat Mode. Controls the timer interrupt function.	0x0: Countdown timer will halt once it reaches 0. 0x1: Countdown timer reloads the value from the timer initial register upon reaching 0 and continues counting.
TFS	1:0	Timer Frequency Selection	0x0: 1024Hz 0x1: 256Hz 0x2: 64Hz 0x3: 16Hz

SECONDS (0x6)

Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SECONDS[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC Seconds in Multiples of 10
SECONDS	3:0	RTC Seconds Value

MINUTES (0x7)

Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MINUTES[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	RTC Minutes in Multiples of 10

BITFIELD	BITS	DESCRIPTION
MINUTES	3:0	RTC Minutes Value

HOURS (0x8)

Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-Hour or 24-Hour Format	0x0: 24-hour format 0x1: 12-hour format
HR_20_AM_PM	5	In 12-hour format, this works as the AM/PM indicator. In 24-hour format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hour format. 0x1: Indicates PM in 12-hour format.
HR_10	4	RTC Hours in Multiples of 10 (BCD)	
HOUR	3:0	RTC Hours Value (BCD)	

DAY (0x9)

Day Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DAY[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read, Dual		

BITFIELD	BITS	DESCRIPTION
DAY	2:0	RTC Days

DATE (0xA)

Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x1			
Access Type	–	–	Write, Read, Dual		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	RTC Date in Multiples of 10 (BCD)
DATE	3:0	RTC Date (BCD)

MONTH (0xB)

Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x1			
Access Type	Write, Read, Dual	–	–	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
CENTURY	7	Century Bit	0x0: Year is in 21st century. 0x1: Year is in 22nd century.
MONTH_10	4	RTC Month in Multiples of 10 (BCD)	
MONTH	3:0	RTC Months (BCD)	

YEAR (0xC)

Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read, Dual				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	RTC Year Multiples of 10 (BCD)

BITFIELD	BITS	DESCRIPTION
YEAR	3:0	RTC Years (BCD)

ALM1_SEC (0xD)

Alarm1 Seconds Configuration Register

DY_DT	A1M6	A1M5	A1M4	A1M3	A1M2	A1M1	ALARM RATE
x	1	1	1	1	1	1	Once per sec
x	1	1	1	1	1	0	Sec match
x	1	1	1	1	0	0	Min and sec match
x	1	1	1	0	0	0	Hour, min, and sec match
0	1	1	0	0	0	0	Date and time match
0	1	0	0	0	0	0	Month, date, and time match
0	0	0	0	0	0	0	Year, month, date, and time match
1	1	1	0	0	0	0	Day and time match

Alarm 1 can be set by writing to registers 0Dh–12h. See the Register Map. The alarm can be programmed by the A1IE bit in Int_en reg (01h) register to activate the INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers, and Bit 7 and 6 of the month alarm register are mask bits. When all of the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarm can also be programmed to repeat every second, minute, hour, day, date, month, or year. The table above shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with the day of the week.

BIT	7	6	5	4	3	2	1	0
Field	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M1	7	Alarm1 Mask Bit for Seconds
A1_SEC_10	6:4	Alarm1 Seconds in Multiples of 10
A1_SECONDS	3:0	Alarm1 Seconds

ALM1_MIN (0xE)

Alarm1 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M2	A1_MIN_10[2:0]			A1_MINUTES[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M2	7	Alarm1 Mask Bit for Minutes
A1_MIN_10	6:4	Alarm1 Minutes in Multiples of 10
A1_MINUTES	3:0	Alarm1 Minutes

ALM1_HRS (0xF)

Alarm1 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]			
Reset	0b0	–	0b0	0b0	0x0			
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M3	7	Alarm1 Mask Bit for Hours	
A1_HR_20_AM_PM	5	In 12-hour format, this works as the AM/PM indicator. In 24-hour format, it is the Alarm1 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hour format. 0x1: Indicates PM in 12-hour format.

BITFIELD	BITS	DESCRIPTION	DECODE
A1_HR_10	4	Alarm1 Hours in Multiples of 10	
A1_HOUR	3:0	Alarm1 Hours	

ALM1_DAY_DATE (0x10)

Alarm1 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M4	7	Alarm1 Mask Bit for Day/Date	
A1_DY_DT_MATCH	6		0x0: Alarm when dates match 0x1: Alarm when days match
A1_DATE_10	5:4	Alarm1 Date in Multiples of 10	
A1_DAY_DATE	3:0	Alarm1 Day/Date	

ALM1_MON (0x11)

Alarm1 Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			
Reset	0b0	0b0	–	0b0	0x0			
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M5	7	Alarm1 Mask Bit for Month
A1M6	6	Alarm1 Mask Bit for Year
A1_MONTH_10	4	Alarm1 Months in Multiples of 10

BITFIELD	BITS	DESCRIPTION
A1_MONTH	3:0	Alarm1 Months

ALM1_YEAR (0x12)

Alarm1 Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
A1_YEAR_10	7:4	Alarm1 Year in Multiples of 10
A1_YEAR	3:0	Alarm1 Years

ALM2_MIN (0x13)

Alarm 2 can be set by writing to registers 13h–15h. See the Register Map. The alarm can be programmed by the A2IE bit in Int_en reg (01h) register to activate the INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits. When all of the mask bits of each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarm can also be programmed to repeat every minute, hour, day, or date. The table below shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY_DT is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT is written to logic 1, the alarm is the result of a match with day of the week.

DY_DT	A2M4	A2M3	A2M2	ALARM RATE
x	1	1	1	Once per minute
x	1	1	0	Minute match
x	1	0	0	Hour and minute match
0	0	0	0	Date, hour, and minute match
1	0	0	0	Day, hour, and minute match

BIT	7	6	5	4	3	2	1	0

Field	A2M2	A2_MIN_10[2:0]	A2_MINUTES[3:0]
Reset	0b0	0b000	0x0
Access Type	Write, Read	Write, Read	Write, Read

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th></tr>
<tr><td>A2M2</td><td>7</td><td>Alarm2 Mask Bit for Minutes
<table>
<tr><th rowspan="2">DY/DT</th><th colspan="3">ALARM2 MASK BITS (BIT 7)</th><th rowspan="2">ALARM RATE</th></tr>
<tr><th>A2M4</th><th>A2M3</th><th>A2M2</th></tr>
<tr><td>X</td><td>1</td><td>1</td><td>1</td><td>Once per minute</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>0</td><td>Minutes match.</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>0</td><td>Hour and minute match</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Date, hour, and minute match</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Day, hour, and minute match</td></tr>
</table></td></tr>
<tr><td>A2_MIN_10</td><td>6:4</td><td>Alarm2 Minutes in Multiples of 10</td></tr>
<tr><td>A2_MINUTES</td><td>3:0</td><td>Alarm2 Minutes</td></tr>
</table>

ALM2_HRS (0x14)

Alarm2 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
Reset	0b0	–	0b0	0b0	0x0			
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M3	7	Alarm2 Mask Bit for Hours	
A2_HR_20_AM_PM	5	In 12-hour format, this works as the AM/PM indicator. In 24-hour format, it is the Alarm2 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hour format. 0x1: Indicates PM in 12-hour format.
A2_HR_10	4	Alarm2 Hours in Multiples of 10	

BITFIELD	BITS	DESCRIPTION	DECODE
A2_HOUR	3:0	Alarm2 Hours	

ALM2_DAY_DATE (0x15)

Alarm2 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M4	7	Alarm2 Mask Bit for Day/Date	
A2_DY_DT_MATCH	6	Selects Alarm when Days Match or Dates Match	0x0: Alarm when dates match 0x1: Alarm when days match
A2_DATE_10	5:4	Alarm2 Date in Multiples of 10	
A2_DAY_DATE	3:0	Alarm2 Day/Date	

TIMER_COUNT (0x16)

Countdown Timer Value Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TIMER_COUNT	7:0	Countdown Timer Current Count Value. The current timer value can be read by reading this register.

TIMER_INIT (0x17)

Countdown Timer Initialization Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIMER_INIT	7:0	Countdown Timer Initial Value. The timer is loaded with the contents of this register when it reaches 0 in repeat mode.

PWR_MGMT (0x18)

Power-Management Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PFVT[1:0]		D_VBACK_SEL	D_MAN_SEL
Reset	–	–	–	–	0b11		0b0	0b0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PFVT	3:2	Power-Fail Threshold Voltage. Sets analog comparator threshold voltage. Requires D_MAN_SEL = 0 for this setting to have effect.	0x0: Threshold voltage disabled 0x1: 1.85V 0x2: 2.15V 0x3: 2.40V
D_VBACK_SEL	1	Backup Battery Select. Requires D_MAN_SEL = 1 for this bit to have effect. V_{BACK} can only be selected as the supply when $V_{CC} < V_{BACK}$.	0x0: Use V_{CC} as supply. 0x1: Use V_{BACK} as supply.
D_MAN_SEL	0	When this bit is low, power-management comparators are enabled and the input control block decides which supply to use. When this bit is high, comparators are disabled and user can manually select whether to use V_{CC} or V_{BACK} as the supply.	0x0: Circuit decides whether to use V_{CC} or V_{BACK} as the supply. 0x1: User decides whether to use V_{CC} or V_{BACKUP} as the supply by setting the D_VBACK_SEL bit.

TRICKLE_REG (0x19)

Trickle Charge Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	D_TRKCHG_EN	–	–	–	D_TRICKLE[3:0]			

Reset	0x0	–	–	–	0x0
Access Type	Write, Read	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
D_TRKCHG_EN	7	Trickle Charger Enable	0x0: Trickle charger disabled 0x1: Trickle charger enabled
D_TRICKLE	3:0	Sets the Charging Path for Trickle Charger	0x0: 3kΩ in series with a Schottky diode 0x1: 3kΩ in series with a Schottky diode 0x2: 6kΩ in series with a Schottky diode 0x3: 11kΩ in series with a Schottky diode 0x4: 3kΩ in series with a diode + Schottky diode 0x5: 3kΩ in series with a diode + Schottky diode 0x6: 6kΩ in series with a diode + Schottky diode 0x7: 11kΩ in series with a diode + Schottky diode 0x8: No connection 0x9: No connection 0xA: No connection 0xB: No connection 0xC: No connection 0xD: No connection 0xE: No connection 0xF: No connection

Ram_reg (0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F, 0x60, 0x61)

BIT	7	6	5	4	3	2	1	0
Field	DATA[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DATA	7:0	

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	CRYSTAL (Internal Use)
MAX31329ELB+	-40°C to +85°C	10 LGA	Crystal A
MAX31329ELB+T	-40°C to +85°C	10 LGA	Crystal A
MAX31329NELB+	-40°C to +85°C	10 LGA	Crystal B
MAX31329NELB+T	-40°C to +85°C	10 LGA	Crystal B

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Crystal A/B identification is for internal use only. There is no difference in part performance with either crystal.