Click here for production status of specific part numbers.

MAX3280E/MAX3281E/ MAX3283E/MAX3284E

±15kV ESD-Protected 52Mbps, 3V to 5.5V, SOT23 RS-485/RS-422 True Fail-Safe Receivers

General Description

The MAX3280E/MAX3281E/MAX3283E/MAX3284E are single receivers designed for RS-485 and RS-422 communication. These devices guarantee data rates up to 52Mbps, even with a 3V power supply. Excellent propagation delay (15ns max) and package-to-package skew time (8ns max) make these devices ideal for multidrop clock distribution applications.

The MAX3280E/MAX3281E/MAX3283E/MAX3284E have true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are opened or shorted. The receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). These devices feature 1/4-unit-load receiver input impedance, allowing up to 128 receivers on the same bus.

The MAX3280E is a single receiver available in a 5-pin SOT23 package. The MAX3281E/MAX3283E single receivers have a receiver enable (EN or $\overline{EN}$) function and are offered in a 6-pin SOT23 package. The MAX3284E features a voltage logic pin that allows compatibility with low-voltage logic levels, as in digital FPGAs/ASICs. On the MAX3284E, the voltage threshold for a logic high is user-defined by setting V_L in the range from 1.65V to V_{CC}. The MAX3284E is also offered in a 6-pin SOT23 package.

Applications

- Clock Distribution
- Telecom Racks
- Base Stations
- Industrial Control
- Local Area Networks
- Automotive

Pin Configurations appear at end of data sheet.

Benefits and Features

- ESD Protection:
  ±15kV Human Body Model
  ±6kV IEC 1000-4-2, Contact Discharge
  ±12kV IEC 1000-4-2, Air-Gap Discharge
- Guaranteed 52Mbps Data Rate
- Guaranteed 15ns Receiver Propagation Delay
- Guaranteed 2ns Receiver Skew
- Guaranteed 8ns Package-to-Package Skew Time
- V_L Pin for Connection to FPGAs/ASICs
- Allow Up to 128 Transceivers on the Bus (1/4-unit-load)
- Tiny SOT23 Package
- True Fail-Safe Receiver
- -7V to +12V Common-Mode Range
- 3V to 5.5V Power-Supply Range
- Enable (High and Low) Pins for Redundant Operation
- Three-State Output Stage (MAX3281E/MAX3283E)
- Thermal Protection Against Output Short Circuit
- AEC-Q100 (MAX3280EAUK/V+ Only)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX3280EAUK+T	-40°C to +125°C	5 SOT23	+ADVM
MAX3280EAUK/V+T	-40°C to +125°C	5 SOT23	+AFME
MAX3281EAUT+T	-40°C to +125°C	6 SOT23	+ABAT
MAX3283EAUT+T	-40°C to +125°C	6 SOT23	+ABAU
MAX3284EAUT+T	-40°C to +125°C	6 SOT23	+ABAV

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
/V denotes an automotive qualified part.

Selector Guide

PART	VL	ENABLE	DATA RATE	PACKAGE
MAX3280E	—	—	52Mbps	5-Pin SOT23
MAX3281E	—	Active High	52Mbps	6-Pin SOT23
MAX3283E	—	Active Low	52Mbps	6-Pin SOT23
MAX3284E	✔	—	52Mbps (Note 1)	6-Pin SOT23

Note 1: MAX3284E data rate is dependent on V_L.

19-2320; Rev 7; 1/19

maxim integrated™

Absolute Maximum Ratings

(All Voltages Referenced to GND)
Supply Voltage (V_{CC}) ..... -0.3V to +6V
Control Input Voltage (EN, $\overline{EN}$) ..... -0.3V to +6V
V_L Input Voltage ..... -0.3V to +6V
Receiver Input Voltage (A, B) ..... -7.5V to +12.5V
Receiver Output Voltage (RO) ..... -0.3V to (V_{CC} + 0.3V)
Receiver Output Voltage
(RO) (MAX3284E) ..... -0.3V to (V_L + 0.3V)
Receiver Output Short-Circuit Current ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 3.9mW/°C above +70°C) 312.60mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 696mW
Operating Temperature Range
MAX328_EA__ ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOT23-5

PACKAGE CODE	U5+2, U5+2A
Outline Number	21-0057
Land Pattern Number	90-0174
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	324.30°C/W
Junction to Case (θ_{JC})	82°C/W
Thermal Resistance, Multi-Layer Board:	
Junction to Ambient (θ_{JA})	255.90°C/W
Junction to Case (θ_{JC})	81°C/W

SOT23-6	
PACKAGE CODE	**U6+1**
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	80°C/W
Thermal Resistance, Multi-Layer Board:	
Junction to Ambient (θ_{JA})	115°C/W
Junction to Case (θ_{JC})	80°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 3V to 5.5V, V_L = V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		3.0		5.5	V
Supply Current	ICC	No load		9	15	mA
VL Input Range	VL	MAX3284E	1.65		VCC	V
VL Supply Current	IL	No load (MAX3284E)			10	µA
RECEIVER						
Input Current (A and B)	IA, B	VCC = VGND or 5.5V, VIN = +12V			250	µA
		VCC = VGND or 5.5V, VIN = -7V			-200	
Receiver Differential Threshold Voltage	VTH	-7V ≤ VCM ≤ +12V (Note 4)	-200	-125	-50	mV
Receiver Input Hysteresis	ΔVTH	VA + VB = 0V		25		mV
Receiver Enable Input Low	VENIL	MAX3281E, MAX3283E only			0.4	V
Receiver Enable Input High	VENIH	MAX3281E, MAX3283E only	2			V
Receiver Enable Input Leakage	ILEAK	MAX3281E, MAX3283E only			±10	µA
Receiver Output High Voltage	VOH	MAX3280E/MAX3281E/MAX3283E, IOH = -4mA, RO high	VCC - 0.4			V
		MAX3284E, IOH = -1mA, 1.65V ≤ VL ≤ VCC, RO high	VL - 0.4			
Receiver Output Low Voltage	VOL	MAX3280E/MAX3281E/MAX3283E, IOL = 4mA, RO low			0.4	V
		MAX3284E, IOL = 1mA, 1.65V ≤ VL ≤ VCC, RO low			0.4	
Three-State Output Current at Receiver	IOZR	0 ≤ VO ≤ VCC, RO = high impedance			±5	µA
Receiver Input Resistance	RIN	-7V ≤ VCM ≤ +12V (Note 5)	48			kΩ
Receiver Output Short-Circuit Current	IOSR	0 ≤ VRO ≤ VCC			±130	mA
ESD PROTECTION						
ESD Protection (A, B)		Human Body Model		±15		kV
		IEC1000-4-2 (Air-Gap Discharge)		±12		
		IEC1000-4-2 (Contact Discharge)		±6		

Switching Characteristics

(V_{CC} = 3V to 5.5V, V_L = V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V and T_A = +25°C.) (Notes 2, 3)

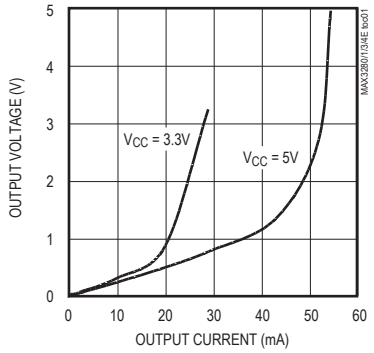
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Data Rate	fMAX	CL = 15pF (Notes 5, 6)	52			Mbps
Receiver Propagation Delay	tPLH	Figure 1, CL = 15pF, VID = 2V, VCM = 0V		7	15	ns
	tPHL	Figure 1, CL = 15pF, VID = 2V, VCM = 0V		8	15	
Receiver Output |tPLH - tPHL|	tPSKEW	Figure 1, CL = 15pF, TA = +25°C			2	ns
Device-to-Device Propagation Delay Matching		Same power supply, maximum temperature difference between devices = +30°C (Note 5)			8	ns
ENABLE/DISABLE TIME FOR MAX3281E/MAX3283E						
Receiver Enable to Output Low	tPRZL	Figure 2, CL = 15pF			500	ns
Receiver Enable to Output High	tPRZH	Figure 2, CL = 15pF			500	ns
Receiver Disable Time from Low	tPRLZ	Figure 2, CL = 15pF			500	ns
Receiver Disable Time from High	tPRHZ	Figure 2, CL = 15pF			500	ns

Note 2: Parameters are 100% production tested at +25°C, limits over temperature are guaranteed by design.
Note 3: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.
Note 4: V_{CM} is the common-mode input voltage. V_{ID} is the differential input voltage.
Note 5: Not production tested. Guaranteed by design.
Note 6: See Table 2 for MAX3284E data rates with V_L < V_{CC}.

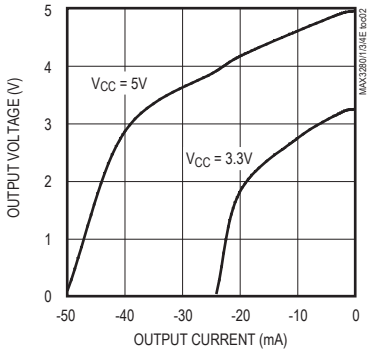
Typical Operating Characteristics

(VCC = 3.3V, TA = +25°C, unless otherwise noted.)

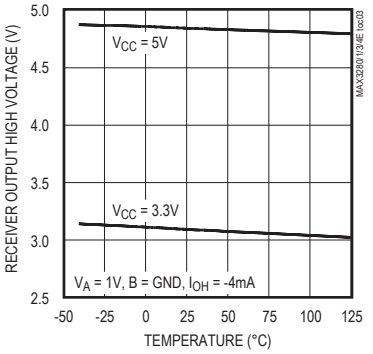
RECEIVER OUTPUT LOW VOLTAGE vs. OUTPUT CURRENT



RECEIVER OUTPUT HIGH VOLTAGE vs. OUTPUT CURRENT



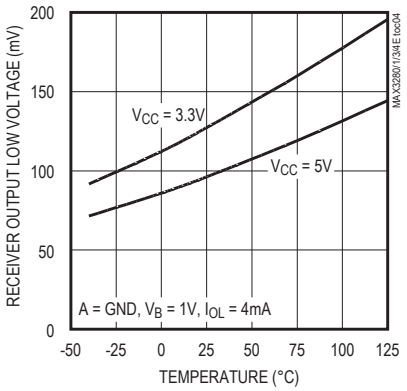
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



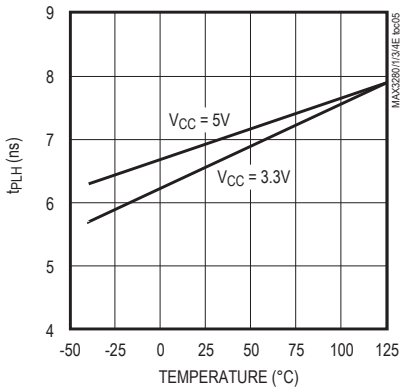
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

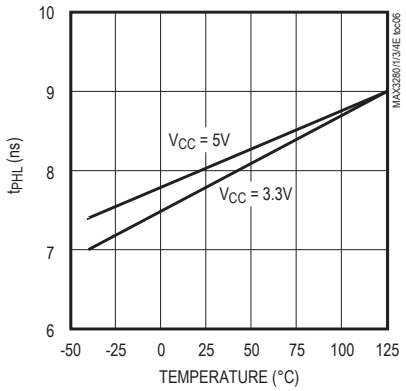
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



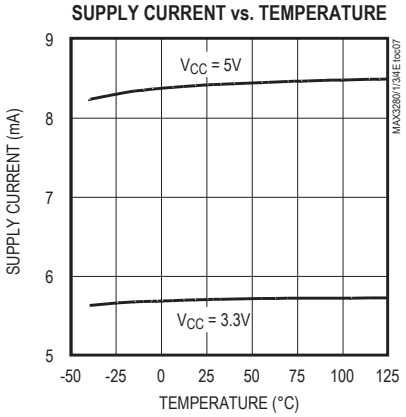
RECEIVER PROPAGATION DELAY (t_{PLH}) vs. TEMPERATURE



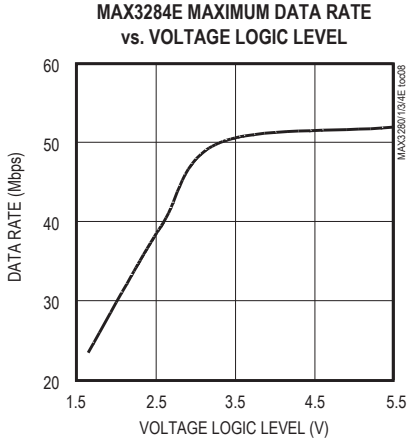
RECEIVER PROPAGATION DELAY (t_{PHL}) vs. TEMPERATURE



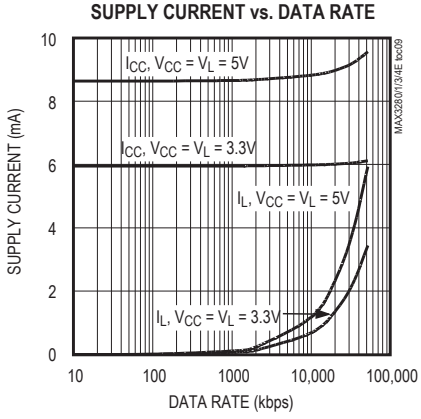
SUPPLY CURRENT vs. TEMPERATURE



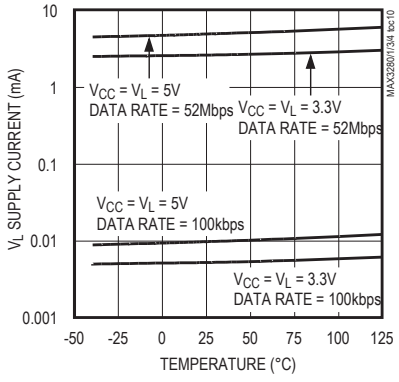
MAX3284E MAXIMUM DATA RATE vs. VOLTAGE LOGIC LEVEL



SUPPLY CURRENT vs. DATA RATE



V_L SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN				NAME	FUNCTION
MAX3280E	MAX3281E	MAX3283E	MAX3284E		
1	1	1	1	VCC	Positive Supply: 3V ≤ VCC ≤ 5.5V. Bypass with a 0.1µF capacitor to GND.
2	2	2	2	GND	Ground
3	3	3	3	RO	Receiver Output. RO will be high if (VA - VB) ≥ -50mV. RO will be low if (VA - VB) ≤ -200mV.
4	4	4	4	B	Inverting Receiver Input
—	—	5	—	$\overline{EN}$	Receiver Output Enable. Drive $\overline{EN}$ low to enable RO. When $\overline{EN}$ is high, RO is high impedance.
—	5	—	—	EN	Receiver Output Enable. Drive EN high to enable RO. When EN is low, RO is high impedance.
—	—	—	5	VL	Low-Voltage Logic-Level Supply Voltage. VL is a user-defined voltage, ranging from 1.65V to VCC. RO output high is pulled up to VL. Bypass with a 0.1µF capacitor to GND.
5	6	6	6	A	Noninverting Receiver Input

Detailed Description

The MAX3280E/MAX3281E/MAX3283E/MAX3284E are single, true fail-safe receivers designed to operate at data rates up to 52Mbps. The fail-safe architecture guarantees a high output signal if both input terminals are open or shorted together. See the *True Fail-Safe* section. This feature assures a stable and predictable output logic state with any transmitter driving the line. These receivers function with a 3.3V or 5V supply voltage and feature excellent propagation delay times (15ns).

The MAX3280E is a single receiver available in a 5-pin SOT23 package. The MAX3281E (EN, active high) and MAX3283E ($\overline{EN}$, active low) are single receivers that also contain an enable pin. Both the MAX3281E and MAX3283E are available in a 6-pin SOT23 package. The MAX3284E is a single receiver that contains a V_L pin, which allows communication with low-level logic included in digital FPGAs. The MAX3284E is available in a 6-pin SOT23 package.

The MAX3284E's low-level logic application allows users to set the logic levels. A logic high level of 1.65V will limit the maximum data rate to 20Mbps.

±15kV ESD Protection

ESD-protection structures are incorporated on the receiver input pins to protect against ESD encountered during handling and assembly. The MAX3280E/MAX3281E/MAX3283E/MAX3284E receiver inputs (A, B) have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ±15kV ESD without damage. After an ESD event, this family of parts continues working without latchup.

ESD protection can be tested in several ways. The receiver inputs are characterized for protection to the following:

- ±15kV using the Human Body Model
- ±6kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
- ±12kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 3a shows the Human Body Model, and Figure 3b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3280E/MAX3281E/MAX3283E/MAX3284E help

users design equipment that meets Level 3 of IEC 1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 4a), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 4b shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. All pins (not just the RS-485 inputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC 1000-4-2.

True Fail-Safe

The MAX3280E/MAX3281E/MAX3283E/MAX3284E guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This guaranteed logic high is achieved by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (V_A - V_B) is greater than or equal to -50mV, RO is logic high. If (V_A - V_B) is less than or equal to -200mV, RO is logic low.

In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to ground by the termination. This results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Receiver Enable (MAX3281E and MAX3283E only)

The MAX3281E and MAX3283E feature a receiver output enable (EN, MAX3281E or $\overline{EN}$, MAX3283E) input that controls the receiver. The MAX3281E receiver enable (EN) pin is active high, meaning the receiver outputs are active when EN is high. The MAX3283E receiver enable ($\overline{EN}$) pin is active low. Receiver outputs are high impedance when the MAX3281E's EN pin is low and when the MAX3283E's $\overline{EN}$ pin is high.

Table 1. MAX3281E/MAX3283E Enable Table

PART	ENABLE = HIGH	ENABLE = LOW
MAX3281E	Active	High Z
MAX3283E	High Z	Active

Low-Voltage Logic Levels (MAX3284E only)

An increasing number of applications now operate at low-voltage logic levels. To enable compatibility with these low-voltage logic level applications, such as digital FPGAs, the MAX3284E V_L pin is a user-defined supply voltage that designates the voltage threshold for a logic high.

At lower V_L voltages, the data rate will also be lower. A logic-high level of 1.65V will receive data at 20Mbps. Table 2 gives data rates at various voltages at V_L.

Table 2. MAX3284E Data Rate Table

VCC = 3V TO 5.5V	
VL	MAXIMUM DATA RATE
1.65V	20Mbps
2.2V	33Mbps
≥3.3V	52Mbps

Applications Information

Propagation Delay Matching

The MAX3280E/MAX3281E/MAX3283E/MAX3284E (V_{CC} = V_L) exhibit propagation delays that are closely matched from one device to another, even between devices from different production lots. This feature allows multiple data lines to receive data and clock signals with minimal skew with respect to each other. Figure 5 shows the typical propagation delays. Small receiver skew times, the difference between the low-to-high and high-to-low propagation delay, help maintain a symmetrical ratio (50% duty cycle). The receiver skew time | t_{PLH} - t_{PHL} | is under 2ns for either a 3.3V supply or a 5V supply.

Multidrop Clock Distribution

Low package-to-package skew (8ns max) makes the MAX3280E/MAX3281E/MAX3283E/MAX3284E (V_{CC} = V_L) ideal for multidrop clock distribution. When distributing a clock signal to multiple circuits over long transmission lines, receivers in separate locations, and possibly at two different temperatures, would ideally

provide the same clock to their respective circuits. Thus, minimal package-to-package skew is critical. The skew must be kept well below the period of the clock signal to ensure that all of the circuits on the network are synchronized.

128 Receivers on the Bus

The standard RS-485 input impedance is 12kΩ (one-unit load). The standard RS-485 transmitter can drive 32 unit loads. The MAX3280E/MAX3281E/MAX3283E/MAX3284E present a 1/4-unit-load input impedance (48kΩ), which allows up to 128 receivers on the bus. Any combination of these RS-485 receivers with a total of 32 unit loads can be connected to the same bus.

Thermal Protection

The MAX3280E/MAX3281E/MAX3283E/MAX3284E feature thermal protection. Thermal protection sets the output stage in high-impedance mode when a short circuit occurs at the output, limiting both the power dissipation and temperature. The thermal temperature threshold is +165°C, with a hysteresis of 20°C.

Test Circuits/Timing Diagrams

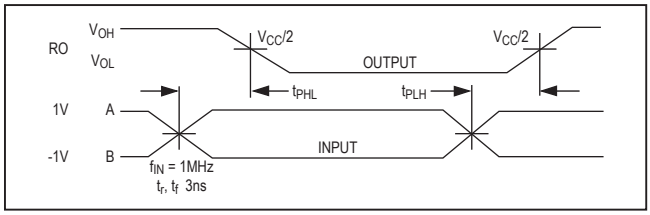


Figure 1. Receiver Propagation Delay

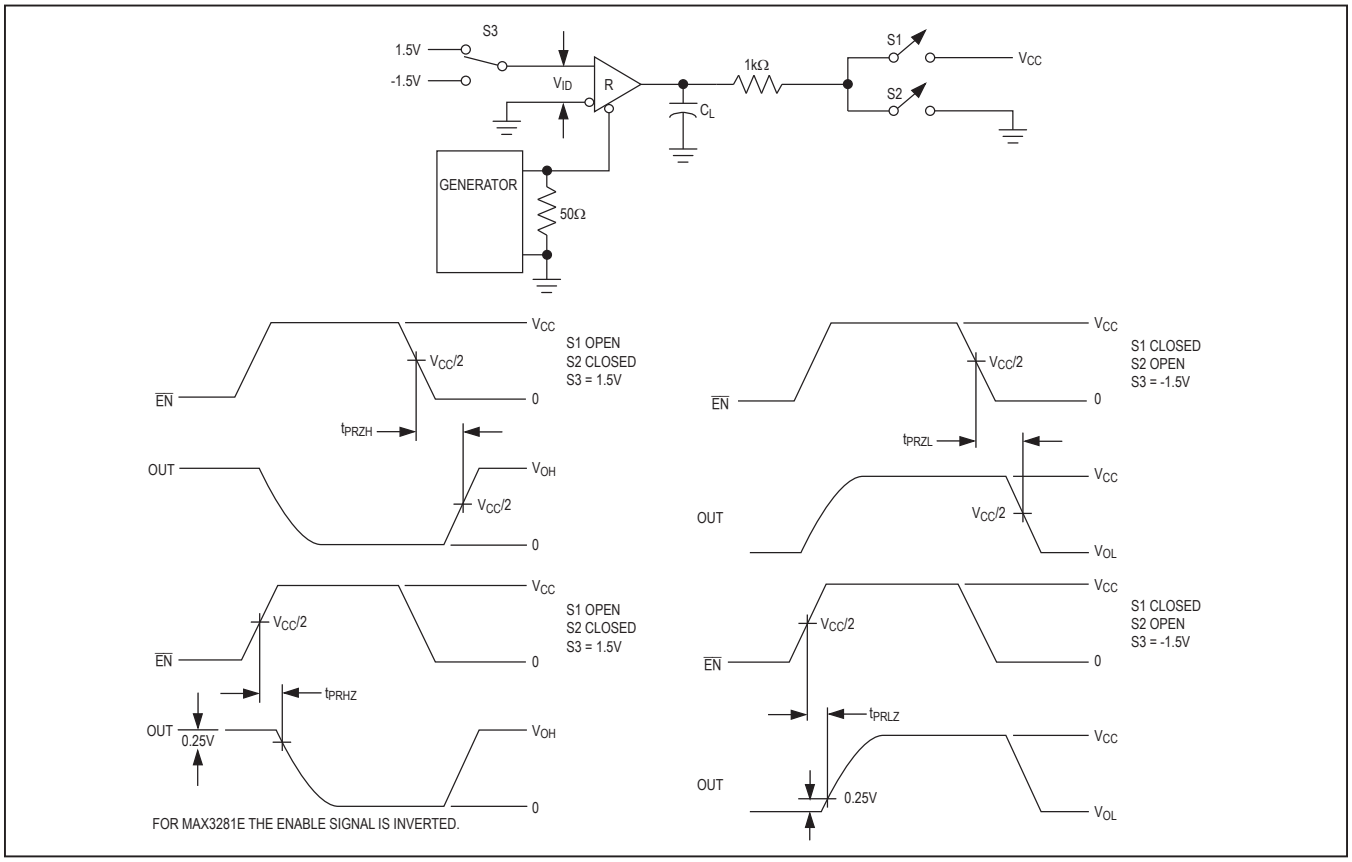


Figure 2. MAX3281E/MAX3283E Receiver Enable/Disable Timing

Test Circuits/Timing Diagrams (continued)

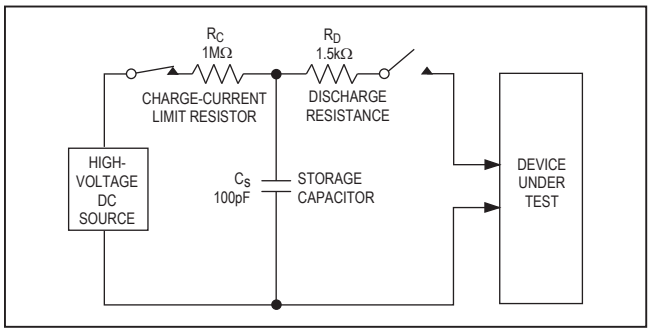


Figure 3a. Human Body ESD Test Model

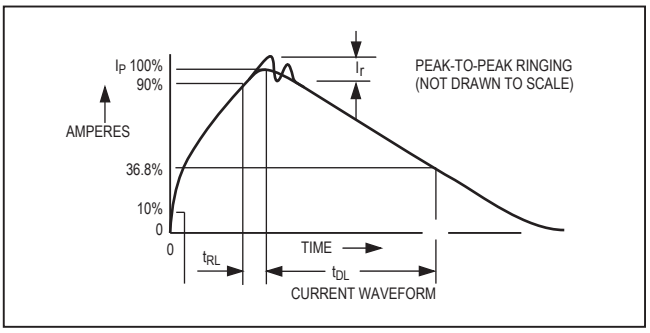


Figure 3b. Human Body Model Current Waveform

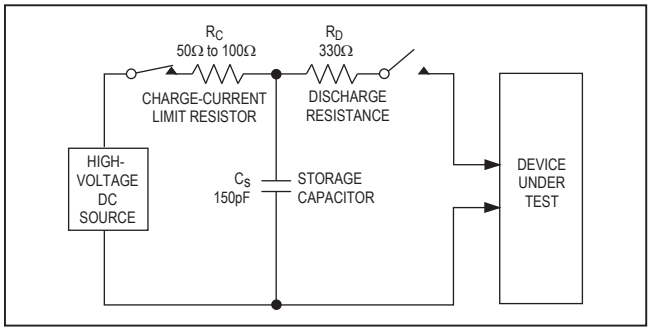


Figure 4a. IEC 1000-4-2 ESD Test Model

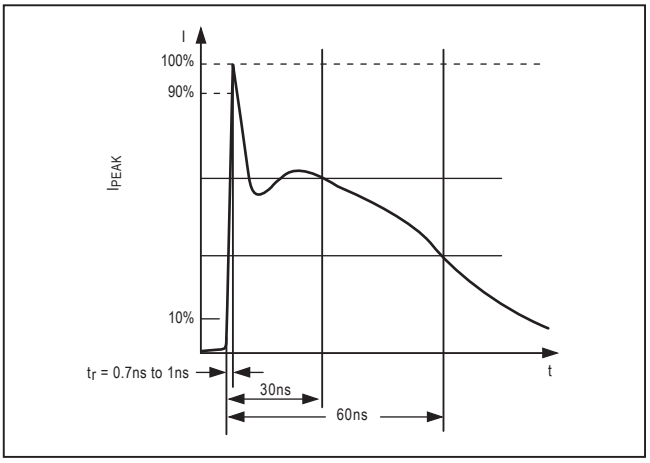


Figure 4b. IEC 1000-4-2 ESD Generator Current Waveform

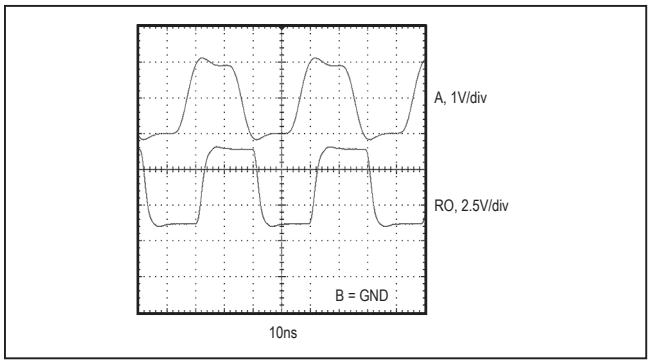
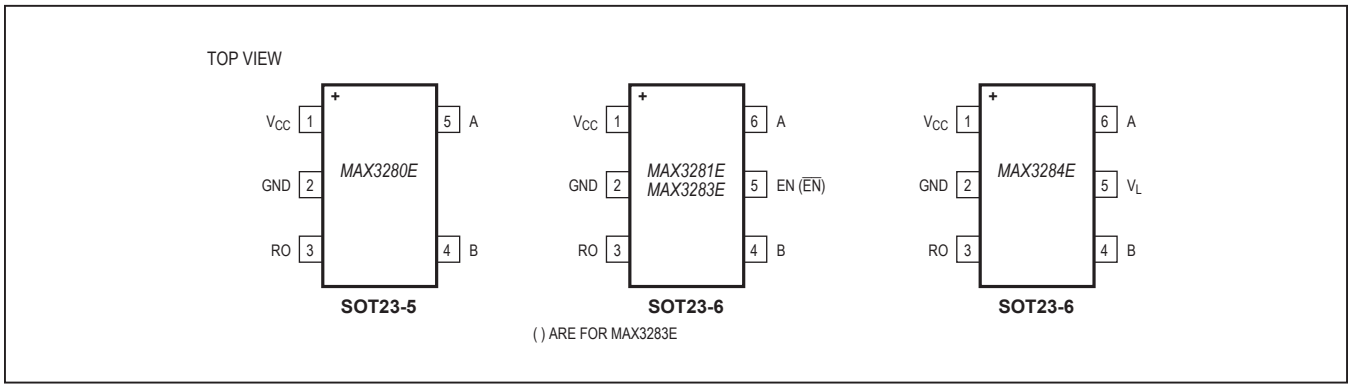
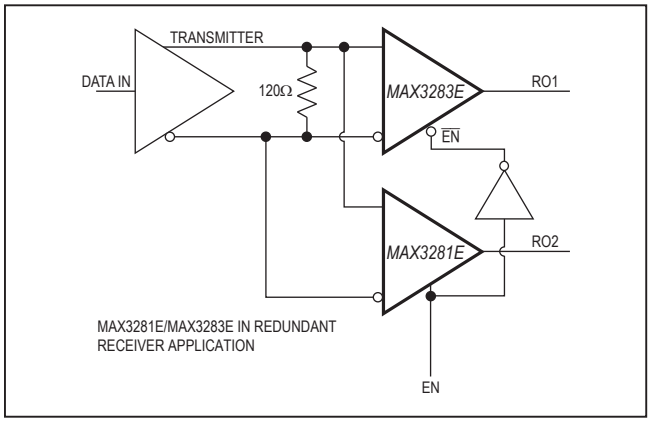


Figure 5. Receiver Propagation Delay Driven by External RS-485 Device

Pin Configurations



Typical Operating Circuit



Chip Information

PROCESS: BiCMOS