MAX4090

3V/5V, 6dB Video Buffer with Sync-Tip Clamp and 150nA Shutdown Current

General Description

The MAX4090 3V/5V, 6dB video buffer with sync-tip clamp, and low-power shutdown mode is available in tiny SOT23, SC70, and µDFN packages. The MAX4090 is designed to drive DC-coupled, 150Ω back-terminated video loads in portable video applications such as digital still cams, portable DVD players, digital camcorders, PDAs, video-enabled cell phones, portable game systems, and notebook computers. The input clamp positions the video waveform at the output and allows the MAX4090 to be used as a DC-coupled output driver.

The MAX4090 operates from a single 2.7V to 5.5V supply and consumes only 6.5mA of supply current. The low-power shutdown mode reduces the supply current to 150nA, making the MAX4090 ideal for low-voltage, battery-powered video applications.

The MAX4090 is available in tiny 6-pin SOT23, SC70, and µDFN packages and is specified over the extended (-40°C to +85°C) and automotive (-40°C to +125°C) temperature ranges.

Applications

- Portable Video/Game Systems/DVD Players
- Digital Camcorders/Televisions/Still Cameras
- PDAs
- Video-Enabled Cell Phones
- Notebook Computers
- Portable/Flat-Panel Displays

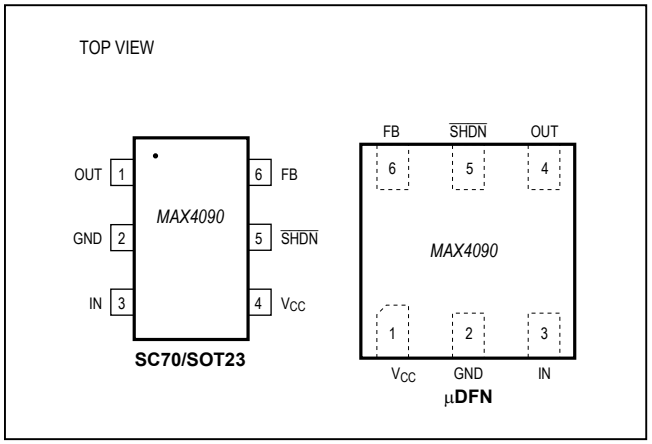
Features

- Single-Supply Operation from 2.7V to 5.5V
- Input Sync-Tip Clamp
- DC-Coupled Output
- Low-Power Shutdown Mode Reduces Supply Current to 150nA
- Available in Space-Saving SOT23, SC70, and µDFN Packages

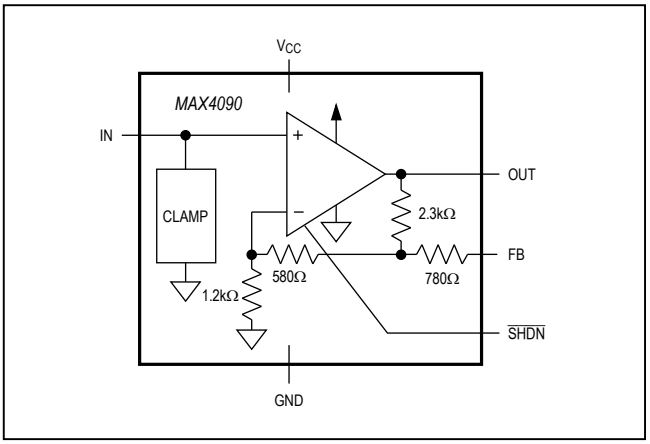
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4090EXT-T	-40°C to +85°C	6 SC70	ABM
MAX4090EUT-T	-40°C to +85°C	6 SOT23	ABOX
MAX4090ELT-T	-40°C to +85°C	6 µDFN	AAI
MAX4090AAXT-T	-40°C to +125°C	6 SC70	ACW
MAX4090AAUT-T	-40°C to +125°C	6 SOT23	ABWQ
MAX4090AALT-T	-40°C to +125°C	6 µDFN	AAN

Pin Configurations



Block Diagram



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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V
OUT, FB, $\overline{SHDN}$ to GND ..... -0.3V to (V_{CC} + 0.3V)
IN to GND (Note 1) ..... VCLP to (V_{CC} + 0.3V)
IN Short-Circuit Duration from -0.3V to V_{CLP} 1min
Output Short-Circuit Duration to V_{CC} or GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 695mW
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
6-Pin µDFN (derate 3.6mW/°C above +70°C) 290mW
Operating Temperature Range
MAX4090E..... -40°C to +85°C
MAX4090A..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: V_{CLP} is the input clamp voltage as defined in the DC Electrical Characteristics table.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC} = 3.0V, V_{GND} = 0V, C_{IN} = 0.1µF from IN to GND, R_L = infinity to GND, FB shorted to OUT, $V_{\overline{SHDN}}$ = 3.0V, T_A = -40°C to +85°C (MAX4090E), T_A = -40°C to +125°C (MAX4090A). Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Guaranteed by PSRR		2.7		5.5	V
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CLP}	V_{CC} = 3V		6.5	10	mA
			V_{CC} = 5V		6.5	10	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V			0.15	1	µA
Input Clamp Voltage	V_{CLP}	Input referred		0.27	0.38	0.47	V
Input Voltage Range	V_{IN}	Inferred from voltage gain (Note 3)		V_{CLP}		1.45	V
Input Bias Current	I_{BIAS}	V_{IN} = 1.45V			22.5	35	µA
Input Resistance		V_{CLP} + 0.5V < V_{IN} < V_{CLP} + 1V			3		MΩ
Voltage Gain	A_V	R_L = 150Ω, 0.5V < V_{IN} < 1.45V (Note 4)		1.9	2	2.1	V/V
Power-Supply Rejection Ratio	PSRR	2.7V < V_{CC} < 5.5V		60	80		dB
Output-Voltage High Swing	V_{OH}	R_L = 150Ω to GND	V_{CC} = 3V	2.55	2.7		V
			V_{CC} = 5V	4.3	4.6		
Output-Voltage Low Swing	V_{OL}	R_L = 150Ω to GND			V_{CLP}	0.47	V
Output Current	I_{OUT}	Sourcing, R_L = 20Ω to GND		45	85		mA
		Sinking, R_L = 20Ω to V_{CC}		40	85		
Output Short-Circuit Current	I_{SC}	OUT shorted to V_{CC} or GND			110		mA
$\overline{SHDN}$ Logic-Low Threshold	V_{IL}					V_{CC} x 0.3	V
$\overline{SHDN}$ Logic-High Threshold	V_{IH}			V_{CC} x 0.7			V
$\overline{SHDN}$ Input Current	I_{IH}				0.003	1	µA
Shutdown Output Impedance	R_{OUT} (Disabled)	$V_{\overline{SHDN}}$ = 0V	At DC		4		kΩ
			At 3.58MHz or 4.43MHz		2		

AC Electrical Characteristics

(V_{CC} = 3.0V, V_{GND} = 0V, FB shorted to OUT, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $V_{\overline{SHDN}}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 100mV_{P-P}			55		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2V_{P-P}			45		MHz
Small-Signal 0.1dB Gain Flatness	$BW_{0.1dBSS}$	V_{OUT} = 100mV_{P-P}			25		MHz
Large-Signal 0.1dB Gain Flatness	$BW_{0.1dBLS}$	V_{OUT} = 2V_{P-P}			17		MHz
Slew Rate	SR	V_{OUT} = 2V step			275		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			25		ns
Power-Supply Rejection Ratio	PSRR	f = 100kHz			50		dB
Output Impedance	Z_{OUT}	f = 5MHz			2.5		Ω
Differential Gain	DG	NTSC	V_{CC} = 3V		1		%
			V_{CC} = 5V		0.5		
Differential Phase	DP	NTSC	V_{CC} = 3V		0.8		Degrees
			V_{CC} = 5V		0.5		
Group Delay	D/dT	f = 3.58MHz or 4.43MHz			20		ns
Peak Signal to RMS Noise	SNR	V_{IN} = 1V_{P-P}, 10MHz BW			65		dB
Droop		C_{IN} = 0.1µF (Note 4)			2	3	%
$\overline{SHDN}$ Enable Time	t_{ON}	V_{IN} = V_{CLP} + 1V, $V_{\overline{SHDN}}$ = 3V, V_{OUT} settled to within 1% of the final voltage			250		ns
$\overline{SHDN}$ Disable Time	t_{OFF}	V_{IN} = V_{CLP} + 1V, $V_{\overline{SHDN}}$ = 0V, V_{OUT} settled to below 1% of the output voltage			50		ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

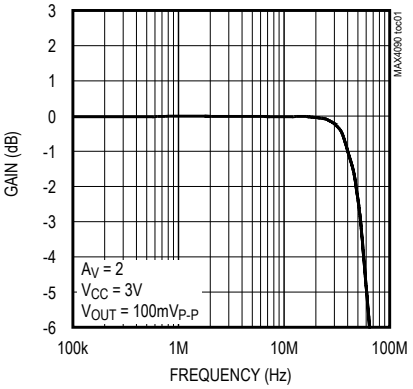
Note 3: Voltage gain (A_V) is referenced to the clamp voltage, i.e., an input voltage of V_{IN} = V_{CLP} + VI would produce an output voltage of V_{OUT} = V_{CLP} + A_V x VI.

Note 4: Droop is guaranteed by the Input Bias Current specification.

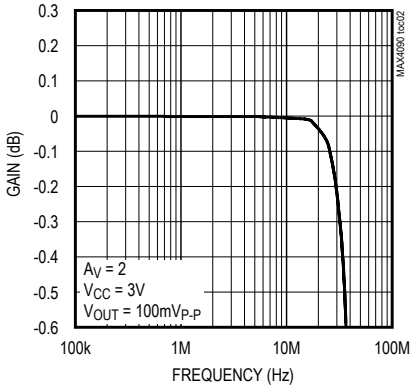
Typical Operating Characteristics

(V_{CC} = 3.0V, GND = 0V, FB shorted to OUT, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

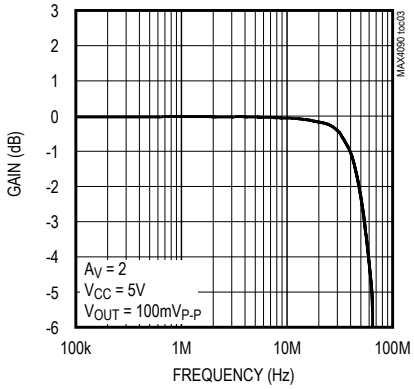
SMALL-SIGNAL GAIN vs. FREQUENCY



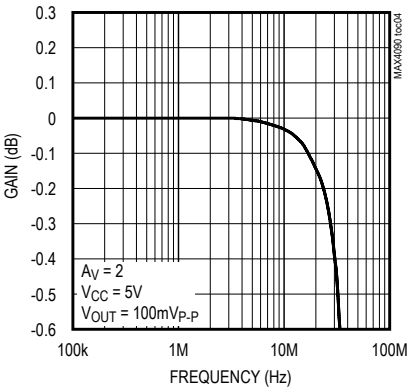
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



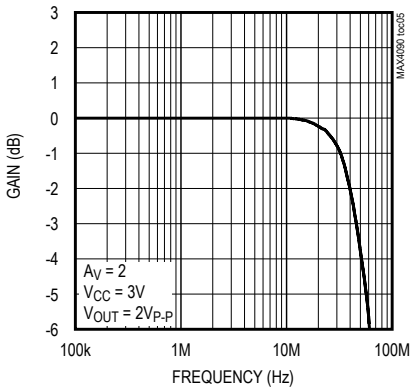
SMALL-SIGNAL GAIN vs. FREQUENCY



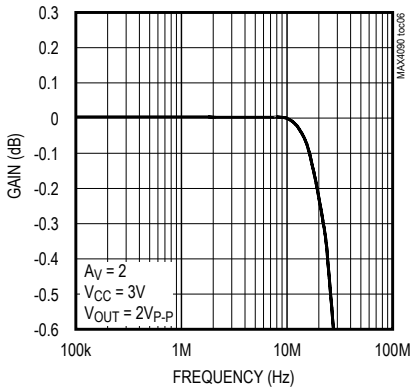
SMALL-SIGNAL GAIN FLATNESS vs. FREQUENCY



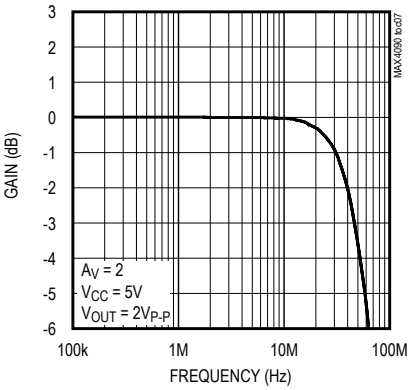
LARGE-SIGNAL GAIN vs. FREQUENCY



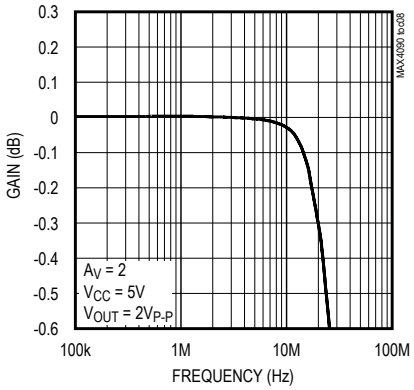
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



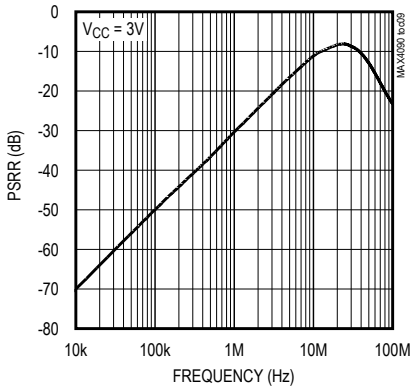
LARGE-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



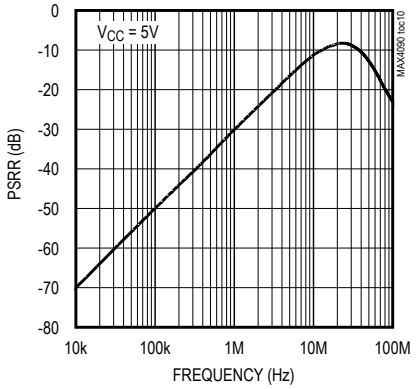
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



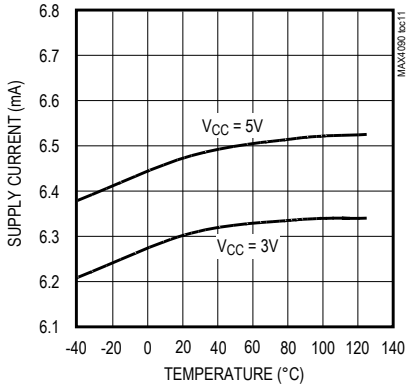
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, GND = 0V, FB shorted to OUT, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

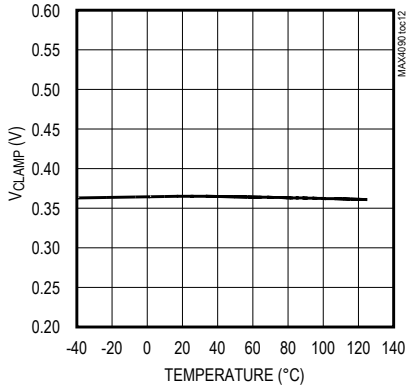
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



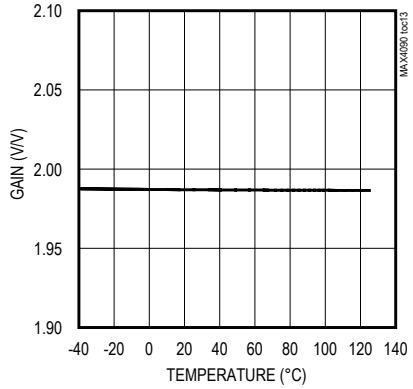
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



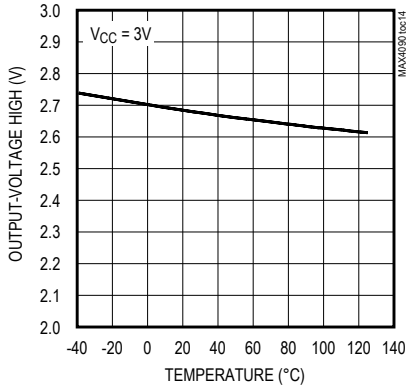
CLAMP VOLTAGE vs. TEMPERATURE



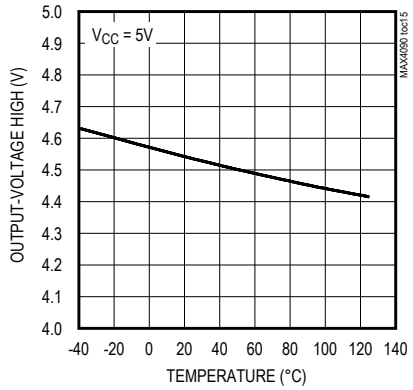
VOLTAGE GAIN vs. TEMPERATURE



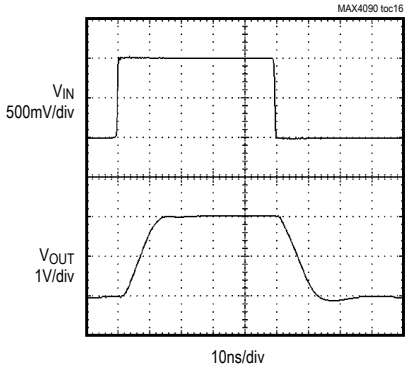
OUTPUT-VOLTAGE HIGH SWING vs. TEMPERATURE



OUTPUT-VOLTAGE HIGH SWING vs. TEMPERATURE

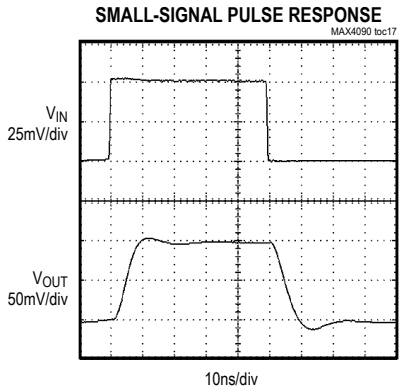


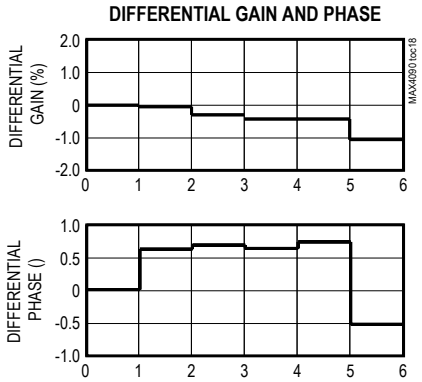
LARGE-SIGNAL PULSE RESPONSE



Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, GND = 0V, FB shorted to OUT, C_{IN} = 0.1µF, R_{IN} = 75Ω to GND, R_L = 150Ω to GND, $\overline{SHDN}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

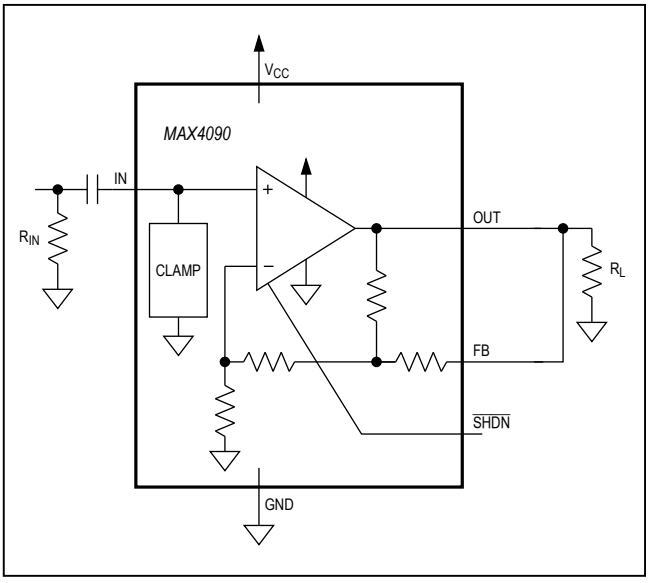




Pin Description

PIN		NAME	FUNCTION
SOT23/ SC70	µDFN		
1	4	OUT	Video Output
2	2	GND	Ground
3	3	IN	Video Input
4	1	V_{CC}	Power-Supply Voltage. Bypass with a 0.1µF capacitor to ground as close to pin as possible.
5	5	$\overline{SHDN}$	Shutdown. Pull $\overline{SHDN}$ low to place the MAX4090 in low-power shutdown mode.
6	6	FB	Feedback. Connect to OUT.

Typical Application Circuit



Detailed Description

The MAX4090 3V/5V, 6dB video buffer with sync-tip clamp and low-power shutdown mode is available in tiny SOT23 and SC70 packages. The MAX4090 is designed to drive DC-coupled, 150Ω back-terminated video loads in portable video applications such as digital still cams, portable DVD players, digital camcorders, PDAs, video-enabled cell phones, portable game systems, and notebook computers. The input clamp positions the video waveform at the output and allows the MAX4090 to be used as a DC-coupled output driver.

The MAX4090 operates from a single 2.7V to 5.5V supply and consumes only 6.5mA of supply current. The low-power shutdown mode reduces the supply current to 150nA, making the MAX4090 ideal for low-voltage, battery-powered video applications.

The input signal to the MAX4090 is AC-coupled through a capacitor into an active sync-tip clamp circuit, which places the minimum of the video signal at approximately 0.38V. The output buffer amplifies the video signal while still maintaining the 0.38V clamp voltage at the output. For example, if V_{IN} = 0.38V, then V_{OUT} = 0.38V. If V_{IN} = 1.38V, then V_{OUT} = 0.38V + (2 x 1V) = 2.38V. The net result is that a 2V video output signal swings within the usable output voltage range of the output buffer when V_{CC} = 3V.

Shutdown Mode

The MAX4090 features a low-power shutdown mode ($I_{\overline{SHDN}}$ = 150nA) for battery-powered/portable applications. Pulling the $\overline{SHDN}$ pin high enables the output. Connecting the $\overline{SHDN}$ pin to ground (GND) disables the output and places the MAX4090 into a low-power shutdown mode.

Applications Information

Input Coupling the MAX4090

The MAX4090 input must be AC-coupled because the input capacitor stores the clamp voltage. The MAX4090 requires a typical value of 0.1µF for the input clamp to meet the Line Droop specification. A minimum of a ceramic capacitor with an X7R temperature coefficient is recommended to avoid temperature-related problems with Line Droop. For extended temperature operation, such as outdoor applications, or where the impressed voltage is close to the rated voltage of the capacitor, a film dielectric is recommended. Increasing the capacitor value slows the clamp capture time. Values above 0.5µF should be avoided since they do not improve the clamp's performance.

The active sync-tip clamp also requires that the input impedance seen by the input capacitor be less than 100Ω typically to function properly. This is easily met by the 75Ω input resistor prior to the input-coupling capacitor and the back termination from a prior stage. Insufficient input resistance to ground causes the MAX4090 to appear to oscillate. Never operate the MAX4090 in this mode.

Using the MAX4090 with the Reconstruction Filter

In most video applications, the video signal generated from the DAC requires a reconstruction filter to smooth out the signal and attenuate the sampling aliases. The MAX4090 is a direct DC-coupled output driver, which can be used after the reconstruction filter to drive the video signal. The driving load from the video DAC can be varied from 75Ω to 300Ω. A low input impedance (<100Ω) is required by the MAX4090 in normal operation, special care must be taken when a reconstruction filter is used in front of the MAX4090.

For standard video signal, the video passband is about 6MHz and the system oversampling frequency is at 27MHz. Normally, a 9MHz BW lowpass filter can be used for the reconstruction filter. This section demonstrates the methods to build simple 2nd- and 3rd-order passive butterworth lowpass filters at the 9MHz cutoff frequency and the techniques to use them with the MAX4090 (Figures 1 and 4).

2nd-Order Butterworth Lowpass Filter Realization

Table 1 shows the normalized 2nd-order butterworth LPF component values at 1rad/s with a source/load impedance of 1Ω.

With the following equations, the L and C can be calculated for the cutoff frequency at 9MHz. Table 2 shows the appropriated L and C values for different source/load impedance, the bench measurement values for the -3dB BW and attenuation at 27MHz. There is approximately 20dB attenuation at 27MHz, which effectively attenuates the sampling aliases. The MAX4090 requires low input impedance for stable operation and it does not like the reactive input impedance. For R1/R2 greater than 100Ω, a series resistor R_{IS} (Figure 1)

Table 1. 2nd-Order Butterworth Lowpass Filter Normalized Values

Rn1 = Rn2 (Ω)	Cn1 (F)	Ln1 (H)
1	1.414	1.414

between 20Ω to 100Ω is needed to isolate the input capacitor (C4) to the filter to prevent the oscillation problem.

$$C=\frac{C_n}{2\pi f_C R_L} \quad L=\frac{L_n R_L}{2\pi f_C}$$

Figure 2 shows the frequency response for R1 = R2 = 150Ω. At 6MHz, the attenuation is about 1.4dB. The attenuation at 27MHz is about 20dB. Figure 3 shows the multiburst response for R1 = R2 = 150Ω.

3rd-Order Butterworth Lowpass Filter Realization

If more flat passband and more stopband attenuation are needed, a 3rd-order LPF can be used. The design procedures are similar to the 2nd-order butterworth LPF.

Table 3 shows the normalized 3rd-order butterworth lowpass filter with the cutoff frequency at 1 rad/s and the stopband frequency at 3 rad/s. Table 4 shows the appropriated L and C values for different source/load impedance and the bench measurement values for -3dB BW and attenuation at 27MHz. The attenuation is over 40dB at 27MHz. At 6MHz, the attenuation is approximately 0.6dB for R1 = R2 = 150Ω (Figure 5).

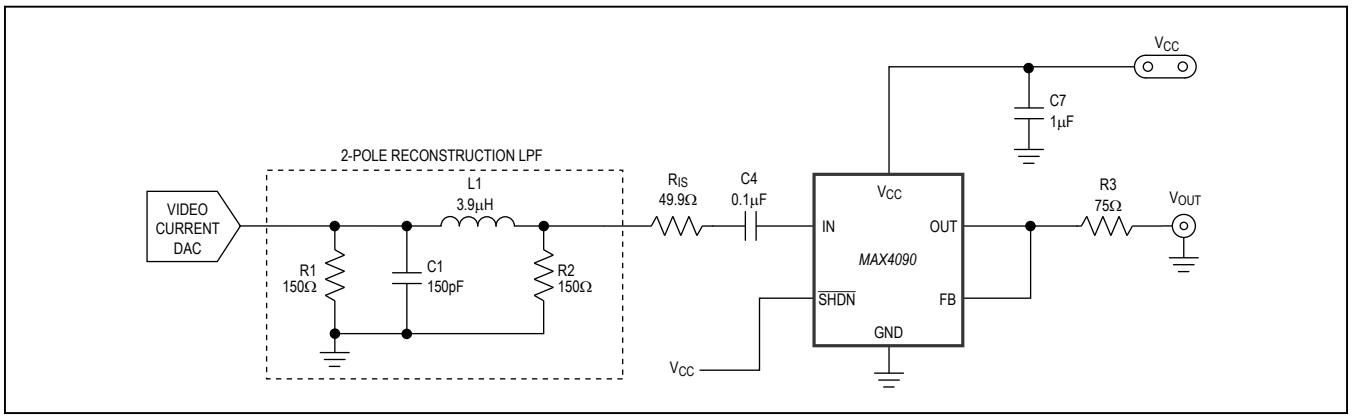


Figure 1. 2nd-Order Butterworth LPF with MAX4090

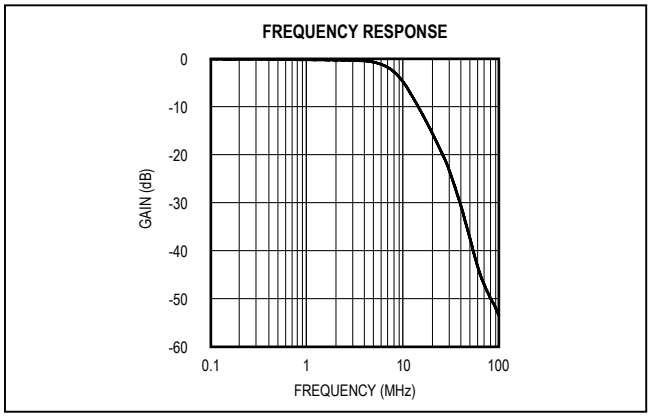


Figure 2. Frequency Response

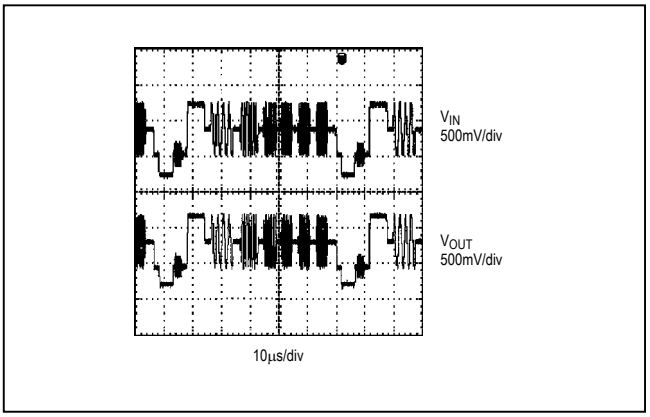


Figure 3. Multiburst Response

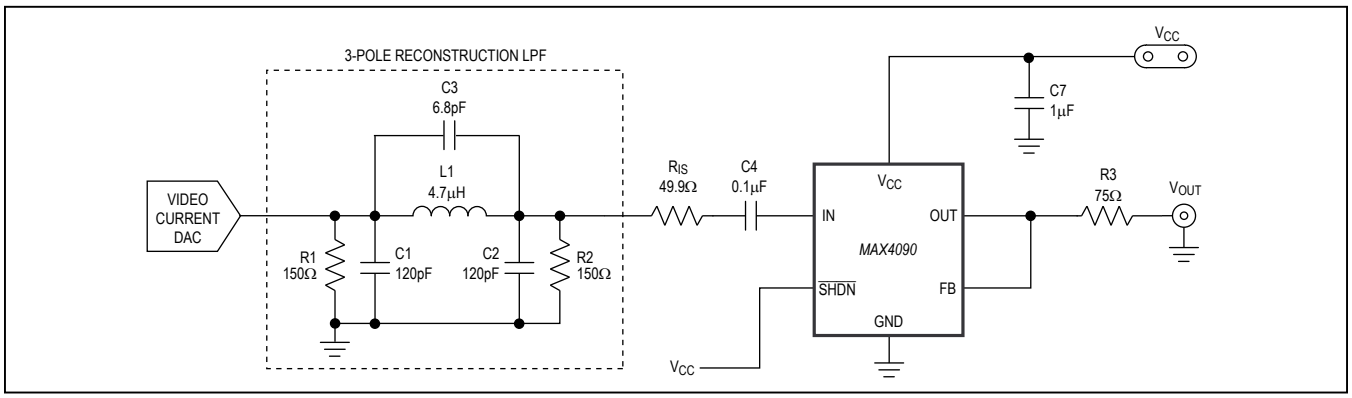


Figure 4. 3rd-Order Butterworth LPF with MAX4090

Table 2. Bench Measurement Values

R1 = R2 (Ω)	C1 (pf)	L1 (MH)	R_{IS} (Ω)	3dB BW (MHz)	ATTENUATION AT 27MHz (dB)
75	330	1.8	0	8.7	20
150	150	3.9	50	9.0	20
200	120	4.7	50	9.3	22
300	82	8.2	100	8.7	20

Table 3. 3rd-Order Butterworth Lowpass Filter Normalized Values

Rn1 = Rn2 (Ω)	Cn1 (F)	Cn2 (F)	Cn3 (F)	Ln1 (H)
1	0.923	0.923	0.06	1.846

Table 4. Bench Measurement Values

R1 = R2 (Ω)	C1 (pF)	C2 (pF)	C3 (pF)	L (µH)	R_{IS} (Ω)	3dB BW (MHz)	ATTENUATION AT 27MHz (dB)
75	220	220	15.0	2.2	0	9.3	43
150	120	120	6.8	4.7	50	8.9	50
300	56	56	3.3	10.0	100	9.0	45

Sag Correction

In a 5V application, the MAX4090 can use the sag configuration if an AC-coupled output video signal is required. Sag correction refers to the low-frequency compensation for the highpass filter formed by the 150Ω load and the output capacitor. In video applications, the cutoff frequency must be low enough to pass the vertical sync interval to avoid field tilt. This cutoff frequency should be less than 5Hz, and the coupling capacitor must be very large in normal configuration, typically > 220µF. In sag configuration, the MAX4090 eliminates the need for large coupling capacitors, and instead requires two 22µF capacitors (Figure 6) to reach the same performance as the large capacitor. Bench experiments show that increasing the output coupling capacitor C5 beyond 47µF does not improve the performance. If the supply voltage is less than 4.5V, the sag correction is not recommended for the MAX4090.

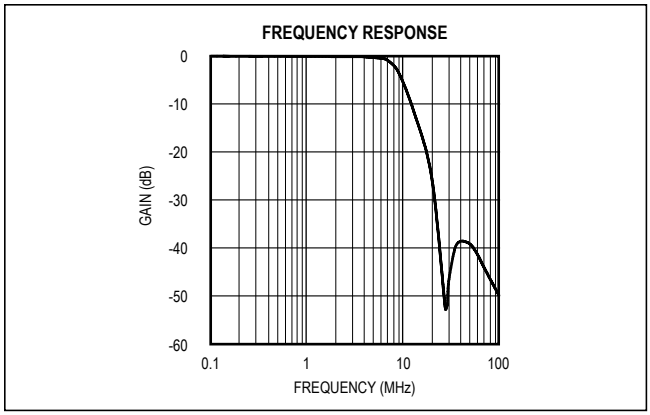


Figure 5. Frequency Response for R1 = R2 = 150W

Layout and Power-Supply Bypassing

The MAX4090 operates from single 2.7V to 5.5V supply. Bypass the supply with a 0.1µF capacitor as close to the pin as possible. Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the device's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following design guidelines:

- Do not use wire-wrap boards; they are too inductive.
- Do not use IC sockets; they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better, high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

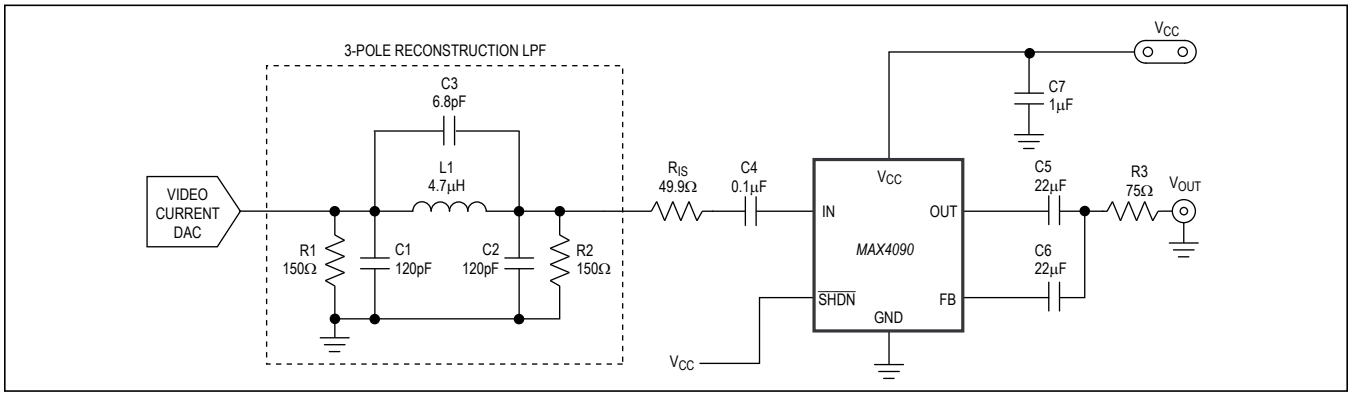


Figure 6. Sag Correction Configuration

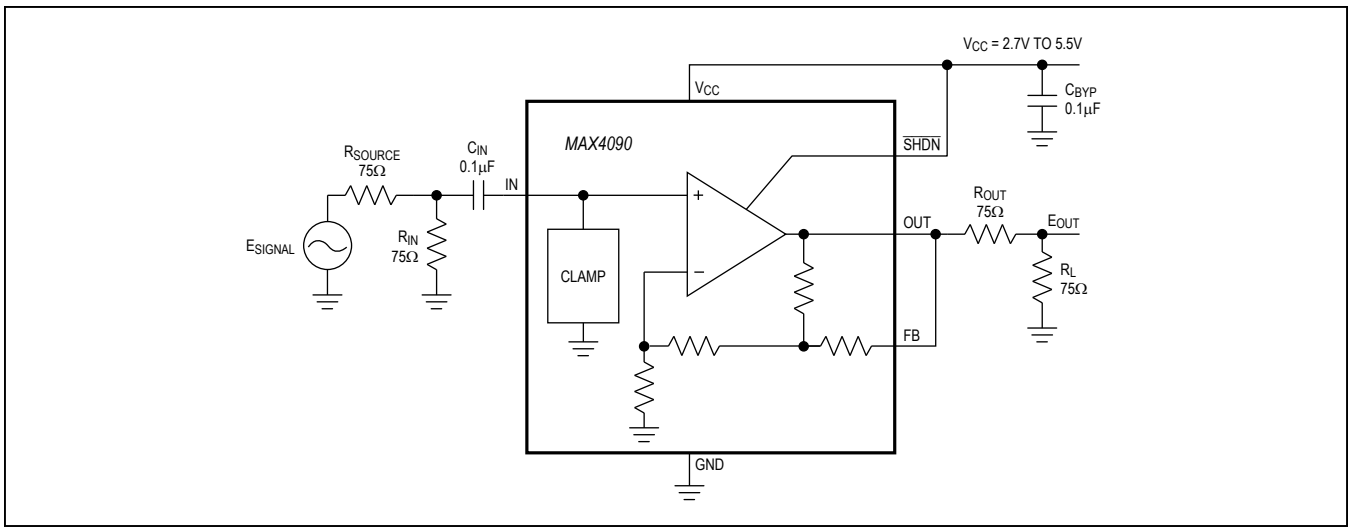


Figure 7. Typical Operating Circuit

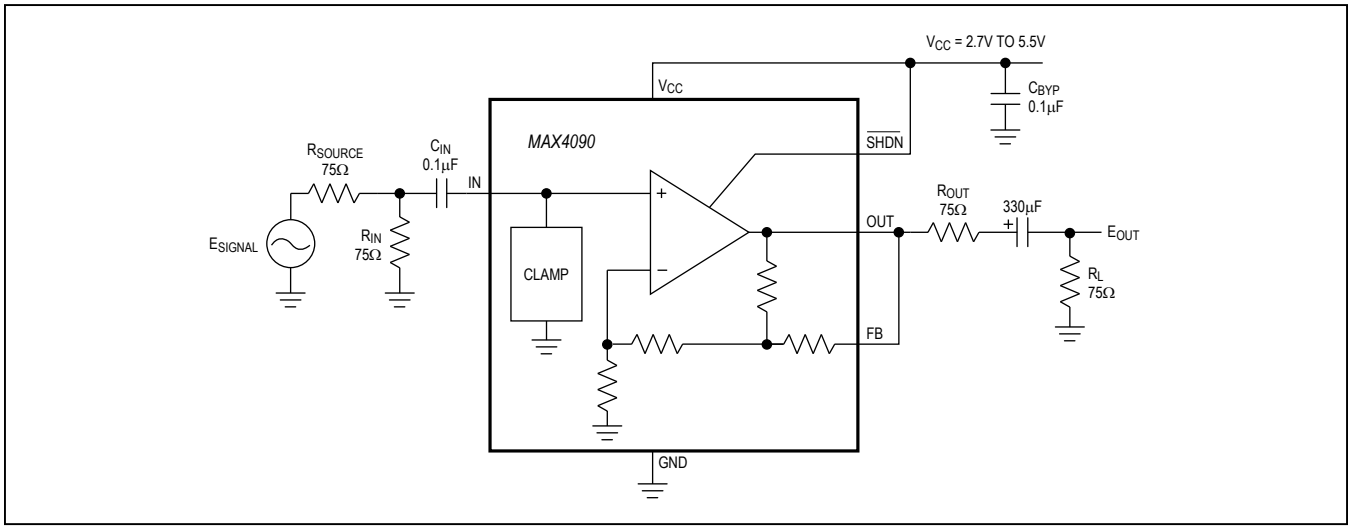


Figure 8. AC-Coupled Output Circuit

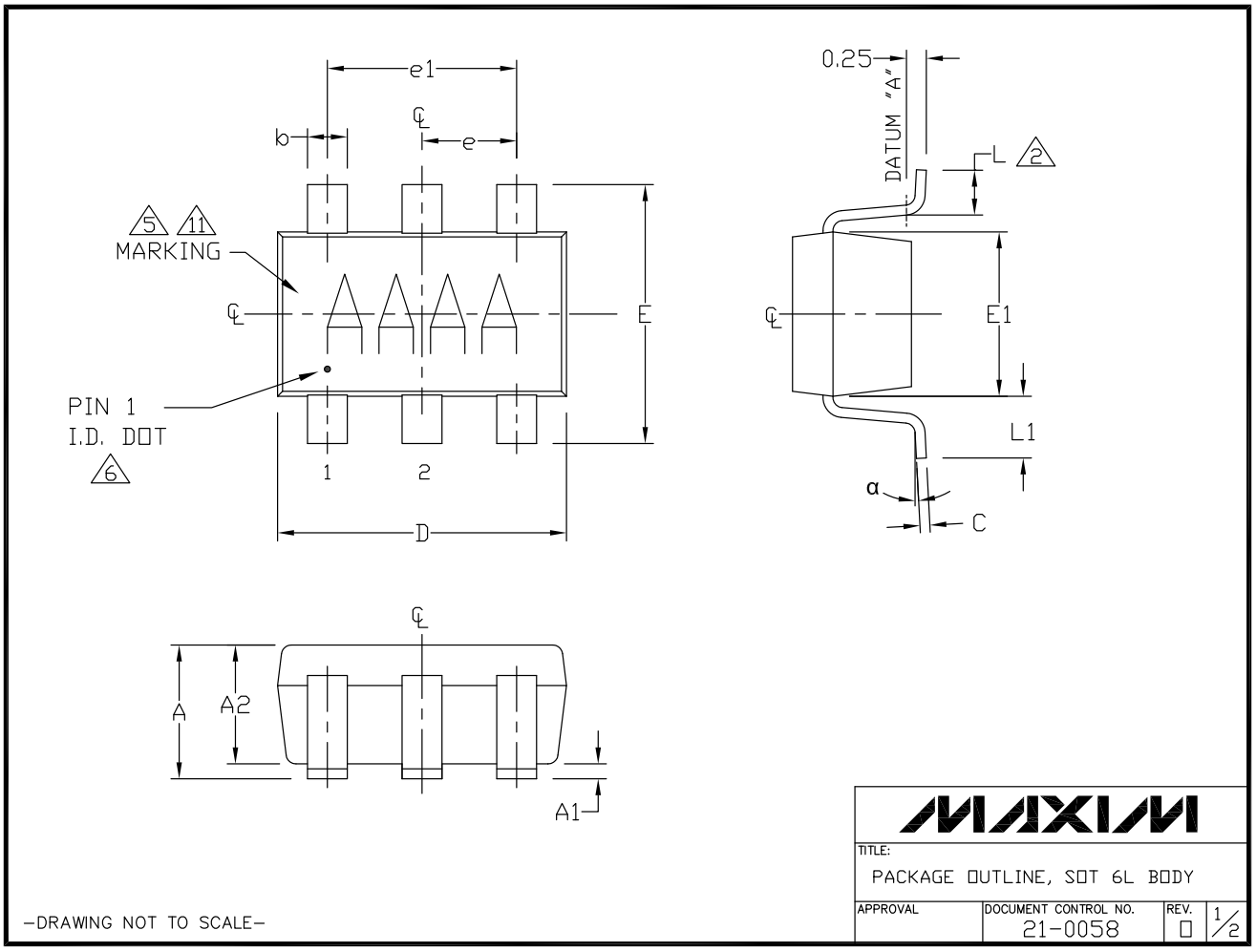
Chip Information

TRANSISTOR COUNT: 755
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SOT23	U6F-6	21-0058
6 µDFN	L622-1	21-0164
6 SC70	X6SN-1	21-0077



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHER SPECIFIED.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT.
6. PIN 1 I.D. DOT IS Ø0.3mm MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6-5,
U6CN-2, U6SN-1, U6F-6,
U6FH-6; U6FH-7; U6-8, U6-9

** U6FH-7 TO BE USED FOR NP42 PARTS ONLY
** U6-9 TO BE USED FOR RF50 PARTS ONLY WHICH USES A SI SPACER
** U6-5 USES LOW STRESS MOLD COMPOUND

—DRAWING NOT TO SCALE—

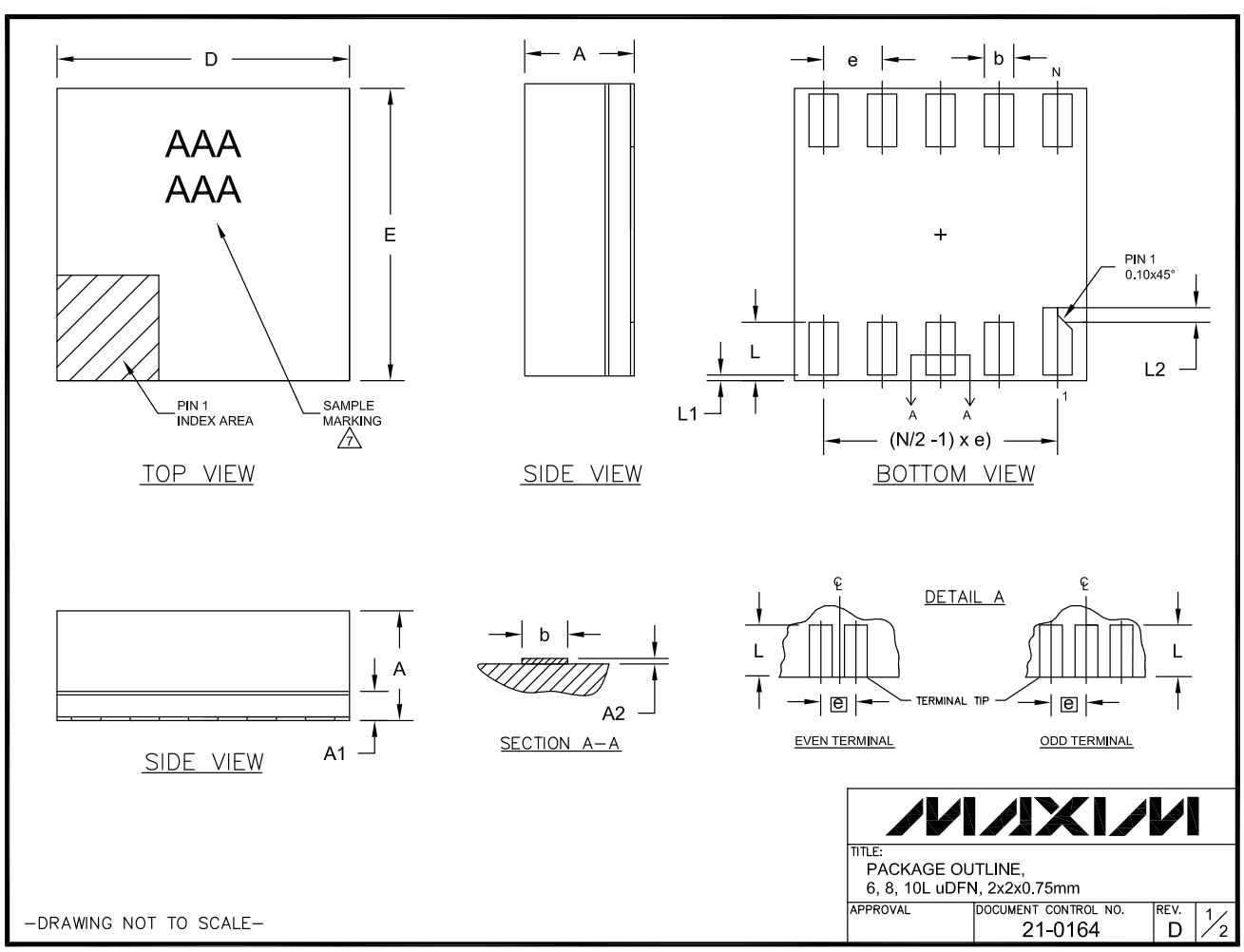
MAXIM

TITLE:
PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	D	2/2

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.00	–	0.05
L2	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. ONLY 8L PACKAGE COMPLIES TO JEDEC MO252.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PACKAGE CODES.
10. LEAD PLATING MATERIAL: GOLD, 0.5 MICROMETER MINIMUM THICKNESS.

–DRAWING NOT TO SCALE–

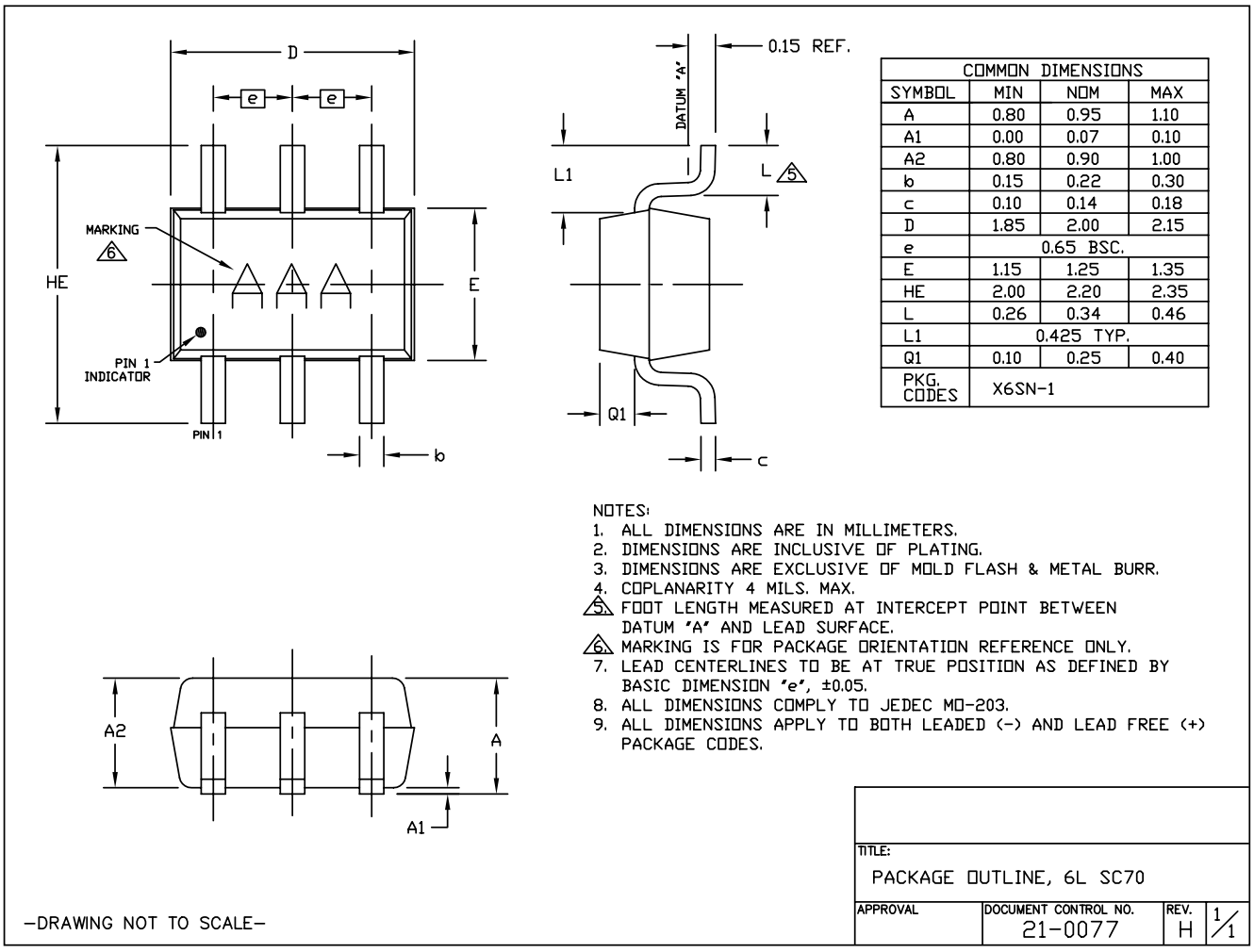
MAXIM

TITLE:
PACKAGE OUTLINE,
6, 8, 10L uDFN, 2x2x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0164	D	2/2

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.85	2.00	2.15
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	2.00	2.20	2.35
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		