MAX4968B/MAX4968C

16-Channel, Linear, High-Voltage Analog Switches in BGA Package

General Description

The MAX4968B/MAX4968C are 16-channel, high-linearity, high-voltage (HV), bidirectional SPST analog switches with 18Ω (typ) on-resistance. The devices are ideal for use in applications requiring high-voltage switching controlled by a low-voltage control signal, such as ultrasound imaging and industrial printing. The MAX4968C provides integrated 40kΩ bleed resistors on each switch terminal to discharge capacitive loads. Using HVCMOS technology, these switches combine high-voltage bilateral MOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

In typical ultrasound applications, the MAX4968B/MAX4968C do not require a dedicated HV supply, which implies a significant simplification of system requirements. The negative voltage supply can be shared with the transmitter and the positive voltage supply is typically +12V.

The devices are available in a 64-bump BGA package and are specified over the -40°C to +85°C extended temperature range.

Applications

- Medical Ultrasound Imaging
- Nondestructive Testing (NDT)
- Industrial Printing

***Ordering Information* appears at end of data sheet.**

Features

- Save Space—Optimized for High-Channel-Count Systems
  - Small BGA Package
  - 16 Integrated Channels
- High Performance—Designed to Enhance Image Quality
  - True Linear Switching—R_{ON} Flatness Guaranteed in Entire Input Range 46dB (typ) THD
  - Low Parasitic Capacitance Guarantees High Bandwidth
  - Low-Charge Injection and Voltage Spiking
  - 2nd Harmonic Distortion < -45dB at 2MHz ± 90V Pulse Analog Class AB
  - DC to 30MHz Small-Signal Analog Bandwidth (C_{LOAD} = 200pF)
  - 500kHz to 20MHz High-Signal Analog Bandwidth (C_{LOAD} = 200pF)
  - Extended Input Range Up to $210V_{P-P}$
  - -68dB (Typ) Off-Isolation at 5MHz (50Ω)
- Increased Flexibility Saves Design Time
  - No Dedicated High-Voltage Supplies Required
  - Daisy-Chainable Serial Interface
  - Asynchronous Set/Clear Input to Program All Switches Without Need for SPI
- Superior Reliability
  - Latch-Free SOI HVCMOS Process Technology for High Performance and Robustness
  - Integrated Overvoltage Protection

19-7312; Rev 0; 3/14

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{DD} Logic Supply Voltage .....-0.3V to +6V
V_{P-P} Supply Voltage .....-0.3V to +13V
V_{NN} Negative Supply Voltage .....+0.3V to -200V
V_{CC10} Input Voltage.....-0.3V to MAX (12V to V_{P-P} + 0.3V)
Logic Inputs Voltage (CLK, DIN, $\overline{LE}$, CLR, SET) ...-0.3V to +6V
Logic Output Voltage (DOUT) .....-0.3V to (V_{DD} + 0.3V)
Analog Signal Range (SW_) .....(V_{NN} - 0.3V) to (V_{NN} + 214V)

Continuous Power Dissipation (T_A = +70°C)
64-bump BGA (derate 30.30mW/°C above +70°C)..1969.7mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature..... +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....3.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +2.37V to +5.5V, V_{P-P} = +10V to +12.5V, V_{NN} = 0 to -200V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{P-P} = +12V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{DD} Logic Supply Voltage	V_{DD}		2.37		5.5	V
V_{NN} Supply Voltage	V_{NN}		-200		0	V
V_{P-P} Supply Voltage	V_{P-P}		10	12	12.5	V
V_{DD} Static Current	I_{DDS}			25	50	µA
V_{DD} Dynamic Current	I_{DD}	V_{DD} = +5V, f_{CLK} = 5MHz, f_{DIN} = 2.5MHz		100	200	µA
V_{NN} Static Current	I_{NNS}	All switches remain on or off, SW_ = GND		15	25	µA
V_{NN} Supply Dynamic Current (All Channel Switching Simultaneously)	I_{NN}	V_{P-P} = +12V, V_{NN} = -100V, $f_{TURN_ON/OFF}$ = 50kHz, SW_ = GND		4.3	8	mA
V_{P-P} Supply Static Current	I_{PPS}	All switches remain on or off, SW_ = GND		75	160	µA
V_{P-P} Supply Dynamic Current (All Channel Switching Simultaneously)	I_{PP}	V_{P-P} = +12V, V_{NN} = -100V, $f_{TURN_ON/OFF}$ = 50kHz, SW_ = GND		5.4	9	mA
V_{CC10} Static Output Voltage	V_{CC10s}	V_{P-P} = +12V, all switches remain on or off, SW_ = GND	10	10.5		V
V_{CC10} Dynamic Output Voltage	V_{CC10}	V_{P-P} = +12V, I_{OUT} = 30mA	9.5	10.25		V

Electrical Characteristics (continued)

(V_{DD} = +2.37V to +5.5V, V_{P-P} = +10V to +12.5V, V_{NN} = 0 to -200V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{P-P} = +12V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCH CHARACTERISTICS						
Analog Dynamic Signal Range	$V_{SW_}$	AC operation only, f > 500kHz	V_{NN}		V_{NN} +210	V
Small-Signal On-Resistance	R_{ONS}	V_{P-P} = +12V, V_{NN} = -100V, $V_{SW_}$ = 0V, $I_{SW_}$ = 5mA		18	34	Ω
Small-Signal On-Resistance Matching	ΔR_{ONS}	V_{P-P} = +12V, V_{NN} = -100V, $I_{SW_}$ = 5mA		3		%
Small-Signal On-Resistance Flatness	R_{ONF}	AC measured, f_{SW} = 0.5MHz, V_{SW} = 80V_{P-P}, R_{LOAD} = 50Ω, V_{P-P} = +12V, V_{NN} = -100V		2		%
Output Switch Bleed Resistor	R_{INT}	MAX4968C only	30	40	50	kΩ
Switch-Off Leakage	$I_{SW_(OFF)}$	V_{SW} = 0V, switch off (MAX4968B only)		0	1	ΩA
Switch-Off DC Offset		R_L = 100kΩ on both sides	-15		+15	mV
Switch-On DC Offset		R_L = 100kΩ on both sides	-15		+15	mV
Switch Output Isolation Diode Current		300ns pulse width, 2% duty cycle		3.0		A
SWITCH DYNAMIC CHARACTERISITICS						
Turn-On Time	t_{ON}	$V_{SW_}$ = +1V, R_L = 100Ω, V_{NN} = -100V, from SET to $V_{SW_}$ = +0.9V		2	5	µs
Turn-Off Time	t_{OFF}	$V_{SW_}$ = +1V, R_L = 100Ω, V_{NN} = -100V, from CLR to $V_{SW_}$ = +0.9V		2	3.5	µs
Maximum $V_{SW_}$ Slew Rate	dV/dt	C_L = 100pF	20			V/ns
Off-Isolation	V_{ISO}	f = 5MHz, R_L = 50Ω		-68		dB
Crosstalk	V_{CT}	f = 5MHz, R_L = 50Ω		-69		dB
SW_ Off-Capacitance	$C_{SW_(OFF)}$	f = 1MHz, small signal close to zero		8		pF
SW_ On-Capacitance	$C_{SW_(ON)}$	f = 1MHz, small signal close to zero		14		pF
Output Voltage Spike	V_{SPK}	R_L = 50Ω	-150		+150	mV
Large-Signal Analog Bandwidth (-3dB)	f_{BW_L}	C_{LOAD} = 200pF, 60V amplitude sinusoidal burst, 1% duty cycle		30		MHz
Small-Signal Analog Bandwidth (-3dB)	f_{BW_S}	C_{LOAD} = 200pF, 100mV amplitude sinusoidal		50		MHz
Charge Injection	Q	V_{NN} = -100V, Figure 1		150		pC
LOGIC LEVELS						
Logic-Input Low Voltage	V_{IL}				0.75	V
Logic-Input High Voltage	V_{IH}		V_{DD} - 0.75			V
Logic-Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V

Electrical Characteristics (continued)

(V_{DD} = +2.37V to +5.5V, V_{P-P} = +10V to +12.5V, V_{NN} = 0 to -200V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +3.3V, V_{NN} = -100V, V_{P-P} = +12V at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 1mA	V_{DD} - 0.4			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage	I_{IN}		-1		+1	µA
Pulldown Resistor in SET Pin	$R_{PULLDOWN}$		65	100	140	kΩ
TIMING CHARACTERISTICS (Figure 2)						
CLK Frequency	f_{CLK}				25	MHz
DIN-to-CLK Setup Time	t_{DS}		4			ns
DIN-to-CLK Hold Time	t_{DH}		4			ns
CLK to LE Setup Time	t_{CS}		28			ns
$\overline{LE}$ Low Pulse Width	t_{WL}		12			ns
CLR High Pulse Width	t_{WC}		16			ns
SET High Pulse Width	t_{WS}		16			ns
CLK Rise and Fall Times	t_R, t_F				50	ns
CLK to DOUT Delay	t_{DO}	V_{DD} = +5V ±10%, C_{DOUT} = 15pF			28	ns
		V_{DD} = +2.5V ±5%, C_{DOUT} = 15pF			45	

Note 2: All devices are 100% tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design.

Pin Test Circuits/Timing Diagrams

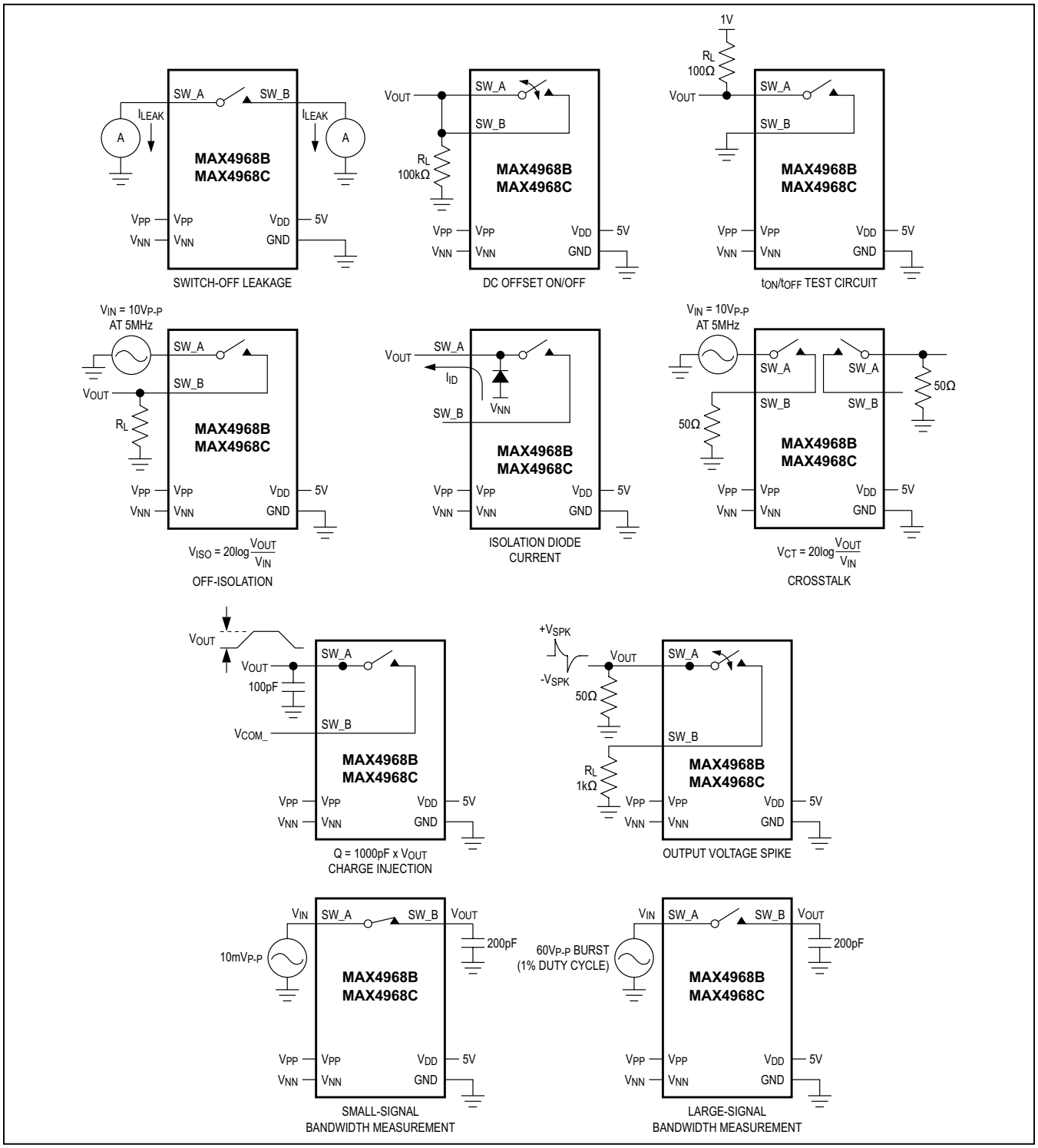


Figure 1. Test Circuits

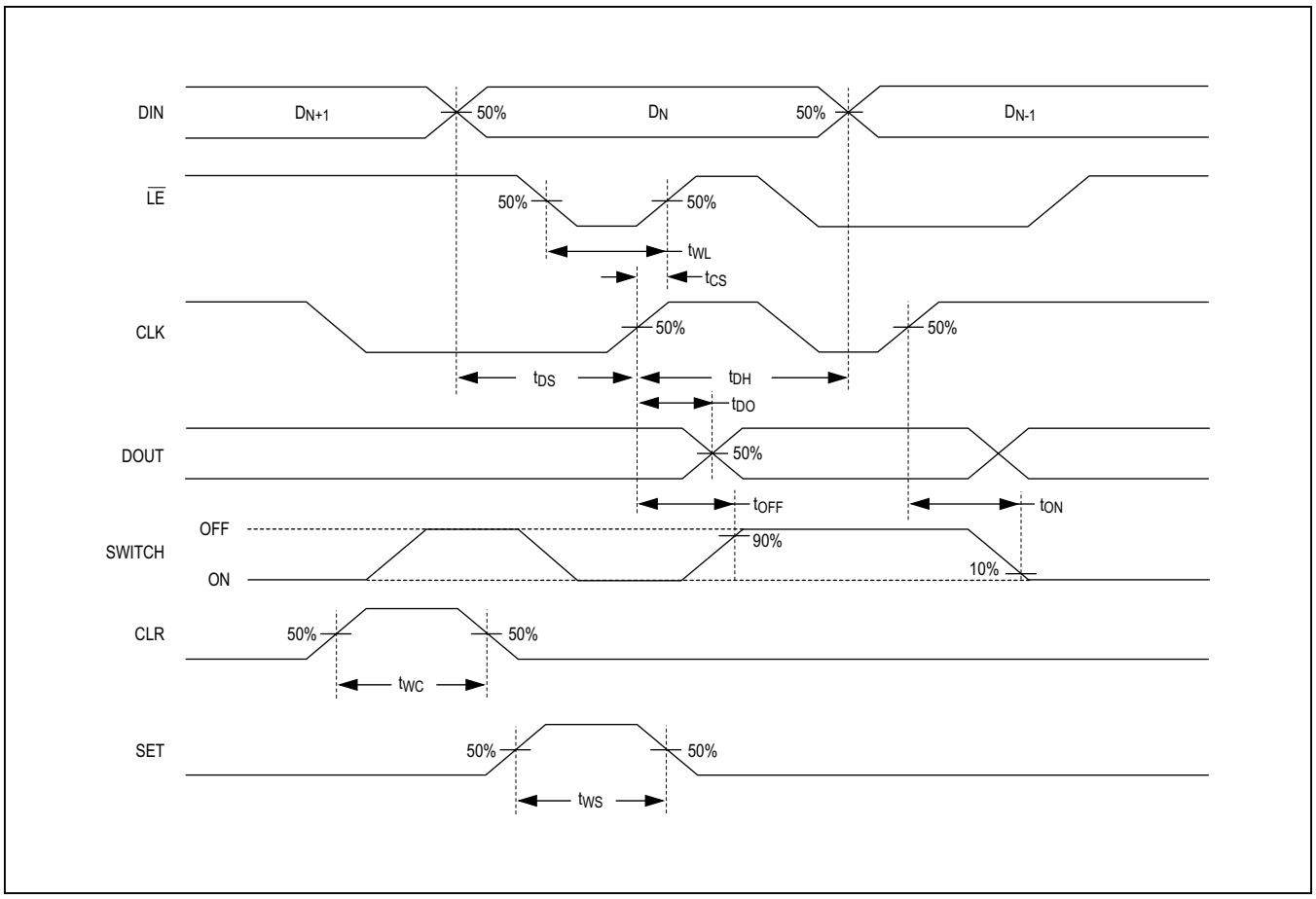
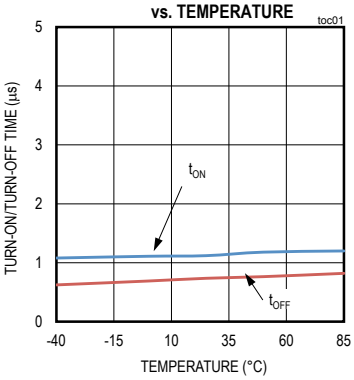


Figure 2. Serial Interface Timing

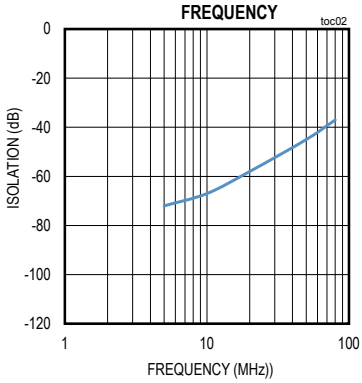
Typical Operating Characteristics

(V_{DD} = +3V, V_{P-P} = +12V, V_{NN} = -100V, R_L = 100Ω, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

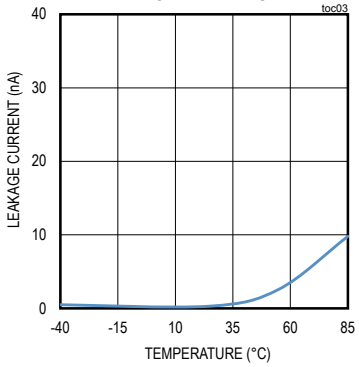
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



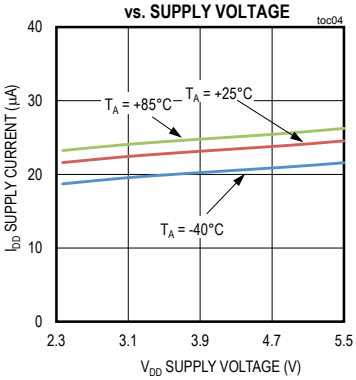
ISOLATION vs. FREQUENCY



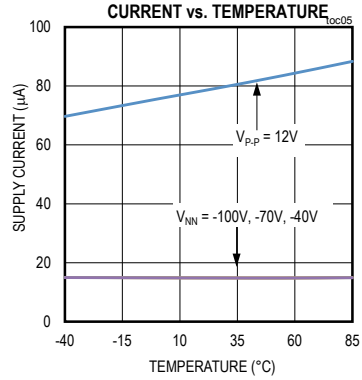
SWITCH-OFF LEAKAGE CURRENT vs. TEMPERATURE



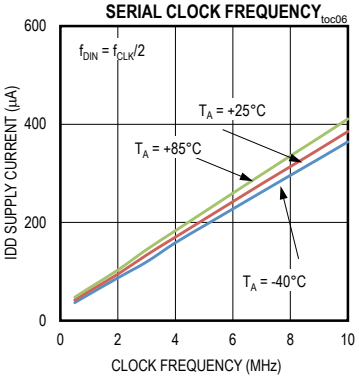
LOGIC SUPPLY CURRENT vs. SUPPLY VOLTAGE



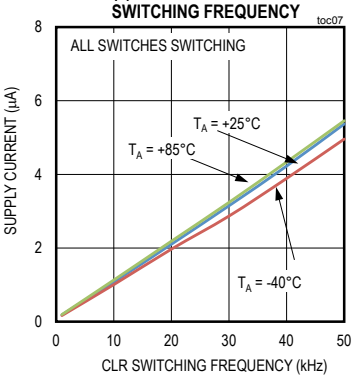
POSITIVE AND NEGATIVE POWER-SUPPLY CURRENT vs. TEMPERATURE



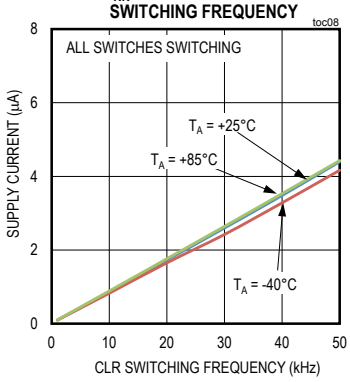
LOGIC SUPPLY CURRENT vs. SERIAL CLOCK FREQUENCY



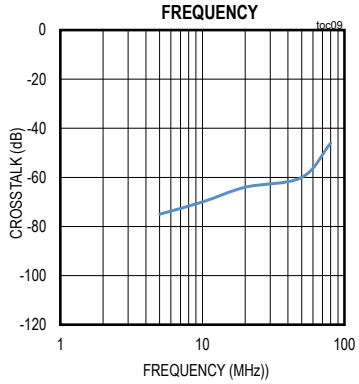
V_{P-P} SUPPLY CURRENT vs. SWITCHING FREQUENCY



V_{NN} SUPPLY CURRENT vs. SWITCHING FREQUENCY



CROSSTALK vs. FREQUENCY



Pin Configuration

TOP VIEW
(BUMPS ON BOTTOM)

MAX4968B
MAX4968C

	1	2	3	4	5	6	7	8
A	SW5A	SW5B	SW6B	SW7B	SW8B	SW9B	SW10B	SW10A
B	SW4B	SW4A	SW6A	SW7A	SW8A	SW9A	SW11A	SW11B
C	SW3A	SW3B	N.C.	N.C.	N.C.	N.C.	SW12B	SW12A
D	SW2A	SW2B	N.C.	N.C.	N.C.	N.C.	SW13B	SW13A
E	SW1A	SW1B	N.C.	N.C.	N.C.	N.C.	SW14B	SW14A
F	SW0B	SW0A	N.C.	N.C.	N.C.	N.C.	SW15B	SW15A
G	N.C.	N.C.	V_{PP}	GND	CLK	CLR	N.C.	N.C.
H	V_{NN}	N.C.	V_{CC10}	V_{DD}	DIN	LE	DOUT	SET

7mm x 7mm
(64-BUMP BGA)

Pin Description

PIN	NAME	FUNCTION
A1	SW5A	Analog Switch 5 –Terminal
A2	SW5B	Analog Switch 5 – Terminal
A3	SW6B	Analog Switch 6 – Terminal
A4	SW7B	Analog Switch 7 – Terminal
A5	SW8B	Analog Switch 8 – Terminal
A6	SW9B	Analog Switch 9 – Terminal
A7	SW10B	Analog Switch 10 – Terminal
A8	SW10A	Analog Switch 10 – Terminal
C3-C6, D3-D6, E3-E6, F3-F6, G1, G2, G7, G8, H2	N.C.	No Connection. Not connected internally.
B1	SW4B	Analog Switch 4 – Terminal
B2	SW4A	Analog Switch 4 – Terminal
B3	SW6A	Analog Switch 6 – Terminal
B4	SW7A	Analog Switch 7 – Terminal
B5	SW8A	Analog Switch 8 – Terminal
B6	SW9A	Analog Switch 9 – Terminal
B7	SW11A	Analog Switch 11 – Terminal
B8	SW11B	Analog Switch 11 – Terminal
C1	SW3A	Analog Switch 3 – Terminal
C2	SW3B	Analog Switch 3 – Terminal
C7	SW12B	Analog Switch 12 – Terminal
C8	SW12A	Analog Switch 12 – Terminal
D1	SW2A	Analog Switch 2 – Terminal
D2	SW2B	Analog Switch 2 – Terminal
D7	SW13B	Analog Switch 13 – Terminal
D8	SW13A	Analog Switch 13 – Terminal
E1	SW1A	Analog Switch 1 – Terminal
E2	SW1B	Analog Switch 1 – Terminal
E7	SW14B	Analog Switch 14 – Terminal
E8	SW14A	Analog Switch 14 – Terminal
F1	SW0B	Analog Switch 0 – Terminal
F2	SW0A	Analog Switch 0 – Terminal
F7	SW15B	Analog Switch 15 – Terminal
F8	SW15A	Analog Switch 15 – Terminal
G3	V_{PP}	Positive Voltage Supply. Bypass V_{P-P} to GND with a 0.1µF or greater ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
G4	GND	Ground
G5	CLK	Serial-Clock Input
G6	CLR	Latch Clear Input
H1	V_{NN}	Negative High-Voltage Supply. Bypass V_{NN} to GND with a 0.1µF or greater ceramic capacitor.
H3	V_{CC10}	+10V LDO Output. Bypass V_{CC10} to GND with a 0.1µF or greater ceramic capacitor.
H4	V_{DD}	Logic Supply Voltage. Bypass V_{DD} to GND with a 0.1µF or greater ceramic capacitor.
H5	DIN	Serial-Data Input
H6	$\overline{LE}$	Active-Low Latch-Enable Input
H7	DOUT	Serial-Data Output
H8	SET	Latch-Set Input. Pulldown resistor 100kΩ.

Detailed Description

The MAX4968B/MAX4968C are 16-channel, high-linearity, high-voltage, bidirectional SPST analog switches with 18Ω (typ) on-resistance. The devices are ideal for use in applications requiring high-voltage switching controlled by a low-voltage control signal, such as ultrasound imaging and industrial printing. The MAX4968C provides integrated 40kΩ bleed resistors on each switch terminal to discharge capacitive loads. Using HVCMOS technology, these switches combine high-voltage, bilateral MOS switches and low-power CMOS logic to provide efficient control of high-voltage analog signals.

In typical ultrasound applications, the MAX4968B/MAX4968C do not require a dedicated HV supply, which implies a significant simplification of system requirements. The negative voltage supply can be shared with the transmitter and the positive voltage supply is typically +12V.

Analog Switch

The devices can transmit analog signals up to $210V_{P-P}$, with an analog signal range from V_{NN} to V_{NN} + 210V. Before starting the high-voltage burst transmission (V_{P-P} > +20V), the input voltage must be close to GND to allow a proper settling of the pass FET. The high-voltage burst frequency must be greater than 500kHz.

Extremely long high-voltage bursts (V_{P-P} > 10V) with duty cycle greater than 20% could result in signal degradation, especially for unipolar transmission. In general, this applies for burst transmission with a nonzero DC content.

Low-voltage signals (V_{P-P} < 10V) continuous wave bipolar transmission is supported for frequencies greater than 500kHz. For very small signals, such as the small echoes in typical ultrasound imaging systems (V_{P-P} < 10V), the devices are not limited to a low-frequency bandwidth and can transmit DC signals.

Voltage Supplies

The devices operate with a high voltage supply V_{NN} from -200V to 0, V_{P-P} supply of +12V (typ), and a logic supply V_{DD} (+2.37V to +5.5V).

Bleed Resistors (MAX4968C)

The MAX4968C features integrated 40kΩ bleed resistors to discharge capacitive loads such as piezoelectric transducers. Each analog switch terminal is connected to GND with a bleed resistor.

Serial Interface

The MAX4968B/MAX4968C are controlled by a serial interface with a 16-bit serial shift register and transparent latch. Each of the 16 data bits controls a single analog switch (see Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 16 clock cycles (see Figure 2 and Figure 3).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the high-voltage switches (Figure 3); drive $\overline{LE}$ logic-high to freeze the contents of the latch and prevent changes to the switch states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

Latch Clear (CLR)

The MAX4968B/MAX4968C feature a latch-clear input. Drive CLR logic-high to reset the contents of the latch to zero and open all switches simultaneously. CLR does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch.

Latch Set (SET)

The MAX4968B/MAX4968C feature a latch-set input. Drive SET logic-high to set the contents of the latch to logic-high and close all switches simultaneously. SET does not affect the contents of the data shift register. Pulse $\overline{LE}$ logic-low to reload the contents of the shift register into the latch. CLR is dominant with respect to SET.

Power-On Reset

The MAX4968B/MAX4968C feature a power-on-reset circuit to ensure all switches are open at power-on. The internal 16-bit serial shift register and latch are set to zero on power-up.

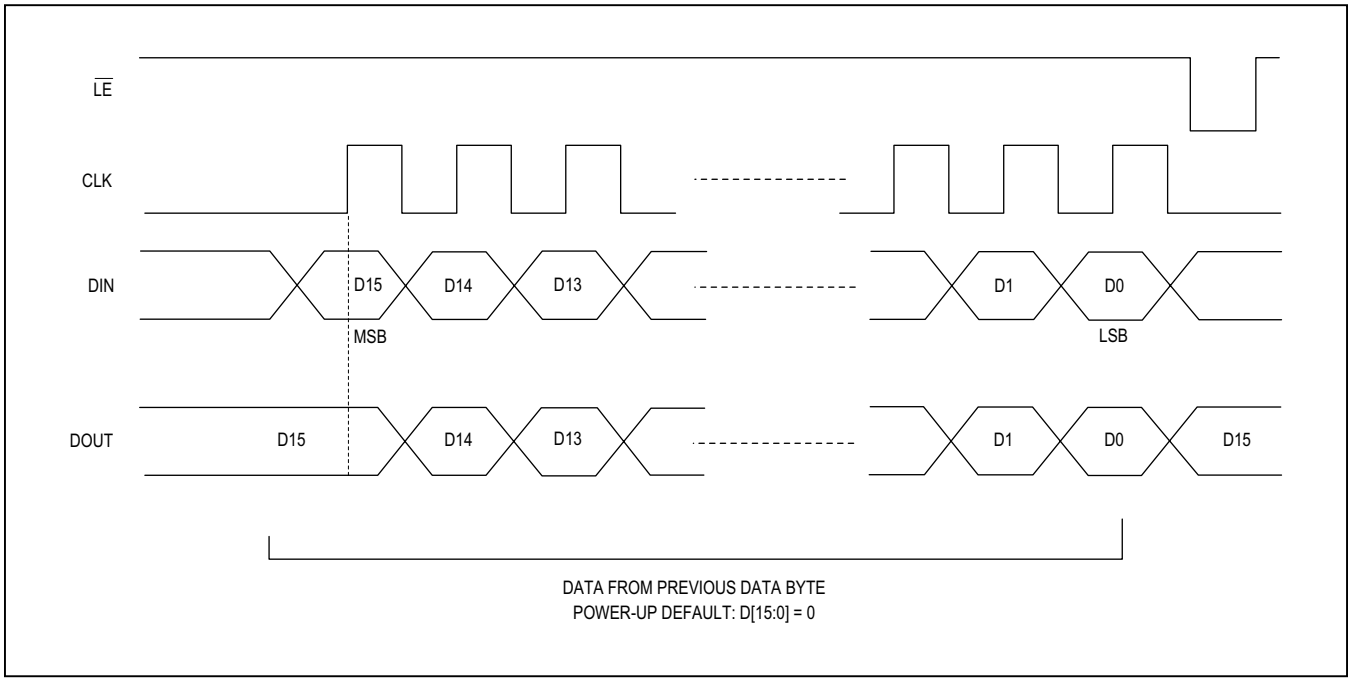


Figure 3. Latch-Enable Interface Timing

Table 1. Serial Interface Programming (Notes 3–8)

DATA BITS								CONTROL BITS			FUNCTION							
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SET	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	L	OFF							
H								L	L	L	ON							
	L							L	L	L		OFF						
	H							L	L	L		ON						
		L						L	L	L			OFF					
		H						L	L	L			ON					
			L					L	L	L				OFF				
			H					L	L	L				ON				
				L				L	L	L					OFF			
				H				L	L	L					ON			
					L			L	L	L						OFF		
					H			L	L	L						ON		
						L		L	L	L							OFF	
						H		L	L	L							ON	
							L	L	L	L								OFF
							H	L	L	L								ON
X	X	X	X	X	X	X	X	H	L	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	X	L	H	ON	ON	ON	ON	ON	ON	ON	ON

DATA BITS								CONTROL BITS			FUNCTION							
D8	D9	D10	D11	D12	D13	D14	D15 (MSB)	$\overline{LE}$	CLR	SET	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
L								L	L	L	OFF							
H								L	L	L	ON							
	L							L	L	L		OFF						
	H							L	L	L		ON						
		L						L	L	L			OFF					
		H						L	L	L			ON					
			L					L	L	L				OFF				
			H					L	L	L				ON				
				L				L	L	L					OFF			
				H				L	L	L					ON			
					L			L	L	L						OFF		

Table 1. Serial Interface Programming (Notes 3–8) (continued)

DATA BITS								CONTROL BITS			FUNCTION							
D8	D9	D10	D11	D12	D13	D14	D15 (MSB)	$\overline{LE}$	CLR	SET	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
					H			L	L	L						ON		
						L		L	L	L							OFF	
						H		L	L	L							ON	
							L	L	L	L								OFF
							H	L	L	L								ON
X	X	X	X	X	X	X	X	H	L	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	X	L	H	ON	ON	ON	ON	ON	ON	ON	ON

X = Don't care.

Note 3: The 16 switches operate independently.
Note 4: Serial data is clocked in on the rising edge of CLK.
Note 5: The switches go to a state retaining their present condition on the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift register data flows through the latch.
Note 6: DOUT is high when switch 15 is on.
Note 7: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
Note 8: The CLR input overrides all other inputs.

Applications Information

In typical ultrasound applications, the MAX4968B/MAX4968C do not require dedicated high-voltage supplies; the negative voltage supply can be shared with the transmitter and the positive voltage supply is typically +12V. See Figure 4, Figure 5, and Figure 6 for medical ultrasound applications.

Logic Levels

The MAX4968B/MAX4968C digital interface inputs (CLK, DIN, $\overline{LE}$, CLR, and SET) operate on the V_{DD} logic supply voltage.

Daisy-Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple MAX4968B/MAX4968C devices by daisy-chaining (Figure 8). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, CLR, and SET inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Drive SET high to close all the switches simultaneously. Additional shift registers can be included anywhere in series with the MAX4968B/MAX4968C data-chain.

Supply Sequencing and Bypassing

The MAX4968B/MAX4968C do not require special sequencing of the V_{DD}, V_{P-P} and V_{NN} supply voltages. Bypass V_{DD}, V_{P-P}, and V_{NN} to GND with a 0.1µF ceramic capacitor as close as possible to the device.

Application Diagrams

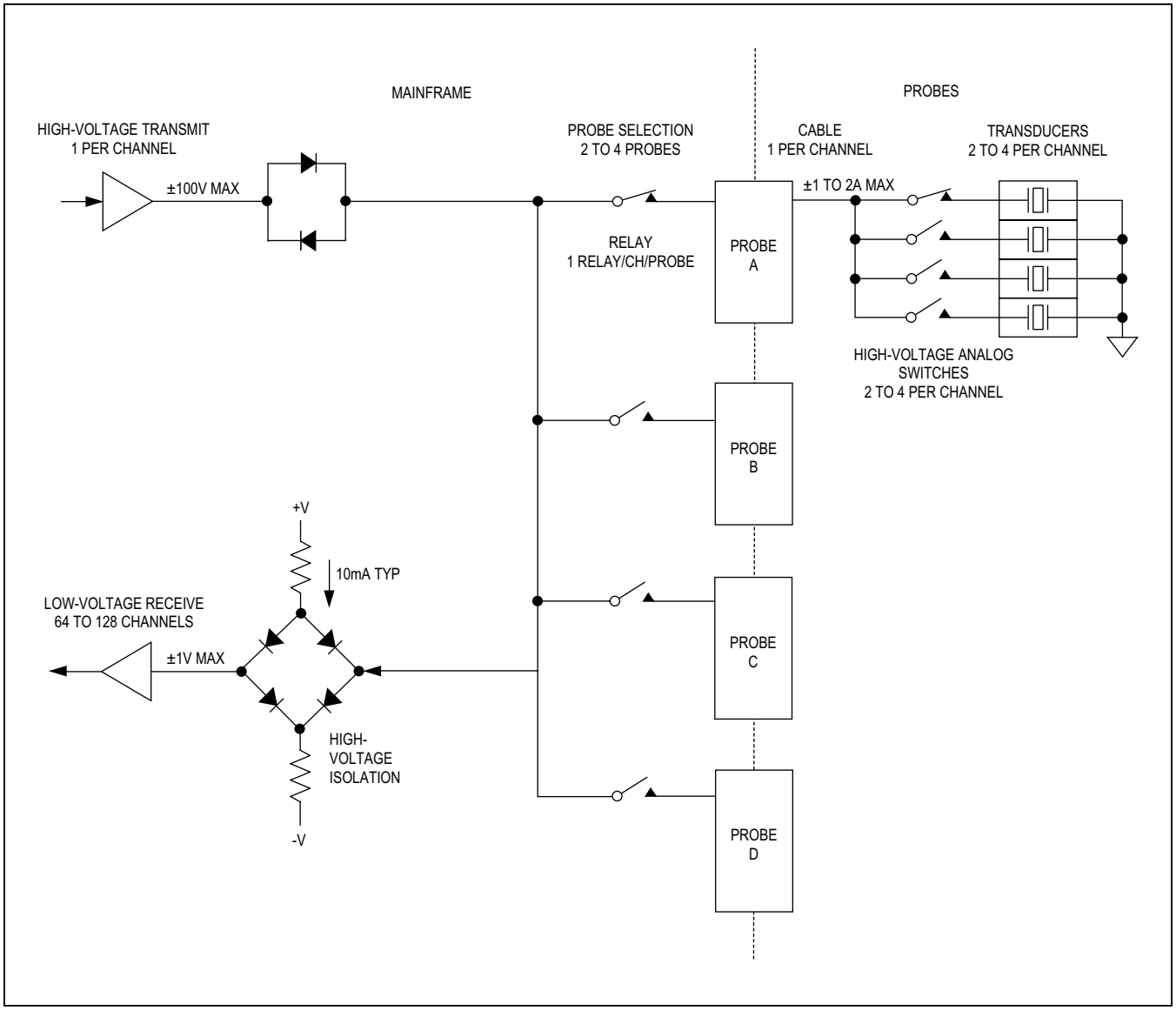


Figure 4. Medical Ultrasound Application — High-Voltage Analog Switches in Probe

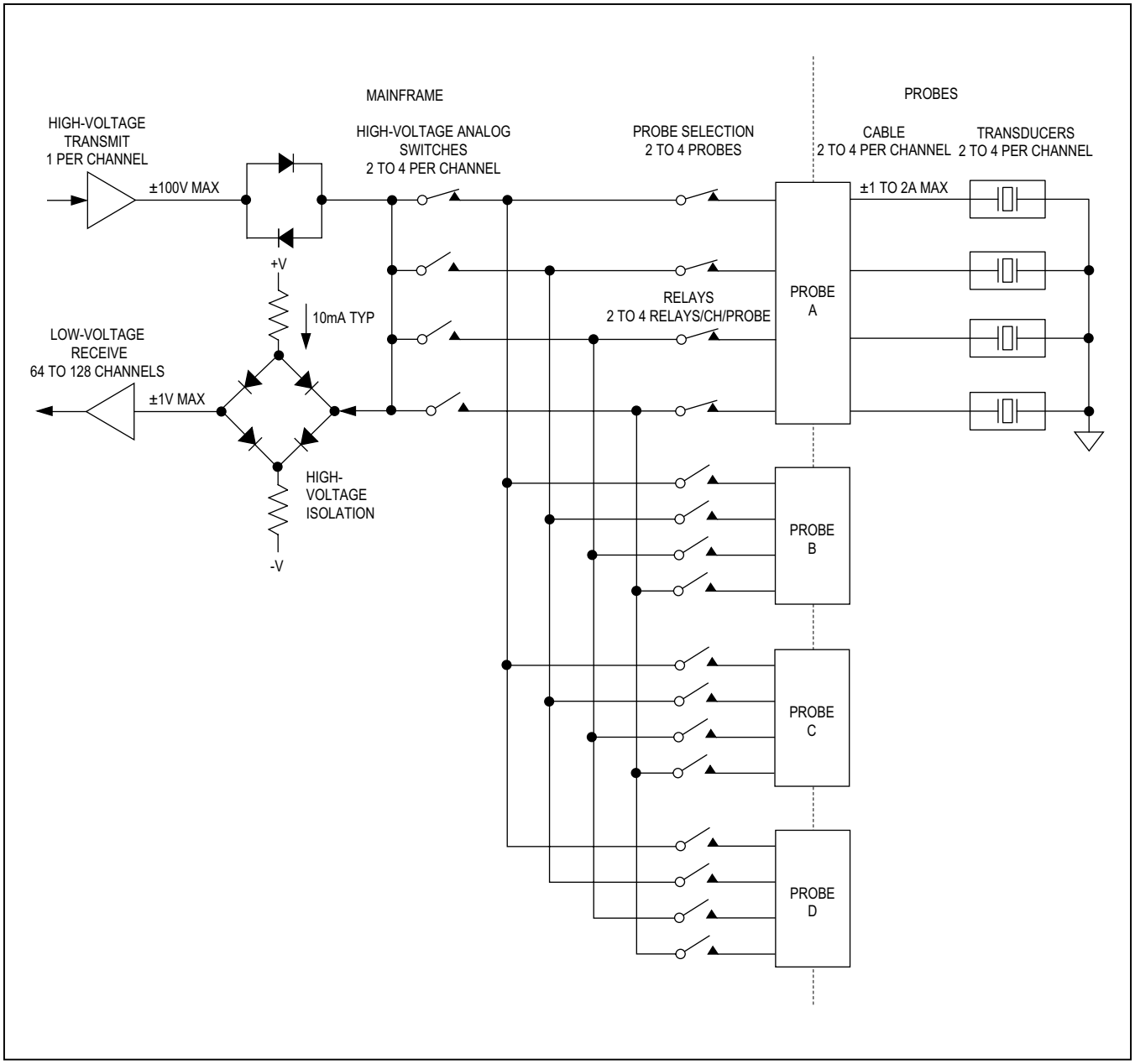


Figure 5. Medical Ultrasound Application — High-Voltage Analog Switches in Mainframe

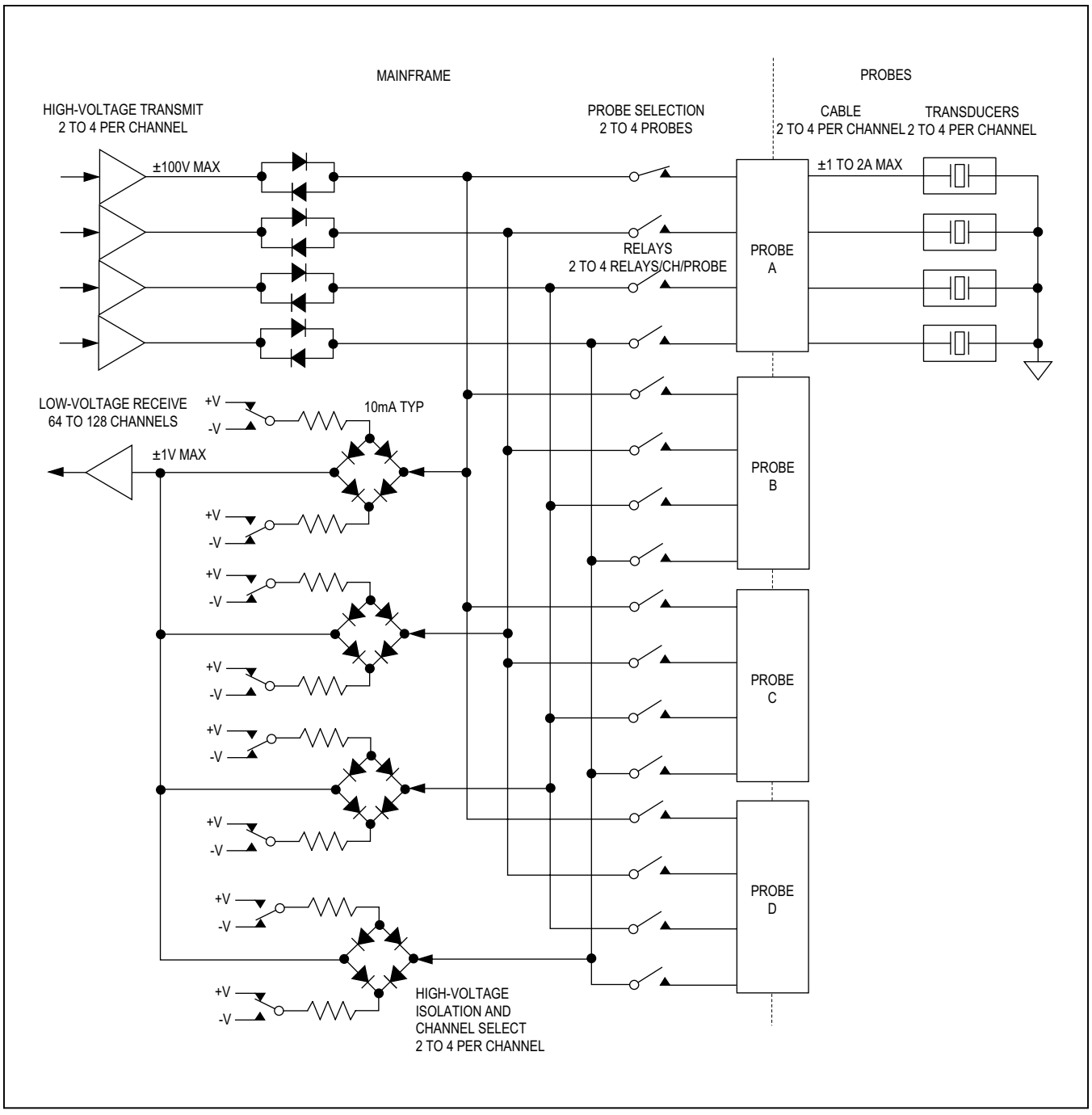


Figure 6. Medical Ultrasound Application — Multiple Transmit and Isolation per Receiver Channel

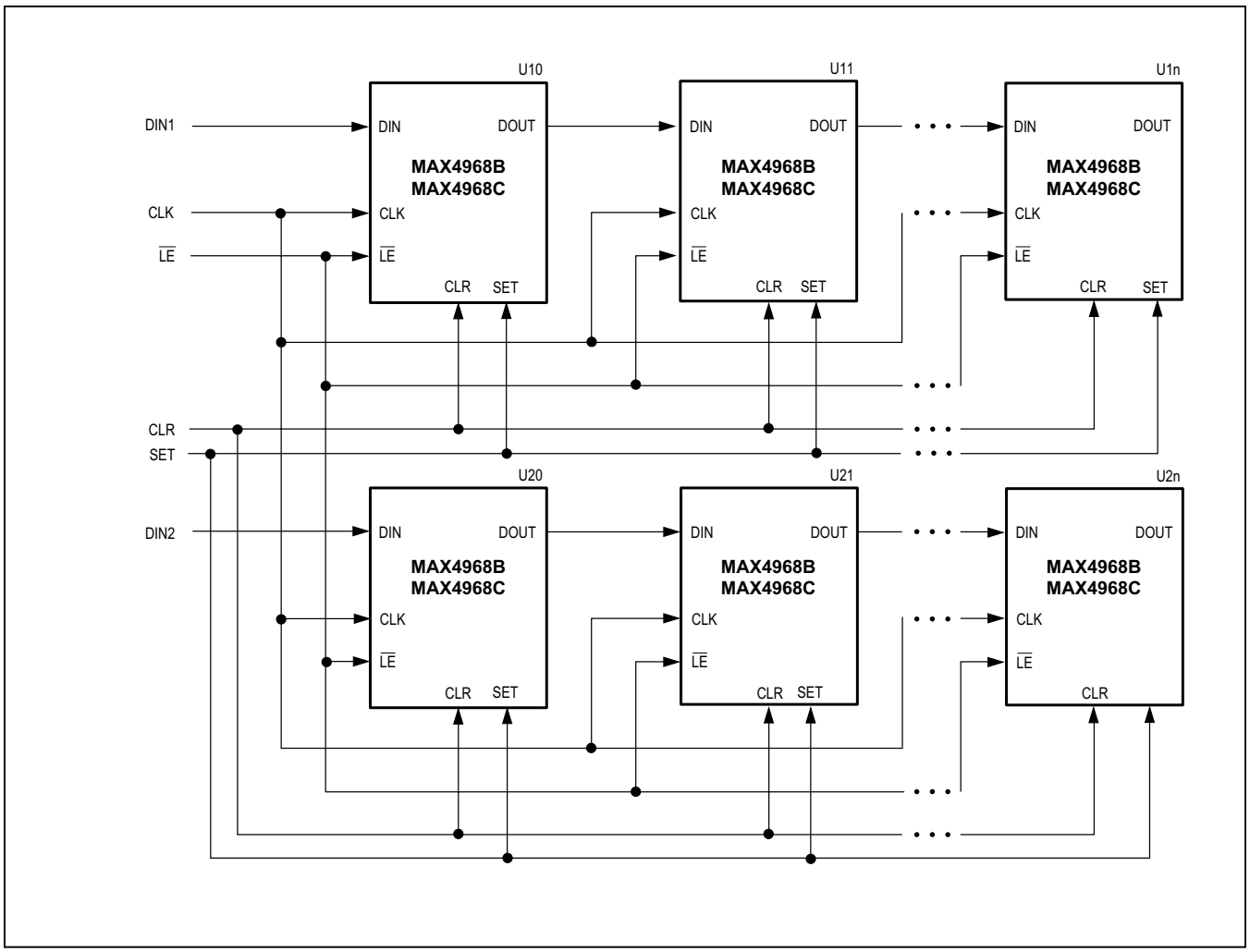
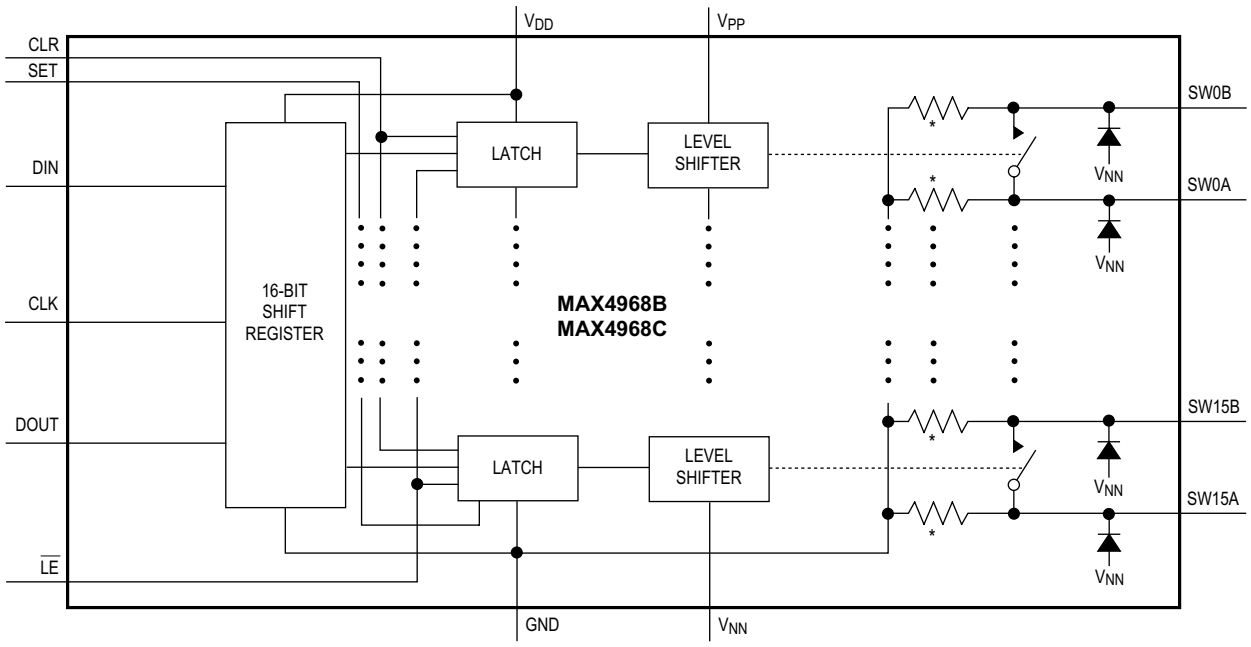


Figure 7. Interfacing Multiple Devices by Daisy-Chaining

Functional Diagram



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SWITCH CHANNELS	BLEED RESISTOR
MAX4968BEXB+	-40°C to +85°C	64 BGA (7mm x 7mm)	16	No
MAX4968CEXB+	-40°C to +85°C	64 BGA (7mm x 7mm)	16	Yes

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 BGA	X6477+2	21-0461	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—

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