



# 4A, 20ns, Dual MOSFET Drivers

MAX5054-MAX5057

## General Description

The MAX5054–MAX5057 dual, high-speed MOSFET drivers source and sink up to 4A peak current. These devices feature a fast 20ns propagation delay and 20ns rise and fall times while driving a 5000pF capacitive load. Propagation delay time is minimized and matched between the inverting and noninverting inputs and between channels. High sourcing/sinking peak currents, low propagation delay, and thermally enhanced packages make the MAX5054–MAX5057 ideal for high-frequency and high-power circuits.

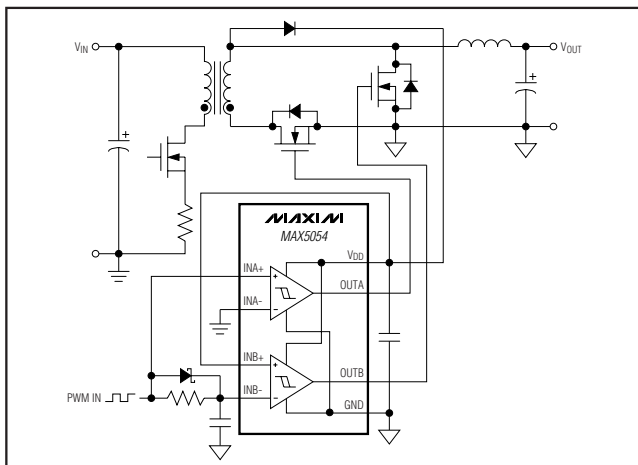
The MAX5054–MAX5057 operate from a 4V to 15V single power supply and consume 40 $\mu$ A (typ) of supply current when not switching. These devices have internal logic circuitry that prevents shoot-through during output state changes to minimize the operating current at high switching frequency. The logic inputs are protected against voltage spikes up to +18V, regardless of the  $V_{DD}$  voltage. The MAX5054A is the only version that has CMOS input logic levels while the MAX5054B/MAX5055/MAX5056/MAX5057 have TTL input logic levels.

The MAX5055–MAX5057 provide the combination of dual inverting, dual noninverting, and inverting/noninverting input drivers. The MAX5054 feature both inverting and noninverting inputs per driver for greater flexibility. They are available in 8-pin TDFN (3mm x 3mm), standard SO, and thermally enhanced SO packages. These devices operate over the automotive temperature range of -40°C to +125°C.

## Applications

Power MOSFET Switching      Motor Control  
Switch-Mode Power Supplies      Power-Supply Modules  
DC-DC Converters

## Typical Operating Circuit



## Features

- ◆ 4V to 15V Single Power Supply
- ◆ 4A Peak Source/Sink Drive Current
- ◆ 20ns (typ) Propagation Delay
- ◆ Matching Delay Between Inverting and Noninverting Inputs
- ◆ Matching Propagation Delay Between Two Channels
- ◆  $V_{DD} / 2$  CMOS Logic Inputs (MAX5054AATA)
- ◆ TTL Logic Inputs (MAX5054B/MAX5055/MAX5056/MAX5057)
- ◆  $0.1 \times V_{DD}$  (CMOS) and 0.3V (TTL) Logic-Input Hysteresis
- ◆ Up to +18V Logic Inputs (Regardless of  $V_{DD}$  Voltage)
- ◆ Low Input Capacitance: 2.5pF (typ)
- ◆ 40 $\mu$ A (typ) Quiescent Current
- ◆ -40°C to +125°C Operating Temperature Range
- ◆ 8-Pin TDFN and SO Packages

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX5054AATA+	-40°C to +125°C	8 TDFN-EP*	AGS
MAX5054AATA/V+	-40°C to +125°C	8 TDFN-EP*	BMF
MAX5054BATA+	-40°C to +125°C	8 TDFN-EP*	AGR
MAX5055AASA+	-40°C to +125°C	8 SO-EP*	—
MAX5055BASA+	-40°C to +125°C	8 SO	—
MAX5056AASA+	-40°C to +125°C	8 SO-EP*	—
MAX5056BASA+	-40°C to +125°C	8 SO	—
MAX5057AASA+	-40°C to +125°C	8 SO-EP*	—
MAX5057BASA+	-40°C to +125°C	8 SO	—

\*EP = Exposed pad.

N Denotes an automotive qualified part.

+ Denotes a lead (Pb)-free/RoHS-compliant package.

Selector Guide and Pin Configurations appear at end of data sheet.



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## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V <sub>DD</sub>	-0.3V to +18V
INA+, INA-, INB+, INB-	-0.3V to +18V
OUTA, OUTB	-0.3V to (V <sub>DD</sub> + 0.3V)
OUTA, OUTB Short-Circuit Duration	10ms
Continuous Source/Sink Current at OUT <sub>-</sub> (P <sub>D</sub> < P <sub>D</sub> MAX)	200mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
8-Pin TDFN-EP (derate 18.2mW/°C above +70°C)	1454mW

8-Pin SO-EP (derate 19.2mW/°C above +70°C)	1538mW
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

8 TDFN-EP

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> )	+41°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	+8°C/W

8 SO

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> )	+132°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	+40°C/W

8 SO-EP

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> )	+41°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	+7°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 4V to 15V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>DD</sub> = 15V and T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>							
V <sub>DD</sub> Operating Range	V <sub>DD</sub>			4		15	V
V <sub>DD</sub> Undervoltage Lockout	UVLO	V <sub>DD</sub> rising		3.00	3.50	3.85	V
V <sub>DD</sub> Undervoltage Lockout Hysteresis					200		mV
V <sub>DD</sub> Undervoltage Lockout to Output Delay		V <sub>DD</sub> rising			12		μs
V <sub>DD</sub> Supply Current	I <sub>DD</sub>	INA- = INB- = V <sub>DD</sub> , INA+ = INB+ = 0V (not switching)	V <sub>DD</sub> = 4V		28	55	μA
			V <sub>DD</sub> = 15V		40	75	
	I <sub>DD-SW</sub>	INA- = 0V, INB+ = V <sub>DD</sub> = 15V, INA+ = INB- both channels switching at 250kHz, C <sub>L</sub> = 0F		1	2.4	4	mA
<b>DRIVER OUTPUT (SINK)</b>							
Driver Output Resistance Pulling Down	R <sub>ON-N</sub>	V <sub>DD</sub> = 15V, I <sub>OUT-</sub> = -100mA	T <sub>A</sub> = +25°C		1.1	1.8	Ω
			T <sub>A</sub> = +125°C		1.5	2.4	
		V <sub>DD</sub> = 4.5V, I <sub>OUT-</sub> = -100mA	T <sub>A</sub> = +25°C		2.2	3.3	
			T <sub>A</sub> = +125°C		3.0	4.5	
Peak Output Current (Sinking)	I <sub>PK-N</sub>	V <sub>DD</sub> = 15V, C <sub>L</sub> = 10,000pF			4		A
Output-Voltage Low		I <sub>OUT-</sub> = -100mA	V <sub>DD</sub> = 4.5V			0.45	V
			V <sub>DD</sub> = 15V			0.24	
Latchup Protection	I <sub>LUP</sub>	Reverse current I <sub>OUT-</sub> (Note 2)		400			mA

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 4V$  to  $15V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{DD} = 15V$  and  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DRIVER OUTPUT (SOURCE)</b>						
Driver Output Resistance Pulling Up	$R_{ON-P}$	$V_{DD} = 15V$ , $I_{OUT\_} = 100mA$	$T_A = +25^{\circ}C$	1.5	2.1	$\Omega$
			$T_A = +125^{\circ}C$	1.9	2.75	
		$V_{DD} = 4.5V$ , $I_{OUT\_} = 100mA$	$T_A = +25^{\circ}C$	2.75	4	
			$T_A = +125^{\circ}C$	3.75	5.5	
Peak Output Current (Sourcing)	$I_{PK-P}$	$V_{DD} = 15V$ , $C_L = 10,000pF$		4		A
Output-Voltage High		$I_{OUT\_} = 100mA$	$V_{DD} = 4.5V$	$V_{DD} - 0.55$		V
			$V_{DD} = 15V$	$V_{DD} - 0.275$		
<b>LOGIC INPUT (Note 4)</b>						
Logic 1 Input Voltage	$V_{IH}$	MAX5054A	$0.7 \times V_{DD}$			V
		MAX5054B/MAX5055/MAX5056/MAX5057 (Note 5)	2.1			
Logic 0 Input Voltage	$V_{IL}$	MAX5054A		$0.3 \times V_{DD}$		V
		MAX5054B/MAX5055/MAX5056/MAX5057		0.8		
Logic-Input Hysteresis	$V_{HYS}$	MAX5054A	$0.1 \times V_{DD}$			V
		MAX5054B/MAX5055/MAX5056/MAX5057	0.3			
Logic-Input-Current Leakage		INA+, INB+, INA-, INB- = 0V or $V_{DD}$	-1	+0.1	+1	$\mu A$
Input Capacitance	$C_{IN}$			2.5		pF
<b>SWITCHING CHARACTERISTICS FOR <math>V_{DD} = 15V</math> (Figure 1)</b>						
OUT_ Rise Time	$t_R$	$C_L = 1000pF$	4			ns
		$C_L = 5000pF$	18			
		$C_L = 10,000pF$	32			
OUT_ Fall Time	$t_F$	$C_L = 1000pF$	4			ns
		$C_L = 5000pF$	15			
		$C_L = 10,000pF$	26			
Turn-On Delay Time	$t_{D-ON}$	$C_L = 10,000pF$ (Note 3)	10	20	34	ns
Turn-Off Delay Time	$t_{D-OFF}$	$C_L = 10,000pF$ (Note 3)	10	20	34	ns
<b>SWITCHING CHARACTERISTICS FOR <math>V_{DD} = 4.5V</math> (Figure 1)</b>						
OUT_ Rise Time	$t_R$	$C_L = 1000pF$	7			ns
		$C_L = 5000pF$	37			
		$C_L = 10,000pF$	85			
OUT_ Fall Time	$t_F$	$C_L = 1000pF$	7			ns
		$C_L = 5000pF$	30			
		$C_L = 10,000pF$	75			
Turn-On Delay Time	$t_{D-ON}$	$C_L = 10,000pF$ (Note 3)	18	35	70	ns
Turn-Off Delay Time	$t_{D-OFF}$	$C_L = 10,000pF$ (Note 3)	18	35	70	ns

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 4V$  to  $15V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $V_{DD} = 15V$  and  $T_A = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>MATCHING CHARACTERISTICS</b>						
Mismatch Propagation Delays from Inverting and Noninverting Inputs to Output	$\Delta t_{ON-OFF}$	$V_{DD} = 15V, C_L = 10,000pF$		2		ns
		$V_{DD} = 4.5V, C_L = 10,000pF$		4		
Mismatch Propagation Delays Between Channel A and Channel B	$\Delta t_{A-B}$	$V_{DD} = 15V, C_L = 10,000pF$		1		ns
		$V_{DD} = 4.5V, C_L = 10,000pF$		2		

**Note 2:** All devices are 100% tested at  $T_A = +25^\circ C$ . Specifications over  $-40^\circ C$  to  $+125^\circ C$  are guaranteed by design.

**Note 3:** Limits are guaranteed by design, not production tested.

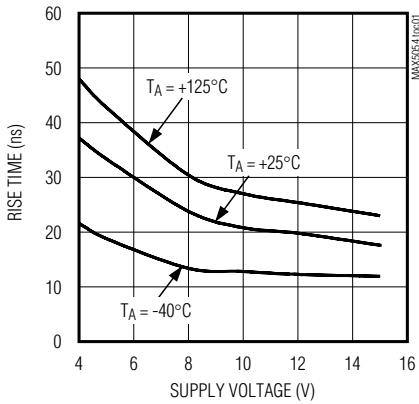
**Note 4:** The logic-input thresholds are tested at  $V_{DD} = 4V$  and  $V_{DD} = 15V$ .

**Note 5:** TTL compatible with reduced noise immunity.

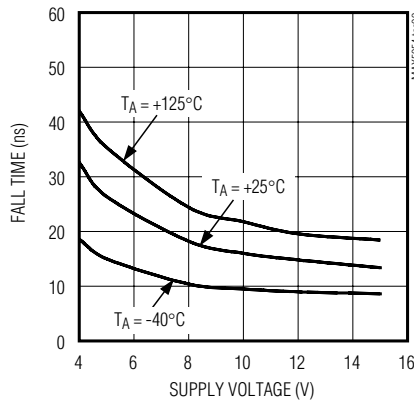
## Typical Operating Characteristics

( $T_A = +25^\circ C$ , unless otherwise noted.)

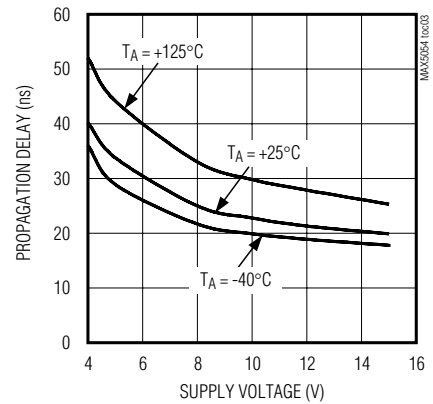
**RISE TIME vs. SUPPLY VOLTAGE**  
( $C_L = 5000pF$ )



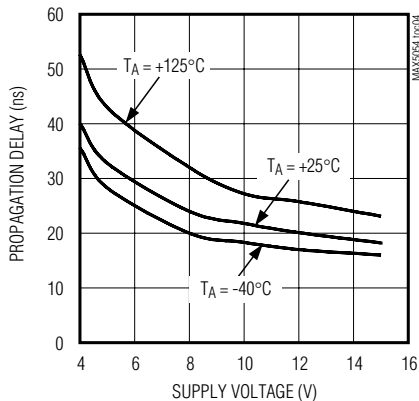
**FALL TIME vs. SUPPLY VOLTAGE**  
( $C_L = 5000pF$ )



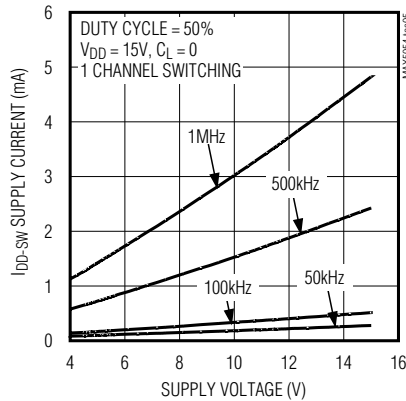
**PROPAGATION DELAY TIME, LOW-TO-HIGH vs. SUPPLY VOLTAGE**  
( $C_L = 5000pF$ )



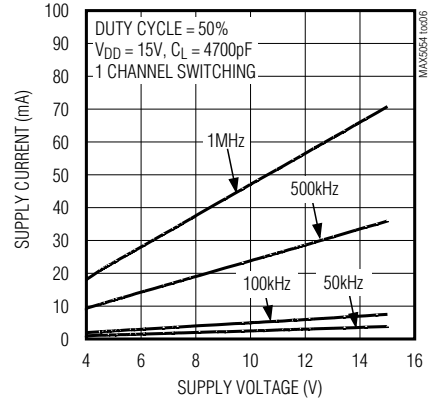
**PROPAGATION DELAY TIME, HIGH-TO-LOW vs. SUPPLY VOLTAGE**  
( $C_L = 5000pF$ )



**$I_{DD-SW}$  SUPPLY CURRENT vs. SUPPLY VOLTAGE**



**SUPPLY CURRENT vs. SUPPLY VOLTAGE**

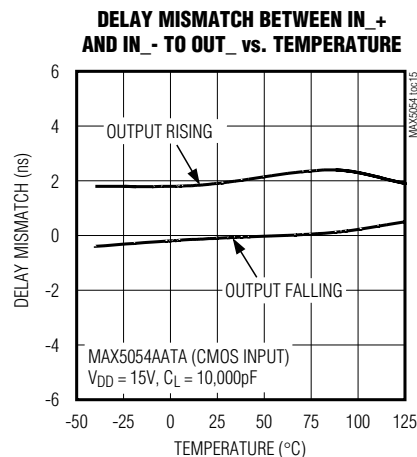
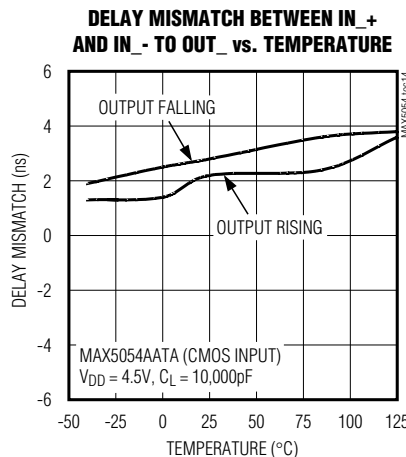
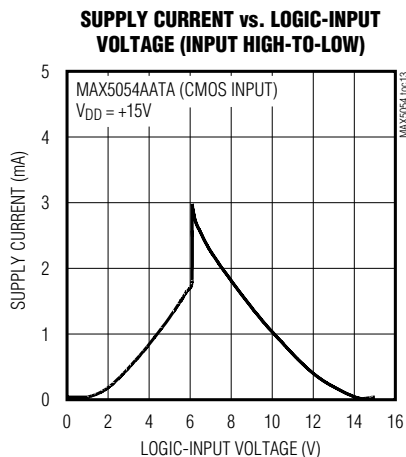
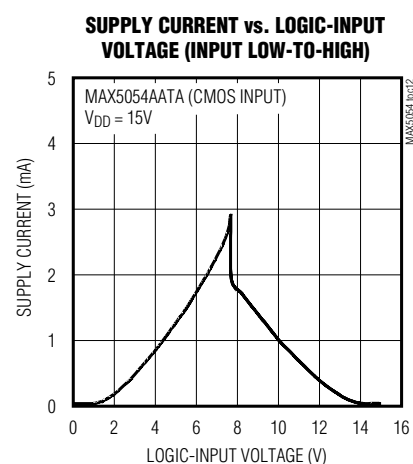
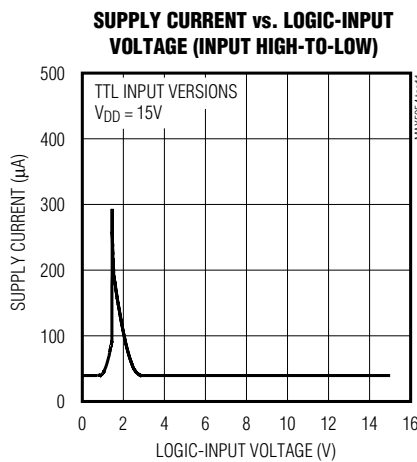
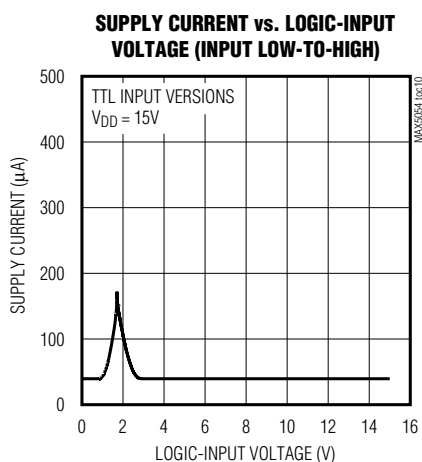
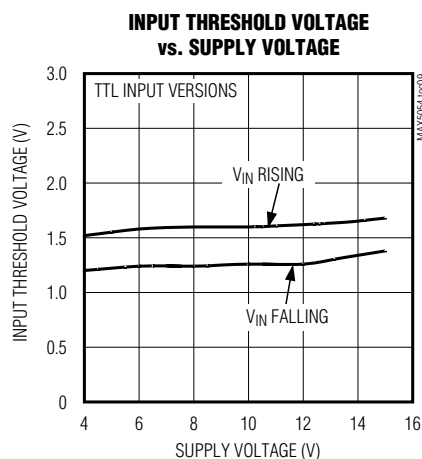
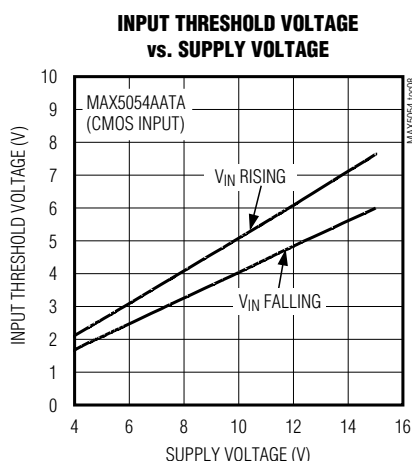
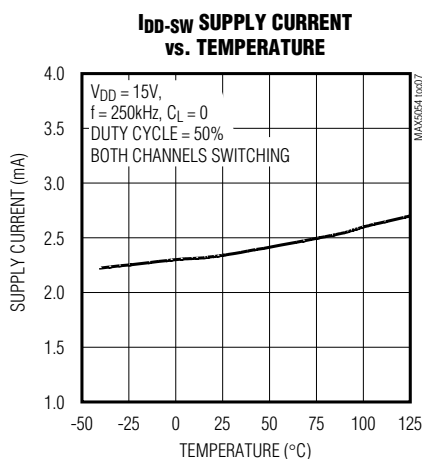


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## Typical Operating Characteristics (continued)

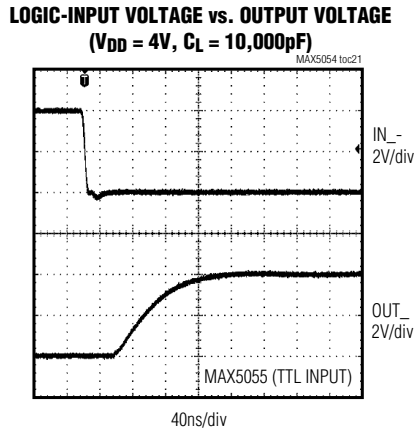
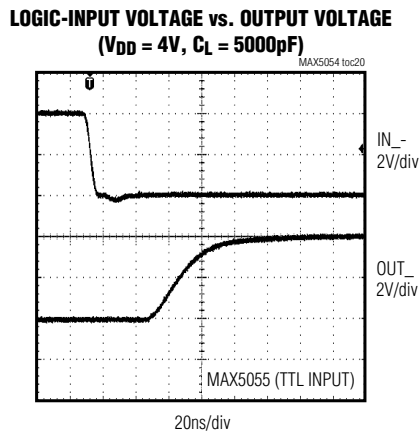
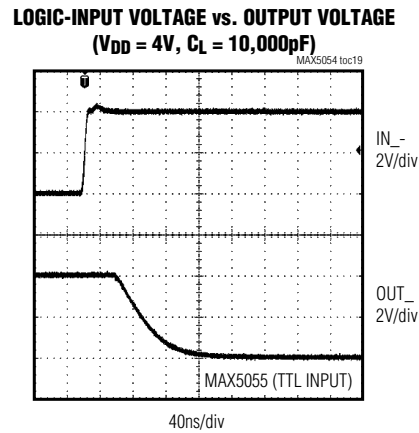
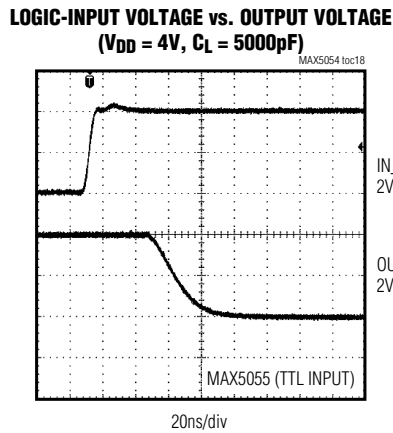
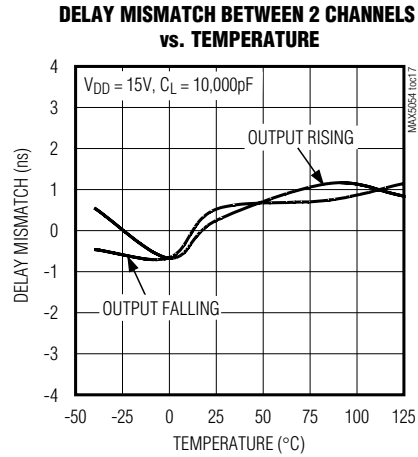
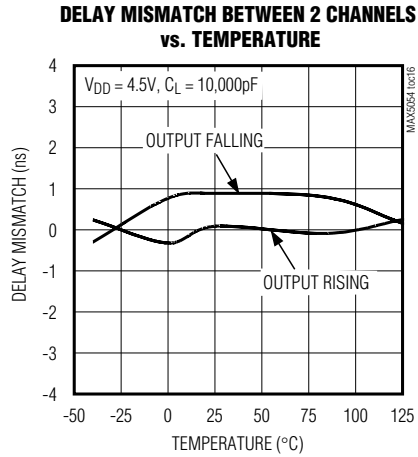
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# 4A, 20ns, Dual MOSFET Drivers

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



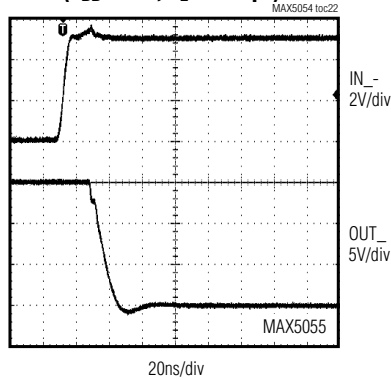
# 4A, 20ns, Dual MOSFET Drivers

## Typical Operating Characteristics (continued)

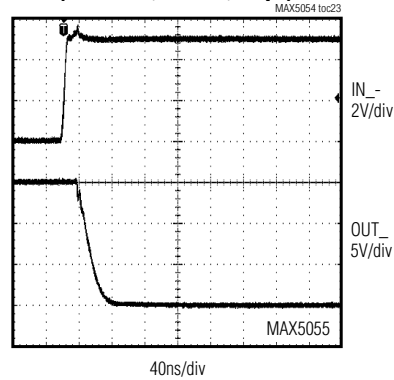
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MAX5054-MAX5057

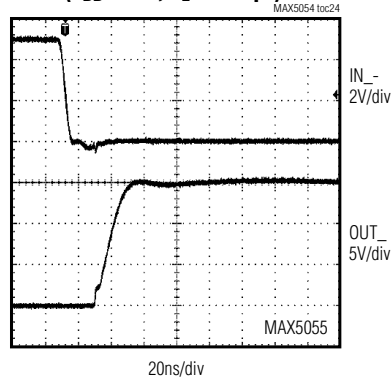
**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_{DD} = 15\text{V}$ ,  $C_L = 5000\text{pF}$ )



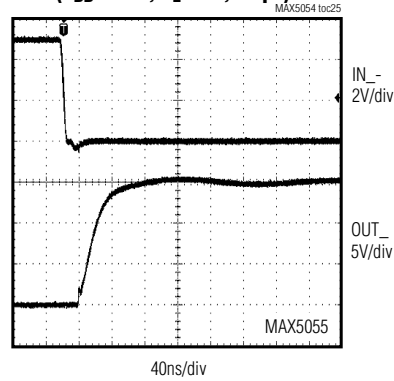
**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_{DD} = 15\text{V}$ ,  $C_L = 10,000\text{pF}$ )



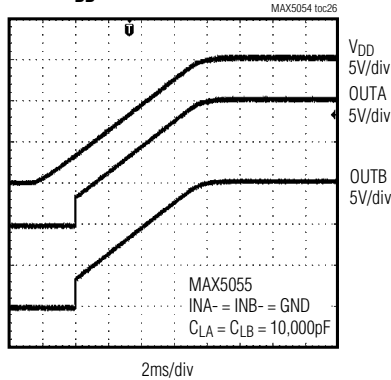
**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_{DD} = 15\text{V}$ ,  $C_L = 5000\text{pF}$ )



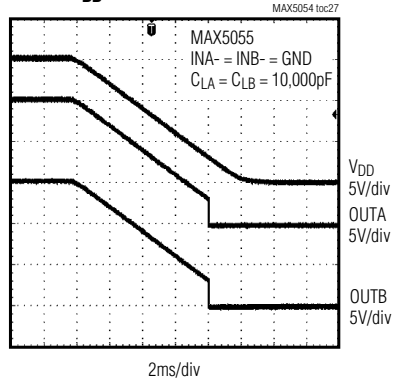
**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_{DD} = 15\text{V}$ ,  $C_L = 10,000\text{pF}$ )



**$V_{DD}$  vs. OUTPUT VOLTAGE**



**$V_{DD}$  vs. OUTPUT VOLTAGE**



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## Pin Descriptions

### MAX5054

PIN	NAME	FUNCTION
1	INA-	Inverting Logic-Input Terminal for Driver A. Connect to GND when not used.
2	INB-	Inverting Logic-Input Terminal for Driver B. Connect to GND when not used.
3	GND	Ground
4	OUTB	Driver B Output. Sources or sinks current for channel B to turn the external MOSFET on or off.
5	V <sub>DD</sub>	Power Supply. Bypass to GND with one or more 0.1μF ceramic capacitors.
6	OUTA	Driver A Output. Sources or sinks current for channel A to turn the external MOSFET on or off.
7	INB+	Noninverting Logic-Input Terminal for Driver B. Connect to V <sub>DD</sub> when not used.
8	INA+	Noninverting Logic-Input Terminal for Driver A. Connect to V <sub>DD</sub> when not used.
—	EP	Exposed Pad. Internally connected to GND. Do not use the exposed pad as the only electrical ground connection.

### MAX5055/MAX5056/MAX5057

PIN			NAME	FUNCTION
MAX5055	MAX5056	MAX5057		
1, 8	1, 8	1, 8	N.C.	No Connection. Not internally connected.
2	—	2	INA-	Inverting Logic-Input Terminal for Driver A. Connect to GND if not used.
3	3	3	GND	Ground
4	—	—	INB-	Inverting Logic-Input Terminal for Driver B. Connect to GND if not used.
5	5	5	OUTB	Driver B Output. Sources or sinks current for channel B to turn the external MOSFET on or off.
6	6	6	V <sub>DD</sub>	Power Supply. Bypass to GND with one or more 0.1μF ceramic capacitors.
7	7	7	OUTA	Driver A Output. Sources or sinks current for channel A to turn the external MOSFET on or off.
—	4	4	INB+	Noninverting Logic-Input Terminal for Driver B. Connect to V <sub>DD</sub> if not used.
—	2	—	INA+	Noninverting Logic-Input Terminal for Driver A. Connect to V <sub>DD</sub> if not used.
—	—	—	EP	Exposed Pad. Internally connected to GND. Do not use the exposed pad as the only electrical ground connection.



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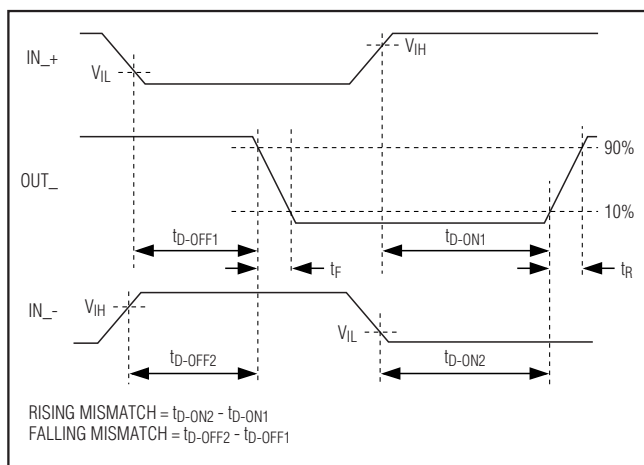


Figure 1. Timing Diagram

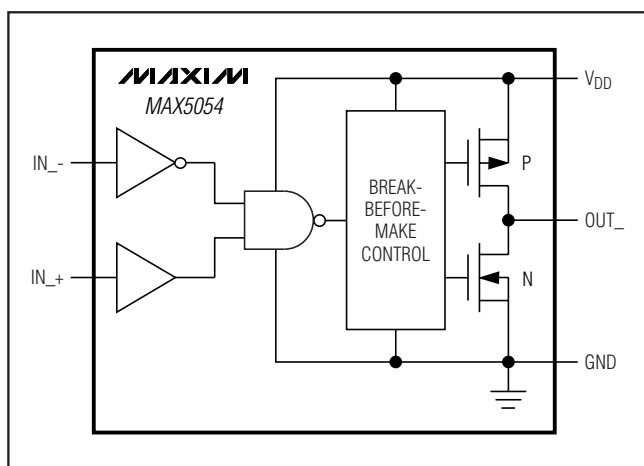


Figure 2. MAX5054 Block Diagram (1 Driver)

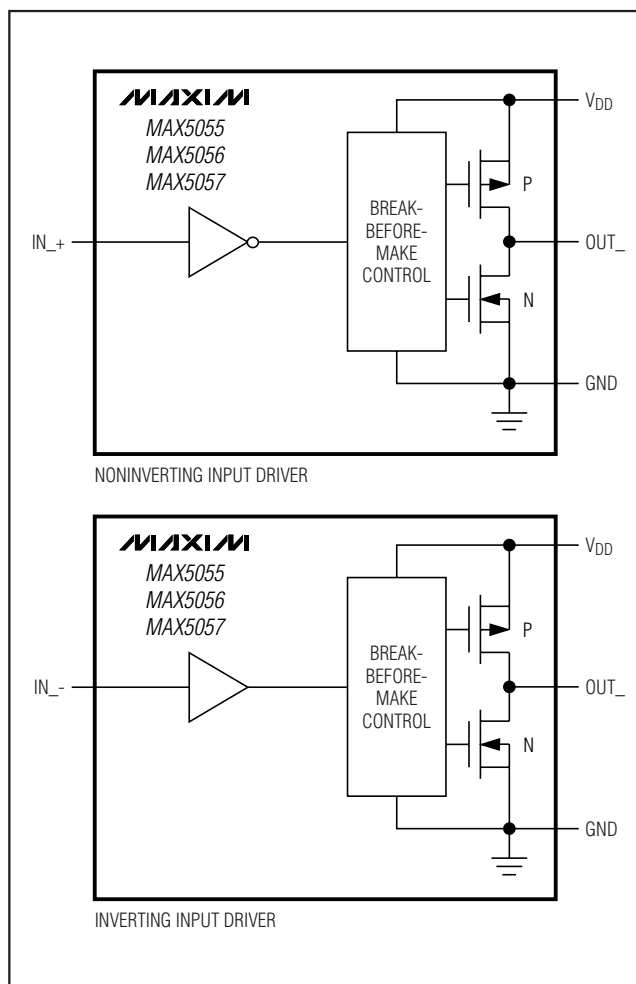


Figure 3. MAX5055/MAX5056/MAX5057 Functional Diagrams (1 Driver)

## Detailed Description

### V<sub>DD</sub> Undervoltage Lockout (UVLO)

The MAX5054–MAX5057 have internal undervoltage lockout for V<sub>DD</sub>. When V<sub>DD</sub> is below the UVLO threshold, OUT<sub>-</sub> is low, independent of the state of the inputs. The undervoltage lockout is typically 3.5V with 200mV typical hysteresis to avoid chattering. When V<sub>DD</sub> rises above the UVLO threshold, the outputs go high or low depending upon the logic-input levels. Bypass V<sub>DD</sub> using low-ESR ceramic capacitors for proper operation (see the *Applications Information* section).

### Logic Inputs

The MAX5054B–MAX5057 have TTL-compatible logic inputs, while the MAX5054A is a CMOS logic-input driver. The logic-input signals can be independent of the V<sub>DD</sub> voltage. For example, the device can be powered by a 5V supply while the logic inputs are provided from CMOS logic. Also, the logic inputs are protected against the voltage spikes up to 18V, regardless of the V<sub>DD</sub> voltage. The TTL and CMOS logic inputs have 300mV and 0.1 × V<sub>DD</sub> hysteresis, respectively, to avoid possible double pulsing during transition. The low 2.5pF input capacitance reduces loading and increases switching speed.

## 4A, 20ns, Dual MOSFET Drivers

Table 1. MAX5054 Truth Table

INA+/INB+	INA-/INB-	OUTA/OUTB
Low	Low	Low
Low	High	Low
High	Low	High
High	High	Low

Table 2. MAX5055/MAX5056/MAX5057 Truth Table

NONINVERTING	
IN_+	OUT_
Low	Low
High	High
INVERTING	
IN_-	OUT_
Low	High
High	Low

The logic inputs are high impedance and must not be left floating. If the inputs are left open, OUT\_ can go to an undefined state as soon as V<sub>DD</sub> rises above the UVLO threshold. Therefore, the PWM output from the controller must assume proper state when powering up the device.

The MAX5054 has two logic inputs per driver providing greater flexibility in controlling the MOSFET. Use IN\_+ for noninverting logic and IN\_- for inverting logic operation. Connect IN\_+ to V<sub>DD</sub> and IN\_- to GND if not used. Alternatively, the unused input can be used as an ON/OFF function. Use IN\_+ for active-low shutdown logic and IN\_- for active-high shutdown logic (see Figure 4). See Table 1 for all possible input combinations.

### Driver Output

The MAX5054–MAX5057 have low R<sub>DS(ON)</sub> p-channel and n-channel devices (totem pole) in the output stage for the fast turn-on and turn-off high gate-charge switching MOSFETs. The peak source or sink current is typically 4A. The OUT\_ voltage is approximately equal to V<sub>DD</sub> when in high state and is ground when in low state. The driver R<sub>DS(ON)</sub> is lower at higher V<sub>DD</sub>, thus higher source-/sink-current capability and faster switching speeds. The propagation delays from the noninverting and inverting logic inputs to outputs are matched to 2ns. The break-before-make logic avoids any cross-conduction between the internal p- and n-channel devices, and eliminates shoot-through currents reducing the quiescent supply current.

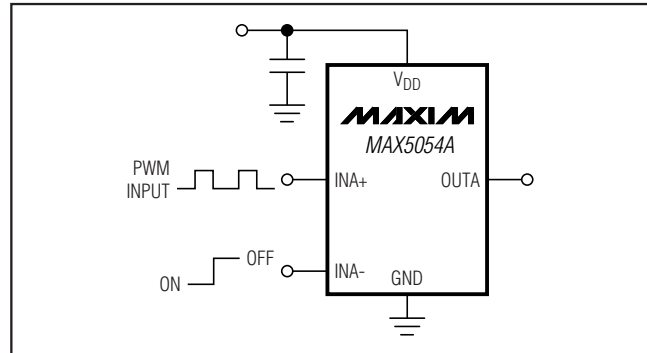


Figure 4. Unused Input as an ON/OFF Function (1/2 MAX5054A)

## Applications Information

### RLC Series Circuit

The driver's R<sub>DS(ON)</sub> (R<sub>ON</sub>), internal bond and lead inductance (L<sub>P</sub>), trace inductance (L<sub>S</sub>), gate inductance (L<sub>G</sub>), and gate capacitance (C<sub>G</sub>) form a series RLC circuit with a second-order characteristic equation. The series RLC circuit has an undamped natural frequency ( $\omega_0$ ) and a damping ratio ( $\xi$ ) where:

$$\omega_0 = \frac{1}{\sqrt{(L_P + L_S + L_G) \times C_G}}$$

$$\xi = \frac{R_{ON}}{2 \times \sqrt{\frac{(L_P + L_S + L_G)}{C_G}}}$$

The damping ratio needs to be greater than 0.5 (ideally 1) to avoid ringing. Add a small resistor (R<sub>GATE</sub>) in series with the gate when driving a very low gate-charge MOSFET, or when the driver is placed away from the MOSFET. Use the following equation to calculate the series resistor:

$$R_{GATE} \geq \sqrt{\frac{(L_P + L_S + L_G)}{C_G}} - R_{ON}$$

L<sub>P</sub> can be approximated as 3nH and 2nH for SO and TDFN packages, respectively. L<sub>S</sub> is on the order of 20nH/in. Verify L<sub>G</sub> with the MOSFET vendor.

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## Supply Bypassing and Grounding

Pay extra attention to bypassing and grounding the MAX5054–MAX5057. Peak supply and output currents may exceed 8A when both drivers drive large external capacitive loads in phase. Supply voltage drops and ground shifts create forms of negative feedback for inverters and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the  $V_{DD}$ ,  $OUT_{-}$ , and/or GND paths can cause oscillations due to the very high  $di/dt$  when switching the MAX5054–MAX5057 with any capacitive load. Place one or more 0.1 $\mu$ F ceramic capacitors in parallel as close to the device as possible to bypass  $V_{DD}$  to GND. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFET as close as possible to the MAX5054–MAX5057 to further minimize board inductance and AC path impedance.

## Power Dissipation

Power dissipation of the MAX5054–MAX5057 consists of three components: caused by the quiescent current, capacitive charge/discharge of internal nodes, and the output current (either capacitive or resistive load). Maintain the sum of these components below the maximum power dissipation limit.

The current required to charge and discharge the internal nodes is frequency dependent (see the Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*). The power dissipation ( $P_Q$ ) due to the quiescent switching supply current ( $I_{DD-SW}$ ) per driver can be calculated as:

$$P_Q = V_{DD} \times I_{DD-SW}$$

For capacitive loads, use the following equation to estimate the power dissipation per driver:

$$P_{CLOAD} = C_{LOAD} \times (V_{DD})^2 \times f_{SW}$$

where  $C_{LOAD}$  is the capacitive load,  $V_{DD}$  is the supply voltage, and  $f_{SW}$  is the switching frequency.

Calculate the total power dissipation ( $P_T$ ) per driver as follows:

$$P_T = P_Q + P_{CLOAD}$$

Use the following equation to estimate the MAX5054–MAX5057 total power dissipation per driver when driving a ground-referenced resistive load:

$$P_T = P_Q + P_{RLOAD}$$
$$P_{RLOAD} = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where  $D$  (duty cycle) is the fraction of the period the MAX5054–MAX5057's output pulls high duty cycle,  $R_{ON(MAX)}$  is the maximum on-resistance of the device with the output high, and  $I_{LOAD}$  is the output load current of the MAX5054–MAX5057.

## Layout Information

The MAX5054–MAX5057 MOSFET drivers source and sink large currents to create very fast rising and falling edges at the gate of the switching MOSFET. The high  $di/dt$  can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5054–MAX5057:

- Place one or more 0.1 $\mu$ F decoupling ceramic capacitors from  $V_{DD}$  to GND as close to the device as possible. Connect  $V_{DD}$  and GND to large copper areas. Place one bulk capacitor of 10 $\mu$ F (min) on the PC board with a low resistance path to the  $V_{DD}$  input and GND of the MAX5054–MAX5057.
- Two AC current loops form between the device and the gate of the driven MOSFET. The MOSFET looks like a large capacitance from gate to source when the gate pulls low. The active current loop is from the MOSFET gate to  $OUT_{-}$  of the MAX5054–MAX5057, to GND of the MAX5054–MAX5057, and to the source of the MOSFET. When the gate of the MOSFET pulls high, the active current is from the  $V_{DD}$  terminal of the decoupling capacitor, to  $V_{DD}$  of the MAX5054–MAX5057, to  $OUT_{-}$  of the MAX5054–MAX5057, to the MOSFET gate, to the MOSFET source, and to the negative terminal of the decoupling capacitor. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.
- In a multilayer PC board, the inner layers should consist of a GND plane containing the discharging and charging current loops.
- Pay extra attention to the ground loop and use a low-impedance source when using a TTL logic-input device. Fast fall time at  $OUT_{-}$  may corrupt the input during transition.

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### Exposed Pad

Both the SO-EP and TDFN-EP packages have an exposed pad on the bottom of their package. These pads are internally connected to GND. For the best thermal conductivity, solder the exposed pad to the

ground plane to dissipate 1.5W and 1.9W in SO-EP and TDFN-EP packages, respectively. Do not use the ground-connected pads as the only electrical ground connection or ground return. Use GND (pin 3) as the primary electrical ground connection.

### Additional Application Circuits

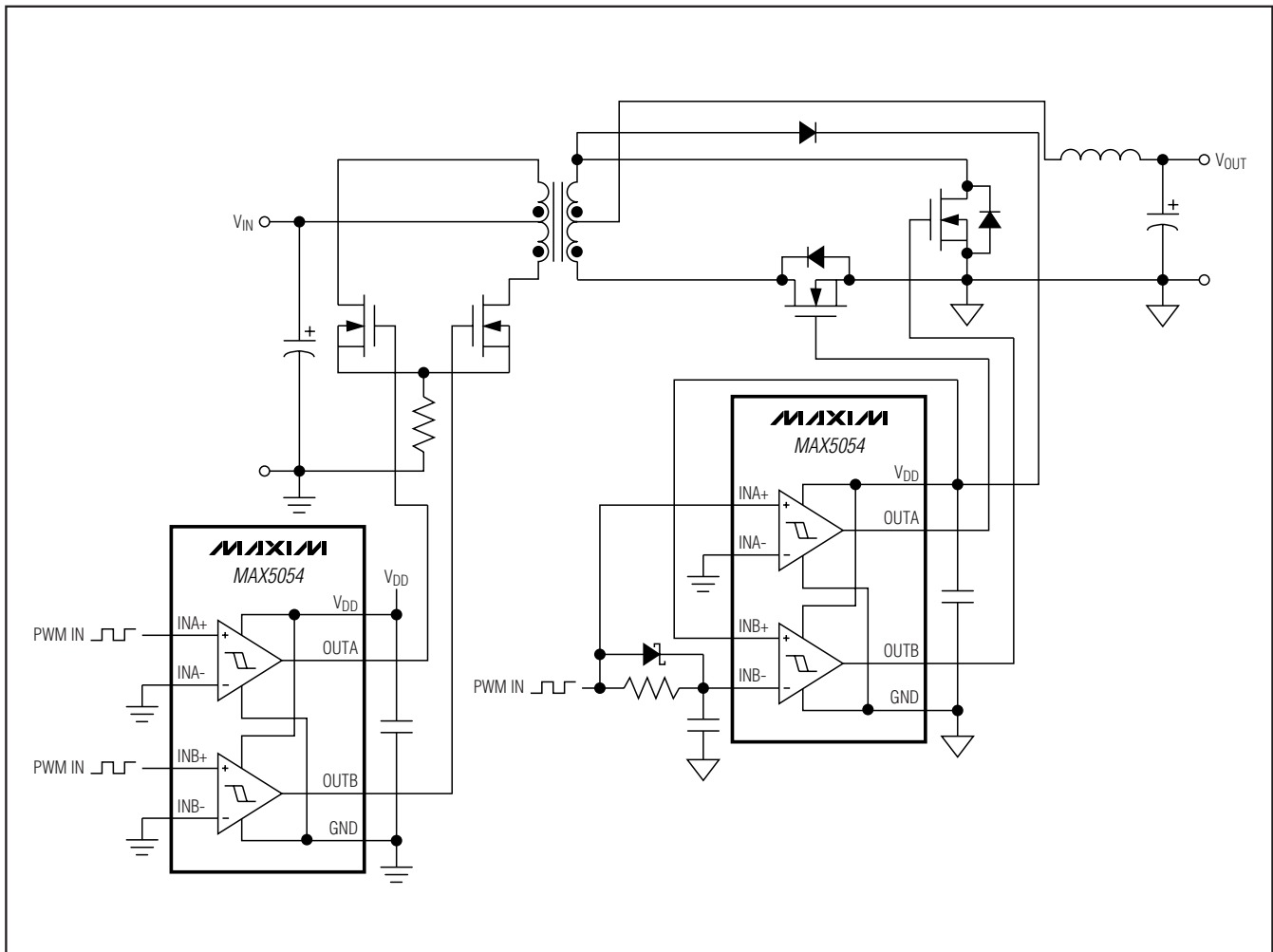


Figure 5. Push-Pull Converter with Synchronous Rectification Drive Using MAX5054

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MAX5054-MAX5057

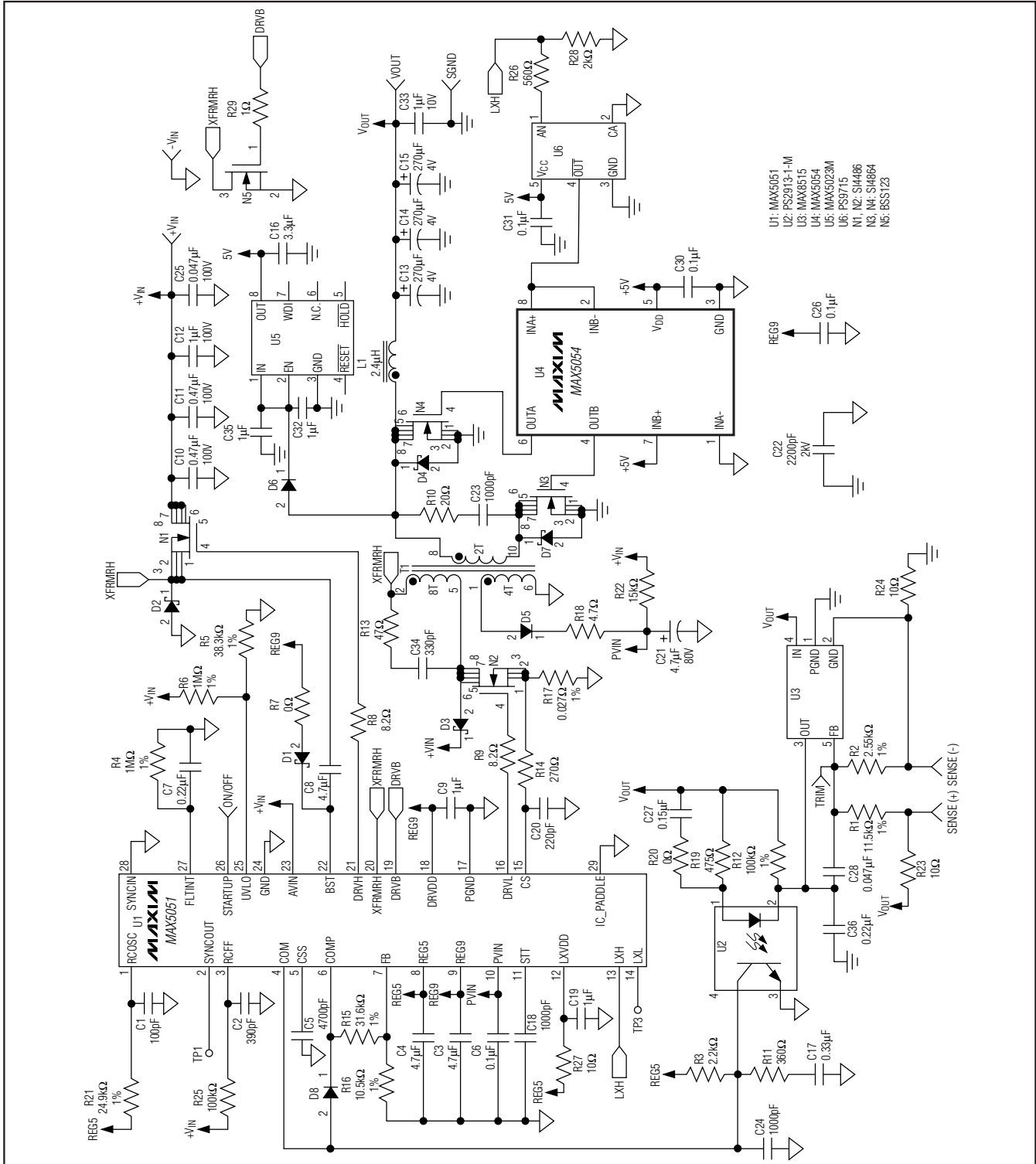
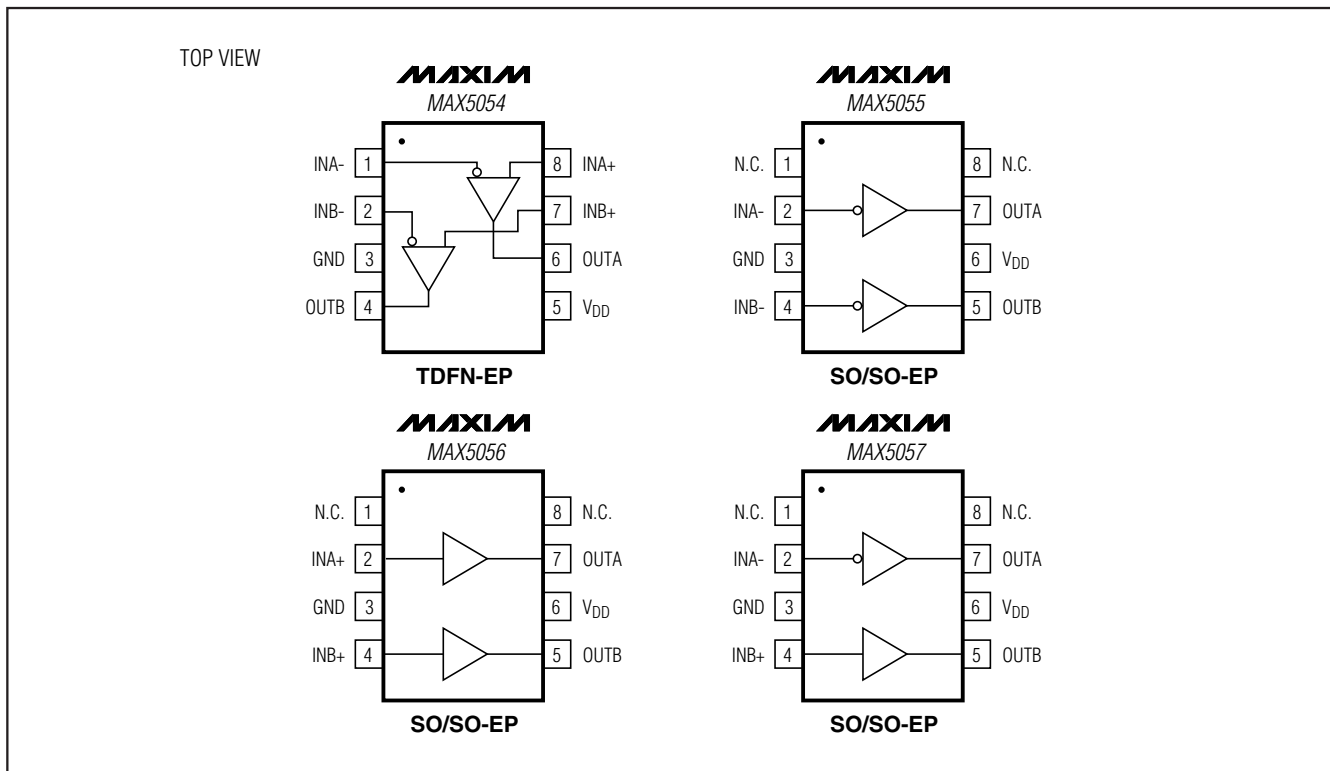


Figure 6. Schematic of a 48V Input, 3.3V at 15A Output Synchronously Rectified, Isolated Power Supply

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## Pin Configurations



## Selector Guide

PART	PIN-PACKAGE	LOGIC INPUT
MAX5054AATA	8 TDFN-EP*	V <sub>DD</sub> / 2 CMOS Dual Inverting and Dual Noninverting Inputs
MAX5054BATA	8 TDFN-EP*	TTL Dual Inverting and Dual Noninverting Inputs
MAX5055AASA	8 SO-EP*	TTL Dual Inverting Inputs
MAX5055BASA	8 SO	TTL Dual Inverting Inputs
MAX5056AASA	8 SO-EP*	TTL Dual Noninverting Inputs
MAX5056BASA	8 SO	TTL Dual Noninverting Inputs
MAX5057AASA	8 SO-EP*	TTL Inverting and Noninverting Inputs
MAX5057BASA	8 SO	TTL Inverting and Noninverting Inputs

\*EP = Exposed pad.

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T833+2	<a href="#">21-0137</a>	<a href="#">90-0059</a>
8 SO-EP	S8E+14	<a href="#">21-0111</a>	<a href="#">90-0151</a>
8 SO	S8+4	<a href="#">21-0041</a>	<a href="#">90-0096</a>