MAX5386/MAX5388

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

General Description

The MAX5386/MAX5388 dual, 256-tap, volatile, low- voltage linear taper digital potentiometers offer three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. Operating from a single +2.6V to +5.5V power supply these devices provide a low 35ppm/°C end-to-end temperature coefficient. The devices feature an SPI interface.

The small package size, low supply voltage, low supply current, and automotive temperature range of the MAX5386/MAX5388 make the devices uniquely suitable for the portable consumer market and battery-backup industrial applications.

The MAX5386 includes two digital potentiometers in a voltage-divider configuration. The MAX5388 includes one digital potentiometer in a voltage-divider configuration and one digital potentiometer in a variable-resistor configuration. The MAX5386/MAX5388 are specified over an extended -40°C to +125°C temperature range and are available in 16-pin, 3mm x 3mm TQFN or 10-pin, 3mm x 5mm µMAX® packages, respectively.

Applications

- Low-Voltage Battery Applications
- Portable Electronics
- Mechanical Potentiometer Replacement
- Offset and Gain Control
- Adjustable Voltage References/Linear Regulators

Functional Diagrams appear at end of data sheet.

Features

- Dual, 256-Tap, Linear Taper Positions
- Single +2.6V to +5.5V Supply Operation
- Low (< 1µA) Quiescent Supply Current
- 10kΩ, 50kΩ, 100kΩ End-to-End Resistance Values
- SPI-Compatible Interface
- Power-On Sets Wiper to Midscale
- -40°C to +125°C Operating Temperature Range

Ordering Information

PART	PIN-PACKAGE	END-TO-END RESISTANCE (kΩ)
MAX5386LATE+	16 TQFN-EP*	10
MAX5386MATE+	16 TQFN-EP*	50
MAX5386NATE+	16 TQFN-EP*	100
MAX5388LAUB+	10 µMAX	10
MAX5388MAUB+	10 µMAX	50
MAX5388NAUB+	10 µMAX	100

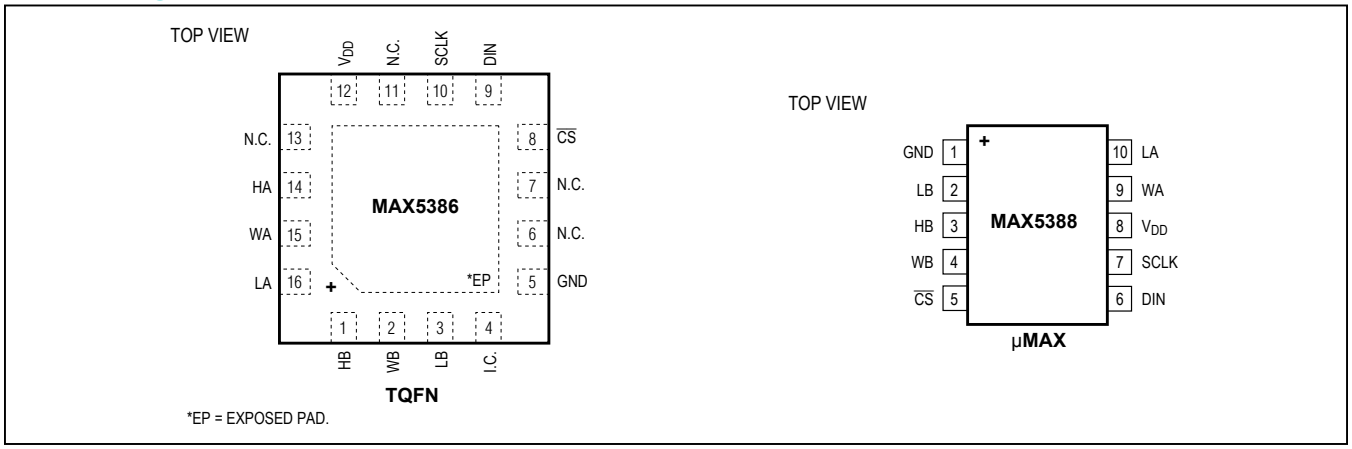
Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Pin Configurations



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND.....-0.3V to +6V
H_, W_, L_ to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +6V
All Other Pins to GND.....-0.3V to +6V
Continuous Current in to H_, W_, and L_
MAX5386L/MAX5388L..... ±5mA
MAX5386M/MAX5388M.....±2mA
MAX5386N/MAX5388N.....±1mA

Continuous Power Dissipation (T_A = +70°C)
16 TQFN (derate 14.7mW/°C above+70°C).....1176.5mW
10 µMAX (derate 8.8mW/°C above+70°C).....707.3mW
Operating Temperature Range.....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +2.6V to +5.5V, $V_{H\_}$ = V_{DD}, $V_{L\_}$ = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25˚C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution	N			256			Tap
DC PERFORMANCE (VOLTAGE-DIVIDER MODE)							
Integral Nonlinearity	INL	(Note 2)		-0.5		+0.5	LSB
Differential Nonlinearity	DNL	(Note 2)		-0.5		+0.5	LSB
Dual Code Matching		Register A = register B		-0.5		+0.5	LSB
Ratiometric Resistor Tempco		($\Delta V_W/V_W$)/ΔT no load			±5		ppm/°C
Full-Scale Error		Code = FFH	MAX5386L/MAX5388L	-3.0	-2.5		LSB
			MAX5386M/MAX5388M	-1.0	-0.5		
			MAX5386N/MAX5388N	-0.5	-0.25		
Zero-Scale Error		Code = 00H	MAX5386L/MAX5388L		2.5	3.0	LSB
			MAX5386M/MAX5388M		+0.5	+1.0	
			MAX5386N/MAX5388N		+0.25	+0.5	
DC PERFORMANCE (VARIABLE-RESISTOR MODE) (Note 3)							
Integral Nonlinearity	R-INL	V_{DD} > +2.6V	MAX5386L/MAX5388L		±1.0	±2.5	LSB
			MAX5386M/MAX5388M		±0.5	±1.0	
			MAX5386N/MAX5388N		±0.25	±0.8	
		V_{DD} > +4.75V	MAX5386L/MAX5388L		±0.4	±1.5	
			MAX5386M/MAX5388M		±0.3	±0.75	
			MAX5386N/MAX5388N		±0.25	±0.5	
Differential Nonlinearity	R-DNL	V_{DD} ≥ 2.6V		-0.5		+0.5	LSB
DC PERFORMANCE (RESISTOR CHARACTERISTICS)							
Wiper Resistance (Note 4)	R_W	V_{DD} ≥ 2.6V			250	600	Ω
		V_{DD} > 4.75V			150	200	
Terminal Capacitance	$C_{H\_}$, $C_{L\_}$	Measured to GND			10		pF
Wiper Capacitance	$C_{W\_}$	Measured to GND			50		pF
End-to-End Resistor Tempco	TC_R	No load			35		ppm/°C
End-to-End Resistor Tolerance	ΔR_{HL}	Wiper not connected		-25		+25	%
AC PERFORMANCE							
Crosstalk		(Note 5)			-90		dB
-3dB Bandwidth	BW	Code = 80H, 10pF load, V_{DD} = +2.6V	MAX5386L/MAX5388L		600		kHz
			MAX5386M/MAX5388M		150		
			MAX5386N/MAX5388N		75		

Electrical Characteristics (continued)

(V_{DD} = +2.6V to +5.5V, $V_{H\_}$ = V_{DD}, $V_{L\_}$ = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	Measured at W, $V_{H\_}$ = $1V_{RMS}$ at 1kHz		0.015		%
Wiper Settling Time (Note 6)	t_S	MAX5386L/MAX5388L		300		ns
		MAX5386M/MAX5388M		1000		
		MAX5386N/MAX5388N		2000		
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.6		5.5	V
Standby Current		Digital inputs = V_{DD} or GND		1		µA
DIGITAL INPUTS						
Minimum Input High Voltage	V_{IH}		70			$\%V_{DD}$
Maximum Input Low Voltage	V_{IL}				30	$\%V_{DD}$
Input Leakage Current			-1		+1	µA
Input Capacitance				5		pF
TIMING CHARACTERISTICS (Note 7)						
Maximum SCLK Frequency	f_{MAX}				10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
CS Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to CS Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to CS Fall Delay	t_{CS0}		10			ns
SCLK Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design and characterization.

Note 2: DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with H = V_{DD} and L = GND. The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 3: R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with the potentiometer configured as a variable resistor. H_ is unconnected and L_ = GND. For V_{DD} = +5V, the wiper terminal is driven with a source current of 400µA for the 10kΩ configuration, 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration. For V_{DD} = +2.6V, the wiper terminal is driven with a source current of 200µA for the 10kΩ configuration, 40µA for the 50kΩ configuration, and 20µA for the 100kΩ configuration.

Note 4: The wiper resistance is the worst value measured by injecting the currents given in Note 3 in to W with L = GND. R_W = $(V_W - V_H)/I_W$.

Note 5: Drive HA with a 1kHz GND to V_{DD} amplitude tone. LA = LB = GND. No load. WB is at midscale with a 10pF load. Measure WB.

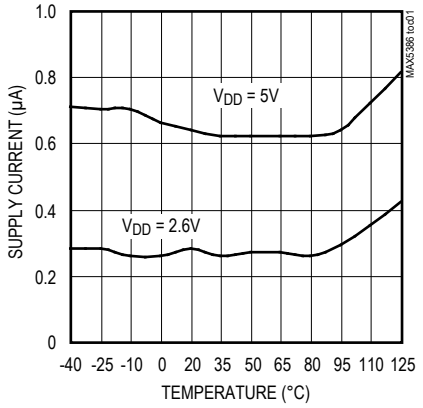
Note 6: The wiper-settling time is the worst case 0 to 50% rise time, measured between tap 0 and tap 127. H = V_{DD}, L = GND, and the wiper terminal is loaded with 10pF capacitance to ground.

Note 7: Digital timing is guaranteed by design and characterization, not production tested.

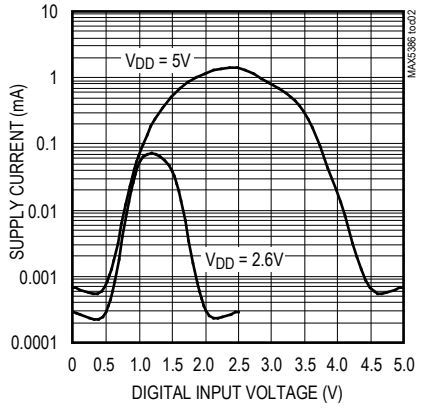
Typical Operating Characteristics

(V_{DD} = 5V, T_A = +25°C, unless otherwise noted.)

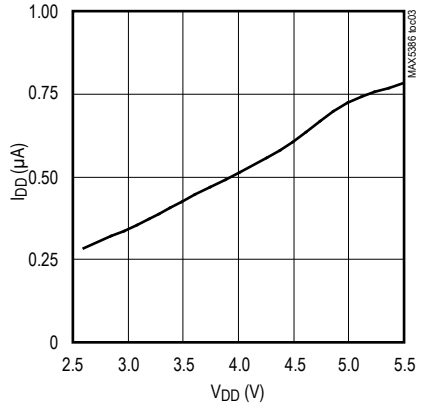
SUPPLY CURRENT vs. TEMPERATURE



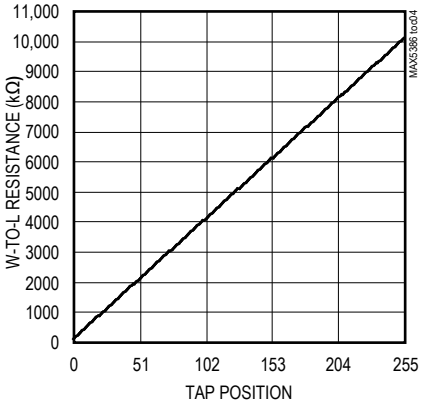
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



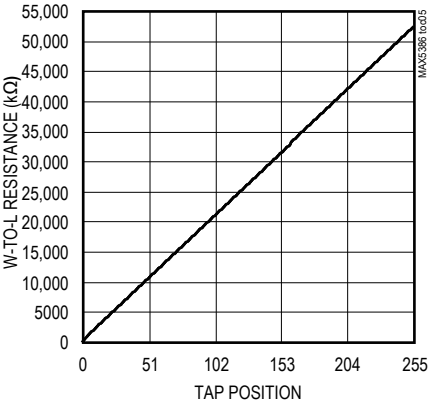
SUPPLY CURRENT vs. SUPPLY VOLTAGE



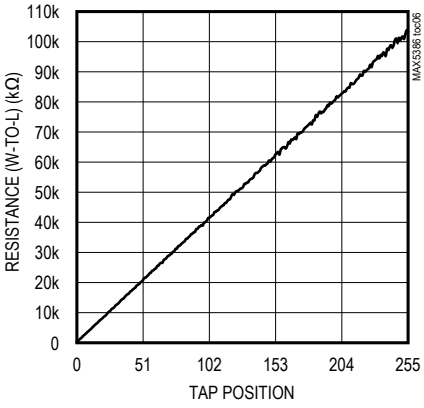
RESISTANCE (W TO L) vs. TAP POSITION (10kΩ)



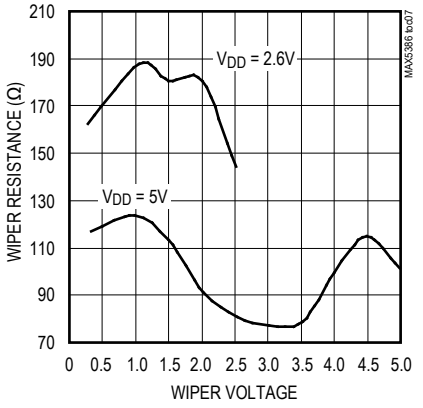
RESISTANCE (W TO L) vs. TAP POSITION (50kΩ)



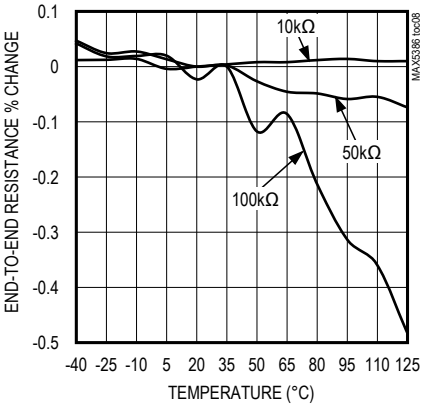
RESISTANCE (W-TO-L) vs. TAP POSITION (100kΩ)



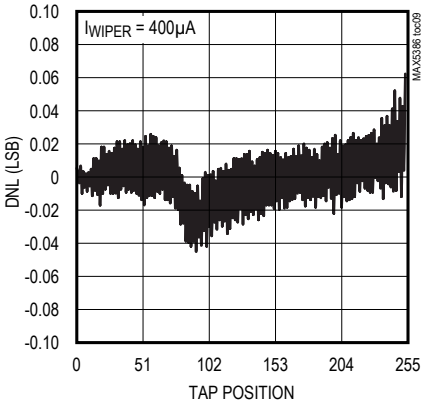
WIPER RESISTANCE vs. WIPER VOLTAGE (10kΩ)



END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



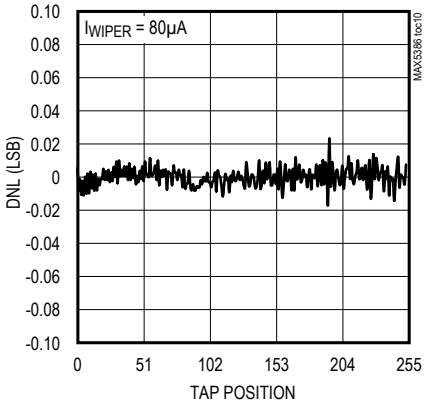
VARIABLE-RESISTOR DNL vs. TAP POSITION (10kΩ)



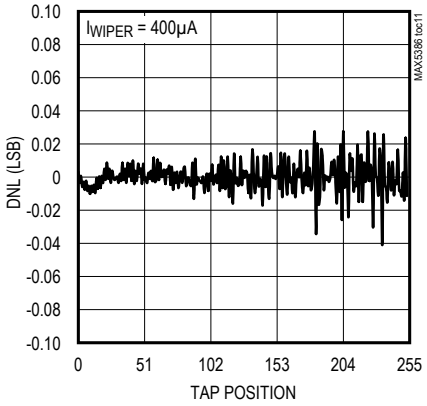
Typical Operating Characteristics (continued)

(V_{DD} = 5V, T_A = +25°C, unless otherwise noted.)

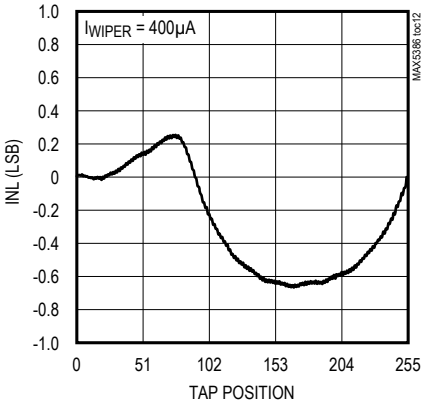
VARIABLE-RESISTOR DNL vs. TAP POSITION (50kΩ)



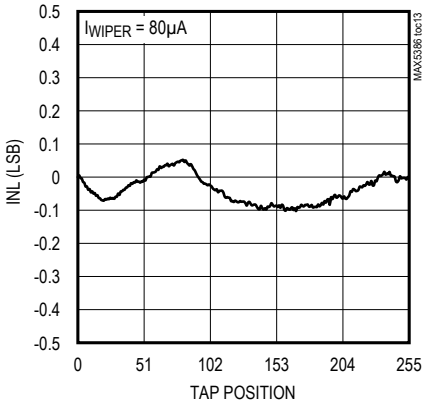
VARIABLE-RESISTOR DNL vs. TAP POSITION (100kΩ)



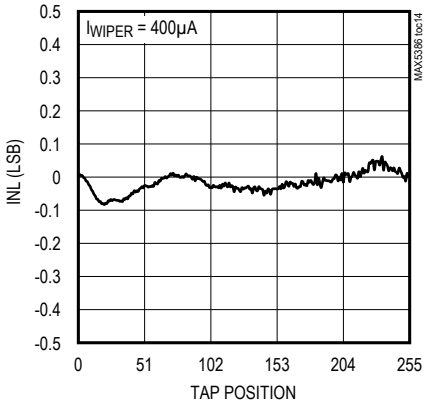
VARIABLE-RESISTOR INL vs. TAP POSITION (10kΩ)



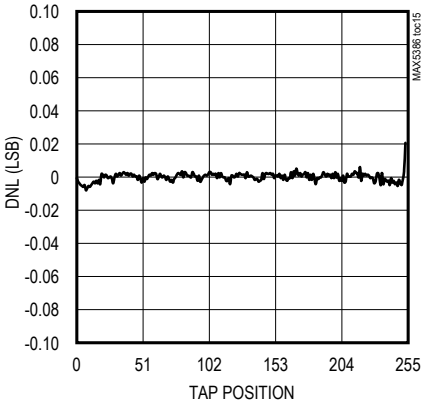
VARIABLE-RESISTOR INL vs. TAP POSITION (50kΩ)



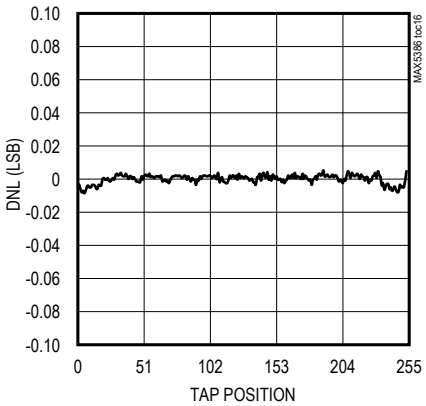
VARIABLE-RESISTOR INL vs. TAP POSITION (100kΩ)



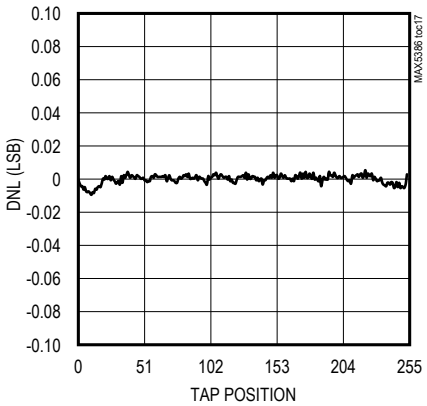
VOLTAGE-DIVIDER DNL vs. TAP POSITION (10kΩ)



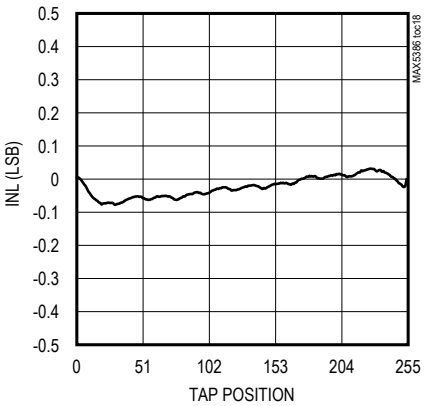
VOLTAGE-DIVIDER DNL vs. TAP POSITION (50kΩ)



VOLTAGE-DIVIDER DNL vs. TAP POSITION (100kΩ)



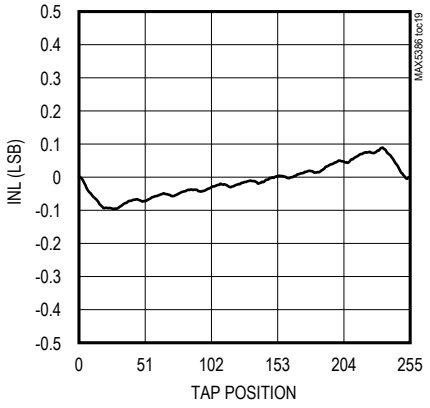
VOLTAGE-DIVIDER INL vs. TAP POSITION (10kΩ)



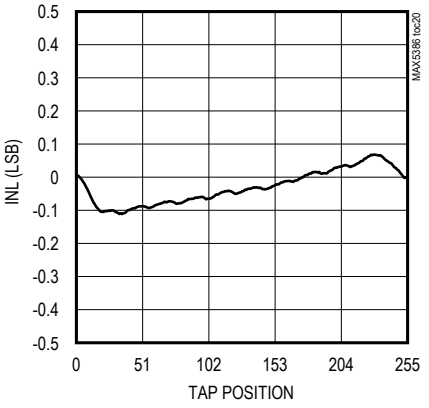
Typical Operating Characteristics (continued)

(V_{DD} = 5V, T_A = +25°C, unless otherwise noted.)

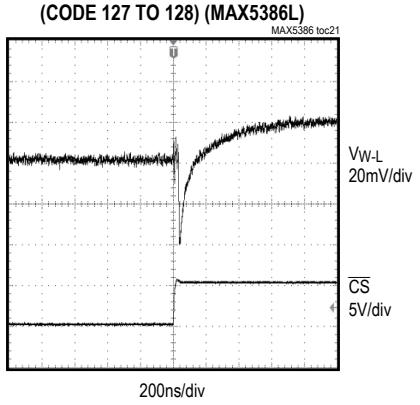
VOLTAGE-DIVIDER INL vs. TAP POSITION (50kΩ)



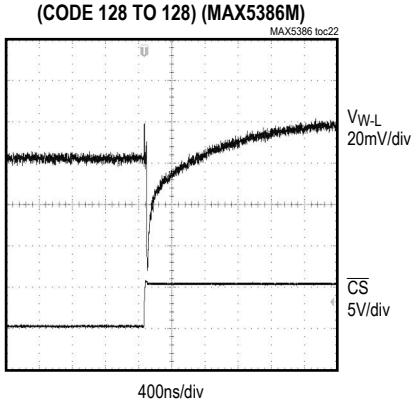
VOLTAGE-DIVIDER INL vs. TAP POSITION (100kΩ)



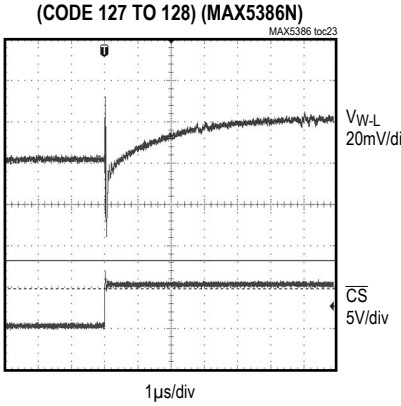
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) (MAX5386L)



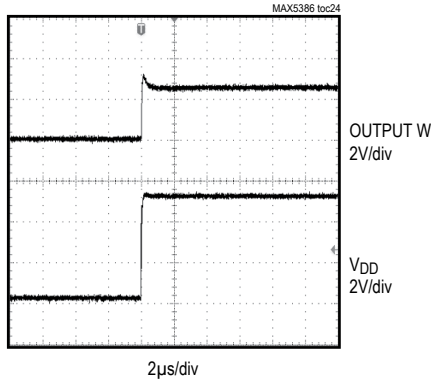
TAP-TO-TAP SWITCHING TRANSIENT (CODE 128 TO 128) (MAX5386M)



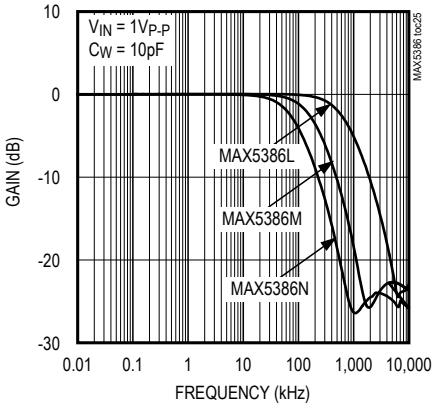
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) (MAX5386N)



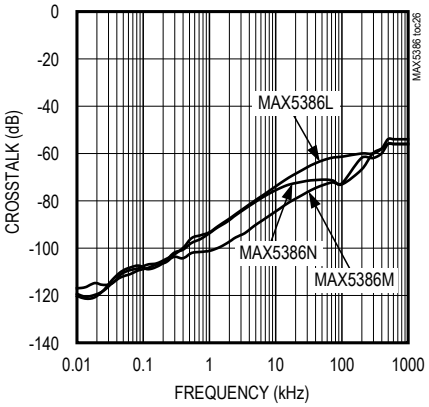
MAX5386 POWER-ON WIPER TRANSIENT CODE 0 TO 128



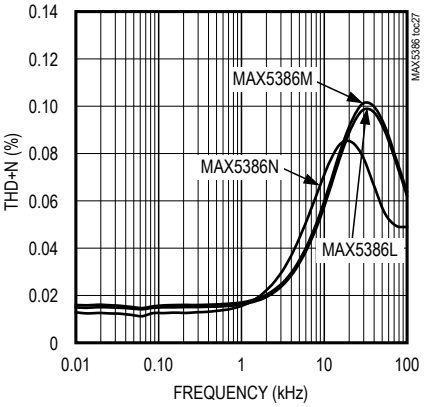
MIDSCALE FREQUENCY RESPONSE



CROSSTALK vs. FREQUENCY



THD+N vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
MAX5386	MAX5388		
1	3	HB	Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow in to or out of HB.
2	4	WB	Resistor B Wiper Terminal
3	2	LB	Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow in to or out of LB.
4	—	I.C.	Internally Connected. Connect to GND.
5	1	GND	Ground. Both pins must be grounded.
6, 7, 11, 13	—	N.C.	No Connection. Not internally connected.
8	5	$\overline{CS}$	Active-Low Chip-Select Input
9	6	DIN	Serial-Interface Data Input
10	7	SCLK	Serial-Interface Clock Input
12	8	V_{DD}	Power-Supply Input. Bypass V_{DD} to GND with a 0.1µF capacitor close to the device.
14	—	HA	Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow in to or out of HA.
15	9	WA	Resistor A Wiper Terminal
16	10	LA	Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow in to or out of LA.
—	—	EP	Exposed Pad (TQFN Only). Internally connected to GND. Connect to ground.

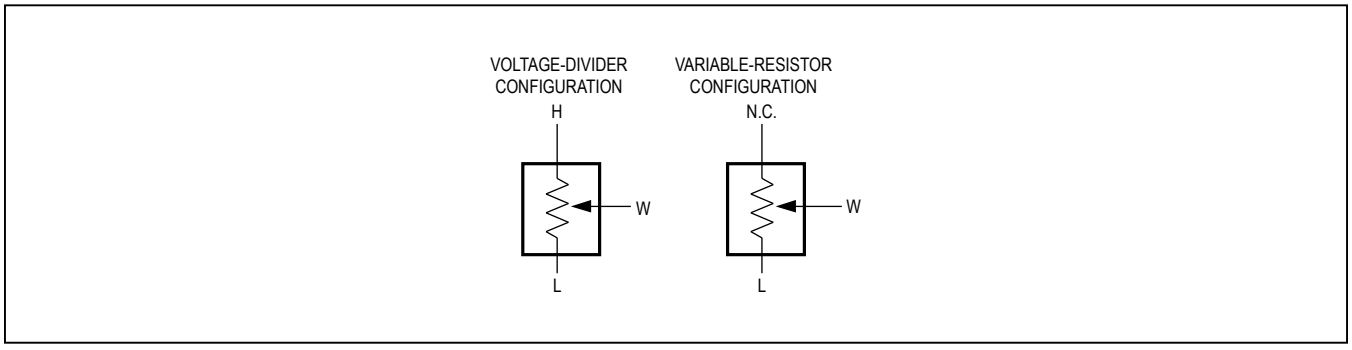


Figure 1. Voltage-Divider/Variable-Resistor Configurations

Detailed Description

The MAX5386/MAX5388 dual, 256-tap, volatile low-voltage linear taper digital potentiometers offer three end-toend resistance values of 10kΩ, 50kΩ, and 100kΩ. Each potentiometer consists of 255 fixed resistors in series between terminals H and L. The potentiometer wiper, W, is programmable to access anyone of the 256 tap points on the resistor string.

The potentiometers in each device are programmable independently of each other. The MAX5386/MAX5388 have an SPI interface.

SPI Digital Interface

The MAX5386/MAX5388 include an SPI interface, which provides a 3-wire write-only serial data interface to control the wiper tap position through inputs chip select ($\overline{CS}$), data in (DIN), and data clock (SCLK). Drive $\overline{CS}$ low to load data from DIN synchronously into the serial shift register on the rising edge of each SCLK pulse. The MAX5386/MAX5388 load the last 9 bits of clocked data once $\overline{CS}$ transitions high. See Figures 2 and 3. After all the data bits are shifted in, data are latched into the appropriate potentiometer control register when $\overline{CS}$ goes from low to high. Data written to a memory register immediately updates the wiper position. Keep $\overline{CS}$ low during the entire data stream to prevent the data from being terminated.

The first bit A0 (address bit) addresses one of the two potentiometers; writing a zero in A0 addresses control register A and writing a one in A0 addresses control register B. See Table 1. The power-on reset (POR) circuitry sets the wiper to midscale (D[7:0] 1000 0000).

The 8 data bits (D7–D0) indicate the position of the wiper. For D[7:0] = 0000 0000, the wiper moves to the position closest to L. For D[7:0] = 1111 1111, the wiper moves closest to H. D[7:0] is 1000 0000 following poweron for both registers A and B.

Register A: The data byte writes to register A, and the wiper of potentiometer A moves to the appropriate position at the rising edge of $\overline{CS}$. D[7:0] indicates the position of the wiper. D[7:0] = 0000 0000 moves the wiper to the position closest to L. D[7:0] = 1111 1111 moves the wiper to the position closest to H. D[7:0] is 1000 0000 following power-on.

Register B: The data byte writes to register B, and the wiper of potentiometer B moves to the appropriate position at the rising edge of $\overline{CS}$. D[7:0] indicates the position of the wiper. D[7:0] = 0000 0000 moves the wiper to the position closest to L. D[7:0] = 1111 1111 moves the wiper to the position closest to H. D[7:0] is 1000 0000 following power-on.

Table 1. SPI Register Map

Bit Number	1	2	3	4	5	6	7	8	9
Bit Name	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register B	1	D7	D6	D5	D4	D3	D2	D1	D0

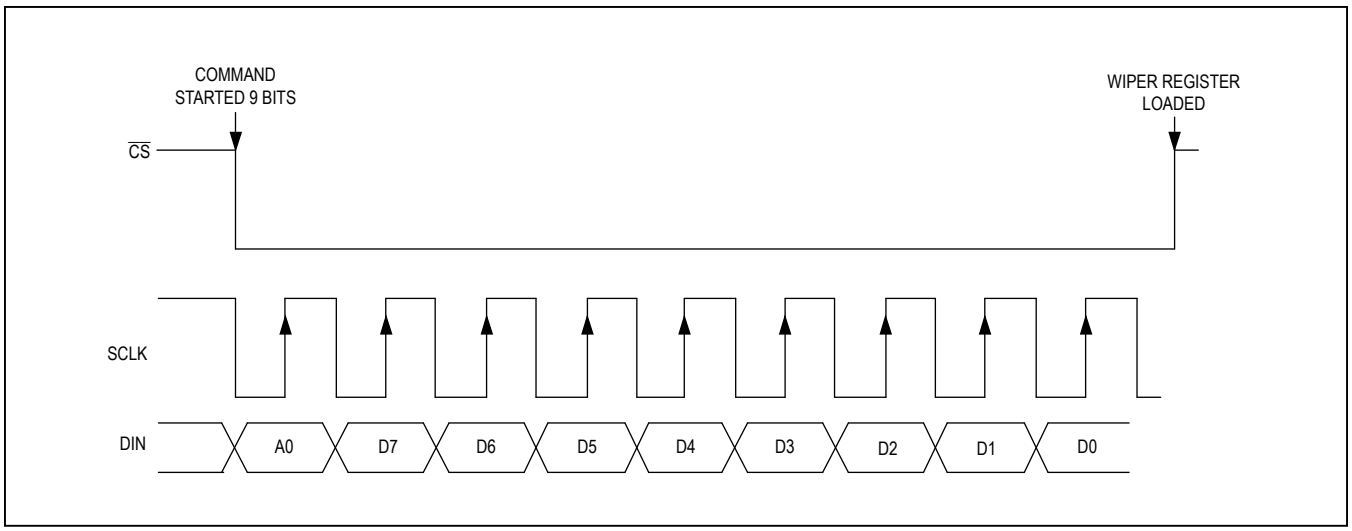


Figure 2. SPI Digital Interface Format

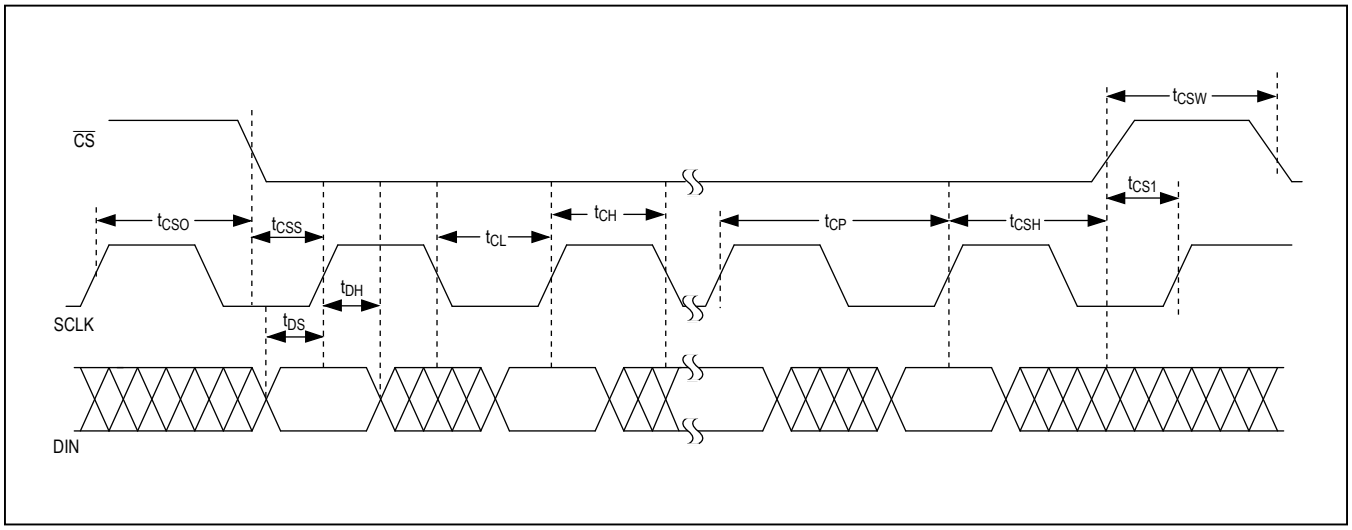


Figure 3. SPI Timing Diagram

Applications Information

Variable-Gain Amplifier

Figure 4 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 5 shows a potentiometer adjusting the gain of an inverting amplifier.

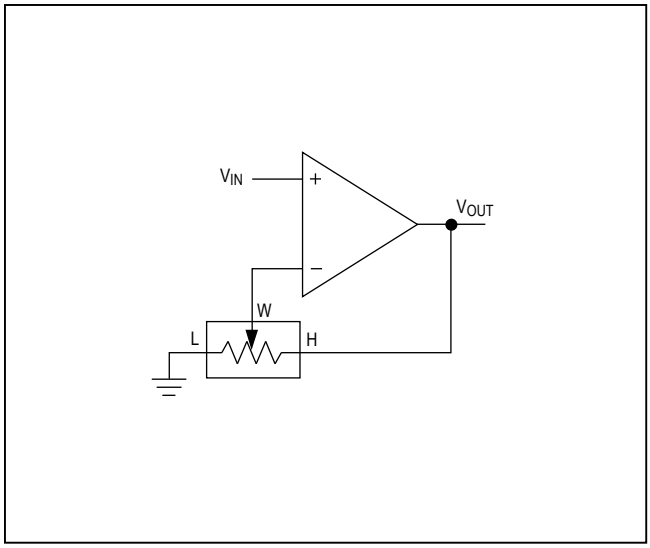


Figure 4. Variable-Gain Noninverting Amplifier

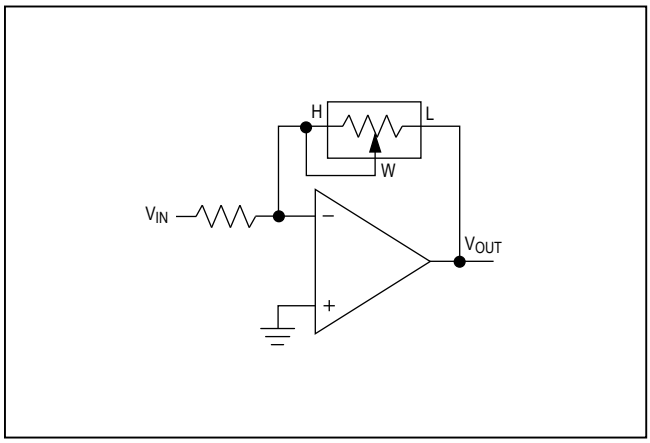


Figure 5. Variable-Gain Inverting Amplifier

Adjustable Dual Linear Regulator

Figure 6 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

Adjustable Voltage Reference

Figure 7 shows an adjustable voltage reference circuit using a potentiometer as a voltage-divider.

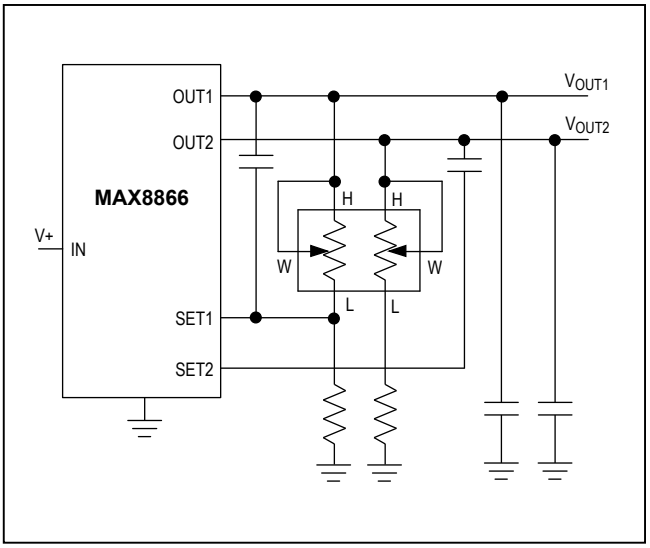


Figure 6. Adjustable Dual Linear Regulator

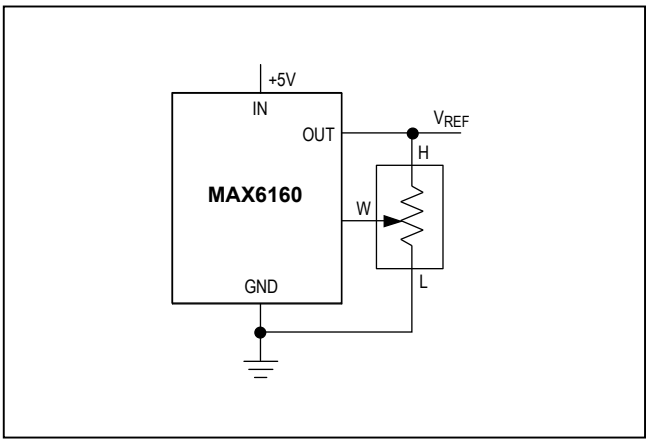


Figure 7. Adjustable Voltage Reference

Variable Gain Current to Voltage Converter

Figure 8 shows a variable gain current-to-voltage converter using a potentiometer as a variable resistor.

LCD Bias Control

Figure 9 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

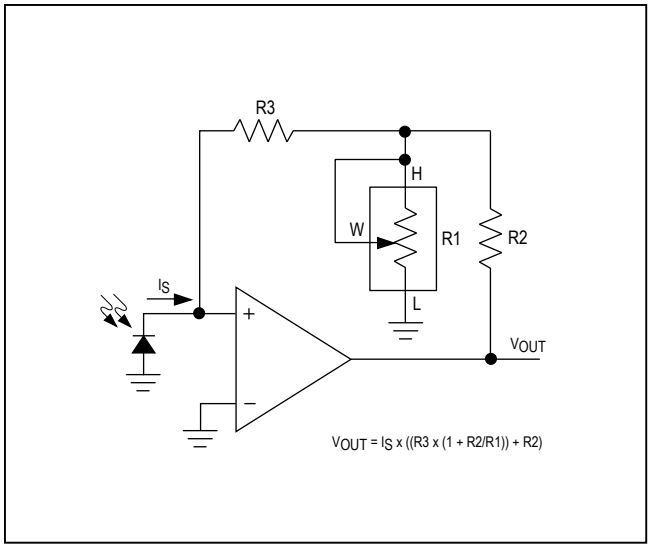


Figure 8. Variable Gain I-to-V Converter

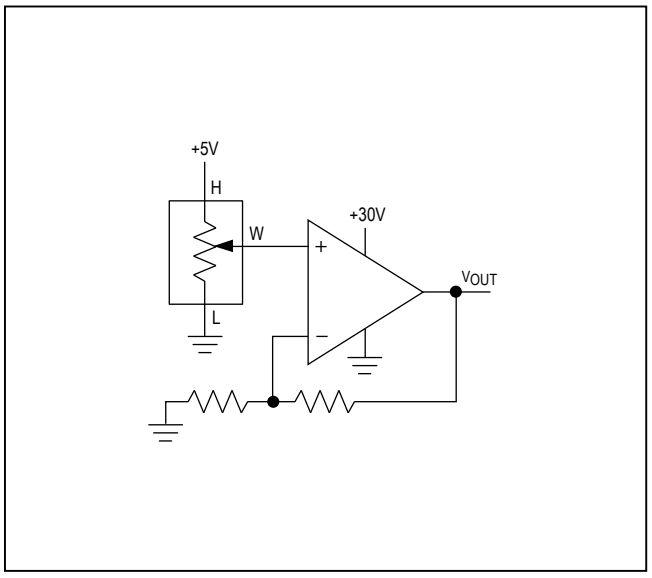


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

Programmable Filter

Figure 10 shows a programmable filter using a dual potentiometer.

Offset Voltage Adjustment Circuit

Figure 11 shows an offset voltage adjustment circuit using a dual potentiometer.

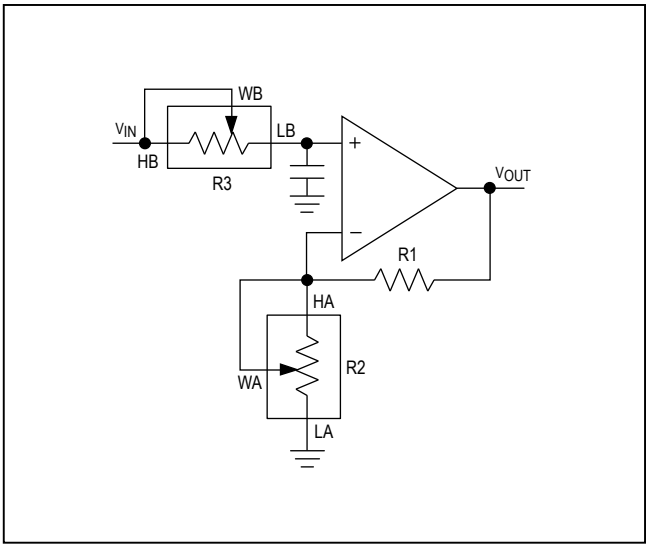


Figure 10. Programmable Filter

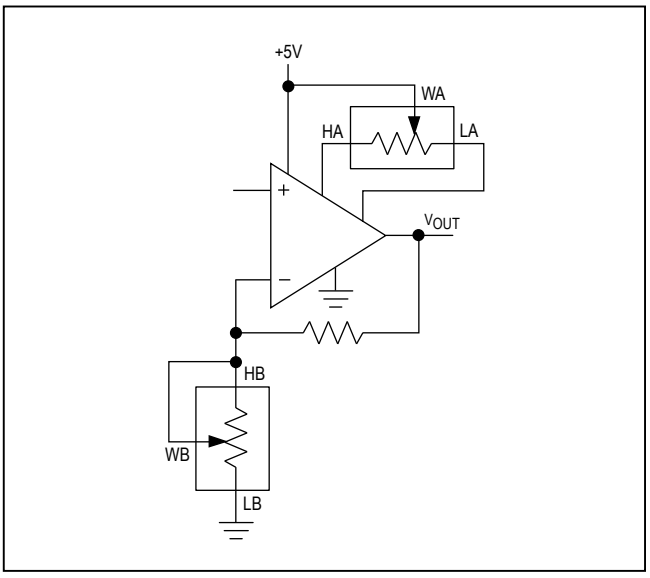
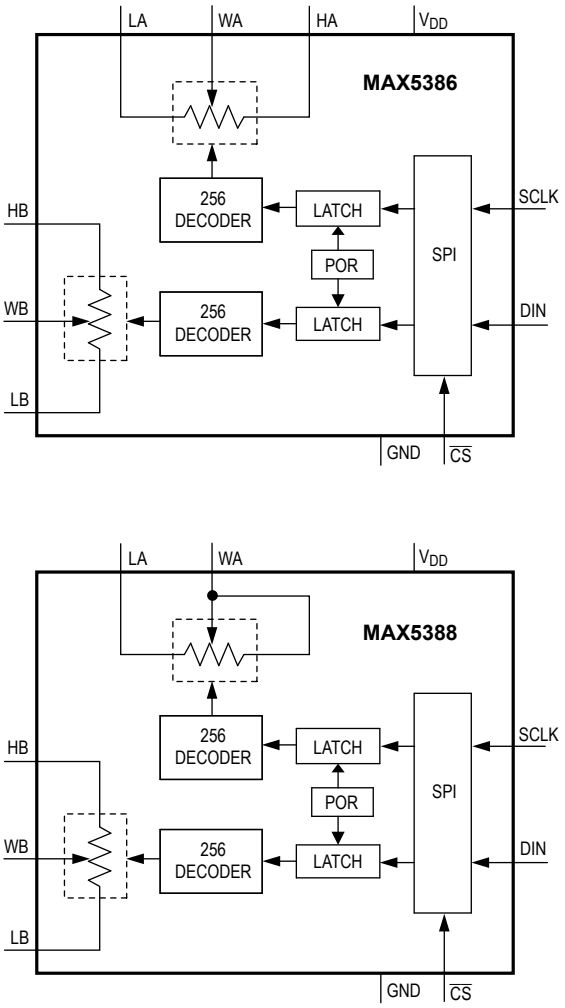


Figure 11. Offset Voltage Adjustment Circuit

Functional Diagrams



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
10 µMAX	U10+2	21-0061	90-0330
16 TQFN-EP	T1633+5	21-0136	90-0332