

MAX5391/MAX5393

General Description

The MAX5391/MAX5393 dual 256-tap, volatile, low-voltage linear taper digital potentiometers offer three end-to-end resistance values of 10k Ω , 50k Ω , and 100k Ω . Operating from a single +1.7V to +5.5V power supply, these devices provide a low 35ppm/ $^{\circ}$ C end-to-end temperature coefficient. The devices feature an SPI interface.

The small package size, low supply voltage, low supply current, and automotive temperature range of the MAX5391/MAX5393 make the devices uniquely suitable for the portable consumer market and battery backup industrial applications.

The MAX5391/MAX5393 include two digital potentiometers in a voltage-divider configuration. The MAX5391/MAX5393 are specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C automotive temperature range and are available in a 16-pin, 3mm x 3mm TQFN and a 14-pin TSSOP package, respectively.

Applications

- Low-Voltage Battery Applications
- Portable Electronics
- Mechanical Potentiometer Replacement
- Offset and Gain Control
- Adjustable Voltage References/Linear Regulators

Dual 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometers

Features

- Dual 256-Tap Linear Taper Positions
- Single +1.7V to +5.5V Supply Operation
- Low 12 μ A Quiescent Supply Current
- 10k Ω , 50k Ω , and 100k Ω End-to-End Resistance Values
- SPI-Compatible Interface
- Wiper Set to Midscale on Power-Up
- -40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range

Ordering Information

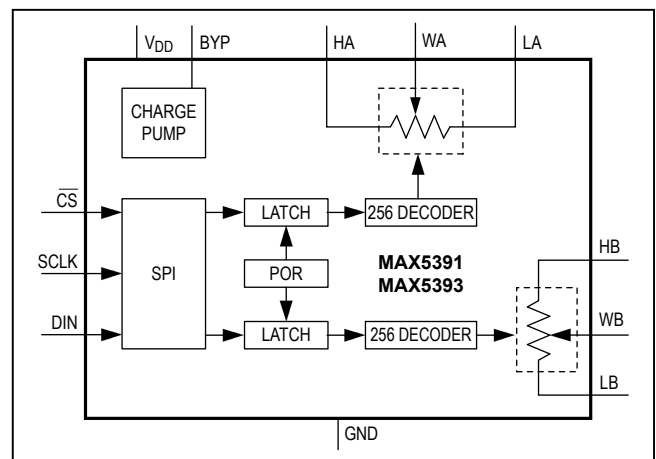
| PART | PIN-PACKAGE | END-TO-END RESISTANCE (k Ω) |
|--------------|-------------|-------------------------------------|
| MAX5391LATE+ | 16 TQFN-EP* | 10 |
| MAX5391MATE+ | 16 TQFN-EP* | 50 |
| MAX5391NATE+ | 16 TQFN-EP* | 100 |
| MAX5393LAUD+ | 14 TSSOP | 10 |
| MAX5393MAUD+ | 14 TSSOP | 50 |
| MAX5393NAUD+ | 14 TSSOP | 100 |

Note: All devices are specified in the -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range.

+Denotes lead(Pb)-free/RoHS-compliant package.

*EP = Exposed paddle.

Functional Diagram



Absolute Maximum Ratings

| | | |
|--|--|--|
| V _{DD} to GND | -0.3V to +6V | Continuous Power Dissipation (T _A = +70°C) |
| H ₋ , W ₋ , L ₋ to GND | -0.3V to the lower of (V _{DD} + 0.3V) or +6V | 14-Pin TSSOP (derate 10mW/°C above +70°C).....796.8mW |
| All Other Pins to GND | -0.3V to +6V | 16-Pin TQFN (derate 14.7mW/°C above +70°C)... 1176.5mW |
| Continuous Current into H ₋ , W ₋ , and L ₋ | | Operating Temperature Range..... -40°C to +125°C |
| MAX5391L/MAX5393L | ±5mA | Junction Temperature..... +150°C |
| MAX5391M/MAX5393M | ±2mA | Storage Temperature Range..... -65°C to +150°C |
| MAX5391N/MAX5393N | ±1mA | Lead Temperature (soldering, 10s)..... +300°C |
| | | Soldering Temperature (reflow)..... +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +1.7V to +5.5V, V_{H-} = V_{DD}, V_{L-} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +1.8V, T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|--|-------------------|------|-------|--------|
| Resolution | N | | 256 | | | Tap |
| DC PERFORMANCE (Voltage-Divider Mode) | | | | | | |
| Integral Nonlinearity | INL | (Note 2) | -0.5 | | +0.5 | LSB |
| Differential Nonlinearity | DNL | (Note 2) | -0.5 | | +0.5 | LSB |
| Dual-Code Matching | | Register A = Register B | -0.5 | | +0.5 | LSB |
| Ratiometric Resistor Tempco | | (ΔV _W /V _W)/ΔT, no load | | 5 | | ppm/°C |
| Full-Scale Error | Code = FFh | MAX5391L/MAX5393L | -3 | -2.2 | | LSB |
| | | MAX5391M/MAX5393M | -1 | -0.6 | | |
| | | MAX5391N/MAX5393N | -0.5 | -0.3 | | |
| Zero-Scale Error | Code = 00h | MAX5391L/MAX5393L | | 2.2 | 3 | LSB |
| | | MAX5391M/MAX5393M | | 0.6 | 1 | |
| | | MAX5391N/MAX5393N | | 0.3 | 0.5 | |
| DC PERFORMANCE (Variable Resistor Mode) | | | | | | |
| Integral Nonlinearity (Note 3) | R-INL | MAX5391L/MAX5393L | -1.5 | | +1.5 | LSB |
| | | MAX5391M/MAX5393M | -0.75 | | +0.75 | |
| | | MAX5391N/MAX5393N | -0.5 | | +0.5 | |
| Differential Nonlinearity | R-DNL | (Note 3) | -0.5 | | +0.5 | LSB |
| DC PERFORMANCE (Resistor Characteristics) | | | | | | |
| Wiper Resistance | R _{WL} | (Note 4) | | | 200 | Ω |
| Terminal Capacitance | C _{H-} , C _{L-} | Measured to GND | | 10 | | pF |
| Wiper Capacitance | C _{W-} | Measured to GND | | 50 | | pF |
| End-to-End Resistor Tempco | TC _R | No load | | 35 | | ppm/°C |
| End-to-End Resistor Tolerance | ΔR _{HL} | Wiper not connected | -25 | | +25 | % |
| AC PERFORMANCE | | | | | | |
| Crosstalk | | (Note 5) | | -90 | | dB |
| -3dB Bandwidth | BW | Code = 80H, 10pF load, V _{DD} = 1.8V | MAX5391L/MAX5393L | 600 | | kHz |
| | | | MAX5391M/MAX5393M | 100 | | |
| | | | MAX5391N/MAX5393N | 50 | | |
| Total Harmonic Distortion Plus Noise | THD+N | Measured at W, V _{H-} = 1V _{RMS} at 1kHz | | 0.02 | | % |

Electrical Characteristics (continued)

($V_{DD} = +1.7V$ to $+5.5V$, $V_{H_} = V_{DD}$, $V_{L_} = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = +1.8V$, $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|--------------------------------------|-----|------|-----|-------------------|
| Wiper Settling Time (Note 6) | t_S | MAX5391L/MAX5393L | | 400 | | ns |
| | | MAX5391M/MAX5393M | | 1200 | | |
| | | MAX5391N/MAX5393N | | 2200 | | |
| Charge-Pump Feedthrough at W_{-} | V_{RW} | $f_{CLK} = 600kHz$, $C_{OUT} = 0nF$ | | 200 | | nV _{P-P} |
| POWER SUPPLIES | | | | | | |
| Supply Voltage Range | V_{DD} | | 1.7 | | 5.5 | V |
| Standby Current | | $V_{DD} = 5.5V$ | | 27 | | μA |
| | | $V_{DD} = 1.7V$ | | 12 | | |
| DIGITAL INPUTS | | | | | | |
| Minimum Input High Voltage | V_{IH} | $V_{DD} = 2.6V$ to $5.5V$ | | 70 | | % x V_{DD} |
| | | $V_{DD} = 1.7V$ to $2.6V$ | | 75 | | |
| Maximum Input Low Voltage | V_{IL} | $V_{DD} = 2.6V$ to $5.5V$ | | | 30 | % x V_{DD} |
| | | $V_{DD} = 1.7V$ to $2.6V$ | | | 25 | |
| Input Leakage Current | | | -1 | | +1 | μA |
| Input Capacitance | | | | 5 | | pF |
| TIMING CHARACTERISTICS—SPI (Note 7) | | | | | | |
| SCLK Frequency | f_{MAX} | | | | 10 | MHz |
| SCLK Clock Period | t_{CP} | | 100 | | | ns |
| SCLK Pulse-Width High | t_{CH} | | 40 | | | ns |
| SCLK Pulse-Width Low | t_{CL} | | 40 | | | ns |
| \overline{CS} Fall to SCK Rise Setup Time | t_{CSS} | | 40 | | | ns |
| SCLK Rise to \overline{CS} Rise Hold Time | t_{CSH} | | 0 | | | ns |
| DIN Setup Time | t_{DS} | | 40 | | | ns |
| DIN Hold Time | t_{DH} | | 0 | | | ns |
| SCLK Rise to \overline{CS} Fall Delay | t_{CS0} | | 10 | | | ns |
| SCLK Rise to SCLK Rise Hold Time | t_{CS1} | | 40 | | | ns |
| CS Pulse-Width High | t_{CSW} | | 100 | | | ns |

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature limits are guaranteed by design and characterization.

Note 2: DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with $H_{-} = V_{DD}$ and $L_{-} = GND$. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

Note 3: R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with the potentiometer configured as a variable resistor. H_{-} is unconnected and $L_{-} = GND$. For $V_{DD} = +5V$, the wiper terminal is driven with a source current of $400\mu A$ for the $10k\Omega$ configuration, $80\mu A$ for the $50k\Omega$ configuration, and $40\mu A$ for the $100k\Omega$ configuration. For $V_{DD} = +1.7V$, the wiper terminal is driven with a source current of $150\mu A$ for the $10k\Omega$ configuration, $30\mu A$ for the $50k\Omega$ configuration, and $15\mu A$ for the $100k\Omega$ configuration.

Note 4: The wiper resistance is the value measured by injecting the currents given in Note 3 into W_{-} with $L_{-} = GND$.

$$R_{W_{-}} = (V_{W_{-}} - V_{H_{-}}) / I_{W_{-}}$$

Note 5: Drive HA with a 1kHz GND to V_{DD} amplitude tone. LA = LB = GND. No load. WB is at midscale with a 10pF load. Measure WB.

Note 6: The wiper-settling time is the worst-case 0 to 50% rise time, measured between tap 0 and tap 127. $H_{-} = V_{DD}$, $L_{-} = GND$, and the wiper terminal is loaded with 10pF capacitance to ground.

Note 7: Digital timing is guaranteed by design and characterization, not production tested.

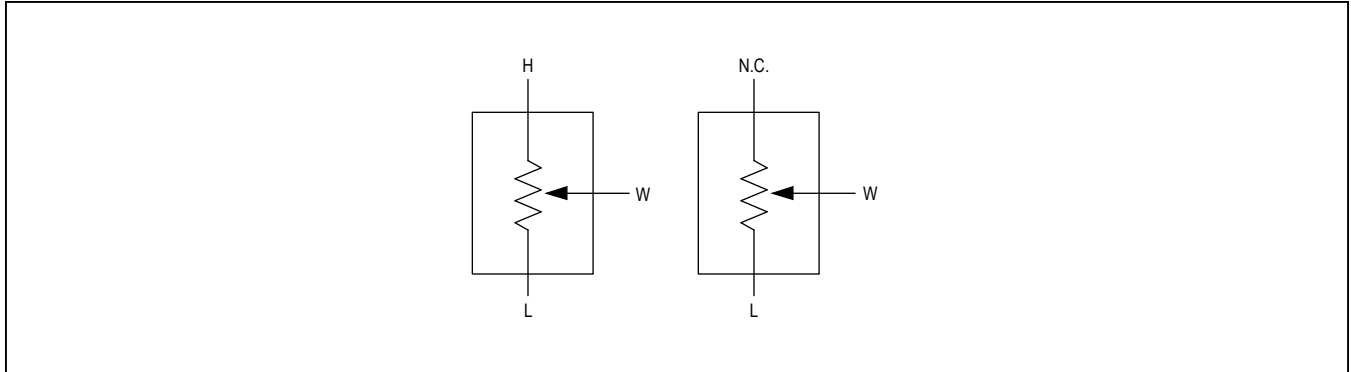
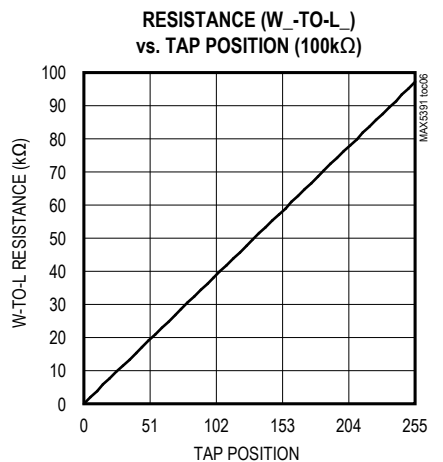
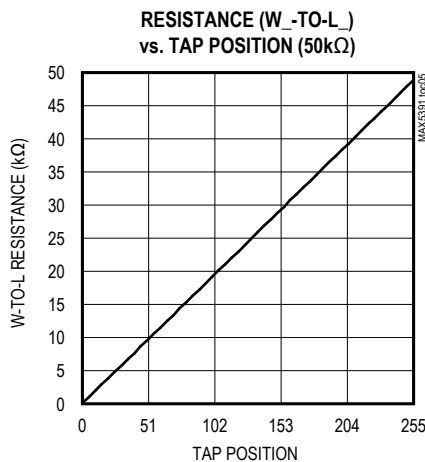
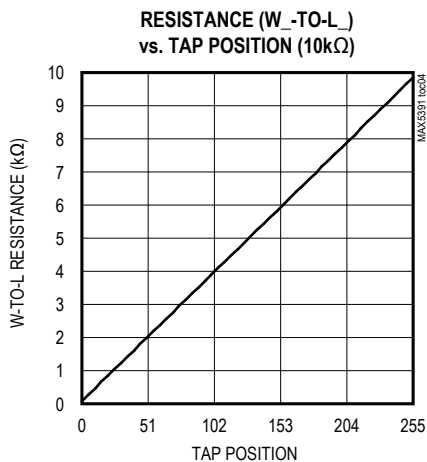
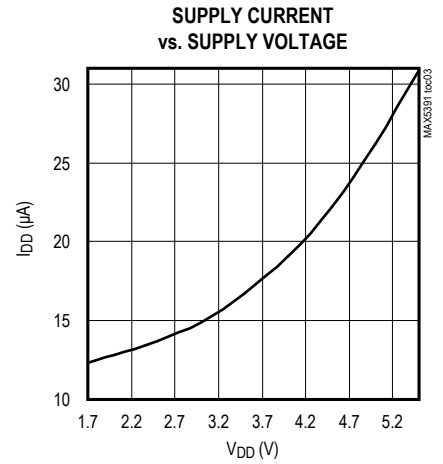
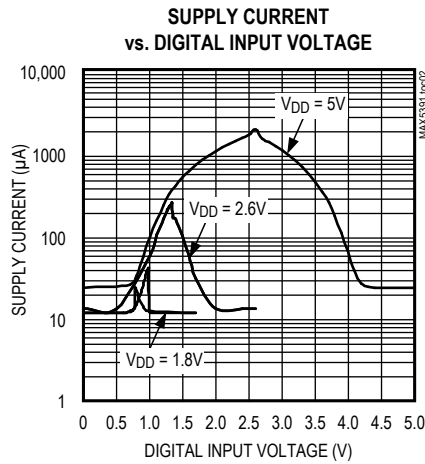
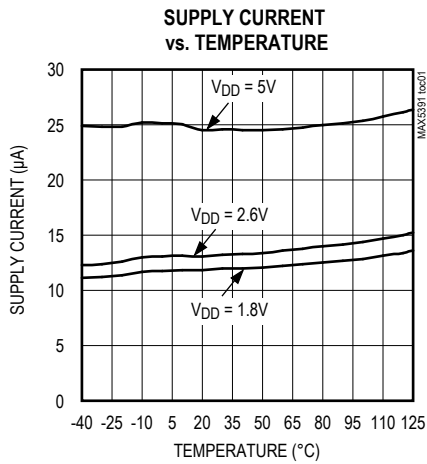


Figure 1. Voltage-Divider and Variable Resistor Configurations

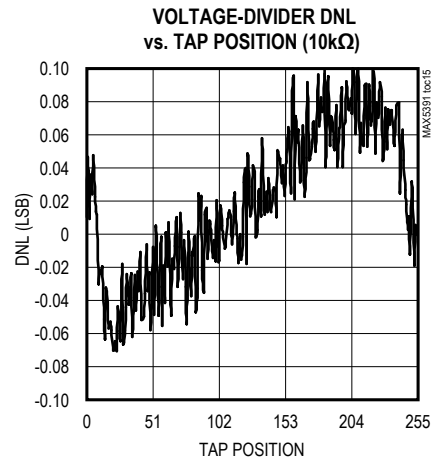
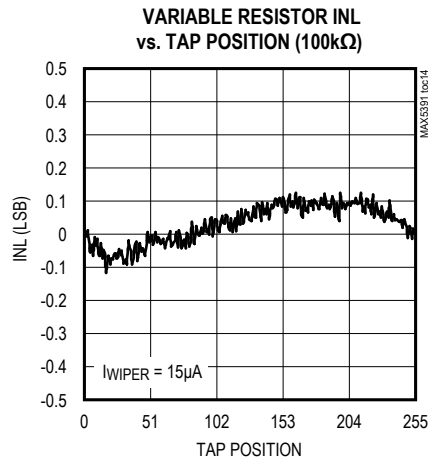
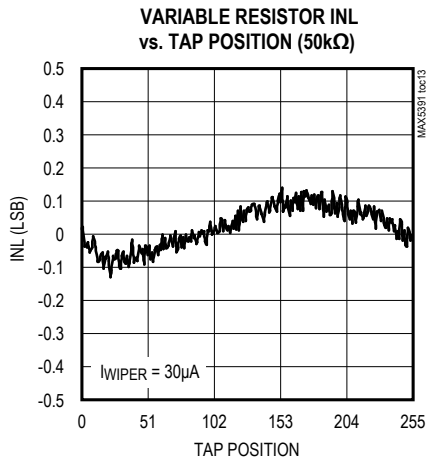
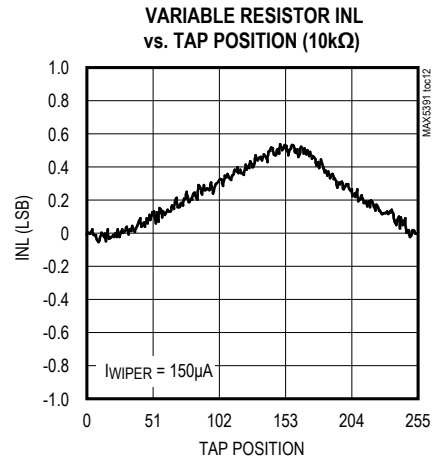
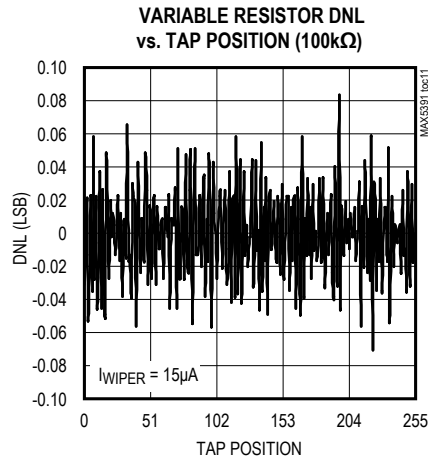
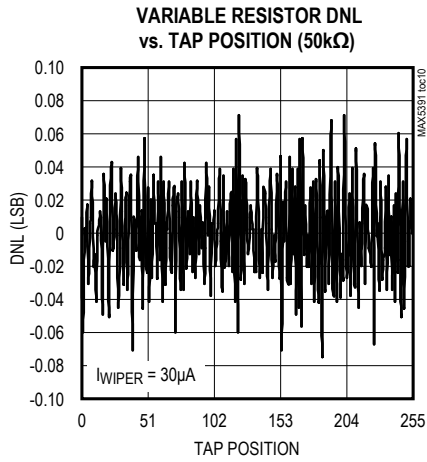
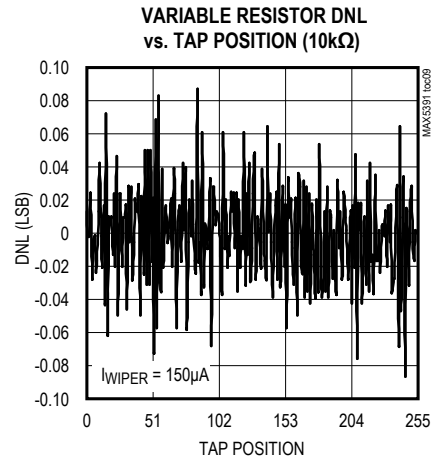
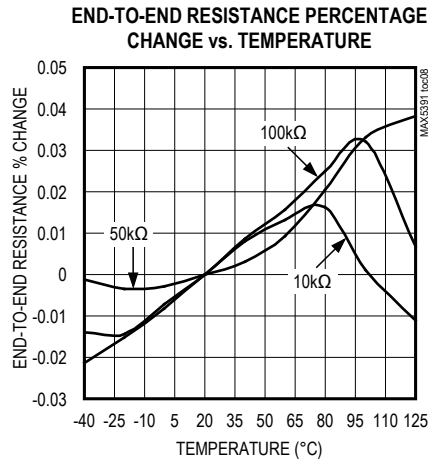
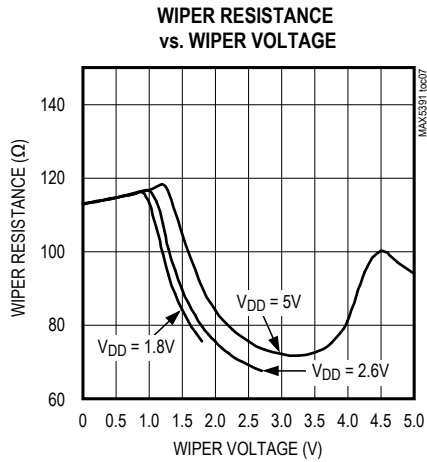
Typical Operating Characteristics

($V_{DD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)



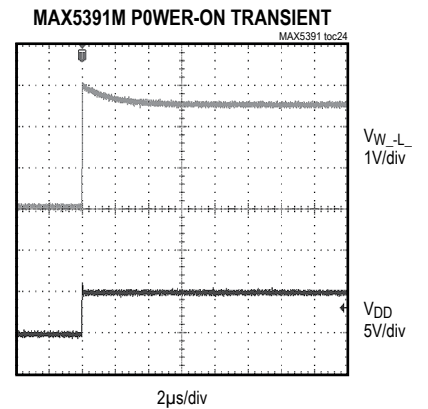
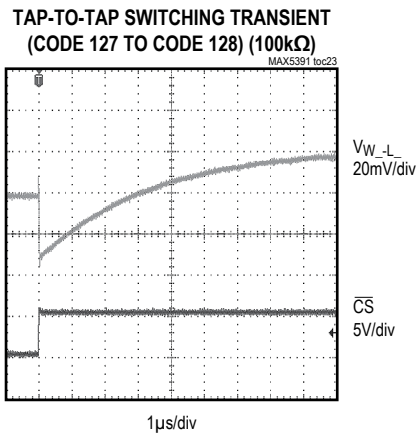
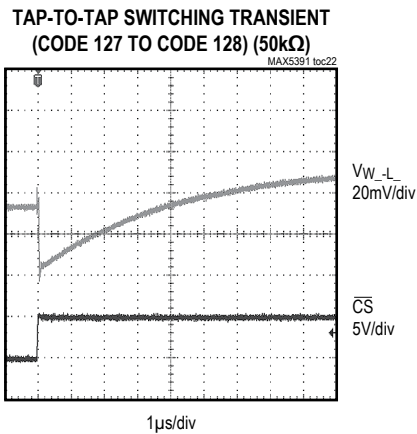
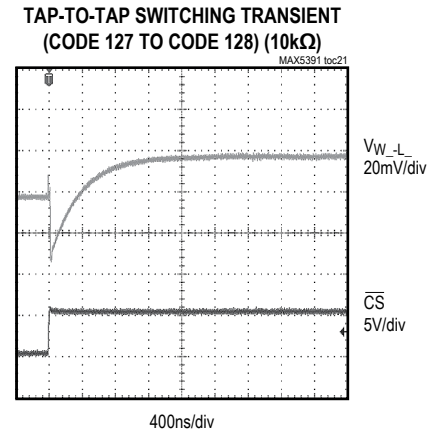
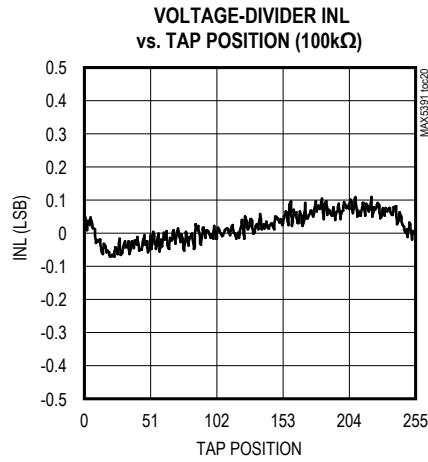
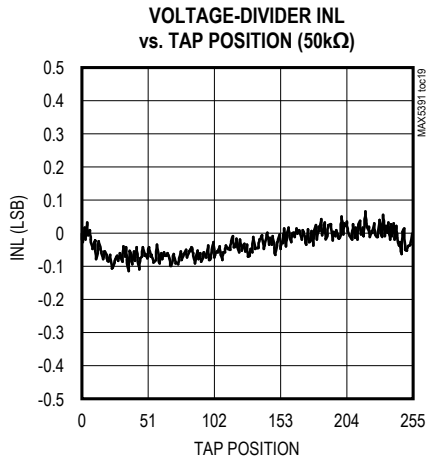
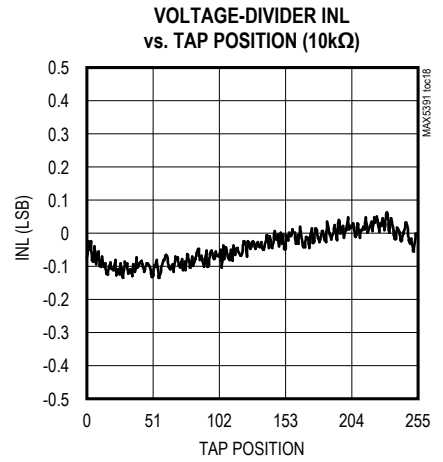
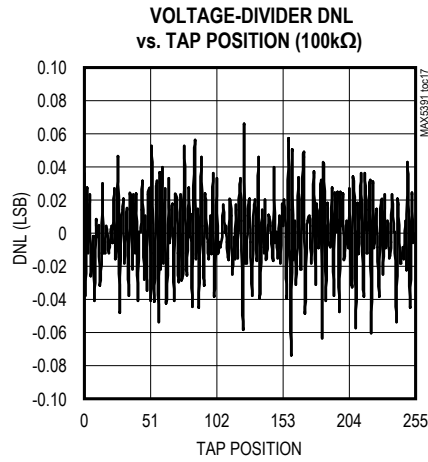
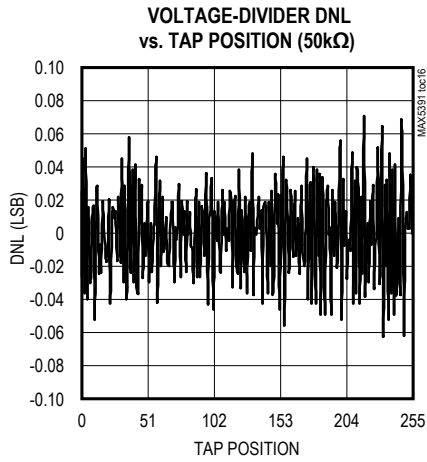
Typical Operating Characteristics (continued)

($V_{DD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)



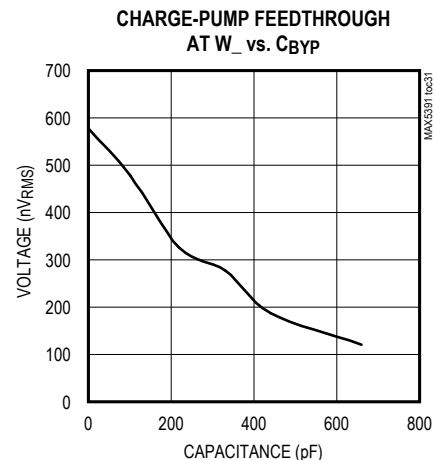
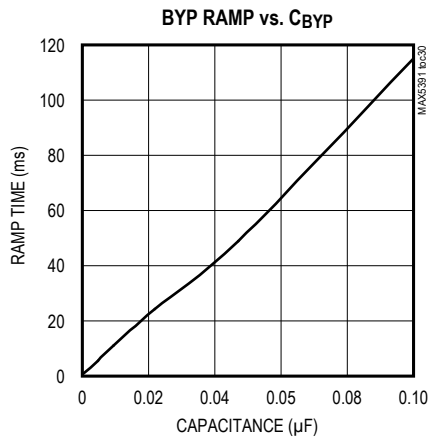
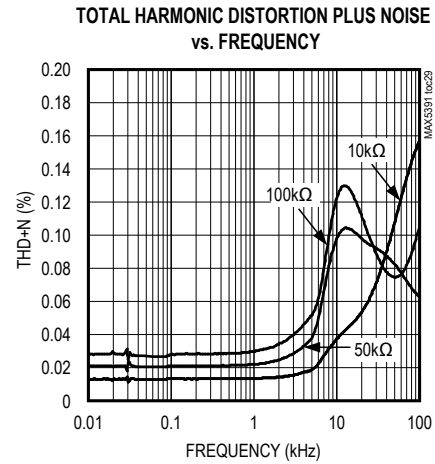
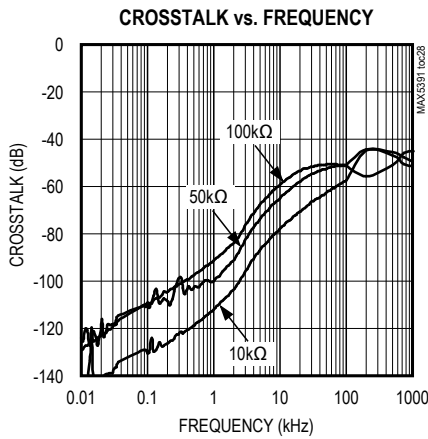
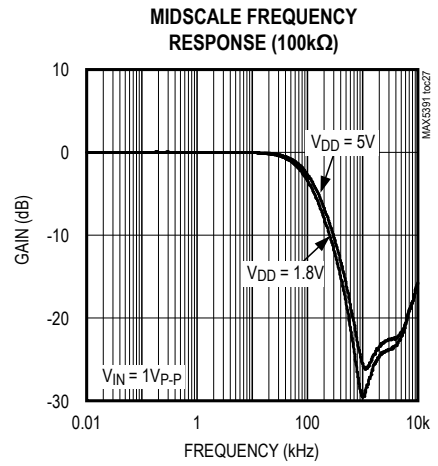
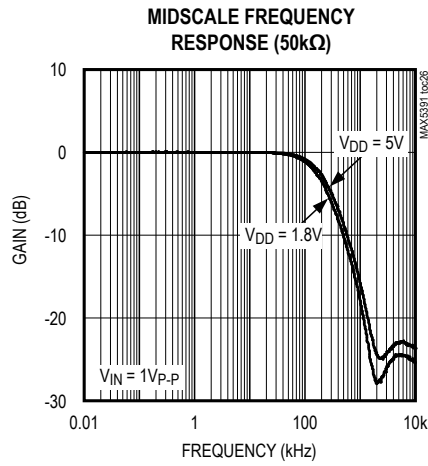
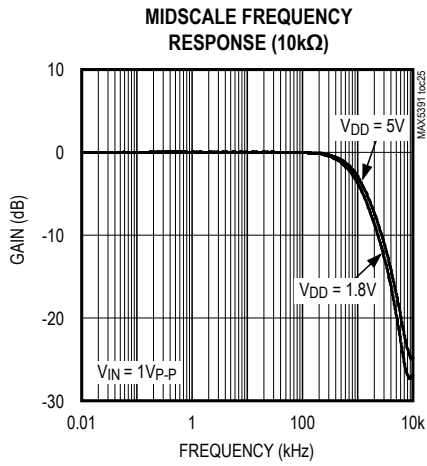
Typical Operating Characteristics (continued)

($V_{DD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)

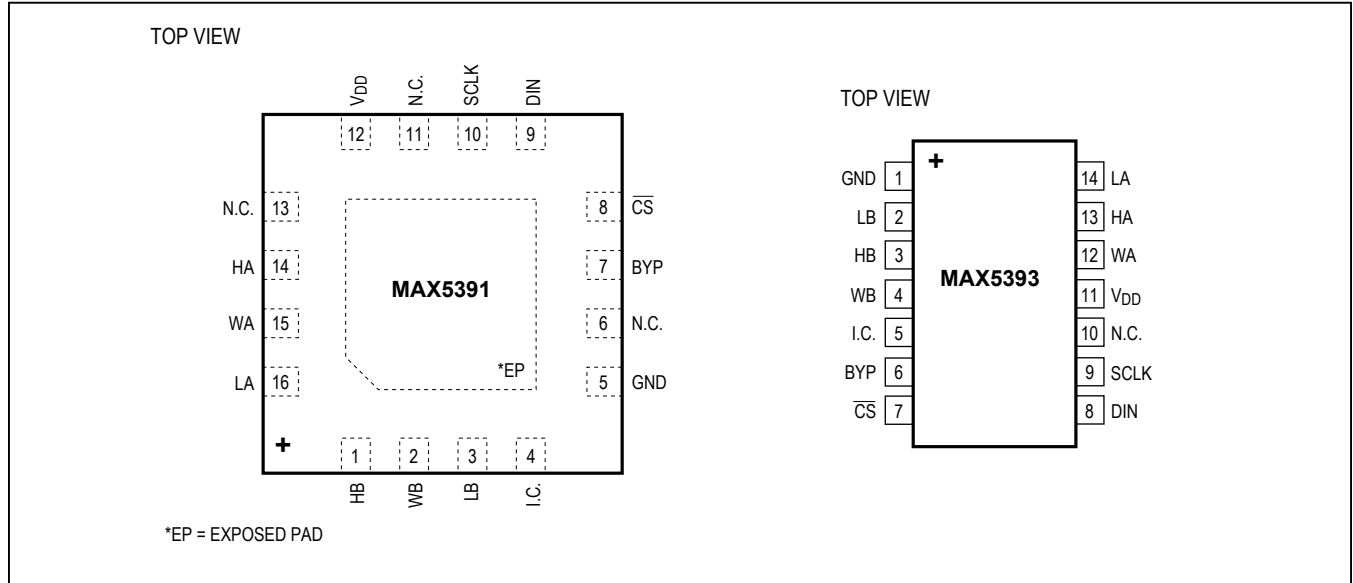


Typical Operating Characteristics (continued)

($V_{DD} = 1.8V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Pin Configurations



Pin Description

| PIN | | NAME | FUNCTION |
|-------------------|-----------------|-----------------|--|
| MAX5391 (TQFN-EP) | MAX5393 (TSSOP) | | |
| 1 | 3 | HB | Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB. |
| 2 | 4 | WB | Resistor B Wiper Terminal |
| 3 | 2 | LB | Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB. |
| 4 | 5 | I.C. | Internally Connected. Connect to GND. |
| 5 | 1 | GND | Ground |
| 6, 11, 13 | 10 | N.C. | No Connection. Not internally connected. |
| 7 | 6 | BYP | Internal Power-Supply Bypass. For additional charge-pump filtering, bypass to GND with a capacitor close to the device. |
| 8 | 7 | \overline{CS} | Active-Low Chip-Select Input |
| 9 | 8 | DIN | Serial-Interface Data Input |
| 10 | 9 | SCLK | Serial-Interface Clock Input |
| 12 | 11 | V _{DD} | Power-Supply Input. Bypass V _{DD} to GND with a 0.1µF capacitor close to the device. |
| 14 | 13 | HA | Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA. |
| 15 | 12 | WA | Resistor A Wiper Terminal |
| 16 | 14 | LA | Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA. |
| — | — | EP | Exposed Pad (MAX5391 Only). Connect to GND. |

Detailed Description

The MAX5391/MAX5393 dual 256-tap, volatile, low-voltage linear taper digital potentiometers offer three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. Each potentiometer consists of 255 fixed resistors in series between terminals H₋ and L₋. The potentiometer wiper, W₋, is programmable to access any one of the 256 tap points on the resistor string.

The potentiometers in each device are programmable independently of each other. The MAX5391/MAX5393 feature an SPI interface.

Charge Pump

The MAX5391/MAX5393 contain an internal charge pump that guarantees the maximum wiper resistance, R_{WL}, to be less than 200Ω for supply voltages down to 1.7V. Pins H₋, W₋, and L₋ are still required to be less than V_{DD} + 0.3V. A bypass input, BYP, is provided to allow additional filtering of the charge-pump output, further reducing clock feed through that may occur on H₋, W₋, or L₋. The nominal clock rate of the charge pump is 600kHz. BYP should remain resistively unloaded as any additional load would produce a ripple of approximately I_{BYP}/(600kHz x C_{BYP}) volts. See the Charge-Pump Feedthrough at W₋ vs. C_{BYP} graph in the *Typical Operating Characteristics* for C_{BYP} sizing guidelines with respect to clock feedthrough

to the wiper. The value of C_{BYP} does affect the startup time of the charge pump; however, C_{BYP} does not impact the ability to communicate with the device, nor is there a minimum C_{BYP} requirement. The maximum wiper impedance specification is not guaranteed until the charge pump is fully settled. See the BYP Ramp vs. C_{BYP} graph in the *Typical Operating Characteristics* for C_{BYP} impact on charge-pump settling time.

SPI Digital Interface

The MAX5391/MAX5393 include a SPI interface that provides a 3-wire write-only serial-data interface to control the wiper tap position through inputs chip select (CS), data in (DIN), and data clock (SCLK). Drive CS low to load data from DIN synchronously into the serial shift register on the rising edge of each SCLK pulse. The MAX5391/MAX5393 load the last 10 bits of clocked data into the appropriate potentiometer control register once CS transitions high. See Figures 2 and 3. Data written to a memory register immediately updates the wiper position. Keep CS low during the entire data stream to prevent the data from being terminated.

The first two bits A1:A0 (address bits) address one of the two potentiometers. See Table 1. The power-on reset (POR) circuitry sets the wiper to midscale.

Table 1. SPI Register Map

| Bit Number | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|------------------------|----|----|----|----|----|----|----|----|----|----|
| Bit Name | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Wiper Register A | 0 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Wiper Register B | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write to Both A and B | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

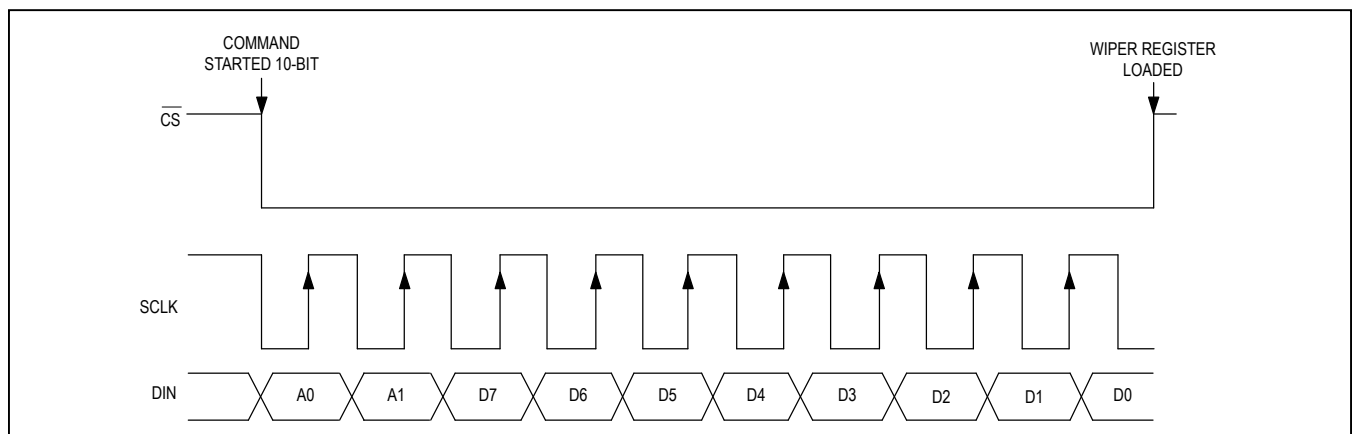


Figure 2. SPI Digital Interface Format

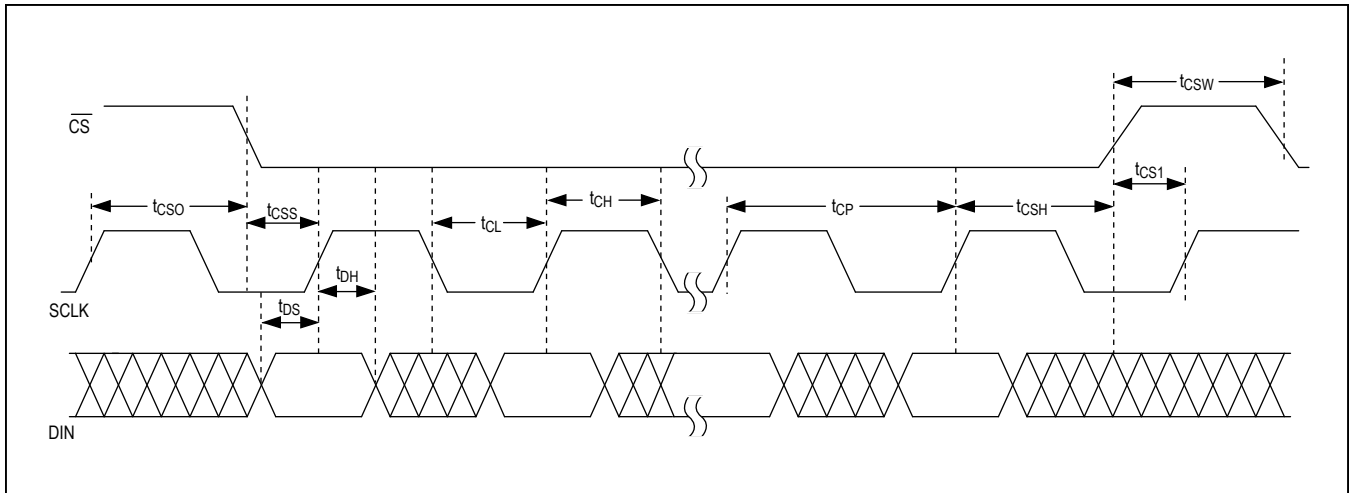


Figure 3. SPI Timing Diagram

REG A: The data byte writes to register A, and the wiper of potentiometer A moves to the appropriate position at the rising edge of \overline{CS} . D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LA. D[7:0] = FFh moves the wiper closest to HA. D[7:0] is 80h following power-on.

REG B: The data byte writes to register B, and the wiper of potentiometer B moves to the appropriate position at the rising edge of \overline{CS} . D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LB. D[7:0] = FFh moves the wiper to the position closest to HB. D[7:0] is 80h following power-on.

REG A and B: The data byte writes to registers A and B, and the wipers of potentiometers A and B move to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to L_. D[7:0] = FFh moves the wiper to the position closest to H_. D[7:0] is 80h following power-on.

Applications Information

Variable Gain Amplifier

Figure 4 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 5 shows a potentiometer adjusting the gain of an inverting amplifier.

Adjustable Dual Regulator

Figure 6 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

Adjustable Voltage Reference

Figure 7 shows an adjustable voltage reference circuit using a potentiometer as a voltage divider.

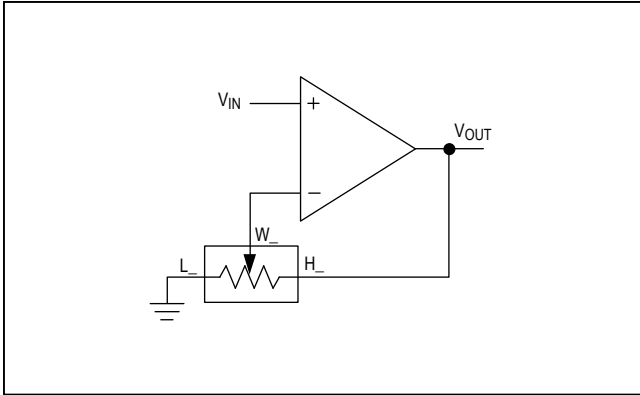


Figure 4. Variable-Gain Noninverting Amplifier

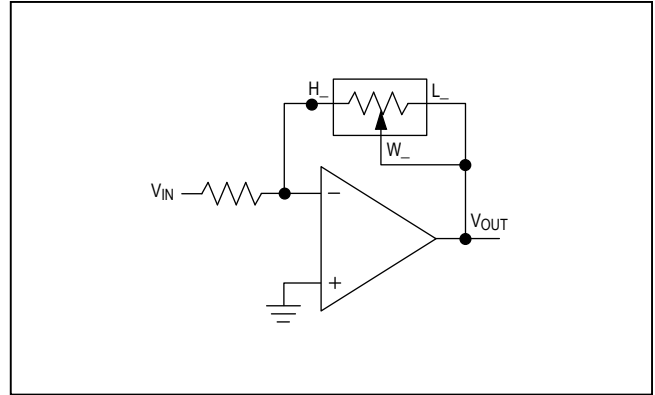


Figure 4. Variable-Gain Noninverting Amplifier

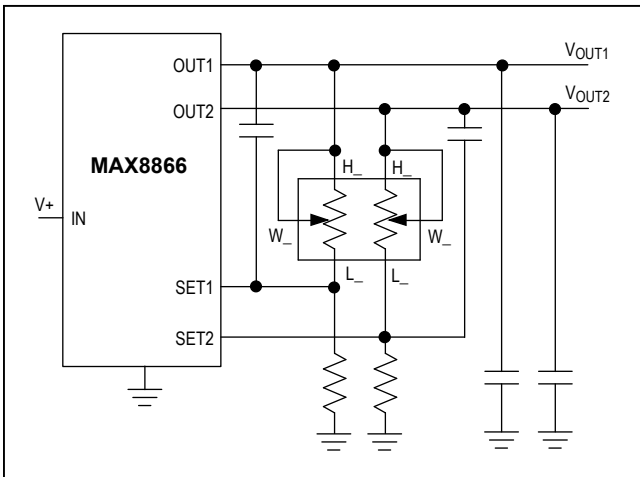


Figure 6. Adjustable Dual Linear Regulator

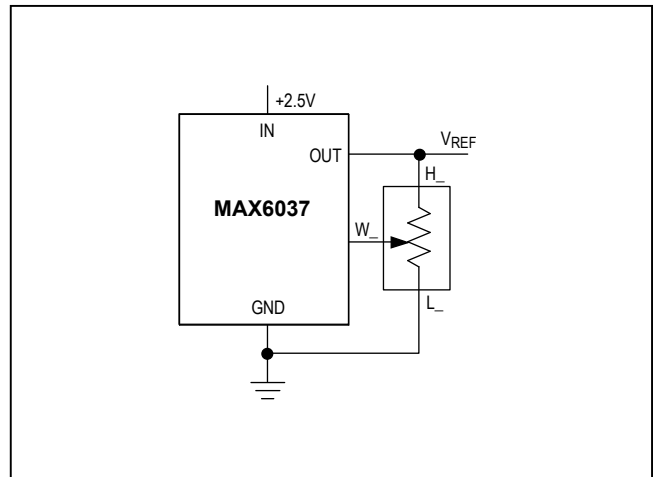


Figure 7. Adjustable Voltage Reference

Variable-Gain Current-to-Voltage Converter

Figure 8 shows a variable-gain current-to-voltage converter using a potentiometer as a variable resistor.

LCD Bias Control

Figure 9 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

Programmable Filter

Figure 10 shows a programmable filter using a dual potentiometer.

Offset Voltage Adjustment Circuit

Figure 11 shows an offset voltage adjustment circuit using a dual potentiometer.

Chip Information

PROCESS: BiCMOS

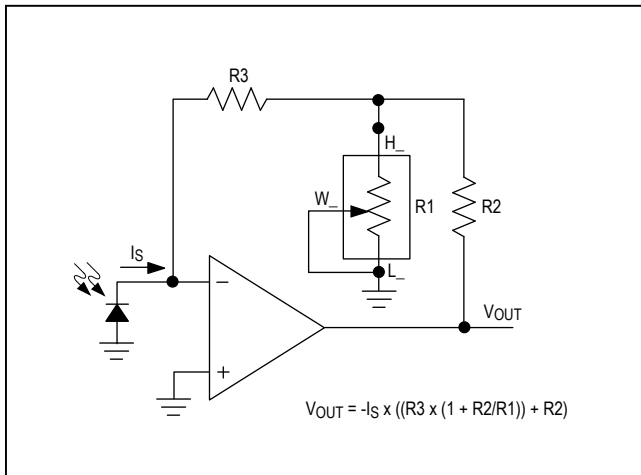


Figure 8. Variable Gain I-to-V Converter

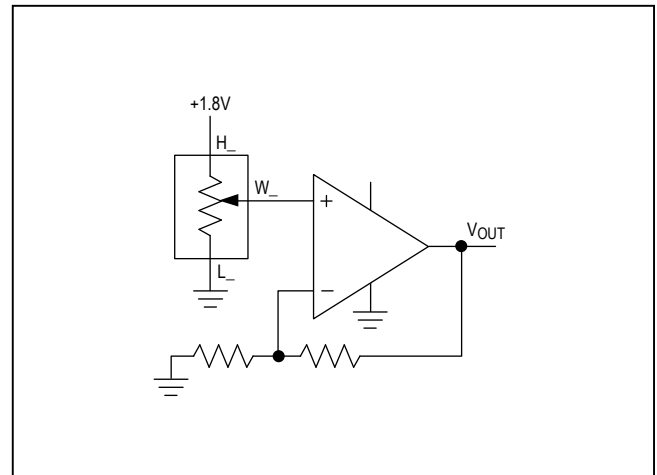


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

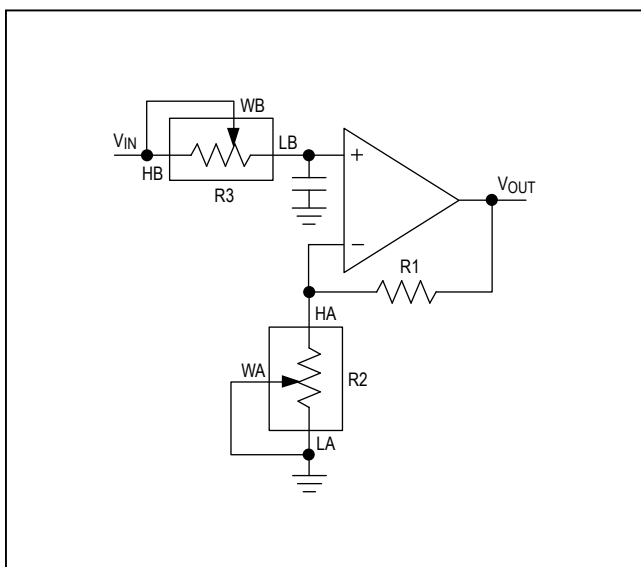


Figure 10. Programmable Filter

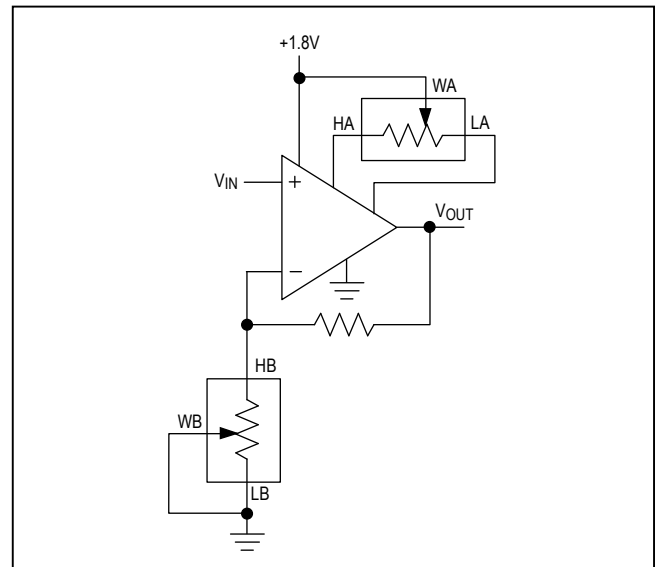


Figure 11. Offset Voltage Adjustment Circuit

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 14 TSSOP | U14+1 | 21-0066 | 90-0113 |
| 16 TQFN-EP | T1633+5 | 21-0136 | 90-0032 |