MAX5924/MAX5925/ MAX5926

1V to 13.2V, n-Channel Hot-Swap Controllers Require No Sense Resistor

General Description

The MAX5924/MAX5925/MAX5926 1V to 13.2V hot-swap controllers allow the safe insertion and removal of circuit cards into live backplanes. These devices hot swap supplies ranging from 1V to 13.2V provided that the device supply voltage, V_{CC}, is at or above 2.25V and the hot-swapped supply, V_S, does not exceed V_{CC}.

The MAX5924/MAX5925/MAX5926 hot-swap controllers limit the inrush current to the load and provide a circuit-breaker function for overcurrent protection. The devices operate with or without a sense resistor. When operating without a sense resistor, load-probing circuitry ensures a short circuit is not present during startup, then gradually turns on the external MOSFET. After the load probing is complete, on-chip comparators provide overcurrent protection by monitoring the voltage drop across the external MOSFET on-resistance. In the event of a fault condition, the load is disconnected.

The devices include many integrated features that reduce component count and design time, including configurable turn-on voltage, slew rate, and circuit-breaker threshold. An on-board charge pump provides the gate drive for a low-cost, external nMOSFET.

The MAX5924/MAX5925/MAX5926 are available with open-drain PGOOD and/or $\overline{PGOOD}$ outputs. The MAX5925/MAX5926 also feature a circuit breaker with temperature-compensated $R_{DS(ON)}$ sensing. The MAX5926 features a selectable 0ppm/°C or 3300ppm/°C temperature coefficient. The MAX5924 temperature coefficient is 0ppm/°C and the MAX5925 temperature coefficient is 3300ppm/°C. Autoretry and latched fault-management configurations are available (see the *Selector Guide*).

Applications

- Base Stations
- RAID
- Remote-Access Servers
- Network Routers and Switches
- Servers
- Portable Device Bays

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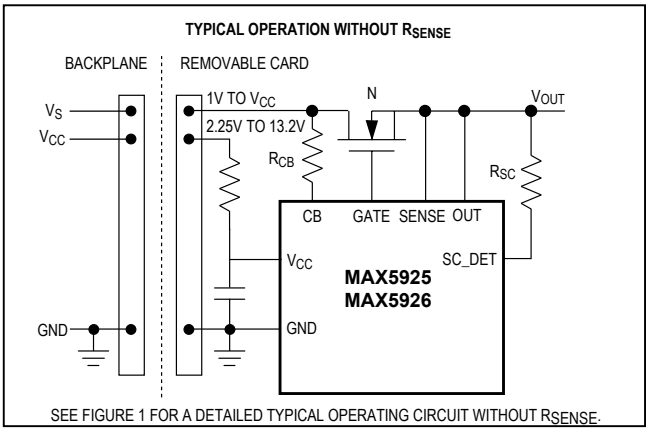
***Selector Guide* and *Ordering Information* appears at end of data sheet.**

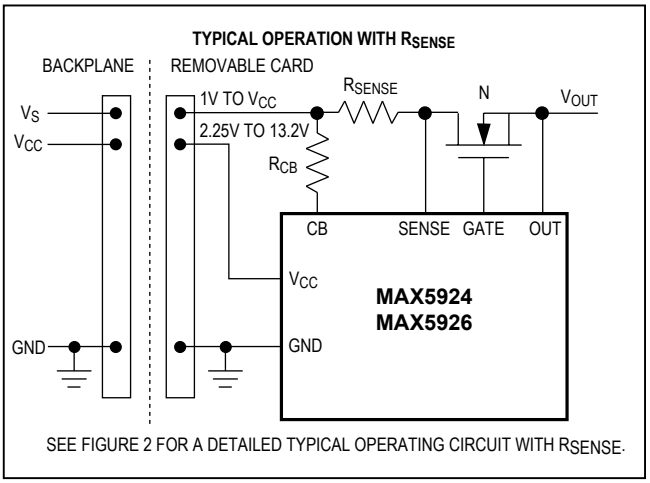
Benefits and Features

- Hot Swap 1V to 13.2V with $V_{CC} \geq 2.25V$
- Drive High-Side nMOSFET
- Operation With or Without R_{SENSE}
- Temperature-Compensated $R_{DS(ON)}$ Sensing
- Protected During Turn-On into Shorted Load
- Adjustable Circuit-Breaker Threshold
- Programmable Slew-Rate Control
- Programmable Turn-On Voltage
- Autoretry or Latched Fault Management
- 10-Pin µMAX® or 16-Pin QSOP Packages

Typical Operating Circuits



SEE FIGURE 1 FOR A DETAILED TYPICAL OPERATING CIRCUIT WITHOUT R_{SENSE}.



SEE FIGURE 2 FOR A DETAILED TYPICAL OPERATING CIRCUIT WITH R_{SENSE}.

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Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V_{CC}.....-0.3V to +14V
GATE*.....-0.3V to +20V
All Other Pins ..... -0.3V to the lower of (V_{CC} + 0.3V) or +14V
SC_DET Current (200ms pulse width, 15% duty cycle) ..140mA
Continuous Current (all other pins).....20mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 6.9mW/°C above +70°C).....556mW
16-Pin QSOP (derate 18.9mW/°C above +70°C) 1509mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

**GATE is internally driven and clamped. Do not drive GATE with external source.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC}, EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.7V to +13.2V; $\overline{EN2}$ (MAX5926) = 0V; V_S (see Figure 1) = +1.05V to V_{CC}; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, R_L = 500Ω from OUT to GND, C_L = 1µF, SLEW = open, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
V_{CC} Operating Range	V_{CC}			2.7		13.2	V
V_S Operating Range	V_S	V_S as defined in Figure 1		1.0		V_{CC}	V
Supply Current	I_{CC}	FET is fully enhanced, SC_DET = V_{CC}			1.5	2.5	mA
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	V_{UVLO}	Default value, V_S and V_{CC} increasing, Figure 1		1.73	2.06	2.47	V
V_{CC} UVLO Deglitch Time	t_{DG}	(Note 2)			900		µs
V_{CC} UVLO Startup Delay	$t_{D,UVLO}$			123	200	350	ms
LOAD-PROBE							
Load-Probe Resistance (Note 3)	R_{LP}	2.7V < V_{CC} < 5V		4	30	65	Ω
		5V < V_{CC} < 13.2V		3	10	20	
Load-Probe Timeout	t_{LP}			43	102	205	ms
Load-Probe Threshold Voltage	$V_{LP,TH}$	(Note 4)		172	200	235	mV
CIRCUIT BREAKER							
Circuit-Breaker Programming Current	I_{CB}	TC = high (MAX5926), MAX5924	V_{CC} = 2.7V and V_{CB} = 1V		37		µA
			2.7V ≤ V_{CC} ≤ 13.2V	34	37	42	
	I_{CB25}	TC = low (MAX5926), MAX5925 (Note 5)	V_{CC} = 2.7V, V_{CB} = 1V, T_A = +25°C	30	40	50	
			V_{CC} = 2.7V, V_{CB} = 1V, T_A = +105°C (MAX5925D)	45	60	80	
			2.7V ≤ V_{CC} ≤ 13.2V, T_A = +25°C	40	50	60	
			2.7V ≤ V_{CC} ≤ 13.2V, T_A = +105°C (MAX5925D)	40	60	80	
	I_{CB85}	TC = low (MAX5926), MAX5925 (Note 5)	V_{CC} = 2.7V and V_{CB} = 1V, T_A = +85°C	40	50	60	
			2.7V ≤ V_{CC} ≤ 13.2V, T_A = +85°C	50	60	70	

Electrical Characteristics (continued)

(V_{CC}, EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.7V to +13.2V; $\overline{EN2}$ (MAX5926) = 0V; V_S (see Figure 1) = +1.05V to V_{CC}; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, R_L = 500Ω from OUT to GND, C_L = 1µF, SLEW = open, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Circuit-Breaker Programming Current During Startup	$I_{CB,SU}$			2 x I_{CB}		µA
Circuit-Breaker Enable Threshold	$V_{CB,EN}$	V_{GATE} - V_{OUT}, rising gate voltage (Note 6)	2.3	3.6	4.65	V
Circuit-Breaker Comparator Offset Voltage	V_{CB_OS}			0.3	±4.7	mV
Fast Circuit-Breaker Offset Resistor	R_{CBF}	Figure 3	1.2	1.9	2.7	kΩ
Slow Circuit-Breaker Delay	t_{CBS}	V_{CB} - V_{SENSE} = 10mV	0.95	1.6	2.95	ms
Fast Circuit-Breaker Delay	t_{CBF}	V_{CB} - V_{SENSE} = 500mV		280		ns
Circuit-Breaker Trip Gate Pulldown Current	$I_{GATE,PD}$	V_{GATE} = 2.5V, V_{CC} = 13.2V, T_A = -40°C to +85°C	13.5	27		mA
		V_{GATE} = 2.5V, V_{CC} = 13.2V, T_A = -40°C to +105°C (MAX5925D)	12	27		mA
Circuit-Breaker Temperature Coefficient	TC_{ICB}	MAX5924, TC = high (MAX5926)		0		ppm/°C
		MAX5925, TC = low (MAX5926)		3300		
OUT Current	I_{OUT}				120	µA
MOSFET DRIVER						
External Gate Drive	V_{GS}	V_{GATE} - V_{OUT}, 2.7V ≤ V_{CC} ≤ 13.2V, T_A = -40°C to +85°C	4.2	5.5	7.2	V
		V_{GATE} - V_{OUT}, 2.7V ≤ V_{CC} ≤ 13.2V, T_A = -40°C to +105°C (MAX5925D)	4.0	5.5	7.2	
Load Voltage Slew Rate	SR	SLEW = open, C_{GATE} = 10nF	2.19	9.5		V/ms
		C_{SLEW} = 300nF, C_{GATE} = 10nF (Note 8)		0.84		
Gate Pullup Current Capacity	I_{GATE}	V_{GATE} = 0V	239			µA
ENABLE COMPARATOR						
EN, EN1 Reference Threshold	$V_{EN/UVLO}$	V_{EN} (MAX5924/MAX5925) or V_{EN1} (MAX5926) rising, T_A = -40°C to +85°C	0.747	0.795	0.850	V
		V_{EN} (MAX5925D) rising, T_A = -40°C to +105°C	0.747	0.795	0.875	
EN, EN1 Hysteresis	$V_{EN,HYS}$			30		mV
EN, EN1 Input Bias Current	I_{EN}	EN (MAX5924/MAX5925) = V_{CC}, EN1 (MAX5926) = V_{CC}		±8	±50	nA
DIGITAL OUTPUTS (PGOOD, $\overline{PGOOD}$)						
Power-Good Output Low Voltage	V_{OL}	I_{OL} = 1mA		0.3	0.4	V
Power-Good Output Open-Drain Leakage Current	I_{OH}	PGOOD/$\overline{PGOOD}$ = 13.2V		0.2	1	µA
Power-Good Trip Point	$V_{THPGOOD}$	V_{GATE} - V_{OUT}, rising gate voltage	V_{CB_EN}	3.6	4.7	V
Power-Good Hysteresis	$V_{PG,HYS}$			0.36		V

Electrical Characteristics (continued)

(V_{CC}, EN (MAX5924/MAX5925), EN1 (MAX5926) = +2.7V to +13.2V; $\overline{EN2}$ (MAX5926) = 0V; V_S (see Figure 1) = +1.05V to V_{CC}; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, R_L = 500Ω from OUT to GND, C_L = 1µF, SLEW = open, T_A = +25°C, unless otherwise noted.) (Note 1)

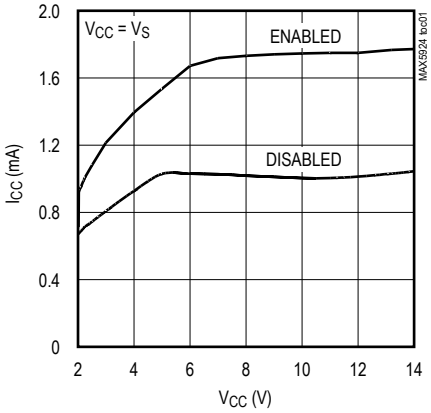
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND TIMING (TC, LATCH (MAX5926), $\overline{EN2}$ (MAX5926)						
Autoretry Delay	t_{RETRY}	Autoretry mode	0.6	1.6	3.3	s
Input Voltage	V_{IH}		2.0			V
	V_{IL}				0.4	
Input Bias Current	I_{BIAS}	Logic high at 13.2V		3		µA
Time to Clear a Latched Fault	T_{CLR}	MAX5924A/MAX5924B MAX5925A/MAX5925B MAX5926 in latched mode		200		µS

Note 1: All devices are 100% tested at T_A = +25°C and +85°C. All temperature limits at -40°C are guaranteed by design.
Note 2: V_{CC} drops 30% below the undervoltage lockout voltage during t_{DG} are ignored.
Note 3: R_{LP} is the resistance measured between V_{CC} and SC_DET during the load-probing phase, t_{LP}.
Note 4: Tested at +25°C and +85°C. Guaranteed by design at -40°C.
Note 5: The circuit-breaker programming current increases linearly from V_{CC} = 2.25V to 5V. See the Circuit-Breaker Current vs. Supply Voltage graph in the *Typical Operating Characteristics*.
Note 6: See the *Startup Mode* section for more information.
Note 7: V_{GATE} is clamped to 17V (typ) above ground.
Note 8: dv/dt = 330 x 10-9/C_{SLEW} (V/ms), nMOS device used for measurement was IRF9530N. Slew rate is measured at the load.

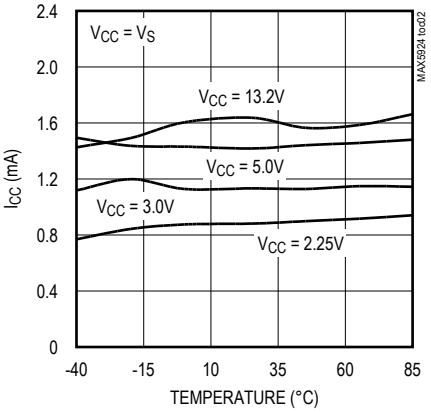
Typical Operating Characteristics

(V_{CC} = 5V, C_L = 1µF, C_{SLEW} = 330nF, C_{GATE} = 10nF, R_L = 500Ω, Figure 1, T_A = +25°C, unless otherwise noted.)

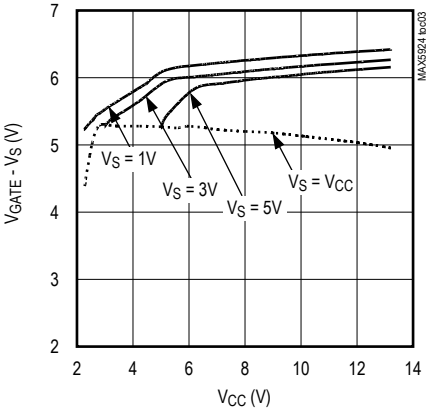
MAX5926 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX5926 SUPPLY CURRENT vs. TEMPERATURE



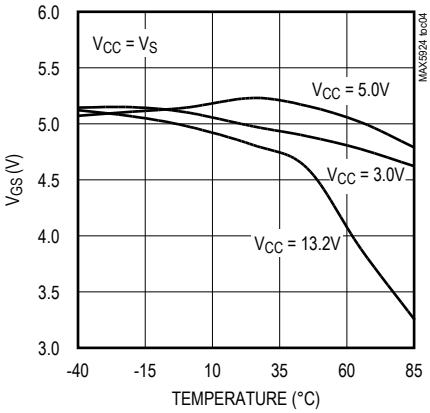
GATE-DRIVE VOLTAGE vs. SUPPLY VOLTAGE



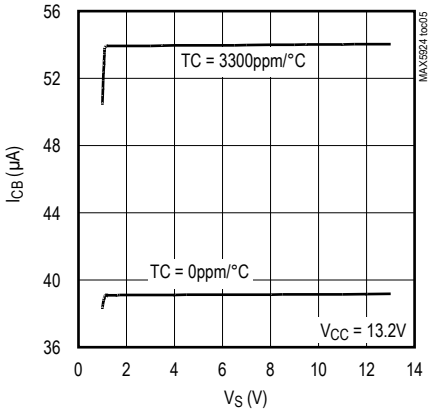
Typical Operating Characteristics (continued)

(V_{CC} = 5V, C_L = 1µF, C_{SLEW} = 330nF, C_{GATE} = 10nF, R_L = 500Ω, Figure 1, T_A = +25°C, unless otherwise noted.)

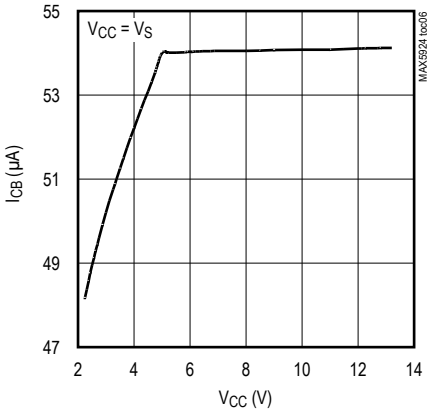
GATE DRIVE VOLTAGE vs. TEMPERATURE



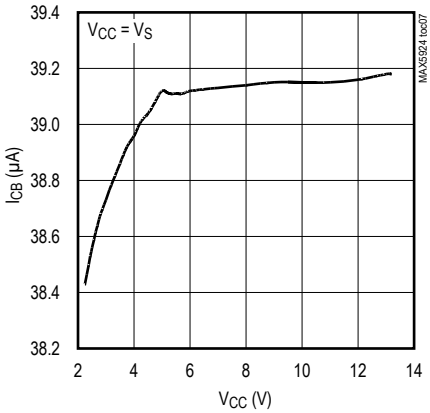
CIRCUIT-BREAKER CURRENT vs. HOT-SWAP VOLTAGE



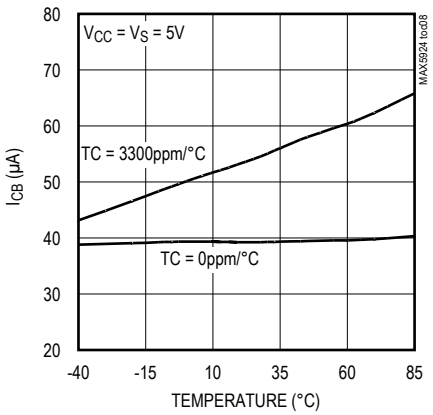
CIRCUIT-BREAKER CURRENT vs. SUPPLY VOLTAGE (TC = 3300ppm/°C)



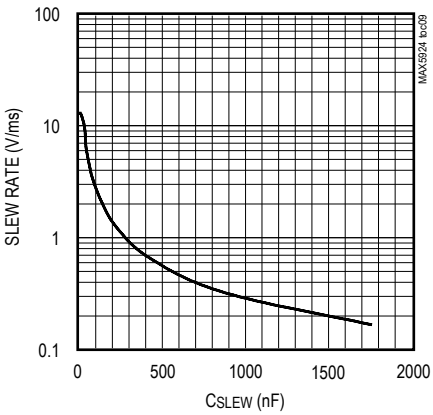
CIRCUIT-BREAKER CURRENT vs. SUPPLY VOLTAGE (TC = 0ppm/°C)



CIRCUIT-BREAKER PROGRAMMING CURRENT vs. TEMPERATURE



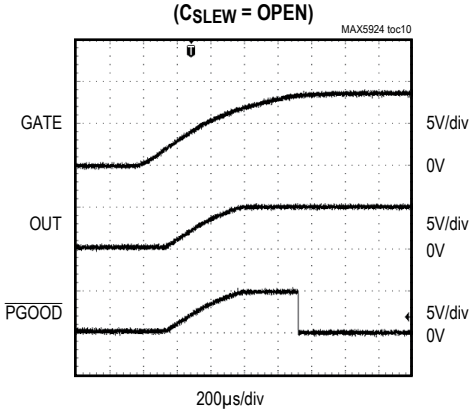
SLEW RATE vs. C_{SLEW}



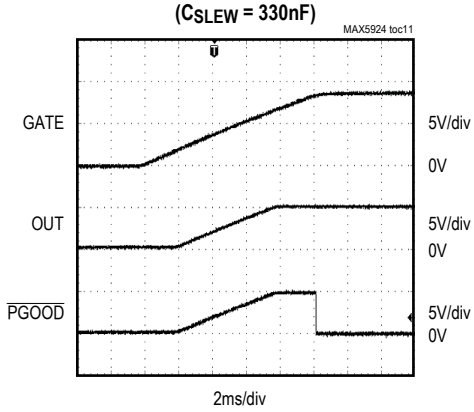
Typical Operating Characteristics (continued)

(V_{CC} = 5V, C_L = 1µF, C_{SLEW} = 330nF, C_{GATE} = 10nF, R_L = 500Ω, Figure 1, T_A = +25°C, unless otherwise noted.)

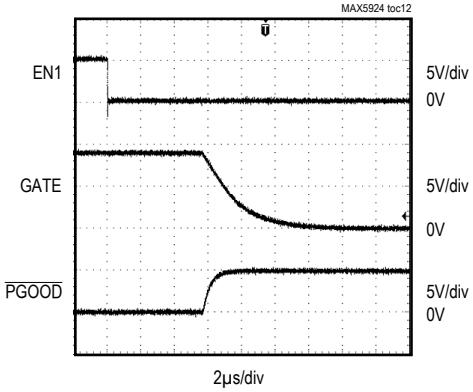
TURN-ON WAVEFORM (C_{SLEW} = OPEN)



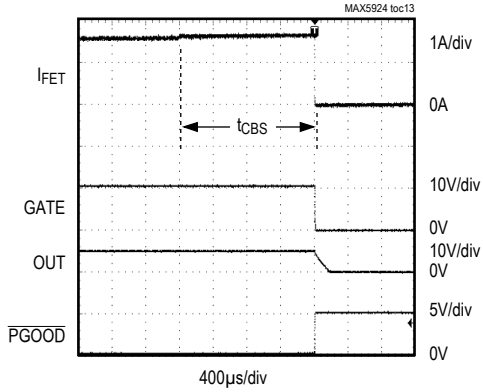
TURN-ON WAVEFORM (C_{SLEW} = 330nF)



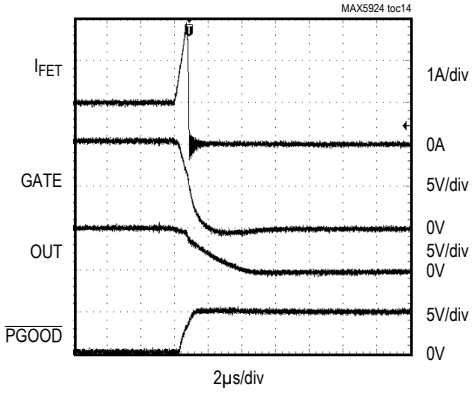
TURN-OFF WAVEFORM



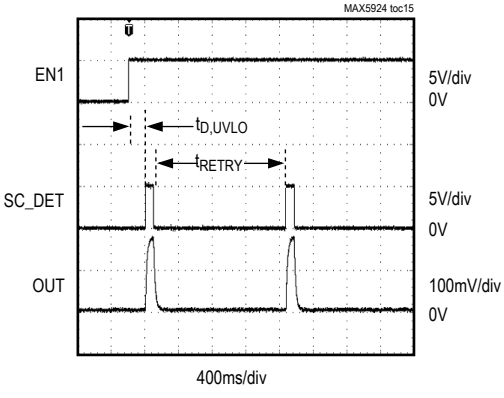
OVERCURRENT CIRCUIT-BREAKER EVENT



SHORT-CIRCUIT CIRCUIT-BREAKER EVENT



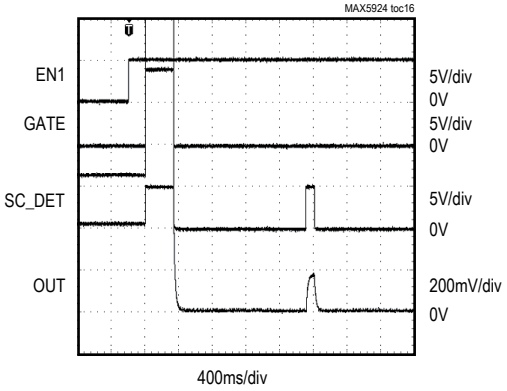
AUTORETRY DELAY



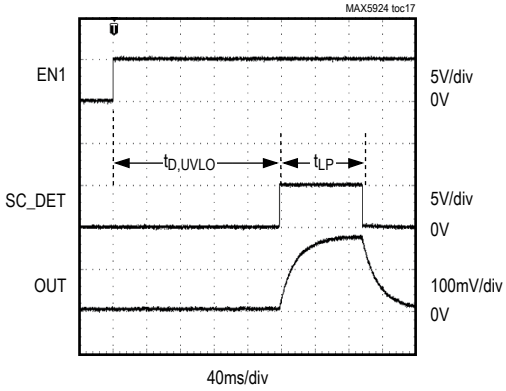
Typical Operating Characteristics (continued)

(V_{CC} = 5V, C_L = 1µF, C_{SLEW} = 330nF, C_{GATE} = 10nF, R_L = 500Ω, Figure 1, T_A = +25°C, unless otherwise noted.)

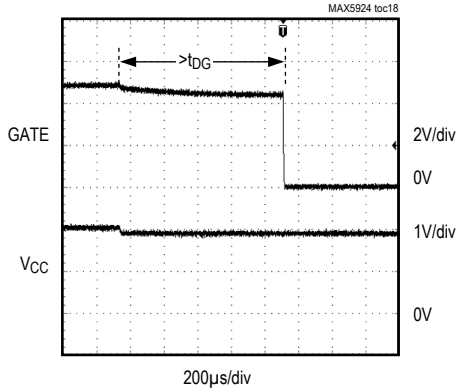
OVERCURRENT FAULT AND AUTORETRY DELAY



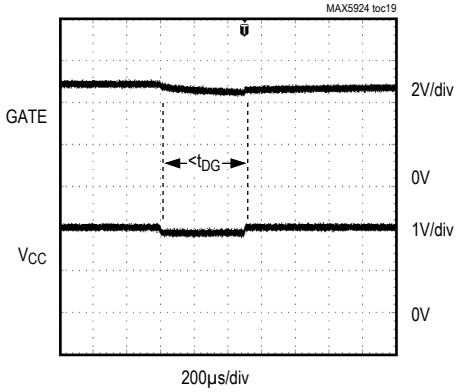
UVLO DELAY AND LOAD PROBING



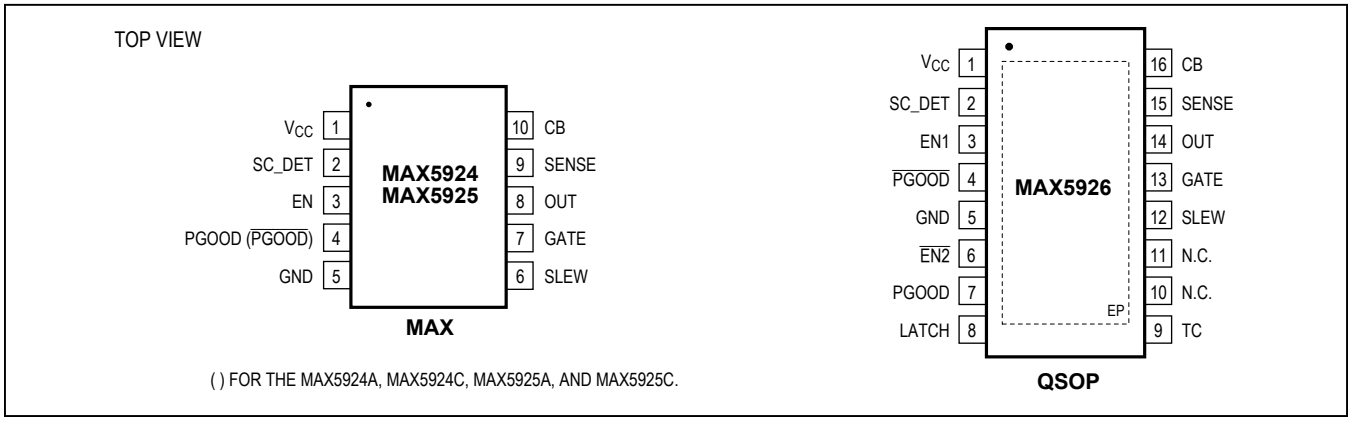
UVLO RESPONSE



UVLO DEGLITCH RESPONSE



Pin Configurations



Pin Description

PIN			NAME	FUNCTION
MAX5924A/ MAX5924C/ MAX5925A/ MAX5925C	MAX5924B/ MAX5924D/ MAX5925B/ MAX5925D	MAX5926		
1	1	1	V_{CC}	Power-Supply Input. Connect V_{CC} to a voltage between 2.47V and 13.2V. **V_{CC} must always be equal to or greater than V_S** (see Figure 1).
2	2	2	SC_DET	Short-Circuit Detection Output. Connect SC_DET to V_{OUT} through a series resistor, R_{SC}, when not using R_{SENSE}. SC_DET forces current (limited to ≈200mA) into the external load through R_{SC} at startup to determine whether there is a short circuit (load probing). Connect SC_DET directly to V_{CC} when using R_{SENSE}, Do not connect SC_DET to V_{CC} when not using R_{SENSE} in an attempt to disable load probing.
3	3	—	EN	ON/OFF Control Input. Drive EN high to enable the device. Drive EN low to disable the device. An optional external resistive-divider connected between V_{CC}, EN, and GND sets the programmable turn-on voltage.
4	—	4	$\overline{PGOOD}$	Open-Drain Active-Low Power-Good Output
—	4	7	PGOOD	Open-Drain Active-High Power-Good Output
5	5	5	GND	Ground
6	6	12	SLEW	Slew-Rate Adjustment Input. Connect an external capacitor between SLEW and GND to adjust the gate slew rate. Leave SLEW unconnected for the default slew rate.
7	7	13	GATE	Gate-Drive Output. Connect GATE to the gate of the external n-channel MOSFET.
8	8	14	OUT	Output Voltage. Connect OUT to the source of the external MOSFET.
9	9	15	SENSE	Circuit-Breaker Sense Input. Connect SENSE to OUT when not using an external R_{SENSE} (Figure 1). Connect SENSE to the drain of the external MOSFET when using an external R_{SENSE} (Figure 2).
10	10	16	CB	Circuit-Breaker Threshold Programming Input. Connect an external resistor, R_{CB}, from CB to V_S to set the circuit-breaker threshold voltage.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX5924A/ MAX5924C/ MAX5925A/ MAX5925C	MAX5924B/ MAX5924D/ MAX5925B/ MAX5925D	MAX5926		
—	—	3	EN1	Active-High ON/OFF Control Input. Drive EN1 high to enable the device when $\overline{EN2}$ is low. Drive EN1 low to disable the device, regardless of the state of $\overline{EN2}$. An optional external resistive-divider between V_{CC}, EN1, and GND sets the programmable turn-on voltage while $\overline{EN2}$ is low.
—	—	6	$\overline{EN2}$	Active-Low ON/OFF Control Input. Drive $\overline{EN2}$ low to enable the device when EN1 is high. Drive $\overline{EN2}$ high to disable the device, regardless of the state of EN1.
—	—	8	LATCH	Latch Mode Input. Drive LATCH low for autoretry mode. Drive LATCH high for latched mode.
—	—	9	TC	Circuit-Breaker Temperature Coefficient Selection Input. Drive TC low to select a 3300ppm/°C temperature coefficient. Drive TC high to select a 0ppm/°C temperature coefficient.
—	—	10, 11	N.C.	No Connection. Not internally connected.
—	—	EP	EP	Exposed Pad. Connect EP to GND.

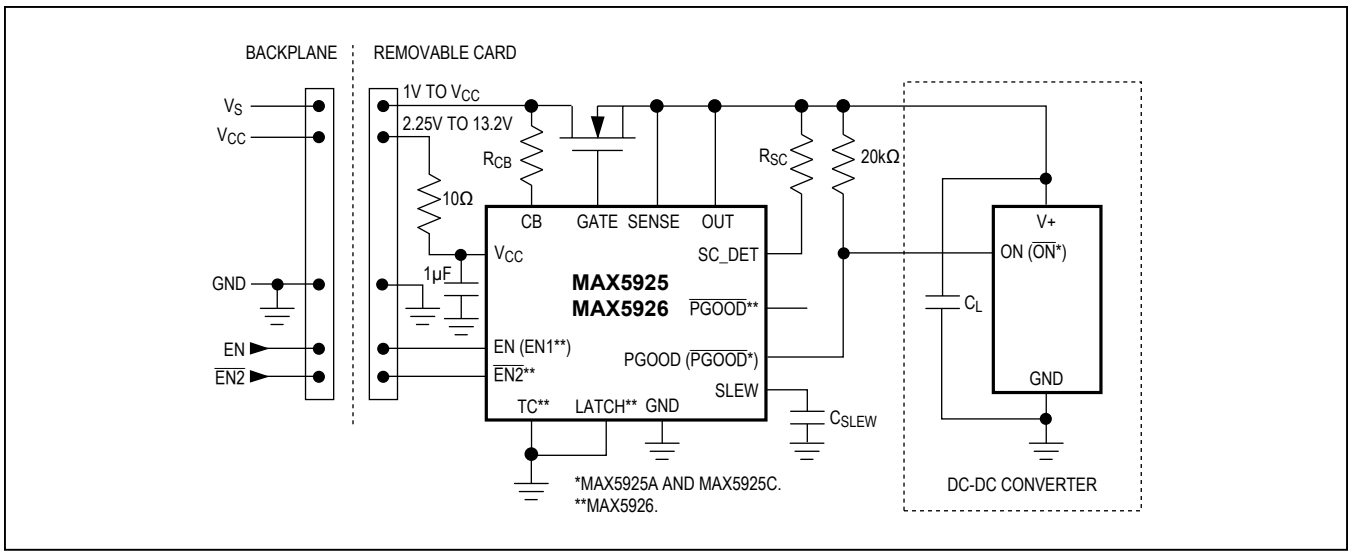


Figure 1. Typical Operating Circuit (Without R_{SENSE})

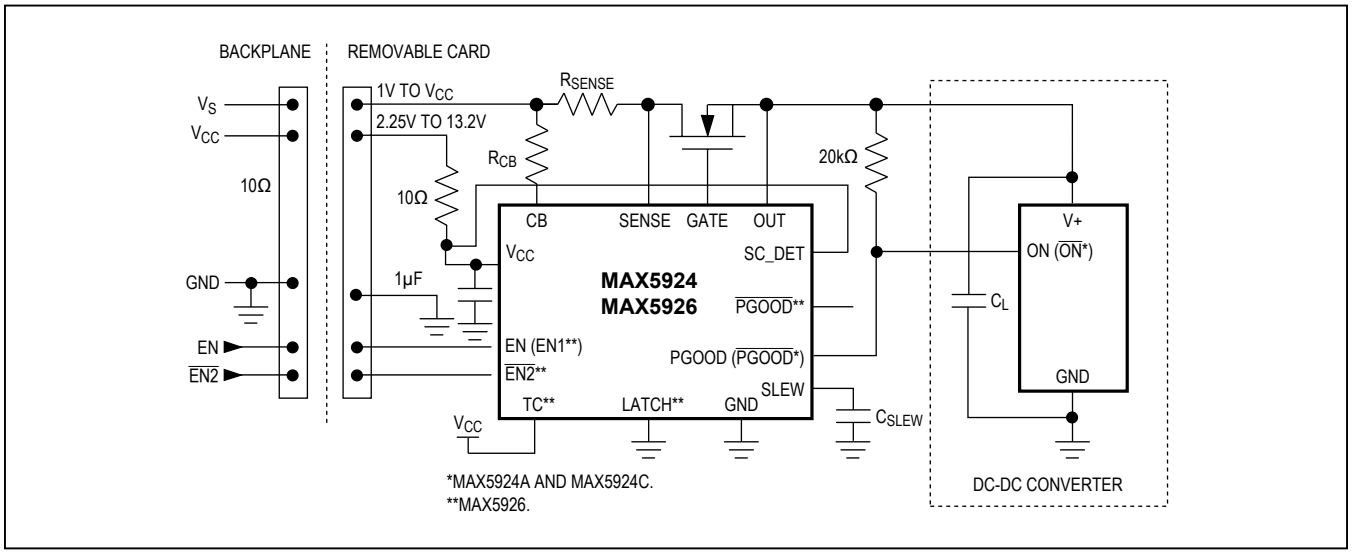


Figure 2. Typical Operating Circuit (With R_{SENSE})

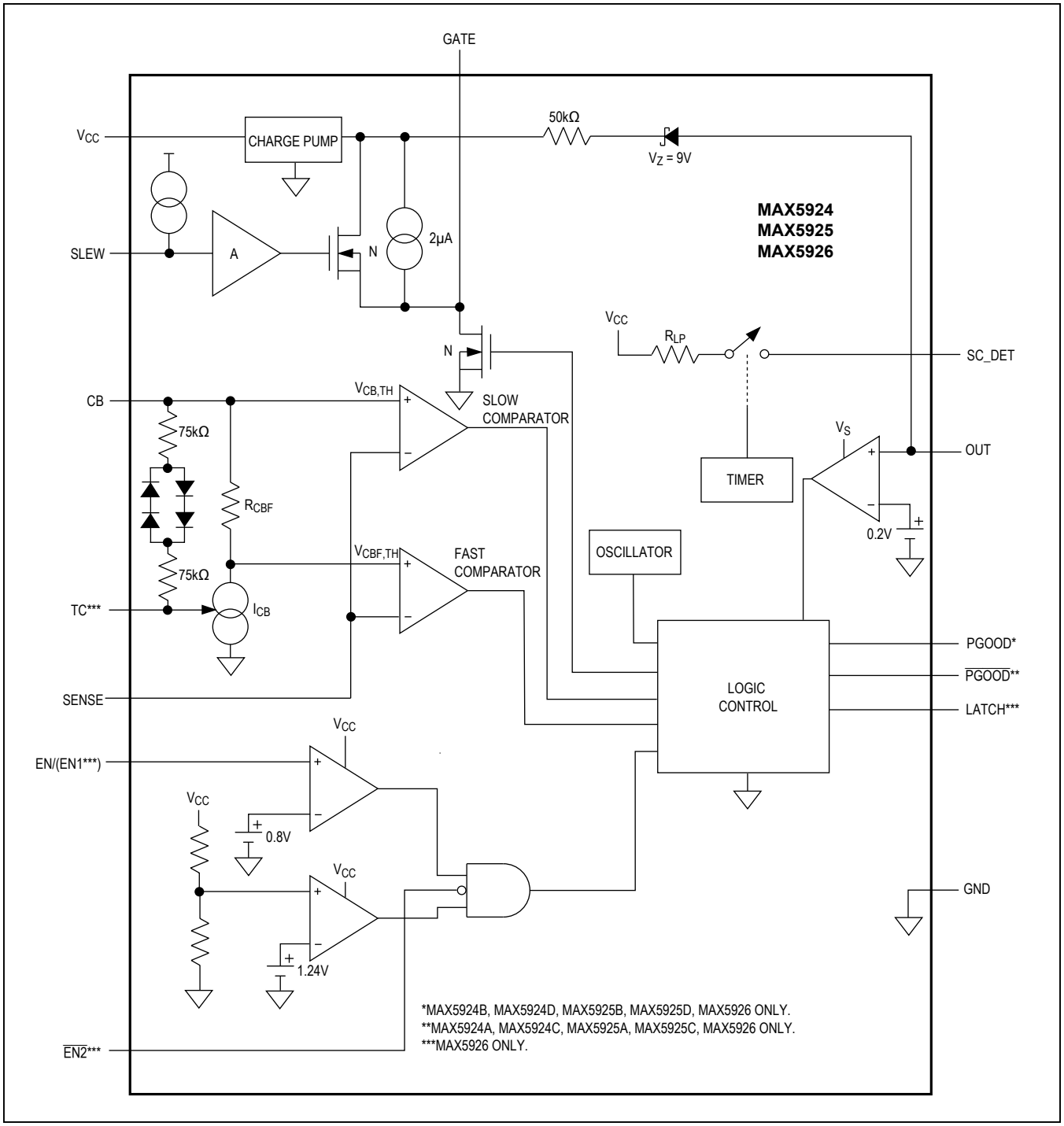


Figure 3. Functional Diagram

Detailed Description

The MAX5924/MAX5925/MAX5926 are hot-swap controller ICs designed for applications where a line card is inserted into a live backplane. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide a low impedance that can momentarily cause the main power supply to collapse. The MAX5924/MAX5925/MAX5926 are designed to reside either in the backplane or in the removable card to provide inrush current limiting and short-circuit protection. This is achieved using an external nMOSFET and an optional external current-sense resistor.

Several critical parameters can be configured:

- Slew rate (inrush current)
- Circuit-breaker threshold
- Turn-on voltage
- Fault-management mode (MAX5926)
- Circuit-breaker temperature coefficient (MAX5926)

See the *Selector Guide* for a device-specific list of factory-preset features and parameters.

Startup Mode

It is important that both V_{CC} and V_S rise at a minimum rate of 100mV/ms during the critical time when power voltages are below those values required for proper logic control of internal circuitry. This applies for $0.5V \le V_{CC} \le 2.5V$ and $0.5V \le V_S \le 0.8V$. This is particularly true when LATCH is tied high.

The MAX5924/MAX5925/MAX5926 control an external MOSFET placed in the positive power-supply pathway. When power is first applied, the MAX5924/MAX5925/MAX5926 hold the MOSFET off indefinitely if the supply voltage is below the undervoltage lockout level or if the device is disabled (see the *EN (MAX5924/MAX5925), EN1/$\overline{EN2}$ (MAX5926)* section). If neither of these conditions exist, the device enters a UVLO startup delay period for ≈200ms. Next, the MAX5924/MAX5925/MAX5926 detect whether an external sense resistor is present; and then autoconfigure accordingly (see Figure 4).

- If no sense resistor is present, bilevel fault protection is disabled and load-probing circuitry is enabled (see the *Load Probing* section).

  If load probing is not successful, the fault is managed according to the selected fault management mode (see the *Latched and Autoretry Fault Management* section).

  If load probing (see the *Load Probing* section) is successful, slew-rate limiting is employed to gradually turn on the MOSFET.

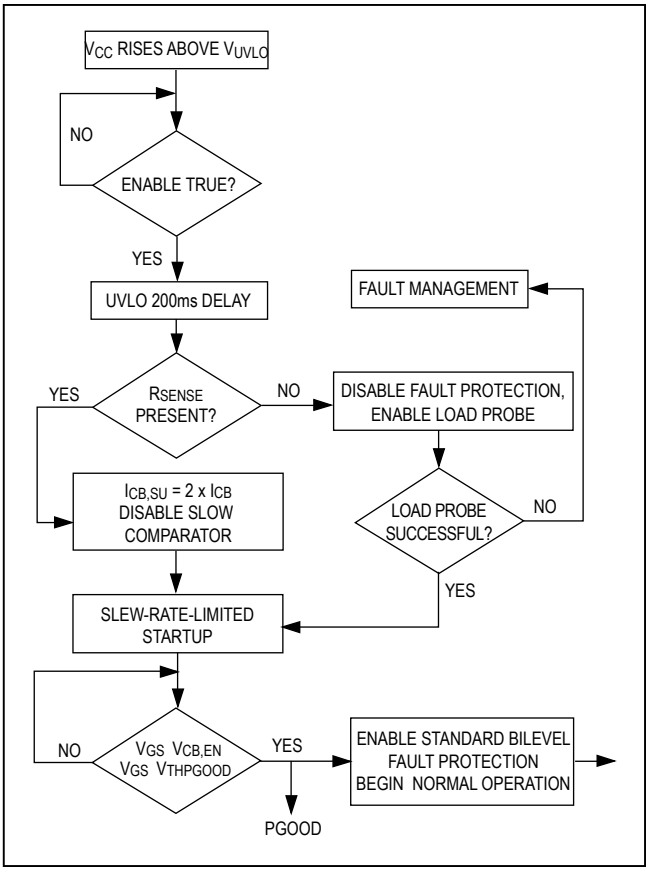


Figure 4. Startup Flow Chart

- If the device detects an external R_{SENSE}, circuit-breaker threshold is set at $2xI_{CB}$, the slow comparator is disabled, the startup phase begins without delay for load probing, and slew-rate limiting is employed to gradually turn on the MOSFET.

During the startup phase, the voltage at the load, V_{OUT}, rises at a rate determined by the selected slew rate (see the *Slew Rate* section). The inrush current (I_{INRUSH}) to the load is limited to a level proportional to the load capacitance (C_L) and the slew rate:

$$I_{INRUSH} = \frac{C_L \times SR}{1000}$$

where SR is the slew rate in V/ms and C_L is load capacitance in µF.

For operation with and without R_{SENSE}, once V_{GATE} - V_{OUT} exceeds $V_{CB,EN}$, PGOOD and/or $\overline{PGOOD}$ assert. When V_{GATE} - V_{OUT} = $V_{CB,EN}$, the devices enable standard bilevel fault protection with normal I_{CB} (see the *Bilevel Fault Protection* section).

Load Probing

The devices' load-probing circuitry detects short-circuit conditions during startup. Load probing is active only when no external R_{SENSE} is detected. As the device begins load probing, SC_DET is connected to V_{CC} through an internal switch with an on-resistance of R_{LP} (Figure 6). V_{CC} then charges the load with a probe current limited at ≈200mA.

$$I_{PROBE} = (V_{CC} - V_{OUT})/(R_{LP} + R_{SC})$$ (Figure 1)

If the load voltage does not reach $V_{LP,TH}$ (0.2V typ) within t_{LP}, a short-circuit fault is detected and the startup mode is terminated according to the selected fault-management mode (see the *Latched and Autoretry Fault Management* section and Figure 5). If no fault condition is present, PGOOD/$\overline{PGOOD}$ asserts at the end of the startup period (see the Turn-On Waveforms in the *Typical Operating Characteristics*).

Load probing can only be, and must be, employed when not using an external R_{SENSE}.

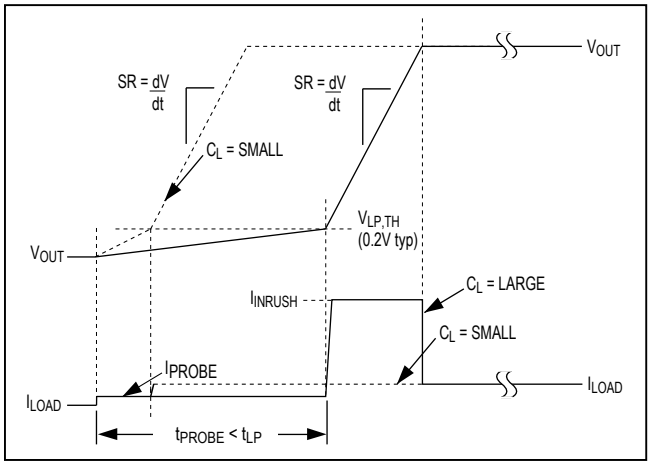


Figure 5. Startup Waveform

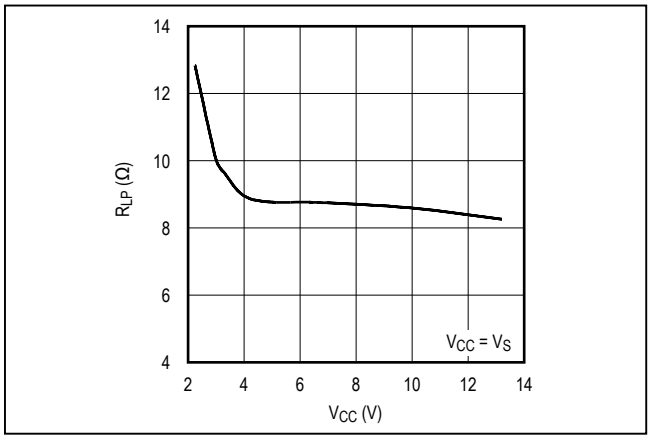


Figure 6. Load-Probe Resistance vs. Supply Voltage

Normal Operation

In normal operation, after startup is complete, protection is provided by turning off the external MOSFET when a fault condition is encountered. Dual-speed/bilevel fault protection incorporates two comparators with different thresholds and response times to monitor the current:

1) Slow comparator. This comparator has a 1.6ms (typ) response time. The slow comparator ignores low-amplitude momentary current glitches. After an extended overcurrent condition, a fault is acknowledged and the MOSFET gate is discharged.
2) Fast comparator. This comparator has a quick response time and a higher threshold voltage. The fast comparator turns off the MOSFET immediately when it detects a large high-current event such as a short circuit.

In each case, when a fault is encountered, the power-good output deasserts and the device drives GATE low. After a fault, the MAX5924A, MAX5924B, MAX5925A, and MAX5925B latch GATE low and the MAX5924C, MAX5924D, MAX5925C, and MAX5925D enter the autoretry mode. The MAX5926 has selectable latched

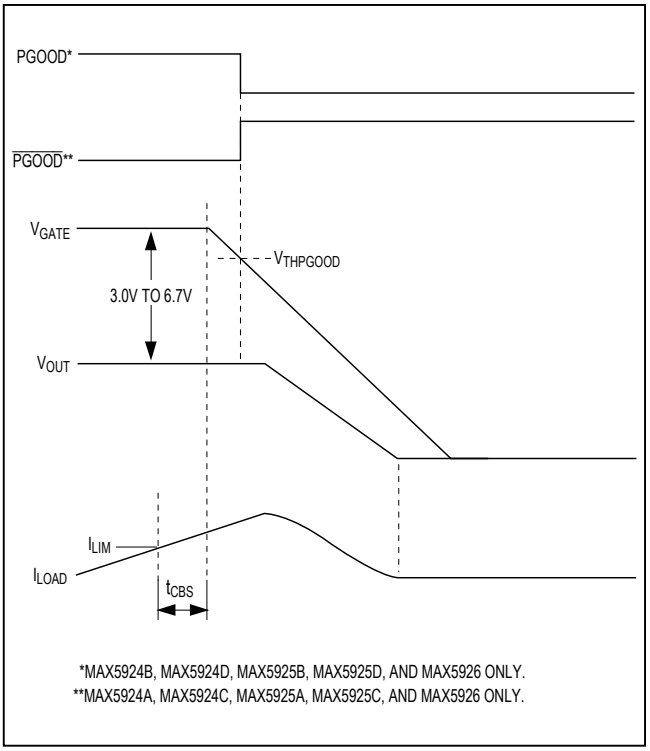


Figure 7. Slow Comparator Response to an Overcurrent Fault

or autoretry modes. Figure 7 shows the slow comparator response to an overcurrent fault.

Bilevel Fault Protection

Bilevel Fault Protection in Startup Mode

Bilevel fault protection is disabled in startup mode, and is enabled when $V_{GATE-VOUT}$ exceeds $V_{CB,EN}$ at the end of the startup period.

When no R_{SENSE} is detected, neither slow nor fast comparator is active during startup because the high $R_{D(ON)}$ of the MOSFET when not fully enhanced would signal an artificially-high $V_{IN-VSENSE}$ voltage. Load probing prior to startup insures that the output is not short-circuited.

When R_{SENSE} is detected, the slow comparator is disabled during startup while the fast comparator remains active. The overcurrent trip level is higher than normal during the startup period because the ICB is temporarily doubled to ICB,SU at this time. This allows higher than normal startup current to allow for output capacitor charging current.

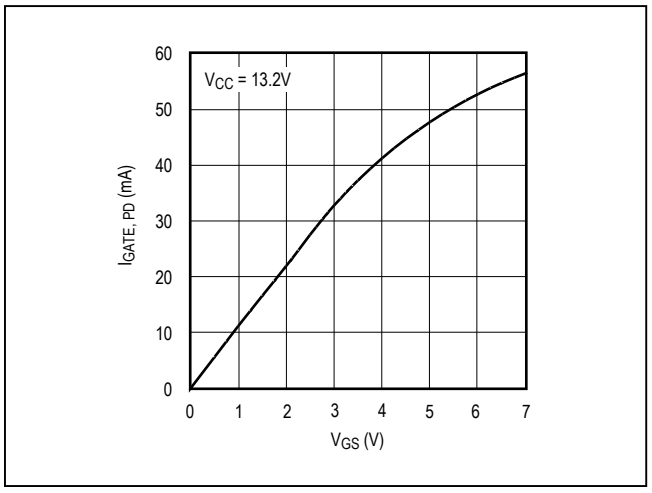


Figure 8a. Gate Discharge Current vs. MOSFET Gate-to-Source Voltage

Table 1. Selecting Fault Management Mode (MAX5926)

LATCH	FAULT MANAGEMENT
Low	Autoretry mode
High	Latched mode

Slow Comparator

The slow comparator is disabled during startup while the external MOSFET turns on.

If the slow comparator detects an overload condition while in normal operation (after startup is complete), it turns off the external MOSFET by discharging the gate capacitance with $I_{GATE,PD}$. The magnitude of $I_{GATE,PD}$ depends on the external MOSFET gate-to-source voltage (V_{GS}). The discharge current is strongest immediately following a fault and decreases as the MOSFET gate is discharged (Figure 8a).

Fast Comparator

The fast comparator is used for serious current overloads or short circuits. If the load current reaches the fast comparator threshold, the device quickly forces the MOSFET off. The fast comparator has a response time of 280ns, and discharges GATE with $I_{GATE,PD}$ (Figure 8a). The fast comparator is disabled during startup when no R_{SENSE} is detected

Latched and Autoretry Fault Management

The MAX5924A, MAX5924B, MAX5925A, and MAX5925B latch the external MOSFET off when an overcurrent fault is detected. Following an overcurrent fault, the MAX5924C, MAX5924D, MAX5925C, and MAX5925D enter autoretry mode. The MAX5926 can be configured for either latched or autoretry mode (see Table 1).

In autoretry, a fault turns the external MOSFET off then automatically restarts the device after the autoretry delay, t_{RETRY}. During the autoretry delay, pull EN or EN1 low to restart the device. In latched mode, pull EN or EN1 low for at least 100µs to clear a latched fault and restart the device.

Power-Good Outputs

The power-good output(s) are open-drain output(s) that deassert:

- When $V_{CC} < V_{UVLO}$
- During $t_{D,UVLO}$
- When $V_{GS} < V_{THPGOOD}$
- During load probing
- When disabled (EN = GND (MAX5924/MAX5925), EN1 = GND or $\overline{EN2}$ = high (MAX5926))
- During fault management
- During t_{RETRY} or when latched off (MAX5924A, MAX5924B, MAX5925A, MAX5925B, or MAX5926 (LATCH = low)).

PGOOD/$\overline{PGOOD}$ asserts only if the part is in normal mode and no faults are present.

Undervoltage Lockout (UVLO)

UVLO circuitry prevents the devices from turning on the external MOSFET until V_{CC} exceeds the UVLO threshold, V_{UVLO}, for $t_{D,UVLO}$. UVLO protects the external MOSFET from insufficient gate-drive voltage, and $t_{D,UVLO}$ ensures that the board is fully plugged into the backplane and V_{CC} is stable prior to powering the hot-swapped system. Any input voltage transient at V_{CC} below the UVLO threshold for more than the UVLO deglitch period (t_{DG}) resets the device and initiates a startup sequence. Device operation is protected from momentary input-voltage steps extending below the UVLO threshold for a deglitch period, t_{DG}. However, the power-good output(s) may momentarily deassert if the magnitude of a negative step in V_{CC} exceeds approximately 0.5V, and V_{CC} drops below V_{UVLO}. Operation is unaffected and the power-good output(s) assert(s) within 200µs, as shown in Figure 8b. This figure also shows that if the UVLO condition exceeds t_{DG} = 900µs (typ), the power-good output(s) again deassert(s) and the load is disconnected.

Determining Inrush Current

Determining a circuit's inrush current is necessary to choose a proper MOSFET. The MAX5924/MAX5925/MAX5926 regulate the inrush current by controlling the output-voltage slew rate, but inrush current is also a function of load capacitance. Determine an anticipated inrush current using the following equation:

$$I_{INRUSH}(A) = C_L \frac{dV_{OUT}}{dt \times 1000} = C_L \times SR$$

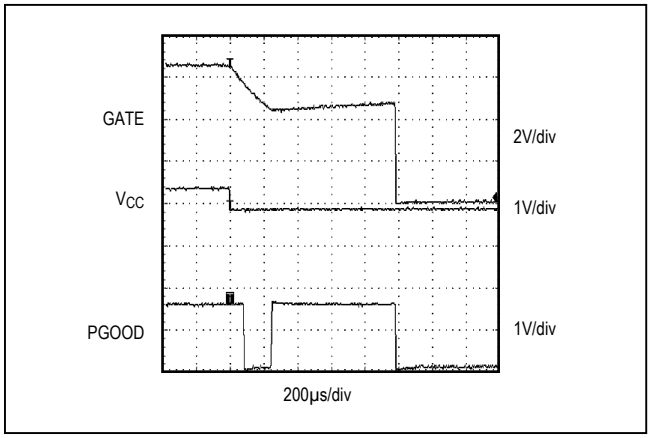


Figure 8b. PGOOD Behavior with Large Negative Input-Voltage Step when VS is Near $V_{S(MIN)}$

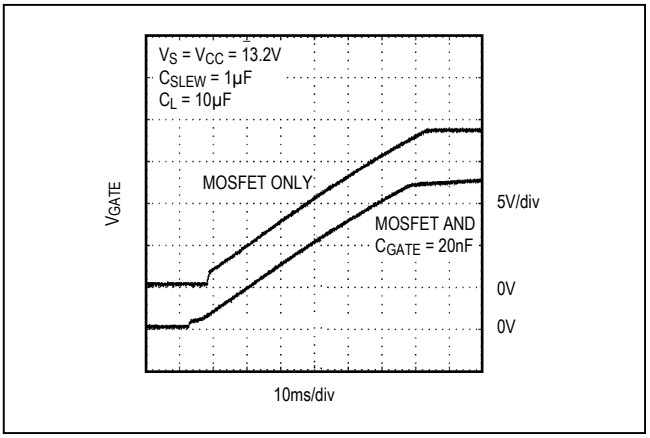


Figure 9. Impact of C_{GATE} on the V_{GATE} Waveform

where C_L is the load capacitance in µF and SR is the selected device output slew rate in V/ms. For example, assuming a load capacitance of 100µF and using the value of SR = 10V/ms, the anticipated inrush current is 1A. If a 16V/ms output slew rate is used, the inrush current increases to 1.6A. Choose SR so the maximum anticipated inrush current does not trip the fast circuit-breaker comparator during startup.

Slew Rate

The MAX5924/MAX5925/MAX5926 limit the slew rate of V_{OUT}. Connect an external capacitor, C_{SLEW}, between SLEW and GND to adjust the slew-rate limit. Floating SLEW sets the maximum slew rate to the minimum value. Calculate C_{SLEW} using the following equation:

$$C_{SLEW} = 330 \ \ 10^{-9} / SR$$

where, SR is the desired slew rate in V/ms and C_{SLEW} is in nF.

This equation is valid for $C_{SLEW} \geq 100nF$. For higher SR, see the *Typical Operating Characteristics*.

A 2µA (typ) pullup current clamped to 1.4V causes an initial jump in the gate voltage, V_{GATE}, if C_{GATE} is small and the slew rate is slow (Figure 3). Figure 9 illustrates how the addition of gate capacitance minimizes this initial jump. C_{GATE} should not exceed 25nF.

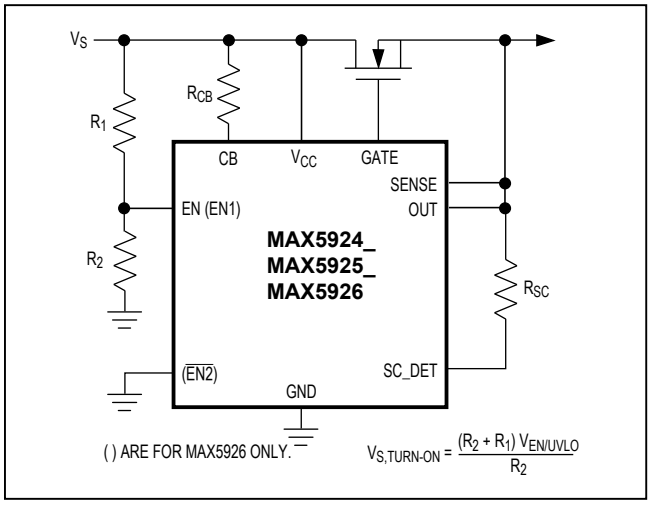


Figure 10. Adjustable Turn-On Voltage

EN (MAX5924/MAX5925), EN1/$\overline{EN2}$ (MAX5926)

The enable comparators control the on/off function of the MAX5924/MAX5925/MAX5926. Enable is also used to reset the fault latch in latch mode. Pull EN or EN1 low for 100µs to reset the latch. A resistive divider between EN or EN1, V_S, and GND sets the programmable turn-on voltage to a voltage greater than V_{UVLO} (Figure 10).

Selecting a Circuit-Breaker Threshold

The MAX5924/MAX5925/MAX5926 offer a circuit-breaker function to protect the external MOSFET and the load from the potentially damaging effects of excessive current. As load current flows through $R_{DS(ON)}$ (Figure 12) or R_{SENSE} (Figure 13), a voltage drop is generated. After V_{GS} exceeds $V_{CB,EN}$, the MAX5924/MAX5925/MAX5926 monitor this voltage to detect overcurrent conditions. If this voltage exceeds the circuit-breaker threshold, the

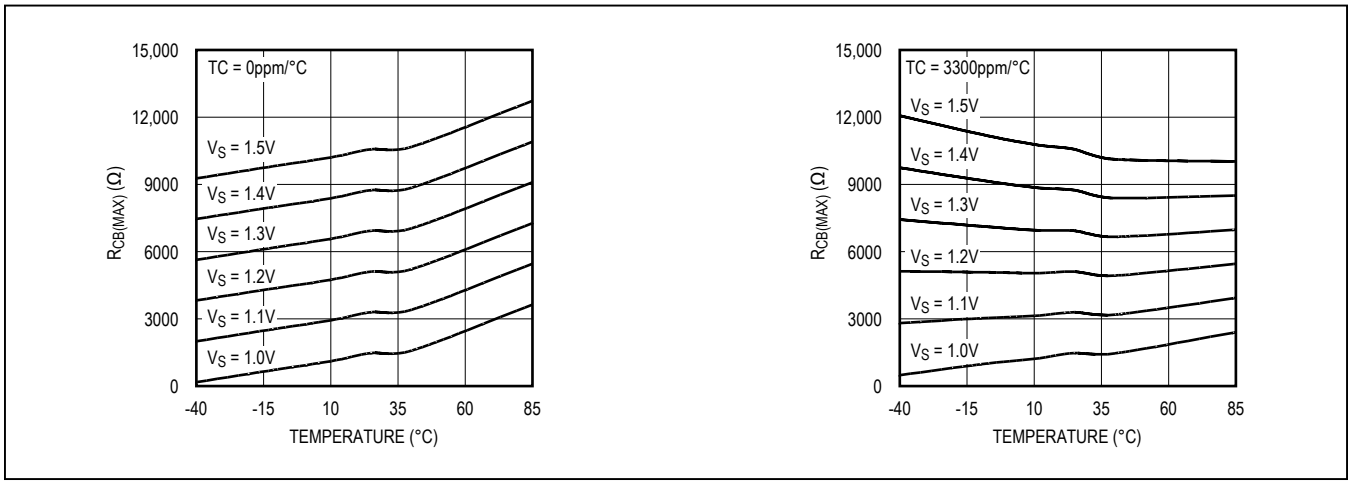


Figure 11. Maximum Circuit-Breaker Programming Resistor vs. Temperature

external MOSFET turns off and the power-good output(s) deassert(s). To accommodate different MOSFETs, sense resistors, and load currents, the MAX5924/MAX5925/MAX5926 voltage across R_{CB} can be set between 10mV and 500mV. The value of the circuit-breaker voltage must be carefully selected based on V_S (Figure 11).

No R_{SENSE} Mode

When operating without R_{SENSE}, calculate the circuit-breaker threshold using the MOSFET's $R_{DS(ON)}$ at the worst possible operating condition, and add a 20% overcurrent margin to the maximum circuit current. For example, if a MOSFET has an $R_{DS(ON)}$ of 0.06Ω at T_A = +25°C, and a normalized on-resistance factor of 1.75 at T_A = +105°C, the $R_{DS(ON)}$ used for calculation is the product of these two numbers, or (0.06Ω) x (1.75) = 0.105Ω. Then, if the maximum current is expected to be 2A, using a 20% margin, the current for calculation is (2A) x (1.2) = 2.4A. The resulting minimum circuit-breaker threshold is then a product of these two numbers, or (0.105Ω) x (2.4A) = 0.252V. Using this method to choose a circuit-breaker threshold allows the circuit to operate under worst-case conditions without causing a circuit-breaker fault, but the circuit-breaker function will still detect a short circuit or a gross overcurrent condition.

To determine the proper circuit-breaker resistor value use the following equation, which refers to Figure 12:

$$R_{CB} = \frac{(I_{TRIPSLOW} \times R_{DS(ON)(T)}) + |V_{CB,OS}|}{I_{CB}}$$

where $I_{TRIPSLOW}$ is the desired slow-comparator trip current.

The fast-comparator trip current is determined by the selected R_{CB} value and cannot be adjusted independently. The fast-comparator trip current is given by:

$$I_{TRIPFAST} = \frac{I_{CB} \times (R_{CBF} + R_{CB}) \pm V_{CB,OS}}{R_{DS(ON)(T)}}$$

SC_DET must be connected to OUT through the selected R_{SC} when not using R_{SENSE}.

R_{SENSE} Mode

When operating with R_{SENSE}, calculate the circuit-breaker threshold using the worst possible operating conditions, and add a 20% overcurrent margin to the maximum circuit current. For example, with a maximum expected current of 2A, using a 20% margin, the current for calculation is (2A) x (1.2) = 2.4A. The resulting minimum circuit-

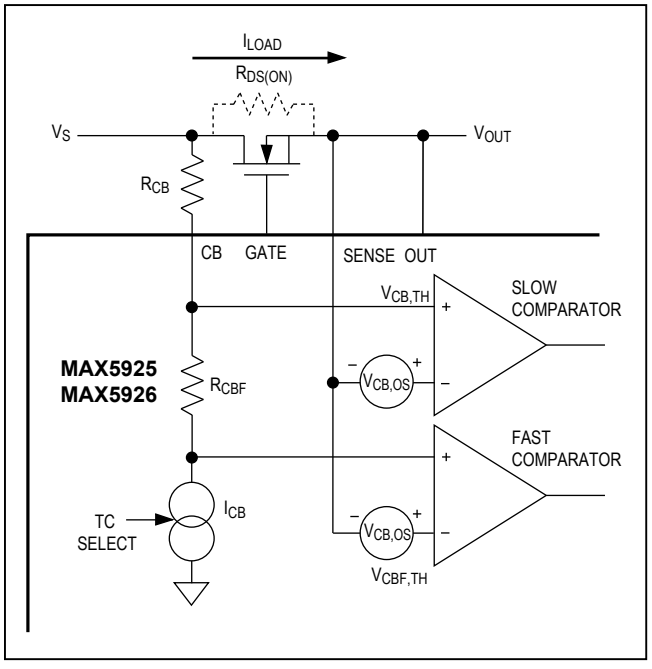


Figure 12. Circuit Breaker Using $R_{DS(ON)}$

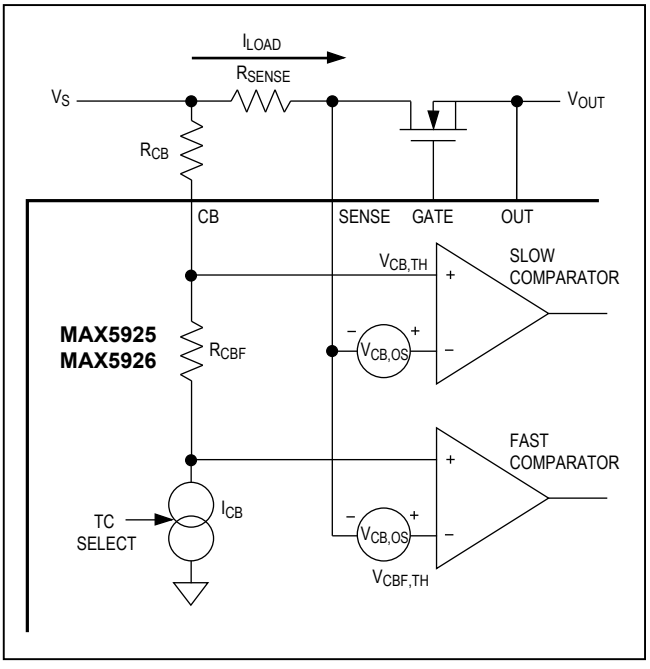


Figure 13. Circuit Breaker Using R_{SENSE}

breaker threshold is then a product of this current and R_{SENSE} = 0.06Ω, or (0.06Ω) x (2.4A) = 0.144V. Using this method to choose a false circuit-breaker threshold allows the circuit to operate under worst-case conditions without causing a circuit-breaker fault, but the circuit-breaker function will still detect a short-circuit or a gross overcurrent condition.

To determine the proper circuit-breaker resistor value, use the following equation, which refers to Figure 13:

$$R_{CB} = \frac{(I_{TRIPSLOW} \times R_{SENSE}) + |V_{CB,OS}|}{I_{CB}}$$

where, $I_{TRIPSLOW}$ is the desired slow-comparator trip current.

The fast-comparator trip current is determined by the selected R_{CB} value and cannot be adjusted independently. The fast-comparator trip current is given by:

$$I_{TRIPFAST} = \frac{I_{CB} \times (R_{CBF} + R_{CB}) \pm V_{CB,OS}}{R_{SENSE}}$$

SC_DET should be connected to V_{CC} when using R_{SENSE}.

Circuit-Breaker Temperature Coefficient

In applications where the external MOSFET's on-resistance is used as a sense resistor to determine overcurrent conditions, a 3300ppm/°C temperature coefficient is desirable to compensate for the $R_{DS(ON)}$ temperature coefficient. Use the MAX5926's TC input to select the circuit-breaker programming current's temperature coefficient, TC_{ICB} (see Table 2). The MAX5924 temperature coefficient is preset to 0ppm/°C, and the MAX5925's is preset to 3300ppm/°C.

Setting TC_{ICB} to 3300ppm/°C allows the circuit-breaker threshold to track and compensate for the increase in the MOSFET's $R_{DS(ON)}$ with increasing temperature. Most MOSFETs have a temperature coefficient within a 3000ppm/°C to 7000ppm/°C range. Refer to the MOSFET data sheet for a device-specific temperature coefficent.

$R_{DS(ON)}$ and I_{CB} are temperature dependent, and can therefore be expressed as functions of temperature. At a given temperature, the MAX5925/MAX5926 indicate an overcurrent condition when:

$$I_{TRIPSLOW} \times R_{DS(ON)}(T) \geq I_{CB}(T) \times R_{CB} + |V_{CB,OS}|$$

Table 2. Programming the Temperature Coefficient (MAX5926)

TC	TC_{ICB} (ppm/°C)
High	0
Low	3300

Table 3. Suggested External MOSFETs

APPLICATION CURRENT (A)	PART	DESCRIPTION
1	International Rectifier IRF7401	SO-8
2	Siliconix Si4378DY	SO-8
5	Siliconix SUD40N02-06	DPAK
10	Siliconix SUB85N02-03	D2PAK

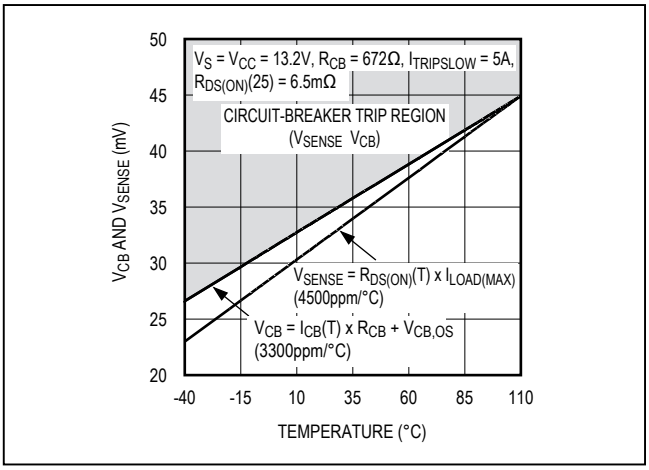


Figure 14. Circuit-Breaker Trip Point and Current-Sense Voltage vs. Temperature

where $V_{CB,OS}$ is the worst-case offset voltage. Figure 14 graphically portrays operating conditions for a MOSFET with a 4500ppm/°C temperature coefficient.

Applications Information

Component Selection

nMOSFET

Most circuit component values may be calculated with the aid of the devices. The "Design calculator for choosing component values" software can be downloaded from the MAX5924–MAX5926 Quickview on the Maxim website.

Table 4. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistors	Dale-Vishay	402-564-3131	www.vishay.com
	IRC	828-264-8861	www.irctt.com
MOSFETs	Fairchild	888-522-5372	www.fairchildsemi.com
	International Rectifier	310-233-3331	www.irf.com

Select the external nMOSFET according to the application's current and voltage level. Table 3 lists some recommended components. Choose the MOSFET's on-resistance, $R_{DS(ON)}$, low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ can cause undesired power loss and output ripple if the board has pulsing loads or triggers an external undervoltage reset monitor at full load. Determine the device power-rating requirement to accommodate a short circuit on the board at startup with the device configured in autoretry mode.

Using the devices in latched mode allows the consideration of MOSFETs with higher $R_{DS(ON)}$ and lower power ratings. A MOSFET can typically withstand single-shot pulses with higher dissipation than the specified package rating. Low MOSFET gate capacitance is not necessary since the inrush current limiting is achieved by limiting the gate dv/dt. Table 4 lists some recommended manufacturers and components.

Be sure to select a MOSFET with an appropriate gate drive (see the *Typical Operating Characteristics*). Typically, for V_{CC} less than 3V, select a 2.5V V_{GS} MOSFET.

Optional Sense Resistor

Select the sense resistor in conjunction with R_{CB} to set the slow and fast circuit-breaker thresholds (see the *Selecting a Circuit-Breaker Threshold* section). The sense-resistor power dissipation depends on the device configuration. If latched mode is selected, $P_{RSENSE} = (I_{OVERLOAD})^2 \times R_{SENSE}$; if autoretry is selected, then $P_{RSENSE} = (I_{OVERLOAD})^2 \times R_{SENSE} \times (t_{ON}/t_{RETRY})$. Choose a sense-resistor power rating of twice the P_{RSENSE} for long-term reliable operation. In addition, ensure that the sense resistor has an adequate I^2T rating to survive instantaneous short-circuit conditions.

No-Load Operation

The internal circuitry is capable of sourcing a current at the OUT terminal of up to 120µA from a voltage $V_{IN} + V_{GS}$. If there is no load on the circuit, the output capacitor will charge to a voltage above V_{IN} until the external MOSFET's body diode conducts to clamp the capacitor voltage at V_{IN} plus the body-diode V_F. When testing or operating with no load, it is therefore recommended that the output capacitor be paralleled with a resistor of value:

$$R = V_X/120\mu A$$

where V_X is the maximum acceptable output voltage prior to hot-swap completion.

Design Procedure

Given:

- $V_{CC} = V_S = 5V$
- $C_L = 150\mu F$
- Full-Load Current = 5A
- No R_{SENSE}
- $I_{INRUSH} = 500mA$

Procedures:

1) Calculate the required slew rate and corresponding C_{SLEW}:

$$SR = \frac{I_{INRUSH}}{1000 \times C_L} = 3.3\frac{V}{ms}$$

$$C_{SLEW} = \frac{330 \times 10^{-9}}{SR} = \frac{330 \times 10^{-9}}{3.3\frac{V}{ms}} = 0.1\mu F$$

2) Select a MOSFET and determine the worst-case power dissipation.

3) Minimize power dissipation at full load current and at high temperature by selecting a MOSFET with an appropriate $R_{DS(ON)}$. Assume a 20°C temperature difference between the devices and the MOSFET.

   For example, at room temperature the IRF7822's $R_{DS(ON)} = 6.5m\Omega$. The temperature coefficient for this device is 4000ppm/°C. The maximum $R_{DS(ON)}$ for the MOSFET at $T_{J(MOSFET)} = +105°C$ is:

$$R_{DS(ON)105} = 6.5m\Omega \times \left(1 + (105°C - 25°C) \times 4000\frac{ppm}{°C}\right)$$

$$= 8.58m\Omega$$

The power dissipation in the MOSFET at full load is:

$$P_D = I^2R = (5A)^2 \times 8.58m\Omega = 215mW$$

4) Select R_{CB}.

Since the MOSFET's temperature coefficient is 4000ppm/°C, which is greater than TC_{ICB} (3300ppm/°C), calculate the circuit-breaker threshold at high temperature so the circuit breaker is guaranteed not to trip at lower temperature during normal operation (Figure 15).

$I_{TRIPSLOW}$ = $I_{FULL\ LOAD}$ + 20% = 5A + 20% = 6A

$R_{DS(ON)105}$ = 8.58mΩ (max), from step 2

I_{CB85} = 58µA x (1 + (3300ppm/°C x (85 - 25)°C) = 69.5µA (min)

$$R_{CB} = \frac{\left(I_{TRIPSLOW} \times R_{DS(ON)105}\right) + \left|V_{CB,OS}\right|}{I_{CB85}}$$

R_{CB} = ((6A x 8.58mΩ) + 4.7mV)/69.5µA = 808Ω

Layout Considerations

Keep all traces as short as possible and maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. Place the MAX5924/MAX5925/MAX5926 close to the card's connector. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections.

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

It is important to maximize the thermal coupling between the MOSFET and the MAX5925/MAX5926 to balance the device junction temperatures. When the temperatures of the two devices are equal, the circuit-breaker trip threshold is most accurate. Keep the MOSFET and the MAX5925/MAX5926 as close to each other as possible to facilitate thermal coupling.

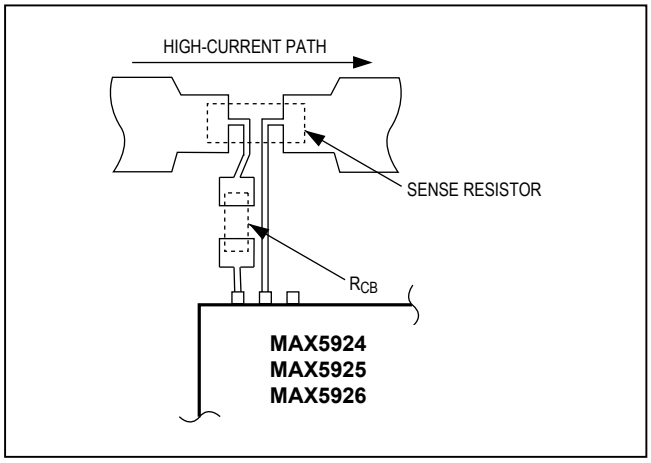


Figure 15. Kelvin Connection for the Current-Sense Resistor

Selector Guide

PART	CIRCUIT-BREAKER TEMPCO (ppm/°C)	FAULT MANAGEMENT	POWER-GOOD OUTPUT	
			$\overline{\text{PGOOD}}$ (OPEN-DRAIN)	PGOOD (OPEN-DRAIN)
MAX5924A	0	Latched	✓	—
MAX5924B	0	Latched	—	✓
MAX5924C	0	Autoretry	✓	—
MAX5924D	0	Autoretry	—	✓
MAX5925A	3300	Latched	✓	—
MAX5925B	3300	Latched	—	✓
MAX5925C	3300	Autoretry	✓	—
MAX5925D	3300	Autoretry	—	✓
MAX5926	0 or 3300 (Selectable)	Latched or Autoretry (Selectable)	✓	✓

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5924AEUB	-40°C to +85°C	10 µMAX
MAX5924BEUB	-40°C to +85°C	10 µMAX
MAX5924CEUB*	-40°C to +85°C	10 µMAX
MAX5924DEUB*	-40°C to +85°C	10 µMAX
MAX5925AEUB	-40°C to +85°C	10 µMAX
MAX5925BEUB*	-40°C to +85°C	10 µMAX
MAX5925CEUB*	-40°C to +85°C	10 µMAX
MAX5925DEUB*	-40°C to +85°C	10 µMAX
MAX5926EEE	-40°C to +85°C	16 QSOP–EP**

**Future product—contact factory for availability.*
***EP = Exposed pad.*

Chip Information

TRANSISTOR COUNT: 3751

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µMAX	U10CN+1	21-0061
10 QSOP-EP	E16E-1	21-0112