

MAX5977A/MAX5977B 1V to 16V, Single-Channel, Hot-Swap Controllers with Precision Current-Sensing Output

General Description

The MAX5977A/MAX5977B hot-swap controllers provide complete protection for systems with a 1V to 16V single-supply voltage.

During the initial insertion, the hot-swap controllers limit the inrush current from damaging the board or from shorting out the backplane. When the input voltage is above the undervoltage threshold and below the overvoltage threshold, a $5\mu\text{A}$ current source powered from the internal 5V charge pump drives the gate of an external n-channel MOSFET, providing a slow turn-on response. An internal current-sense amplifier in the IC monitors the current across an external shunt resistor, providing current sensing for wide input-sense voltage range. The devices provide two levels of overcurrent circuit-breaker protections: a fast-trip threshold for a fast turn-off and a lower slow-trip threshold for a delayed turn-off.

Exceeding either of the overcurrent circuit-breaker thresholds forces the device into fault mode where the external n-channel MOSFET is disabled. The MAX5977 is available in two versions that provide a latched-off (MAX5977A) or autoretry (MAX5977B) output when the device is in fault mode.

A calibration mode allows further calibration of the integrated transconductance amplifier for production testing of the final design. The devices are offered in a 20-pin, 4mm x 4mm, TQFN-EP package and are fully specified from -40°C to $+85^{\circ}\text{C}$.

Features

- 1% Accurate Current-Sense Amplifier Output
- Hot-Swap Monitors Operation from 1V to 16V
- Integrated Charge Pump Fully Enhances the External n-Channel FET ($V_{\text{GATE}} = V_{\text{IN}} + 5\text{V}$)
- VariableSpeed/BiLevel™ Fault Protection Provides Electronic Circuit-Breaker Function
- Output Latched Off After Fault Condition (MAX5977A)
- Autoretry After Fault Condition (MAX5977B)
- Power-Good Indicator
- Calibration Mode
- Small, 20-Pin, 4mm x 4mm TQFN-EP Package

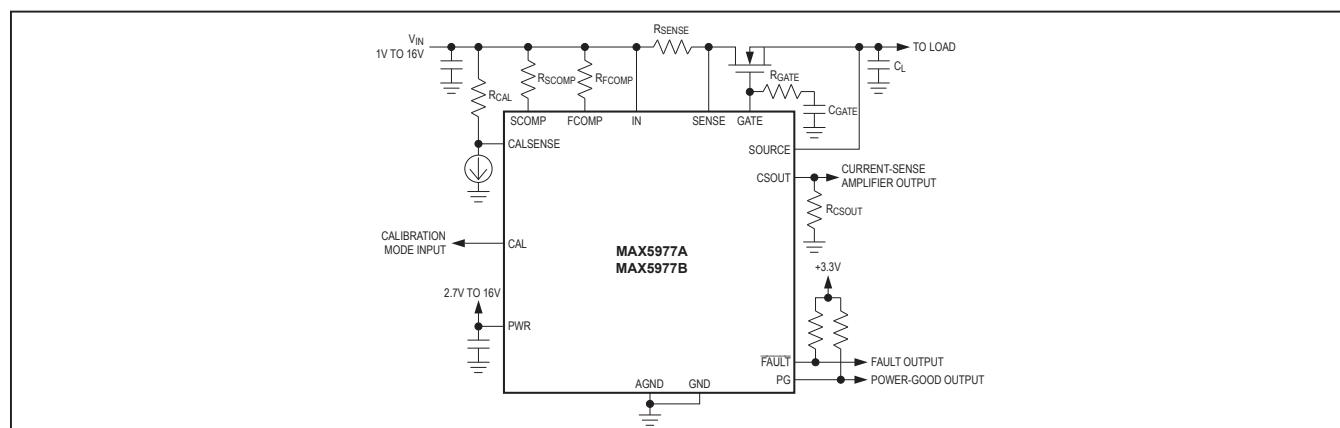
Applications

- Servers
- Storage Systems
- Network Switches and Routers
- General Hot-Swap

Ordering Information appears at end of data sheet.

VariableSpeed/BiLevel is a trademark of Maxim Integrated Products, Inc.

Typical Application Circuit



Absolute Maximum Ratings

PWR, SENSE, IN, FCOMP, SCOMP, GATE, SOURCE, CALSENSE to GND	-0.3V to +28V	Continuous Power Dissipation (T _A = +70°C) 20-Pin TQFN, Single-Layer Board (derate 16.9mW/°C above +70°C)	1355.9mW
PG, CAL, BIAS, UV, OV, FAULT, CSOUT to GND	-0.3V to +6V	20-Pin TQFN, Multilayer Board (derate 25.6mW/°C above +70°C)	2051.3mW
REG to GND	-0.3V to +4V	Operating Temperature Range	-40°C to +85°C
GATE to SOURCE	-0.3V to +6V	Junction Temperature	+150°C
IN to FCOMP, IN to SCOMP, IN to SENSE, IN to CALSENSE	-0.3V to +1V	Storage Temperature Range	-65°C to +150°C
GND to AGND	-0.3V to +0.3V	Lead Temperature (soldering, 10s)	+300°C
FAULT, PG Current	-1mA to +50mA	Soldering Temperature (reflow)	+260°C
GATE, SOURCE, GND Current	750mA		
Input/Output Current (all other pins)	20mA		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20-PIN TQFN	
Package Code	T2044+3
Outline Number	21-0139
Land Pattern Number	90-0037
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ _{JA}) Single-Layer Board	+59°C/W
Junction to Ambient (θ _{JA}) Multilayer Board	+39°C/W
Junction to Case (θ _{JC}) Single-Layer and Multilayer Board	+6°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{PWR} = V_{IN} = 12V$, $R_{SENSE} = 4m\Omega$, $R_{FCOMP} = R_{SCOMP} = 2k\Omega$, $R_{GATE} = 1k\Omega$, $C_{GATE} = 330nF$, $C_{REG} = 1\mu F$, unless otherwise noted. Typical Values at $V_{PWR} = V_{IN} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{PWR}		2.7	3.3	16	V
Undervoltage Lockout	V_{UVLO}	Minimum rising voltage on PWR			2.69	V
Undervoltage-Lockout Hysteresis	$V_{UVLOHYS}$			100		mV
Supply Current	I_{PWR}			0.734	4	mA
Internal LDO Output Voltage	V_{REG}	$2.7V < V_{PWR} < 16V$, 0 to 1mA	2.49		2.6	V
CURRENT-MONITORING FUNCTION						
IN Input Range		Common-mode range	1		16	V
SCOMP Input Range			1		16	V
FCOMP Input Range			1		16	V
IN Input Current				135		μA
SENSE Input Current		$V_{IN} = V_{SENSE} = 1V$ to 16V		6		μA
Circuit-Breaker Current (Slow Comparator)	I_{SCOMP}	$V_{SCOMP} = 1V$ to 16V	24.0	25	26.0	μA
Circuit-Breaker Current (Fast Comparator)	I_{FCOMP}	$V_{FCOMP} = 1V$ to 16V	48.1	50	51.4	μA
Slow Current-Limit Threshold Error		$V_{SENSE} - V_{SCOMP} = 50mV$	-2.0		+2.1	mV
Fast Current-Limit Threshold Error		$V_{SENSE} - V_{FCOMP} = 100mV$	-2.2		+1.4	mV
Slow-Comparator Response Time	t_{SCD}	1mV overdrive		1		ms
		50mV overdrive		130		μs
Fast-Comparator Response Time	t_{FSD}	10mV overdrive, from overload condition, $V_{PWR} = 12V$		200		ns
CURRENT-SENSE AMPLIFIER						
Input Common-Mode Range		$V_{IN} - V_{SENSE}$	1.5			V
Input Offset Error				0.1		mV
Transconductance Gain	g_M	$10mV \leq (V_{IN} - V_{SENSE}) \leq 50mV$, $-40^\circ C \leq T_A \leq +85^\circ C$	2457	2500	2537	μS
		$10mV \leq (V_{IN} - V_{SENSE}) \leq 50mV$, $0^\circ C \leq T_A \leq +25^\circ C$	2467	2500	2532	
Combined Gain and Offset Accuracy		Set $V_{IN} - V_{SENSE} = 50mV$, measure I_{CSOUT} , $V_{CSOUT} = 25mV$ ($-40^\circ C \leq T_A \leq +85^\circ C$)	122.1	125	128	μA
		Set $V_{IN} - V_{SENSE} = 50mV$, measure I_{CSOUT} , $V_{CSOUT} = 25mV$ ($0N \leq T_A \leq +25^\circ C$)	123.5	125	126.5	
		Set $V_{IN} - V_{SENSE} = 10mV$, measure I_{CSOUT} , $V_{CSOUT} = 25mV$ ($-40^\circ C \leq T_A \leq +85^\circ C$)	22.5	25	27.6	
		Set $V_{IN} - V_{SENSE} = 10mV$, measure I_{CSOUT} , $V_{CSOUT} = 25mV$ ($0^\circ \leq T_A \leq +25^\circ C$)	24.0	25	26.0	

Electrical Characteristics (continued)

($V_{PWR} = V_{IN} = 12V$, $R_{SENSE} = 4m\Omega$, $R_{FCOMP} = R_{SCOMP} = 2k\Omega$, $R_{GATE} = 1k\Omega$, $C_{GATE} = 330nF$, $C_{REG} = 1\mu F$, unless otherwise noted.
Typical Values at $V_{PWR} = V_{IN} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Full-Scale Error		$2mV < (V_{IN} - V_{SENSE}) < 10mV$ ($-40^\circ C \leq T_A \leq +85^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (10mV \times 0.0025)$	-10		+10	% of 10mV
		$2mV < (V_{IN} - V_{SENSE}) < 10mV$ ($0^\circ C \leq T_A \leq +25^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (10mV \times 0.0025)$	-4.21		+4.21	Full-Scale Output
		$2mV < (V_{IN} - V_{SENSE}) < 25mV$ ($-40^\circ C \leq T_A \leq +85^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (25mV \times 0.0025)$	-4.1		+4.1	% of 25mV
		$2mV < (V_{IN} - V_{SENSE}) < 25mV$ ($0^\circ C \leq T_A \leq +25^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (25mV \times 0.0025)$	-1.68		+1.68	Full-Scale Output
		$2mV < (V_{IN} - V_{SENSE}) < 50mV$ ($-40^\circ C \leq T_A \leq +85^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (50mV \times 0.0025)$	-2.34		+2.3	% of 50mV
		$2mV < (V_{IN} - V_{SENSE}) < 50mV$ ($0^\circ C \leq T_A \leq +25^\circ C$), % error = $(I_{CSOUT} - (V_{IN} - V_{SENSE}) \times 0.0025) / (50mV \times 0.0025)$	-1.18		+0.9	Full-Scale Output
Output Common-Mode Range		CSOUT voltage range	0		2.5	V
POWER-GOOD						
PG Delay	t_{dPG}			50		ms
PG Threshold Rising	V_{THRPG}	$V_{IN} - V_{SOURCE}$ falling		100		mV
PG Threshold Hysteresis				100		mV
CHARGE PUMP (GATE)						
Charge-Pump Output Voltage	V_{OHGATE}	Relative to V_{SOURCE}	4.5	5	5.5	V
Charge-Pump Output Source Current	I_{GATEPU}	$V_{GATE} = V_{SOURCE} = 0V$	4	5	6	μA
		$V_{IN} - V_{SOURCE} < 100mV$	8	10	12	
Charge-Pump Pulldown Current	I_{GATEPD}	$V_{GATE} = 2V$, $V_{SOURCE} = 0$ to 16V		500		mA
OUTPUTS (FAULT, PG)						
Output Voltage Low	$V_{OLFAULT} / V_{OLPG}$	$I_{SINK} = 3.2mA$			0.4	V
Output Leakage (Open Drain)	$I_{LKFAULT} / I_{LKPG}$	Tested at 0V and 5.2V			1	μA

Electrical Characteristics (continued)

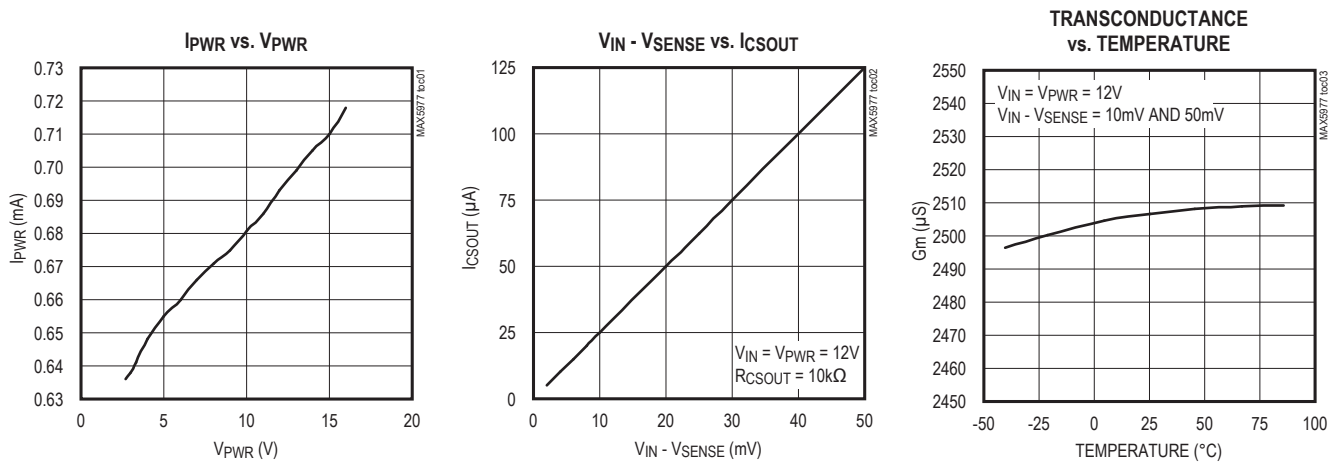
($V_{PWR} = V_{IN} = 12V$, $R_{SENSE} = 4m\Omega$, $R_{FCOMP} = R_{SCOMP} = 2k\Omega$, $R_{GATE} = 1k\Omega$, $C_{GATE} = 330nF$, $C_{REG} = 1\mu F$, unless otherwise noted. Typical Values at $V_{PWR} = V_{IN} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UV/OV COMPARATOR INPUTS						
UV/OV Threshold	$V_{UV/OVR}$	UV, OV rising input voltage threshold	580	590	600	mV
UV/OV Threshold Hysteresis	$V_{UV/OVHYS}$	UV, OV falling input hysteresis		4		%
UV/OV Input Current	I_{LKUV}/I_{LKOv}	$V_{UV} = V_{OV} = 0V$ and $5.5V$	-100		+100	nA
CALIBRATION MODE						
CAL Low-Voltage Input	V_{ILCAL}				0.4	V
CAL High-Voltage Input	V_{IHCAL}		1.4			V
CAL Input Current	I_{IHCAL}	$V_{CAL} = 2.5V$, the CAL input pulls low if left unconnected		20		μA
CALSENSE Input Current				± 300		nA
FAULT RESPONSE						
Retry Timeout Period	t_{RETRY}	MAX5977B		175		ms

Note 1: All devices 100% tested at $T_A = +25^\circ C$. Limits over temperature guaranteed by design.

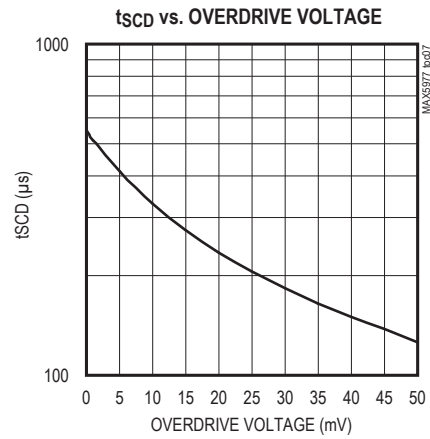
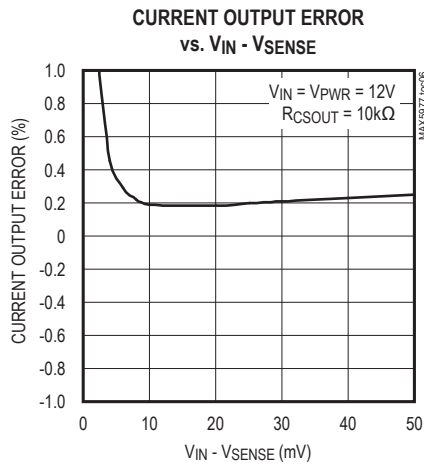
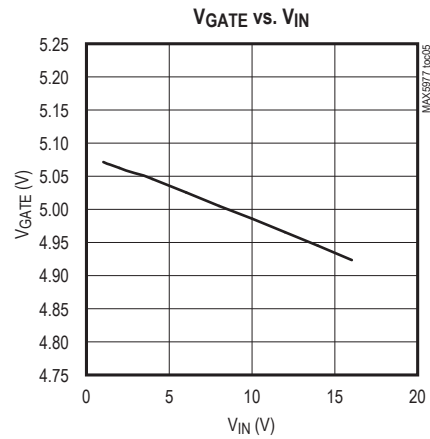
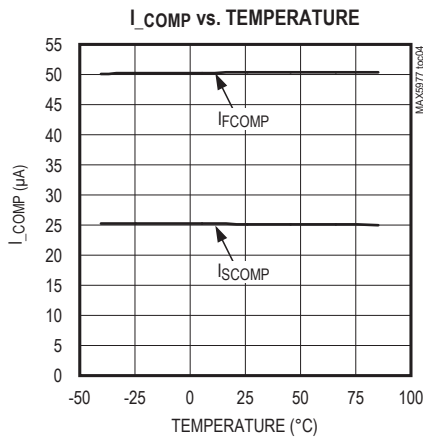
Typical Operating Characteristics

($V_{PWR} = V_{IN} = 3.3V$, $T_A = +25^\circ C$, $R_{FCOMP} = R_{SCOMP} = 2k\Omega$, $R_{GATE} = 1k\Omega$, $C_{GATE} = 330nF$, $C_{REG} = 1\mu F$, unless otherwise noted.)

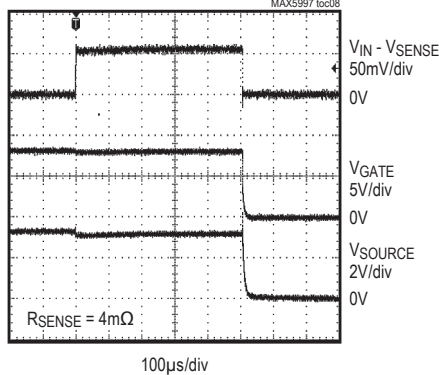


Typical Operating Characteristics (continued)

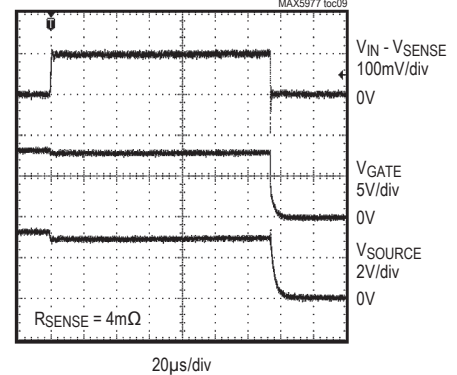
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SLOW-COMPARATOR RESPONSE TIME (50mV OVERDRIVE)



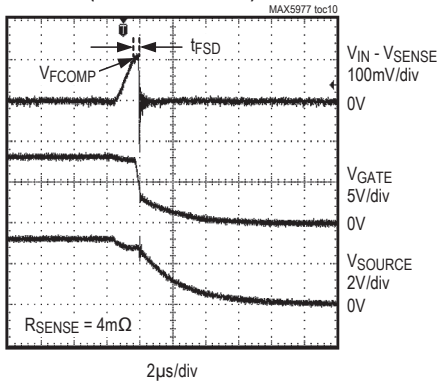
SLOW-COMPARATOR RESPONSE TIME (50mV OVERDRIVE)



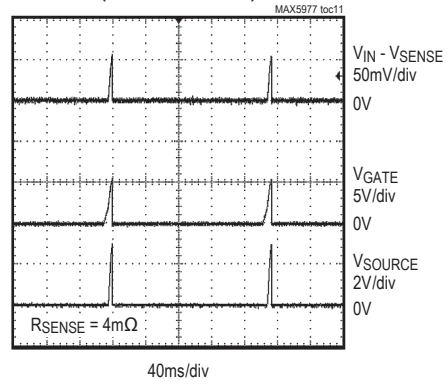
Typical Operating Characteristics (continued)

($V_{PWR} = V_{IN} = 3.3V$, $T_A = +25^\circ C$, $R_{FCOMP} = R_{SCOMP} = 2k\Omega$, $R_{GATE} = 1k\Omega$, $C_{GATE} = 330nF$, $C_{REG} = 1\mu F$, unless otherwise noted.)

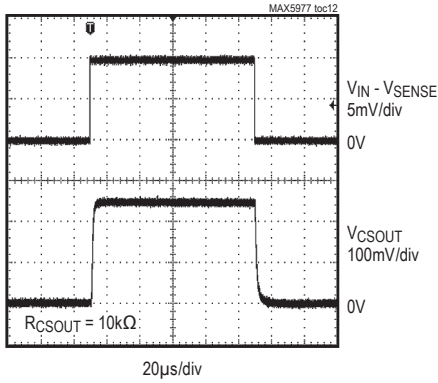
FAST-COMPARATOR RESPONSE TIME
(10mV OVERDRIVE)



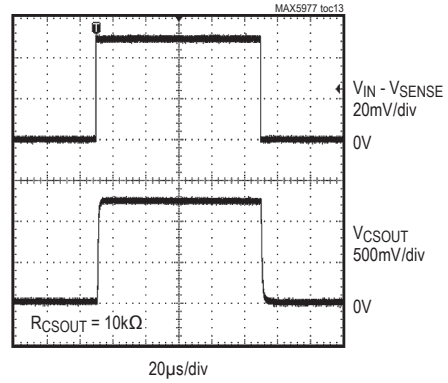
FAULT RETRY TIME
(MAX5977B ONLY)



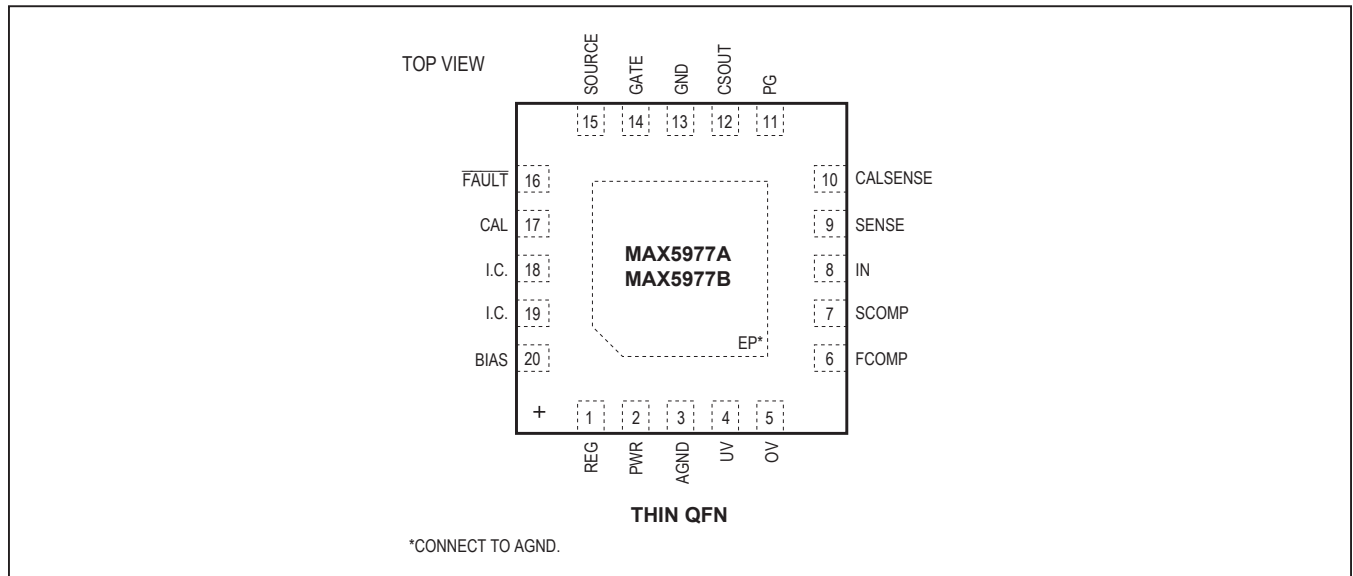
ICSOUT SMALL-SIGNAL
PULSE RESPONSE



ICSOUT LARGE-SIGNAL
PULSE RESPONSE



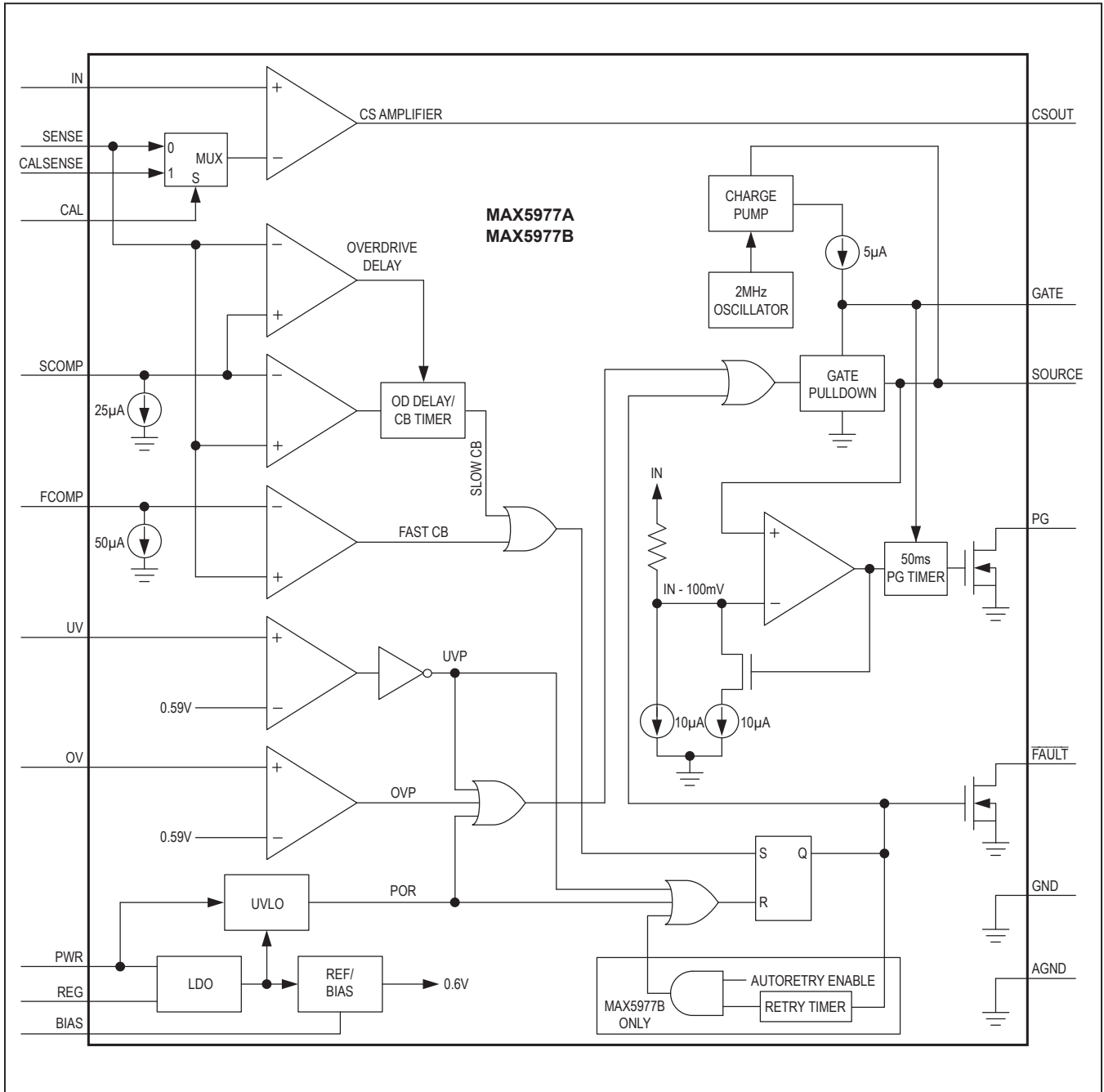
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	REG	Regulator Output. Bypass REG with a 1µF capacitor.
2	PWR	Power-Supply Input. Bypass PWR with a 0.1µF or higher value capacitor.
3	AGND	Analog Ground
4	UV	Active-High Precision Turn-On Input. UV is used to turn on/off the output and set the input undervoltage lockout threshold.
5	OV	Active-Low Precision Turn-On Input. OV is used to turn on/off the output and set the input overvoltage lockout threshold.
6	FCOMP	Fast Circuit-Breaker Comparator Input. Connect FCOMP to IN with a resistor to set the fast-trip circuit-breaker threshold.
7	SCOMP	Slow Circuit-Breaker Comparator Input. Connect SCOMP to IN with a resistor to set the slow-trip circuit-breaker threshold.
8	IN	Hot-Swap Voltage-Monitoring Input
9	SENSE	Current-Sense Voltage Input. The voltage across an external sense resistor between IN and SENSE is used to measure the channel current.
10	CALSENSE	Calibration Voltage Input
11	PG	Power-Good, Active-High Open-Drain Output
12	CSOUT	Transconductance Current-Sense Amplifier Output. The output current of CSOUT is the product of the voltage measured between SENSE and IN and the transconductance gain (2500µS typ).
13	GND	Ground
14	GATE	Gate-Driver Output. Connect GATE to the gate of the external n-channel MOSFET switch.
15	SOURCE	MOSFET Source Voltage Input. Connect SOURCE to the source of the external n-channel MOSFET.
16	FAULT	Active-Low, Open-Drain Fault Output. When an overcurrent occurs, FAULT goes low.
17	CAL	Calibration Mode Select Input
18, 19	I.C.	Internally Connected. Connect to ground.
20	BIAS	Bias Input. Connect BIAS to REG.
—	EP	Exposed Pad. Connect to AGND.

Functional Diagram



Detailed Description

The hot-swap controllers provide electronic circuit-breaker protection and precision current sensing for a single-supply voltage from 1V to 16V. Programmable undervoltage and overvoltage protection qualifies the supply voltage prior to enhancing the external n-channel MOSFET with the internal gate driver.

The VariableSpeed/BiLevel fault levels are programmable with external resistors providing both slow and fast circuit-breaker protection. The transconductance current-sense amplifier provides continuous current monitoring with high accuracy and features a calibration mode for production testing.

Programmable Undervoltage and Overvoltage Protection

The programmable undervoltage and overvoltage protection enables the hot-swap channel when the voltage at UV is above 590mV, and the voltage at OV is below 590mV. After the hot-swap channel is enabled, the hot-swap channel is disabled if the voltage at OV exceeds the 590mV threshold.

Gate Driver

An integrated 5V charge pump supplies the gate-driver output of the devices, allowing it to fully enhance the external n-channel MOSFET during normal operation. The 5 μ A (typ) current source at GATE slowly charges the gate-to-source capacitance of the external n-channel MOSFET to 5V (typ) relative to the SOURCE input.

Programmable Fast-Trip and Slow-Trip Overcurrent Circuit Breaker

During normal operation with the channel turned on, two analog comparators are used to detect an overcurrent condition by comparing the voltage across the external sense resistor (R_{SENSE}) connected between IN and SENSE to the voltages across the respective external overcurrent circuit-breaker threshold set resistors connected from IN to FCOMP and SCOMP. Precision current sources at the FCOMP and SCOMP inputs establish these thresholds.

If the voltage across the sense resistor is less than the fast-trip and slow-trip overcurrent circuit-breaker thresholds, the GATE output remains high. If either of the thresholds is exceeded due to an overcurrent condition, the GATE output is pulled down to SOURCE by a 500mA current sink, and the \overline{FAULT} and PG outputs are asserted low.

If the sense voltage rises above the fast circuit-breaker threshold, the devices turn off the external MOSFET in 200ns (typ).

If the sense voltage rises above the slow circuit-breaker threshold, the internal timer begins counting. If the sense voltage remains above the slow circuit-breaker threshold until the timer expires, the devices turn off the external MOSFET. The slow circuit-breaker timer occurs in 1ms (typ) when the slow-current comparator threshold is overdriven by 1mV and 130 μ s (typ) when overdriven by 50mV.

Current-Sense Amplifier

The integrated transconductance current-sense amplifier features high accuracy with less than 1% error over its 10mV to 50mV input range, and provides continuous current monitoring into the load. The sense voltage of the external sense resistor connected between IN and SENSE is multiplied by the transconductance gain (2500 μ S typ) of the amplifier with the resulting current output at CSOUT.

Calibration Mode

The devices' calibration mode bypasses the transconductance amplifier inputs to measure the voltage between IN and CALSENSE when the calibration mode select input CAL is high.

This enables the user to apply a known calibration voltage across the current-sense amplifier input. This voltage corresponds to a full scale for the actual sense voltage. During the calibration mode, the current-sense amplifier only measures the calibration voltage between IN and CALSENSE.

The calibration mode is completely asynchronous and does not disrupt the circuit-breaker threshold comparison. Once in calibration mode there is no expiration until the CAL input is brought low. This allows the calibration to occur at multiple voltages by applying various calibration voltages during the calibration mode.

Fault Output

The \overline{FAULT} output goes low when a slow or fast comparator current-limit fault has occurred.

On the MAX5977A, the device is latched in fault mode until it is reset either by initiating a full power-on reset or pulling UV below 590mV.

On the MAX5977B, the device reenables the hot-swap output after the autoretry timer has expired in 175ms and \overline{FAULT} is pulled high if the fault condition has been removed and startup conditions are met.

Power-Good Output

The open-drain, active-high output PG indicates the power-good status of the output. Once the input voltage satisfies the undervoltage and overvoltage requirements for startup and $V_{IN} - V_{SOURCE}$ is less than 100mV and the $V_{GATE} - V_{SOURCE} > 4V$, the PG timer is started. At the expiration of the 50ms PG timer, PG is asserted high.

Applications Information

Undervoltage and Overvoltage Protection

The undervoltage and overvoltage protection is programmed with a voltage-divider formed by three resistors (R1, R2, and R3) placed in series. The resistor values should be selected such that the series current, I_S , is greater than 5 μ A. The resistor values are then calculated using the following equations with the overvoltage threshold (V_{OVR}), undervoltage threshold (V_{UVR}), and the overvoltage hysteresis (V_{OVHYS}) obtained from the [Electrical Characteristics](#) table:

$$R3 = \frac{V_{OVR}}{I_S}$$

$$R2 = \left(\frac{V_{IN,OV} \times V_{UVR}}{V_{IN,UV} \times (V_{OVR} - V_{OVHYS})} - 1 \right) \times R3$$

$$R1 = \left(\frac{V_{IN,UV}}{V_{UVR}} - 1 \right) \times (R2 + R3)$$

where $V_{IN,UV}$ and $V_{IN,OV}$ are the desired undervoltage and overvoltage thresholds for the hot-swap input voltage I_N .

Programmable Slow and Fast Current Limit

The slow and fast current-limit thresholds are programmed by connecting resistors between the high side of R_{SENSE} to $SCOMP$ and $FCOMP$. The current-limit thresholds are set using the following equations:

$$R_{SCOMP} = \frac{I_{SENSE, SCOMP} \times R_{SENSE}}{25\mu A}$$

and:

$$R_{FCOMP} = \frac{I_{SENSE, FCOMP} \times R_{SENSE}}{50\mu A}$$

where I_{SENSE_COMP} is the desired circuit-breaker current limit for the slow or fast current limit.

Startup Sequence

When all conditions for channel turn-on are met, the external n-channel MOSFET switch is fully enhanced with a typical gate-to-source voltage of 5V to ensure a low drain-to-source resistance. The charge pump at GATE sources 5 μ A to control the output voltage turn-on voltage slew rate. An external capacitor must be added from GATE to ground to further reduce the voltage slew rate. Placing a 1k Ω resistor in series with this capacitance prevents the added capacitance from increasing the gate turn-off time. Total inrush current is the load current summed with the product of the gate voltage slew rate dV/dt and the load capacitance.

To determine the output dV/dt during startup, divide the GATE pullup current I_{GATEPU} by the GATE to ground capacitance. The voltage at the source of the external MOSFET follows the gate voltage, so the load dV/dt is the same as the gate dV/dt . Inrush current is the product of the dV/dt and the load capacitance. The time to start up t_{SU} is the hot-swap voltage V_{IN} divided by the output dV/dt .

Be sure to choose an external MOSFET that can handle the power dissipated during startup. The inrush current is roughly constant during startup and the voltage drop across the MOSFET (drain to source) decreases linearly as the load capacitance charges. The resulting power dissipation is therefore roughly equivalent to a single pulse of magnitude $(V_{IN} \times I_{inrush})/2$ and duration t_{SU} . Refer to the thermal resistance charts in the MOSFET data sheet to determine the junction temperature rise during startup, and ensure that this does not exceed the maximum junction temperature for worst-case ambient conditions.

Transconductance Current-Sense Amplifier

The current-sense resistor, R_{SENSE} , must be connected between I_N and $SENSE$ to sense the average current into the load. The voltage drop across R_{SENSE} should be less than or equal to the slow current-limit threshold; therefore, R_{SENSE} should be selected based on the following equation:

$$R_{SENSE} \times I_{SENSE,FS} \leq V_{SCOMP}$$

where $I_{SENSE,FS}$ is the full-scale current into the load and V_{SCOMP} is the slow current-limit threshold. A Kelvin sense connection should be used to connect R_{SENSE} to I_N and $SENSE$.

An output resistor, R_{CSOUT} , must be connected between the transconductance current-sense amplifier output CSOUT and AGND. The transconductance G_M of the amplifier is typically $2500\mu S$:

$$R_{CSOUT} \times G_M \times V_{SENSE, FS} \leq 2.5V$$

n-Channel MOSFET Selection

Select the external n-channel MOSFET according to the application's current level. The MOSFET's on-resistance ($R_{DS(ON)}$) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High $R_{DS(ON)}$ causes output ripple if there is a pulsating load. Determine the device power rating to accommodate a short-circuit condition on the board at startup and when the device is in automatic-retry mode (see the [MOSFET Thermal Considerations](#) section).

The MAX5977A's fault latch allows the use of MOSFETs with lower power ratings. A MOSFET typically withstands single-shot pulses with higher dissipation than the specified package rating.

MOSFET Thermal Considerations

During normal operation, the external MOSFETs dissipate little power. The MOSFET $R_{DS(ON)}$ is low when the MOSFET is fully enhanced. The power dissipated in normal operation is $P_D = I_{LOAD}^2 \times R_{DS(ON)}$. The most power dissipation occurs during the turn-on and turn-off transients when the MOSFETs are in their linear regions. Take into consideration the worst-case scenario of a continuous short-circuit fault; consider these two cases:

- 1) The single turn-on with the device latched after a fault (MAX5977A).
- 2) The continuous automatic retry after a fault (MAX5977B).

MOSFET manufacturers typically include the package thermal resistance from junction to ambient ($R_{\theta JA}$) and thermal resistance from junction to case ($R_{\theta JC}$), which determine the startup time and the retry duty cycle

($d = t_{SU}/(t_{SU} + t_{RETRY})$). Calculate the required transient thermal resistance with the following equation:

$$Z_{\theta JA(MAX)} \leq \frac{T_{JMAX} \times T_A}{V_{IN} \times I_{INRUSH}}$$

Layout Considerations

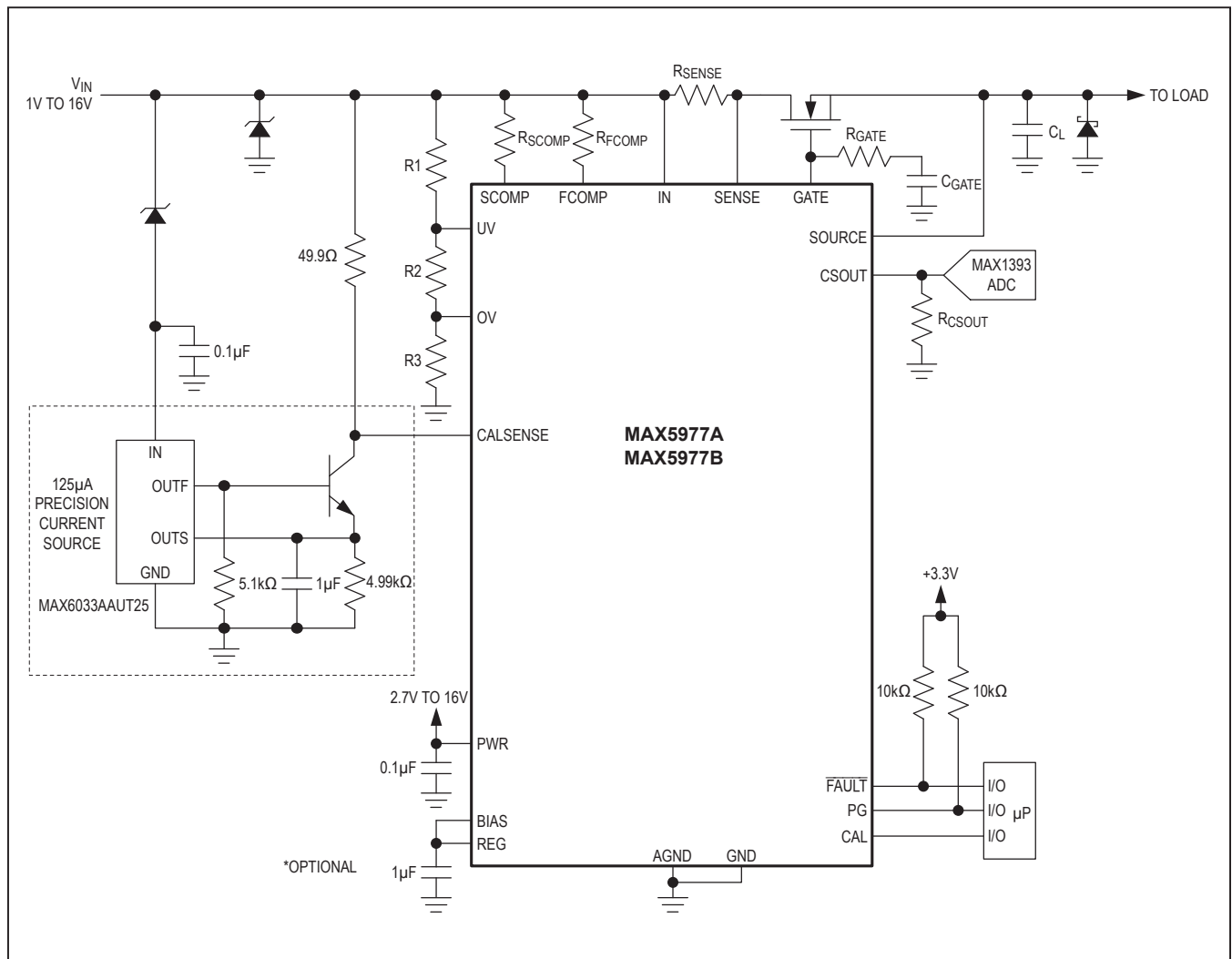
To take full advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic resistance and inductance. Place the devices close to the card's connector, and a $0.01\mu F$ capacitor to GND should be placed as close as possible to V_{IN} . Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length and ensure accurate current sensing with Kelvin connections.

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

Related Parts

PART	DESCRIPTION
MAX5970	0 to 16V, Dual Hot-Swap Controller with a 10-Bit Current and Voltage Monitor and Four LED Drivers
MAX5978	0 to 16V, Single Hot-Swap Controller with a 10-Bit Current and Voltage Monitor Plus Four LED Drivers

Typical Application Circuit



Ordering Information

PART	PIN-PACKAGE	FAULT RESPONSE
MAX5977AETP+	20 TQFN-EP*	Latched
MAX5977BETP+	20 TQFN-EP*	Autoretry

Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS