MAX6791–MAX6796

High-Voltage, Micropower, Single/Dual Linear Regulators with Supervisory Functions

General Description

The MAX6791–MAX6796 ultra-low-quiescent-current, single/dual-output linear regulators are ideal for automotive applications. The devices offer a wide 5V to 72V operating input range, allowing them to withstand automotive load-dump conditions while consuming only 68µA. The MAX6791–MAX6794 are dual-output regulators capable of supplying up to 150mA per output. The MAX6795/MAX6796 offer a single output capable of delivering up to 300mA. These devices offer standard output-voltage options (5V, 3.3V, 2.5V, or 1.8V) and can be adjusted to any voltage from 1.8V to 11V. The MAX6791–MAX6794 also offer a fixed 5V output.

All devices feature a push-pull or open-drain, active-low $\overline{\text{RESET}}$ output with a fixed output reset threshold that is 92.5%/87.5% of the regulator output OUT/OUT1. The reset output asserts low when OUT/OUT1 drops below the reset threshold and remains low for the fixed or capacitor-adjustable reset timeout period after OUT/OUT1 exceeds the reset threshold.

The MAX6791–MAX6796 provide a watchdog input that monitors a pulse train from the microprocessor (µP) and generates reset pulses if the watchdog input remains high or low for a duration longer than the watchdog timeout period. All devices are available with either a fixed watchdog timeout period of 280ms (min) or a period adjustable with an external capacitor. The MAX6791/MAX6792 feature a windowed watchdog timeout period with selectable window ratio. The watchdog feature can be disabled.

The MAX6791–MAX6794 provide dual enable inputs (ENABLE1 and ENABLE2) that control each regulator independently. The single-output MAX6795/MAX6796 feature one enable input (ENABLE).

All devices include a hold input ($\overline{\text{HOLD}}$) that aids the implementation of a self-holding circuit without requiring external components. Once the regulator is enabled, setting $\overline{\text{HOLD}}$ low forces the regulator to remain on even if ENABLE/ENABLE1 is subsequently set low. Releasing $\overline{\text{HOLD}}$ shuts down the regulator.

The MAX6791–MAX6796 are available in a small, thermally enhanced TQFN package. The 5mm x 5mm package dissipates up to 2.7W, supporting continuous regulator operation during high ambient temperatures, high battery voltage, and high load-current conditions.

The MAX6791–MAX6796 are specified for a -40°C to +125°C operating temperature range.

Applications

- Automotive

Benefits and Features

- Low 68µA Quiescent Current
- Wide 5V to 72V Supply Voltage Range
- Output Current
  - Single Output Up to 300mA
  - Dual Outputs Up to 150mA per Output
- Low Dropout Voltage
  - 420mV (typ) at 100mA (Single)
  - 840mV (typ) at 100mA (Dual)
- Fixed Output-Voltage Options: 5V, 3.3V, 2.5V, 1.8V, or Adjustable Output (From 1.8V to 11V)
- ENABLE and HOLD Functionality
- RESET Output: Open-Drain or Push-Pull
- Internally Fixed (35µs, 3.125ms, 12.5ms, 50ms, or 200ms) or Capacitor-Adjustable Reset Timeout Periods
- Internally Fixed or Capacitor-Adjustable Watchdog Timeout Periods
- Windowed (Minimum/Maximum) Watchdog Timer Options (MAX6791/MAX6792)
- Watchdog Disable Feature
- Thermal, Short-Circuit, and Output Overvoltage Protection
- Fully Specified from -40°C to +125°C
- Small, Thermally Enhanced, 5mm x 5mm TQFN
- AEC-Q100 Qualified MAX6795TPLD2/V+, MAX6795TPSD2/V+

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6791TP_D _+	-40°C to +125°C	20 TQFN-EP*
MAX6792TP_D _+	-40°C to +125°C	20 TQFN-EP*
MAX6793TP_ D_+	-40°C to +125°C	20 TQFN-EP*
MAX6794TP_ D_+	-40°C to +125°C	20 TQFN-EP*
MAX6795TP_ D_+	-40°C to +125°C	20 TQFN-EP*
MAX6795TP_D _/V+	-40°C to +125°C	20 TQFN-EP*
MAX6795TPLD2/V+	-40°C to +125°C	20 TQFN-EP*
MAX6795TPSD2/V+	-40°C to +125°C	20 TQFN-EP*
MAX6796TP_D _+	-40°C to +125°C	20 TQFN-EP*

+Denotes lead-free package.
For tape-and-reel, add a T after the "+." Tape-and-reel are offered in 2.5k increments. The first placeholder "_" designates preset output-voltage option and preset reset threshold level; see Table 1. The second placeholder "_" designates the reset timeout period; see Table 2. For example, the MAX6791TPSD3+ indicates a 3.3V output voltage with a reset threshold of 87.5% at nominal voltage and a 50ms reset timeout period. Samples are generally held in stock. Nonstandard versions require a 2.5k minimum order quantity.
/V Denotes an automotive-qualified part.
**EP = Exposed pad.*

Typical Application Circuit, Pin Configurations, and Selector Guide appear at end of data sheet.

19-3875; Rev 3; 10/17

maxim integrated™

Absolute Maximum Ratings

(All pins referenced to GND, unless otherwise noted.)
IN to GND.....-0.3V to +80V
ENABLE, ENABLE1, ENABLE2, PFI, GATEP to GND.....-0.3V to (V_{IN} + 0.3V)
GATEP to IN.....-12V to +0.3V
OUT, OUT1, OUT2, $\overline{PFO}$, $\overline{RESET}$ (open-drain versions), CSRT, CSWT.....-0.3V to +12V
$\overline{HOLD}$, $\overline{RESET}$ (push-pull versions), WDI, WDS0, WDS1, WD-DIS, SET, SET1.....-0.3V to ($V_{OUT/OUT1}$ + 0.3V)
OUT, OUT1, OUT2 Short Circuit to GND.....Continuous
Maximum Current (all pins except IN and OUT_).....50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 33.3mW/°C above +70°C)...2666.7mW
Operating Temperature Range (T_A)..... -40°C to +125°C
Junction Temperature (T_J).....150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}			5		72	V
Supply Current	I_{IN}	Regulators on (I_{LOAD} = 0mA), V_{IN} = 8V			68	85	µA
		Regulators on, $V_{OUT/OUT1}$ = V_{OUT2} = 5V	V_{IN} = 8V, I_{LOAD} = 300mA (MAX6795/MAX6796)		130	220	
			V_{IN} = 14V, I_{LOAD} = 100mA (MAX6795/MAX6796)		100	160	
			V_{IN} = 8V, I_{LOAD1} = I_{LOAD2} = 150mA (MAX6791–MAX6794)		130	220	
			V_{IN} = 14V, I_{LOAD1} = I_{LOAD2} = 50mA (MAX6791–MAX6794)		100	160	
		Regulators on (I_{LOAD} = 0mA), V_{IN} = 42V			74	95	
		Regulators on (I_{LOAD} = 20mA, total) OUT1/OUT2/OUT = 5V, V_{IN} = 42V			100	170	
Shutdown Supply Current	I_{SHDN}	Regulators off, V_{IN} = 14V			27	45	µA

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}/ V_{OUT1}	L/M, I_{LOAD} = I_{LOAD1} = 1mA		4.858	4.974	5.090	V
		L/M, I_{LOAD} = 150mA (MAX6791–MAX6794), V_{IN} = 8V		4.811	4.945	5.078	
		L/M, I_{LOAD} = 300mA (MAX6795/MAX6796), V_{IN} = 8V		4.850	5	5.150	
		T/S, I_{LOAD} = I_{LOAD1} = 1mA		3.206	3.282	3.360	
		T/S, I_{LOAD} = 150mA (MAX6791–MAX6794), V_{IN} = 6V		3.175	3.263	3.351	
		T/S, I_{LOAD} = 300mA (MAX6795/MAX6796), V_{IN} = 6V		3.201	3.3	3.399	
		Z/Y, I_{LOAD} = I_{LOAD1} = 1mA		2.429	2.487	2.546	
		Z/Y, I_{LOAD} = 150mA (MAX6791–MAX6794), V_{IN} = 5.5V		2.405	2.472	2.539	
		Z/Y, I_{LOAD} = 300mA (MAX6795/MAX6796), V_{IN} = 5.5V		2.425	2.5	2.575	
		W/V, I_{LOAD} = I_{LOAD1} = 1mA		1.748	1.791	1.832	
		W/V, I_{LOAD} = 150mA (MAX6791–MAX6794), V_{IN} = 5V		1.731	1.780	1.828	
		W/V, I_{LOAD} = 300mA (MAX6795/MAX6796), V_{IN} = 5V		1.746	1.8	1.854	
Output Voltage (MAX6791–MAX6794)	V_{OUT2}	I_{LOAD2} = 1mA		4.858	4.974	5.090	V
		I_{LOAD2} = 150mA		4.811	4.945	5.079	
SET/SET1 Threshold Voltage	V_{SET}	I_{LOAD} = I_{LOAD1} = 1mA, $V_{OUT/OUT1}$ = 5V		1.207	1.2315	1.256	V
Adjustable Output Voltage	V_{OUT}			1.8		11.0	V
Dual-Mode™ SET Threshold		SET/SET1 rising			124		mV
		SET/SET1 falling			62		
SET/SET1 Input Current		SET/SET1 = 1V, V_{IN} = 11V		-100		+100	nA
Dropout Voltage	ΔV_{DO}	(MAX6795/ MAX6796)	L/M, I_{LOAD} = 20mA (Note 2) L/M, I_{LOAD} = 300mA (Note 2) T/S, I_{LOAD} = 300mA (Note 3)		84	130	mV
			L/M, I_{LOAD} = 300mA (Note 2)		1200	1800	
			T/S, I_{LOAD} = 300mA (Note 3)		1700	2400	
		(MAX6791–MAX6794)	L/M, I_{LOAD} = 150mA (Note 2)		1000	1800	
			L/M, I_{LOAD} = 10mA (Note 2)		84	130	
			T/S, I_{LOAD} = 150mA (Note 3)		1700	2400	
Guaranteed Output Current (Note 4)		MAX6795/MAX6796, inferred from dropout test		300			mA
		MAX6791–MAX6794, inferred from dropout test		150			

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Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Short-Circuit Output Current Limit (Note 4)		MAX6795/MAX6796, output shorted, V_{IN} = 6V	400	480		mA
		MAX6791–MAX6794, output shorted, V_{IN} = 6V	200	240		
Thermal-Shutdown Temperature				+165		°C
Thermal-Shutdown Hysteresis				20		°C
Line Regulation		8V ≤ V_{IN} ≤ 72V, I_{LOAD} = 1mA			1	% of V_{OUT}
		8V ≤ V_{IN} ≤ 72V, I_{LOAD} = 10mA			1	
Load Regulation (Note 5)		I_{OUT} = 1mA to 300mA (MAX6795/MAX6796)			2	%
		I_{OUT} = 1mA to 150mA (MAX6791–MAX6794)			1.5	
Power-Supply Rejection Ratio	PSRR	I_{LOAD} = 10mA, f = 100Hz, V_{IN} = 500mV_{P-P}		69		dB
Startup Response Time	t_{START}	I_{LOAD} = 300mA, V_{OUT} = 5V, V_{OUT} = 90% of its nominal value		180		µs
		I_{LOAD} = 150mA, V_{OUT} = 5V, $V_{OUT1/OUT2}$ = 90% of its nominal value		360		
Output Overvoltage Protection Threshold	OV_{TH}	I_{SINK} = 1mA from OUT/OUT1/OUT2		1.05 x V_{OUT}	1.1 x V_{OUT}	V
Output Overvoltage Protection Sink Current		V_{OUT} = V_{OUT} (nominal) x 1.15	5	10		mA
IN to GATEP Clamp Voltage		I_{GATEP} = -100µA, V_{IN} = 20V	13.8	16.3	18.8	V
IN to GATEP Drive Voltage		I_{GATEP} = 0A, V_{IN} = 20V	8	10	12	V
ENABLE/ENABLE1/ENABLE2/ $\overline{HOLD}$ Input-Voltage Low	V_{IL}				0.4	V
ENABLE/ENABLE1/ENABLE2/ $\overline{HOLD}$ Input-Voltage High	V_{IH}		1.4			V
ENABLE/ENABLE1/ENABLE2 Input Pulldown Current		Enable is internally pulled down to GND		0.5		µA
$\overline{HOLD}$ Input Pullup Current		$\overline{HOLD}$ is internally pulled to OUT/OUT1		2		µA

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET OUTPUT							
Reset Threshold (Preset Output Voltage)		SET/SET1 = GND	L	4.500	4.625	4.750	V
			M	4.250	4.375	4.500	
			T	2.970	3.053	3.135	
			S	2.805	2.888	2.970	
			Z	2.250	2.313	2.375	
			Y	2.125	2.188	2.250	
			W	1.620	1.665	1.710	
			V	1.530	1.575	1.620	
Reset Threshold (Adjustable Output Voltage)		L/T/Z/W		0.90 x V_{OUT}	0.925 x V_{OUT}	0.95 x V_{OUT}	V
		M/S/Y/V		0.85 x V_{OUT}	0.875 x V_{OUT}	0.90 x V_{OUT}	
OUT to Reset Delay		V_{OUT1}/V_{OUT} falling			35		µs
Reset Timeout Period (CSRT = OUT/OUT1)	t_{RP}	V_{OUT1}/V_{OUT} rising	D0		35		µs
			D1	2.187	3.125	4.063	ms
			D2	8.75	12.5	16.25	
			D3	35	50	65	
			D4	140	200	260	
CSRT Ramp Current				800	1000	1250	nA
CSRT Ramp Threshold				1.185	1.218	1.255	V
WATCHDOG INPUT							
Normal Watchdog Timeout Period	t_{WD2}	CSWT = OUT/OUT1 (fixed)		280.0	400.0	520.0	ms
		CSWT = 1500pF (adjustable)		170	236.2	290	
Fast Watchdog Timeout Period SET Ratio = 8	t_{WD1}	CSWT = OUT/OUT1 (fixed)		37.5	50.0	62.5	ms
		CSWT = 1500pF (adjustable)		21.95	29.52	36.90	
Fast Watchdog Timeout Period SET Ratio = 16	t_{WD1}	CSWT = OUT/OUT1 (fixed)		18.75	25.0	31.25	ms
		CSWT = 1500pF (adjustable)		10.80	14.76	18.45	
Fast Watchdog Timeout Period SET Ratio = 64	t_{WD1}	CSWT = OUT/OUT1 (fixed)		4.68	6.25	7.81	ms
		CSWT = 1500pF (adjustable)		2.52	3.69	4.62	
Fast Watchdog Minimum Period	t_{WD0}			2000			ns
CSWT Ramp Current		Adjustable timeout		800	1000	1250	nA
CSWT Ramp Threshold		Adjustable timeout		1.185	1.218	1.255	V
Undercurrent Threshold for Watchdog Enable				7.0	10	13.8	mA
Undercurrent Threshold for Watchdog Disable				3	5	7	mA

Electrical Characteristics (continued)

(V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

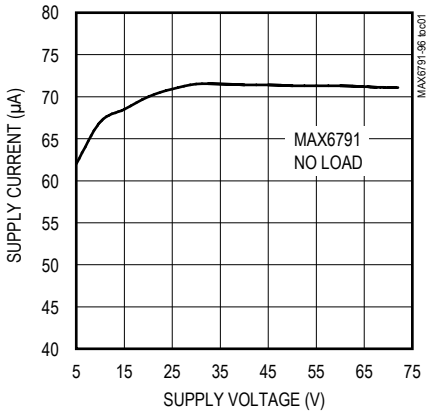
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT (WDS0, WDS1, WD-DIS, WDI)						
Input-Voltage Low	V_{IL}				0.4	V
Input-Voltage High	V_{IH}		1.4			V
Input Current		Inputs connected to OUT/OUT1 or GND	-100		+100	nA
POWER-FAIL COMPARATOR						
PFI Threshold	V_{PFI}		1.199	1.231	1.263	V
PFI Hysteresis				0.5		%
PFI Input Current		V_{PFI} = 14V	-100		+100	nA
PFI to $\overline{PFO}$ Delay		(V_{PFI} + 50mV) to (V_{PFI} - 50mV)		35		µs
LOGIC OUTPUT ($\overline{RESET}$, $\overline{PFO}$)						
Output-Voltage Low (Open-Drain or Push-Pull)	V_{OL}	I_{SINK} = 50µA (output asserted)			0.3	V
		I_{SINK} = 3.2mA (output asserted)			0.4	
Output-Voltage High (Push-Pull)	V_{OH}	V_{OUT} ≥ 1.0V, I_{SOURCE} = 10µA (output not asserted)	0.8 x V_{OUT}			V
		V_{OUT} ≥ 1.5V, I_{SOURCE} = 100µA (output not asserted)	0.8 x V_{OUT}			
		V_{OUT} ≥ 2.2V, I_{SOURCE} = 500µA (output not asserted)	0.8 x V_{OUT}			
Open-Drain Leakage		$V_{\overline{RESET}}$ = $V_{\overline{PFO}}$ = 12V (output not asserted)			100	nA

Note 1: All devices are 100% production tested at T_J = +25°C and +125°C. Limits at -40°C are guaranteed by design.
Note 2: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 98% of V_{OUT} for V_{IN} = 8V.
Note 3: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 98% of V_{OUT} for V_{IN} = 6V.
Note 4: Operation beyond the absolute maximum power dissipation is not guaranteed and may damage the part.
Note 5: Test at V_{IN} = 8V (L/M), V_{IN} = 6V (T/S), V_{IN} = 5V (Z/Y/W/V).

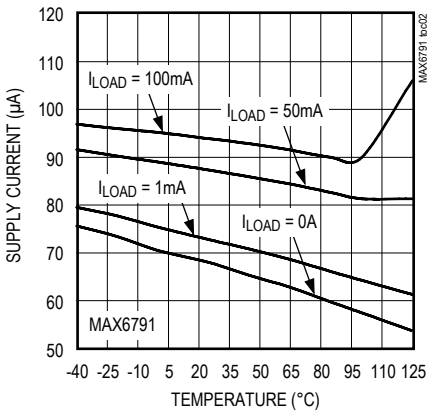
Typical Operating Characteristics

(V_{IN} = V_{EN} = 14V, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_J = T_A = +25°C, unless otherwise noted.)

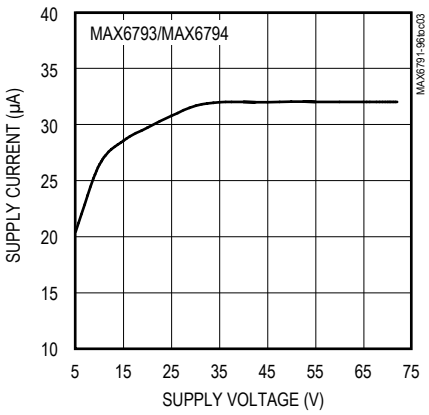
SUPPLY CURRENT vs. SUPPLY VOLTAGE



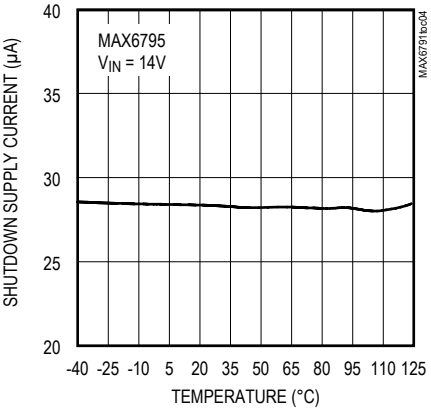
SUPPLY CURRENT vs. TEMPERATURE



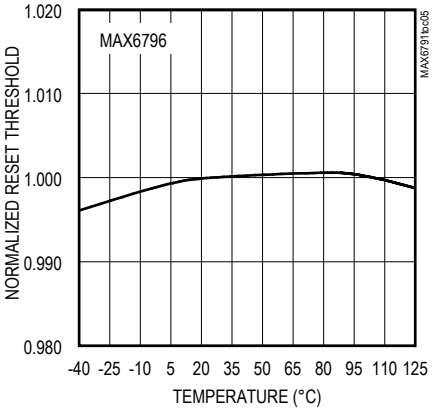
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



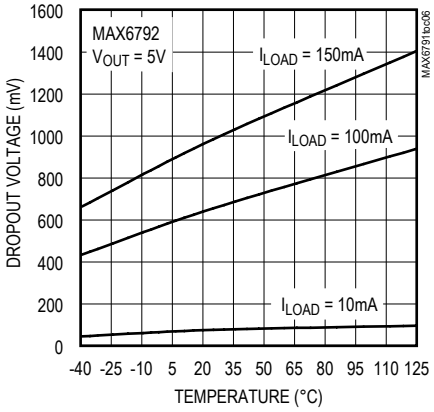
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



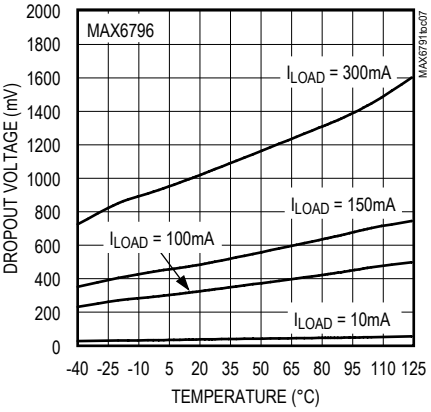
NORMALIZED RESET THRESHOLD vs. TEMPERATURE



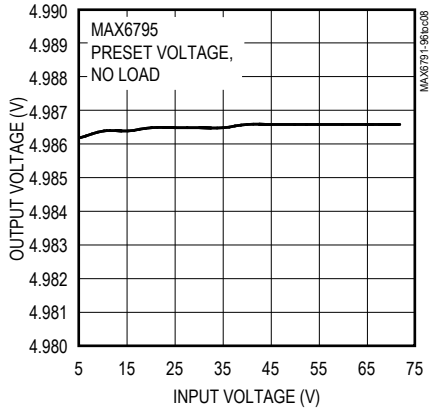
DROPOUT VOLTAGE vs. TEMPERATURE



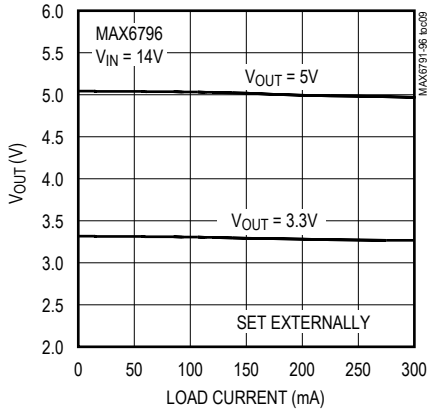
DROPOUT VOLTAGE vs. TEMPERATURE



OUTPUT VOLTAGE vs. INPUT VOLTAGE



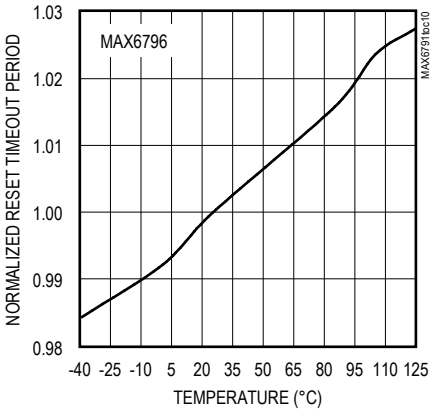
OUTPUT VOLTAGE vs. LOAD CURRENT



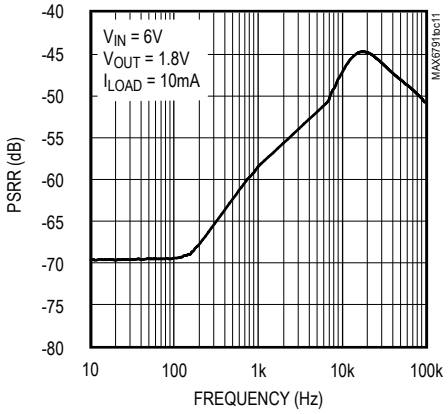
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_J = T_A = +25°C, unless otherwise noted.)

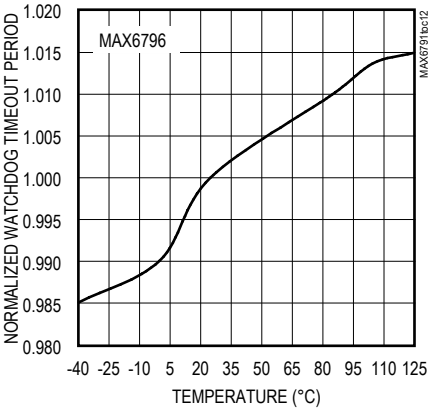
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



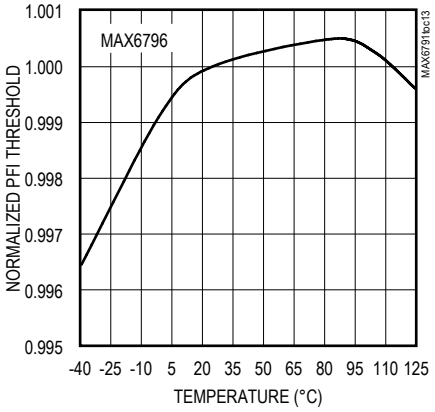
PSRR vs. FREQUENCY



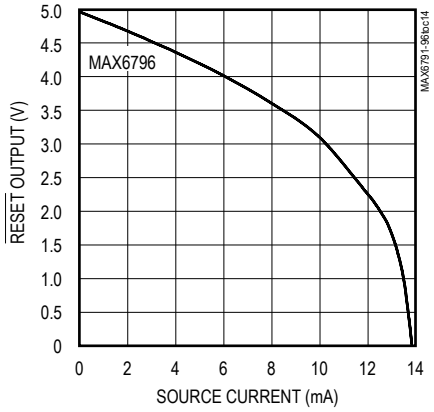
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



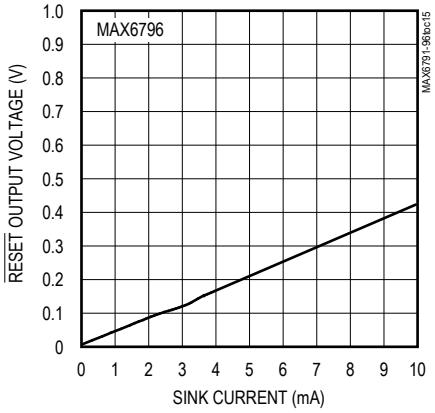
NORMALIZED PFI THRESHOLD vs. TEMPERATURE



$\overline{\text{RESET}}$ OUTPUT vs. SOURCE CURRENT



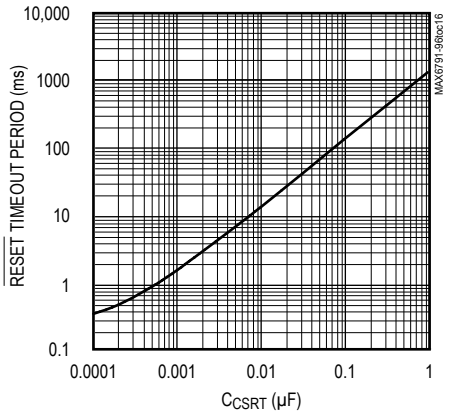
$\overline{\text{RESET}}$ OUTPUT VOLTAGE vs. SINK CURRENT



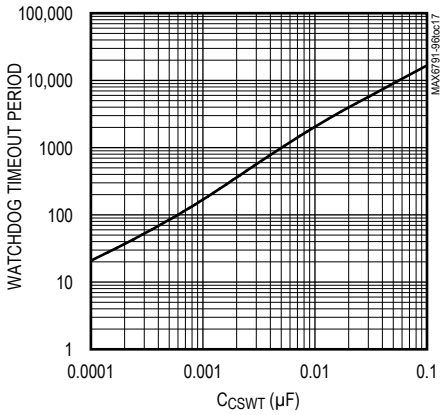
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_J = T_A = +25°C, unless otherwise noted.)

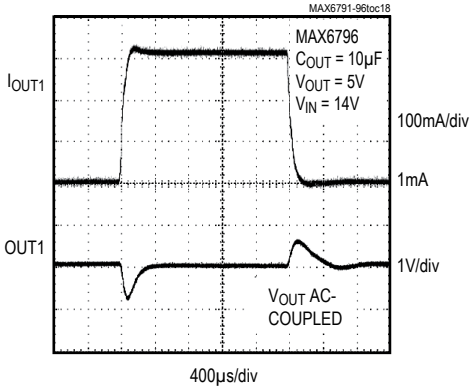
$\overline{\text{RESET}}$ TIMEOUT PERIOD vs. C_{CSRT}



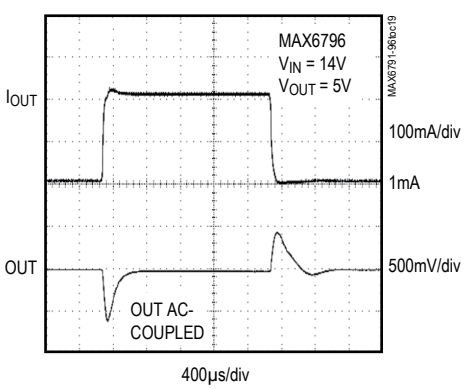
WATCHDOG TIMEOUT PERIOD vs. C_{CSWT}



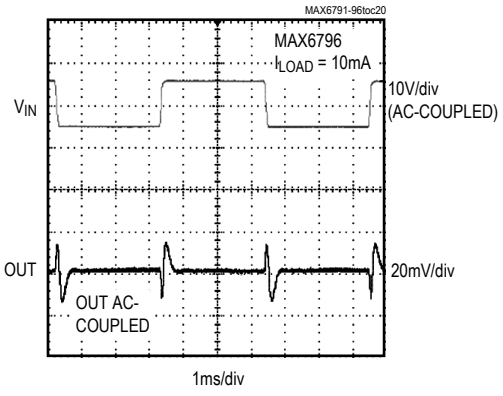
LOAD-TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE



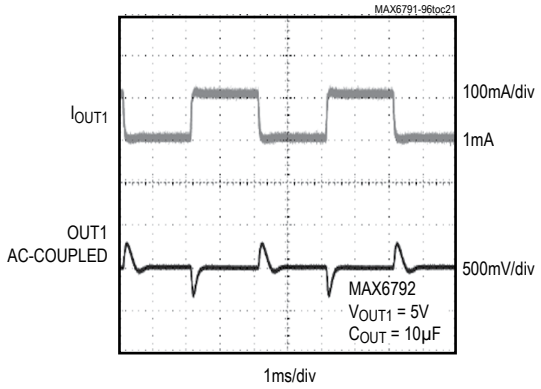
LINE-TRANSIENT RESPONSE



Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_J = T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



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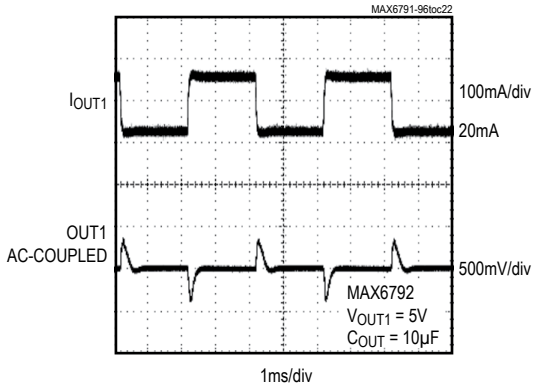


Pin Description

PIN			NAME	FUNCTION
MAX6791/ MAX6792	MAX6793/ MAX6794	MAX6795/ MAX6796		
1, 2	1, 2	—	OUT1	Regulator 1 Output. Fixed (+1.8V, +2.5V, +3.3V, or +5V) or adjustable (+1.8V to +11V). V_{OUT1} = 150mA (max). Connect a 10µF (min) capacitor from OUT1 to GND.
3	3	—	SET1	Feedback Input for Setting the OUT1 Voltage. Connect SET1 to GND to select the preset output voltage. Connect to an external resistive divider for adjustable output operation.
4	4	4	$\overline{PFO}$	Active-Low, Open-Drain, Power-Fail Comparator Output. $\overline{PFO}$ asserts low when PFI is below the internal 1.231V threshold. $\overline{PFO}$ deasserts when PFI is above the internal 1.231V threshold.
5	5	5	CSWT	Watchdog Timeout Period Adjust Input. Connect CSWT to OUT1/OUT for the internally fixed watchdog timeout period. For adjustable watchdog timeout period, connect a capacitor from CSWT to GND. See the *Selecting Watchdog Timeout Period* section for more details.
6	6	6	CSRT	Reset Timeout Period Adjust Input. Connect CSRT to OUT1/OUT for the internally fixed timeout period. For adjustable timeout, connect a capacitor from CSRT to GND. See the *Reset Output* section for more details.
7	7	7	GND	Ground
8	8	8	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low while OUT1/OUT is below the reset threshold. $\overline{RESET}$ remains low for the duration of the reset timeout period after the reset conditions end. $\overline{RESET}$ is available in push-pull and open-drain options.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX6791/ MAX6792	MAX6793/ MAX6794	MAX6795/ MAX6796		
9	—	—	WDS1	Min/Max Watchdog Logic-Select Input. WDS0 and WDS1 select the watchdog window ratio or disable the watchdog timer. Drive WDS0 and WDS1 high or low to select the desired ratio, see Table 4.
10	—	—	WDS0	
11	11	11	WDI	Watchdog Input. MAX6793–MAX6796: A falling or rising transition must occur on WDI within the selected watchdog timeout period or a reset pulse occurs. The watchdog timer clears when a transition occurs on WDI or whenever $\overline{\text{RESET}}$ is asserted. MAX6791/MAX6792: WDI falling and rising transitions within periods shorter than t_{WD1} or longer than t_{WD2} force $\overline{\text{RESET}}$ to assert low for the reset timeout period. The watchdog timer begins to count after $\overline{\text{RESET}}$ is deasserted. The watchdog timer clears when a valid transition occurs on WDI or whenever $\overline{\text{RESET}}$ is asserted. Connect WDS0 high and WDS1 low to disable the watchdog timer function. See the *Watchdog Timer* section.
12	12	12	$\overline{\text{HOLD}}$	Active-Low Regulator Hold Input. When $\overline{\text{HOLD}}$ is forced low, OUT1/OUT remains ON even if ENABLE1/ENABLE is pulled low. To shut down the output of the regulator (OUT/OUT1), release $\overline{\text{HOLD}}$ after ENABLE1/ENABLE is pulled low. Connect $\overline{\text{HOLD}}$ to OUT1/OUT or leave unconnected if unused. $\overline{\text{HOLD}}$ is internally connected to OUT/OUT1 through a 2µA current source.
13, 14	13, 14	—	OUT2	Regulator 2 Output. OUT2 is a fixed +5V output. Connect a 10µF (min) capacitor from OUT2 to GND.
15	15	—	ENABLE2	Active-High Enable Input 2. Drive ENABLE2 high to turn on OUT2. ENABLE2 is internally connected to ground through a 0.5µA current sink.
16	16	16	PFI	Adjustable Power-Fail Comparator Input. Connect PFI to a resistive-divider to set the desired PFI threshold. The PFI input is referenced to an accurate 1.231V threshold.
17, 18	17, 18	17, 18	IN	Regulator Inputs. Bypass IN with a 1µF capacitor to GND.
19	19	19	GATEP	pFET Gate Drive. Connect GATEP to the gate of a p-channel MOSFET to provide low drop reverse-battery voltage protection.
20	20	—	ENABLE1	Active-High Enable Input 1. Drive ENABLE1 high to turn on OUT1. ENABLE1 is internally connected to ground through a 0.5µA current sink.
—	9	9	WD-DIS	Watchdog Disable Input. Drive WD-DIS low to disable the watchdog timer. Drive WD-DIS high or connect to OUT/OUT1 to enable the watchdog timer. The watchdog timer clears when reset asserts.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX6791/ MAX6792	MAX6793/ MAX6794	MAX6795/ MAX6796		
—	10	10, 13, 14, 15	N.C.	Not Internally Connected
—	—	1, 2	OUT	Regulator Output. Fixed +5V, +3.3V, +2.5V, +1.8V, or adjustable output (+1.8V to +11V). Connect a 10µF (min) capacitor from OUT to GND.
—	—	3	SET	Feedback Input for Setting the OUT Voltage. Connect SET to GND to select the preset output voltage. Connect to an external resistive-divider for adjustable output operation.
—	—	20	ENABLE	Active-High Enable Input. Drive ENABLE high to turn on the regulator. ENABLE is internally connected to ground through a 0.5µA current sink.
—	—	—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PC board. Do not use as the electrical connection to GND.

Detailed Description

The MAX6791–MAX6796 ultra-low-quiescent-current, single-/dual-output, high-input-voltage linear regulators operate from 5V to 72V. The MAX6791–MAX6794 feature dual regulators that deliver up to 150mA of load current per output. One output is available with preset output-voltage options (+1.8V, +2.5V, +3.3V, and +5.0V) and can be adjusted to any voltage between +1.8V to +11V using an external resistive-divider at SET1. The other output provides a fixed 5V output voltage. The MAX6795/MAX6796 feature a single regulator that delivers up to 300mA of current with preset output-voltage options (+1.8V, +2.5V, +3.3V, and +5.0V) or can be adjusted to any voltage between +1.8V to +11V.

All devices include an integrated µP reset circuit with a fixed/adjustable reset and watchdog timeout period. The MAX6791–MAX6796 monitor OUT/OUT1 and assert a reset output when the output falls below the reset threshold.

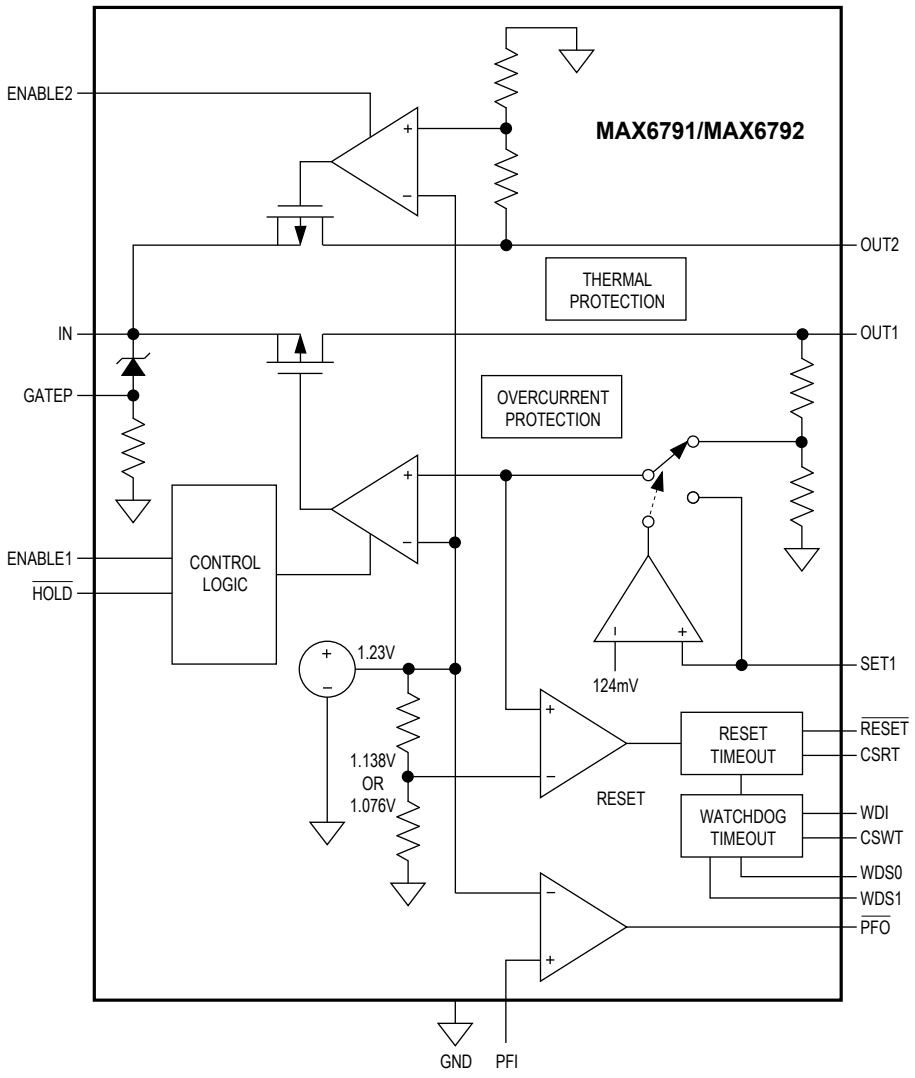
Regulators

The single and dual regulators accept an input voltage from 5V to 72V. The MAX6791–MAX6796 offer fixed preset output voltages of +1.8V, +2.5V, +3.3V, and +5V, or an adjustable output voltage of +1.8V to +11V, selected using an external resistive-divider network connected between OUT1/OUT, SET1/SET, and GND (see Figure 1). In addition to an adjustable output, the MAX6791–MAX6794 feature a fixed 5V output voltage.

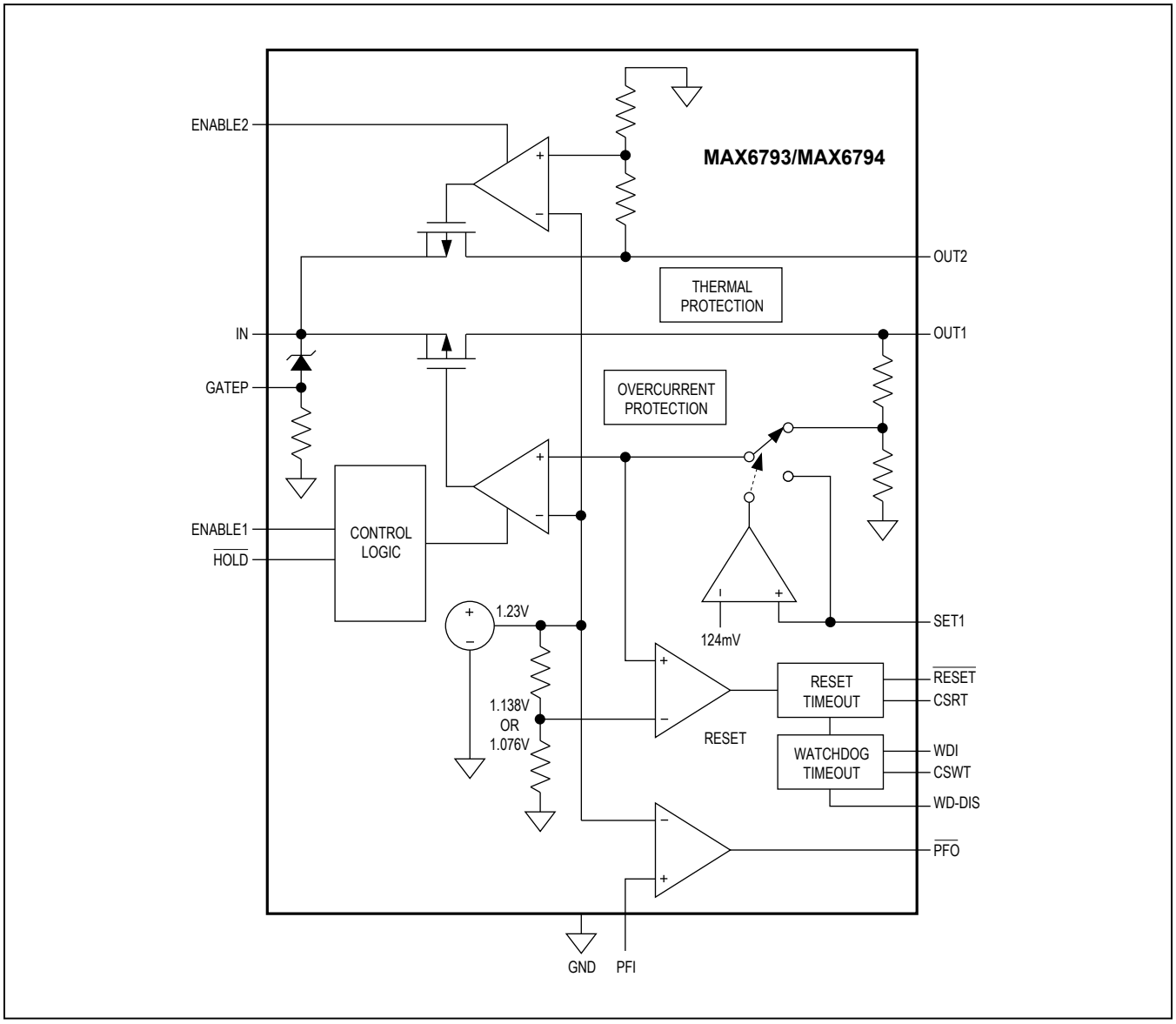
Reset Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6791–MAX6796 supervisory circuits provide the reset logic output to prevent code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Application Circuit*). $\overline{\text{RESET}}$ changes from high to low whenever the monitored output voltage drops below the reset threshold voltage or the watchdog timeout expires. Once the monitored voltage exceeds its respective reset threshold voltage, $\overline{\text{RESET}}$ remains low for the reset timeout period, then goes high.

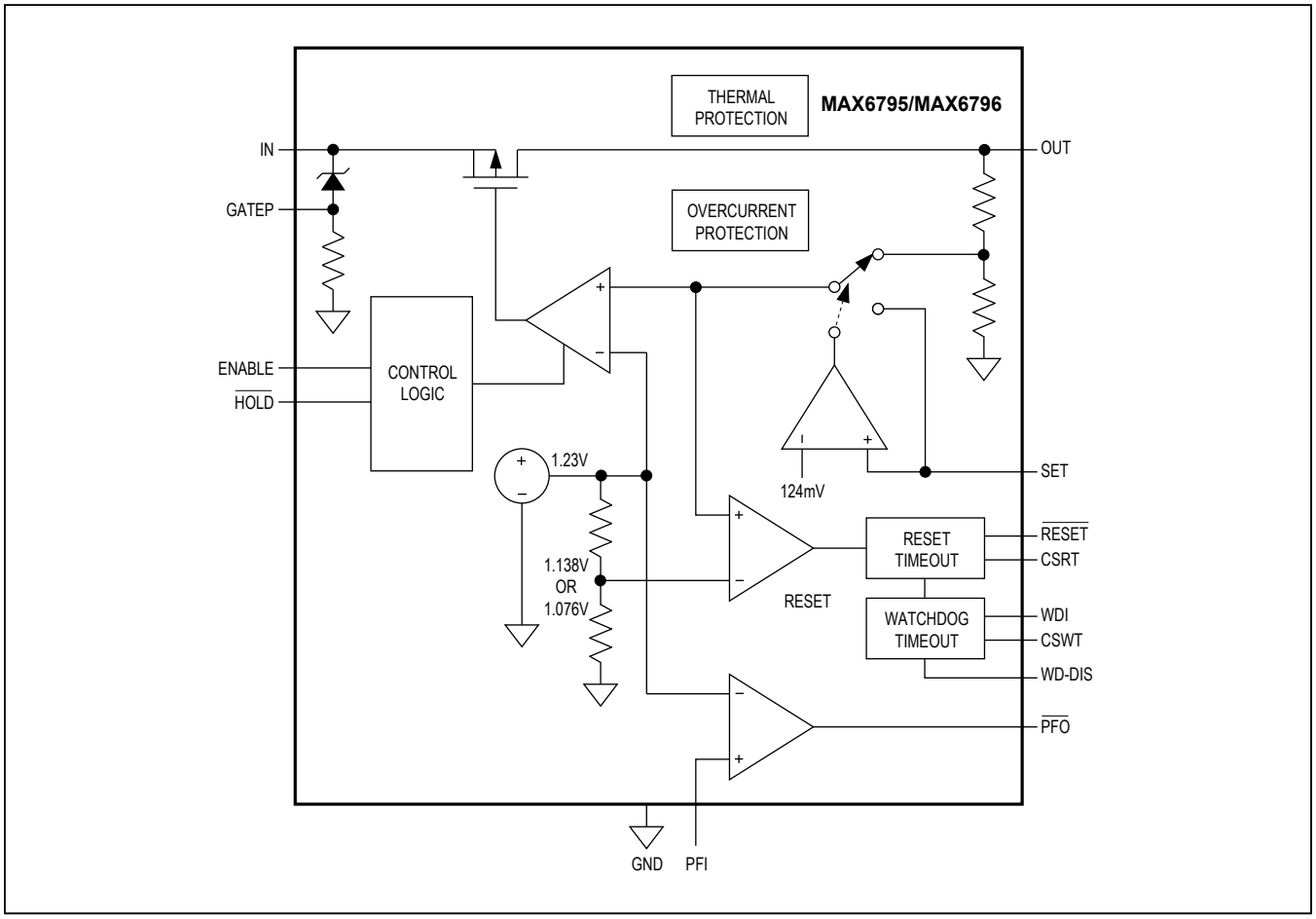
Functional Diagrams



Functional Diagrams (continued)



Functional Diagrams (continued)



Watchdog Timer

The MAX6791–MAX6796 include a watchdog timer that asserts $\overline{RESET}$ if the watchdog input (WDI) does not toggle high to low or low to high within the watchdog timeout period t_{WD} (280ms min or externally adjustable). $\overline{RESET}$ remains low for the fixed or user-adjustable reset timeout period, t_{RP}. If the watchdog is not updated for lengthy periods of time, the reset output appears as a pulse train, asserted for t_{RP}, deasserted for t_{WD}, until WDI is toggled again. Once $\overline{RESET}$ asserts, it stays low for the entire reset timeout period ignoring any WDI transitions that may occur. To prevent the watchdog from asserting $\overline{RESET}$, toggle WDI with a valid rising or falling edge before t_{WD} from the last edge. The watchdog counter clears when WDI toggles prior to t_{WD} from the last edge or when $\overline{RESET}$ asserts. The watchdog resumes counting after $\overline{RESET}$ deasserts.

The MAX6791/MAX6792 have a windowed watchdog timer that asserts $\overline{RESET}$ for the adjusted reset timeout period when the watchdog recognizes a fast watchdog fault ($t_{WDI} < t_{WD1}$), or a slow watchdog fault ($t_{WDI} > t_{WD2}$). The reset timeout period is adjusted independently of the watchdog timeout period.

Enable and Hold Inputs

The MAX6791–MAX6796 support two logic inputs, ENABLE1/ENABLE and $\overline{HOLD}$, making these devices suitable for automotive applications. For example, when the ignition key signal drives ENABLE1/ENABLE high, the regulator turns on and remains on even if ENABLE1/ENABLE goes low, as long as $\overline{HOLD}$ is forced low and stays low after initial regulator power-up. In this state, releasing $\overline{HOLD}$ turns the regulator output (OUT/OUT1) off. This feature makes it possible to implement a self-holding circuit without external components. Forcing ENABLE1/ENABLE low and $\overline{HOLD}$ high or unconnected places the MAX6791–MAX6796 into shutdown mode in which the MAX6791–MAX6796 draw less than 27µA of supply current.

Table 3 shows the state of the regulator output with respect to the voltage level at ENABLE1/ENABLE and $\overline{HOLD}$. Connect $\overline{HOLD}$ to OUT1/OUT or leave it unconnected to allow the ENABLE1/ENABLE input to act as a standard ON/OFF switch for the regulator output (OUT/OUT1).

Power-Fail Comparator

PFI is the noninverting input to a comparator. If PFI is less than V_{PFI} (1.231V), $\overline{PFO}$ goes low. Common uses for the power-fail comparator include monitoring the preregulated input of the power supply (such as a battery) or providing an early power-fail warning so software can conduct an orderly system shutdown. Set the power-fail threshold with a resistive-divider, as shown in Figure 5. The typical comparator delay is 35µs from PFI to $\overline{PFO}$. Connect PFI to GND or IN if unused.

Reverse-Battery Protection Circuitry

The MAX6791–MAX6796 include an overvoltage protection circuit that is capable of driving a p-channel MOSFET to protect against reverse-battery conditions. This MOSFET eliminates the need for external diodes, thus minimizing the input voltage drop. See the *Typical Application Circuit*. The low p-channel MOSFET on-resistance of 30mΩ or less yields a forward-voltage drop of only a few millivolts versus hundreds of millivolts for a diode, thus improving efficiency in battery-operated devices. Connecting a positive battery voltage to the drain of Q1 (see the *Typical Application Circuit*) forward biases its body diode. When the source voltage exceeds Q1's threshold voltage, Q1 turns on. Once the FET is on, the battery is fully connected to the system and can deliver power to the device and the load. An incorrectly inserted battery reverse-biases the FET's body diode. The gate remains at the ground potential. The FET remains off and disconnects the reversed battery from the system. The internal zener diode and resistor combination at GATEP prevent damage to the p-channel MOSFET during an overvoltage condition. See the *Functional Diagrams*.

Thermal Protection

When the junction temperature exceeds T_J = +165°C, the internal protection circuit turns off the internal pass transistor and allows the IC to cool. The thermal sensor turns the pass transistor on again after the junction temperature drops to +145°C, resulting in a cycled output during continuous thermal-overload conditions. Thermal protection protects the MAX6791–MAX6796 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Proper Soldering of Package Heatsink

The MAX6791–MAX6796 package features an exposed thermal pad on its underside that should be used as a heatsink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PC board. Connect the exposed pad and GND to the system ground using a large pad or ground plane, or multiple vias to the ground plane layer.

Applications Information

Output Voltage Selection

The MAX6791–MAX6796 feature dual-mode operation: these devices operate in either a preset voltage mode or an adjustable mode. In preset voltage mode, internal trimmed feedback resistors set the internal linear regulator to +1.8V, +2.5V, +3.3V, or +5V (see the *Selector Guide*). Select preset voltage mode by connecting SET1 (MAX6791–MAX6794)/SET(MAX6795/MAX6796) to GND. In adjustable mode, select an output voltage between +1.8V and +11V using two external resistors connected as a voltage-divider to SET1/SET (see Figure 1). Set the output voltage using the following equation:

$$V_{OUT} = V_{SET}\left(1+\frac{R1}{R2}\right)$$

where V_{SET} = 1.2315V and R1, R2 ≤ 200kΩ.

Available Output-Current Calculation

The MAX6791–MAX6794 provide up to 150mA per output, and the MAX6795/MAX6796 provide up to 300mA of load current. Since the input voltage can be as high as +72V, package power dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figure 2 shows the maximum power-dissipation curve for the MAX6791–MAX6796. The graph assumes that the exposed metal pad of the device package is soldered to a solid 1in^2 section of PC board copper. Use Figure 2 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation:

PD_{MAX} = Maximum Power Dissipation

PD_{MAX} = 2.666W, for T_A ≤ +70°C

PD_{MAX} = [2.666W - 0.0333W x (T_A - 70°C)], for +70°C < T_A ≤ +125°C

where 0.0333W is the MAX6791–MAX6796 package thermal derating in W/°C and T_A is the ambient temperature in °C.

After determining the allowable package dissipation, calculate the maximum output current using the following formula:

PD = Power Dissipation

PD < PD_{MAX} where PD = [(IN - OUT1) x I_{OUT1}] + [(IN - OUT2) x I_{OUT2}], for MAX6791–MAX6794.

Also, I_{OUT1} should be ≤ 150mA and I_{OUT2} should be ≤ 150mA in any case.

PD < PD_{MAX} where PD = [(IN - OUT) x I_{OUT}], for MAX6795/MAX6796.

Also, I_{OUT} should be ≤ 300mA in any case.

Selecting Reset Timeout Period

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period by connecting a capacitor between CSRT and GND. Use the following formula to set the reset time period:

$$t_{RP} = C_{CSRT}\left(1.218\times10^{6}\frac{V}{A}\right)$$

where t_{RP} is in seconds and C_{CSRT} is in Farads.

Connect CSRT to OUT1 (MAX6791–MAX6794) or to OUT (MAX6795/MAX6796) to select an internally fixed timeout period. Connect CSRT to GND to force $\overline{RESET}$ low. C_{CSRT} must be a low-leakage (< 10nA) type capacitor. Ceramic capacitors are recommended; do not use capacitors lower than 100pF to avoid the influence of parasitic capacitances.

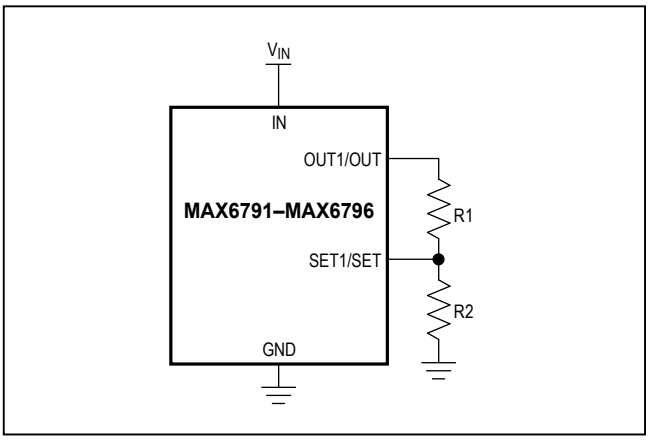


Figure 1. Setting the Output Voltage Using a Resistive-Divider

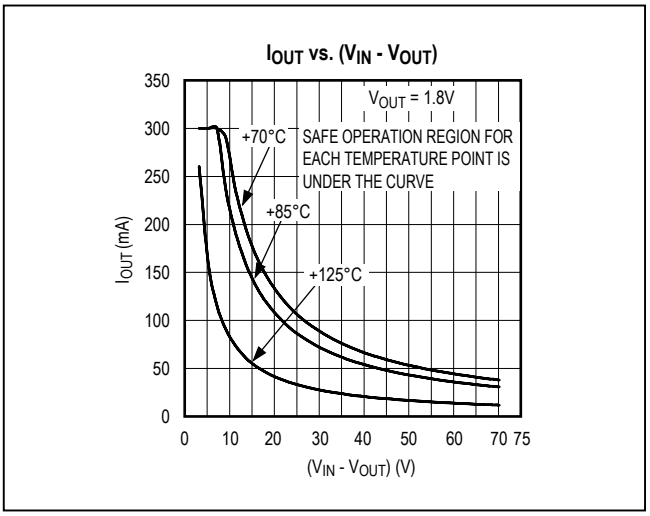


Figure 2. Maximum Power Dissipation for MAX6791–MAX6796

Selcting Watchdog Timeout Period

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a capacitor between CSWT and GND. For normal-mode operation, calculate the watchdog timeout capacitor as follows:

$$t_{WD2} = C_{CSWT}\left(155 \times 10^6 \frac{V}{A}\right)$$

where t_{WD} is in seconds and C_{CSWT} is in Farads.

To select the internally fixed watchdog timeout period for the MAX6791–MAX6794, connect CSWT to OUT1. To select the internally fixed watchdog timeout period for the MAX6795/MAX6796, connect CSWT to OUT.

C_{CSWT} must be a low-leakage (< 10nA) type capacitor. Ceramic capacitors are recommended; do not use capacitors lower than 100pF to avoid the influence of parasitic capacitances.

The MAX6791/MAX6792 have a windowed watchdog timer that asserts $\overline{RESET}$ for t_{RP} when the watchdog recognizes a fast watchdog fault (time between transitions < t_{WD1}), or a slow watchdog fault (time between transitions > t_{WD2}). The reset timeout period is adjusted independently of the watchdog timeout period. The slow watchdog period, t_{WD2}, is calculated as follows:

$$t_{WD2} = C_{CSWT}\left(155 \times 10^6 \frac{V}{A}\right)$$

where t_{WD2} is in seconds and C_{CSWT} is in Farads.

The fast watchdog period, t_{WD1}, is selectable as a ratio from the slow watchdog fault period (t_{WD2}). Select the fast watchdog period by connecting WDS0 and WDS1 to OUT/OUT1 or GND according to Table 4, which illustrates the settings for the 8, 16, and 64 window ratios (t_{WD2}/t_{WD1}). For example, if C_{CSWT} is 2000pF, and WDS0 and WDS1 are low, then t_{WD2} is 318ms (typ) and t_{WD1} is 40ms (typ). $\overline{RESET}$ asserts if the watchdog input has two edges too close to each other (faster than t_{WD1}); or has edges that are too far apart (slower than t_{WD2}).

All WDI inputs are ignored while $\overline{RESET}$ is asserted. The watchdog timer begins to count after $\overline{RESET}$ is deasserted. If the time difference between two transitions on WDI is shorter than t_{WD1} or longer than t_{WD2}, $\overline{RESET}$ is forced to assert low for the reset timeout period. If the time difference between two transitions on WDI is between t_{WD1} (min) and t_{WD1} (max) or t_{WD2} (min) and t_{WD2} (max), $\overline{RESET}$ is not guaranteed to assert or deassert; see Figure 3. To guarantee that the window watchdog does not assert $\overline{RESET}$, strobe WDI between t_{WD1} (max) and t_{WD2} (min). The watchdog timer is cleared when $\overline{RESET}$ is asserted. Disable the watchdog timer by connecting WDS0 high and WDS1 low.

There are several options available to disable the watchdog timer (for system development or test purposes or when the µP is in a low-power sleep mode). One way to disable the watchdog timer is to drive WD-DIS low for the MAX6793–MAX6796 and drive WDS0 high and WDS1 low for the MAX6791/MAX6792. This prevents the capacitor from ramping up. Finally, reducing the OUT/OUT1 regulator current below the specified regulator current watchdog-disable threshold (3mA min) also disables the watchdog timer.

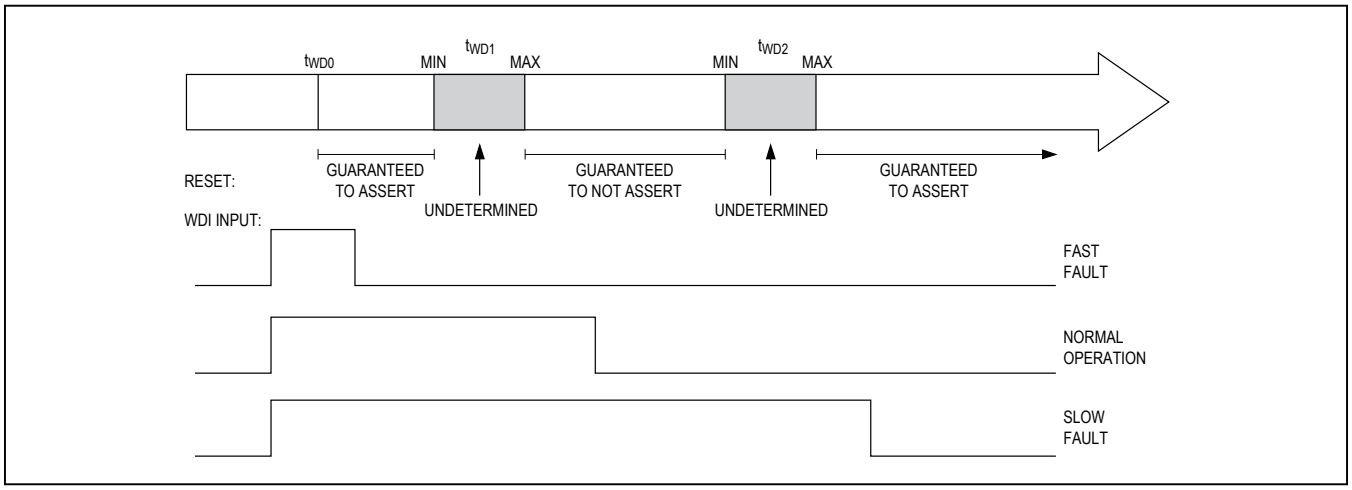


Figure 3. Windowed Watchdog Timing Diagram

The watchdog re-enables immediately when any of these conditions are removed (as long as the $\overline{\text{RESET}}$ is not asserted). Note that the output current threshold limit includes hysteresis so that output current must exceed 13.8mA (max) to reenable the watchdog timer.

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 150mA, use a 10µF (min) output capacitor with an ESR < 0.5Ω. To reduce noise and improve load-transient response and power-supply rejection, use larger output-capacitor values. Some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. For these types of capacitors (such as Z5U and Y5V), much higher-value capacitors are required to maintain stability over the temperaure range. With X7R dielectrics, a 10µF capacitor should be sufficient at all operating temperatures. To improve power-supply rejection and transient response, increase the capacitor between IN and GND.

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{IN} = 0V

When V_{IN} falls below 1V, $\overline{\text{RESET}}$ current-sinking capabilities decline drastically. High-impedance CMOS-logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with a supply voltage below 1V. In those applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pulldown resistor between $\overline{\text{RESET}}$ and GND sinks any stray leakage currents, holding $\overline{\text{RESET}}$ low (Figure 4). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. Open-drain $\overline{\text{RESET}}$ versions are not recommended for applications requiring valid logic for V_{IN} down to 0V.

Adding Hysteresis to PFI

The power-fail comparator has a typical input hysteresis of 0.5% (of V_{TH}). This is sufficient for most applications where a power-supply line is being monitored through an external resistive-divider (Figure 5). Figure 6 shows how to add hysteresis to the power-fail comparator. Select the ratio of R5 and R6 so PFI sees 1.23V when V_{IN} falls to the desired trip point (V_{TRIP}). Since $\overline{\text{PFO}}$ is an open-drain output, resistors R7 and R8 add hysteresis. R7 typically is an order of magnitude greater than R5 or R6. The current through R5 and R6 should be at least 10µA to ensure that the 100nA (max) PFI input current does not shift the trip point. R7 should be larger than 50kΩ to prevent it from loading down the $\overline{\text{PFO}}$.

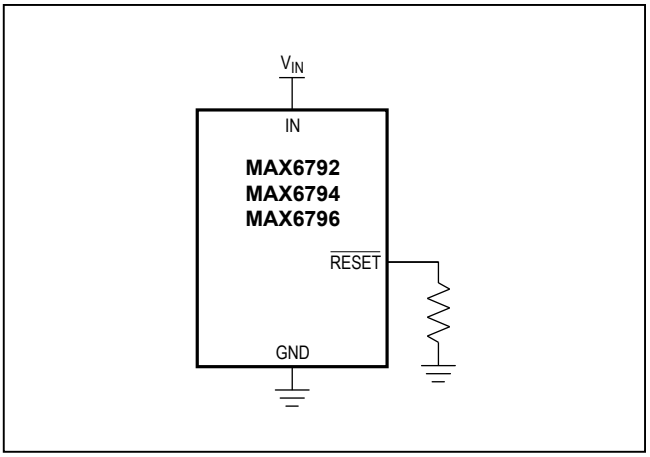


Figure 4. Ensuring $\overline{\text{RESET}}$ Valid to V_{IN} = 0V

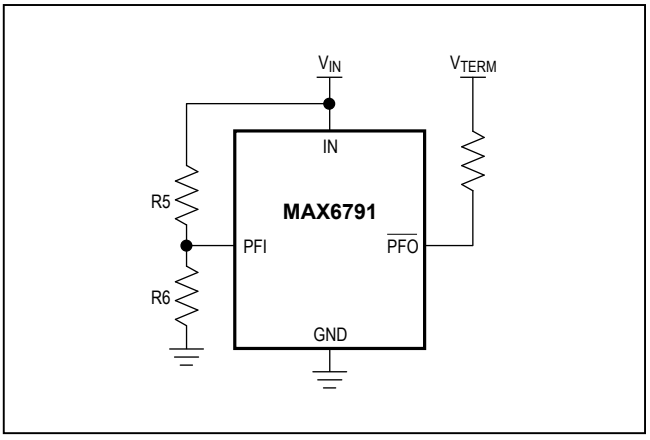


Figure 5. Setting Power-Fail Comparator to Monitor V_{IN}

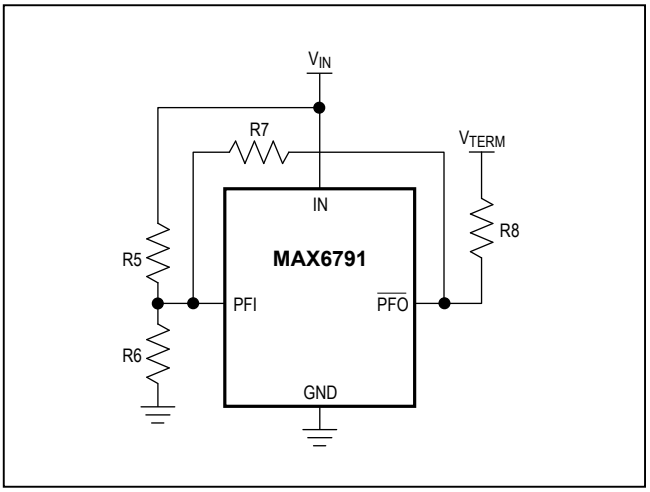


Figure 6. Adding Hysteresis Power-Fail Comparator

Table 1. Preset Output Voltage and Reset Threshold

PART SUFFIX (_)	OUTPUT VOLTAGE (V)	RESET THRESHOLD (NOMINAL)
L	5.0	4.625
M	5.0	4.375
T	3.3	3.053
S	3.3	2.888
Z	2.5	2.313
Y	2.5	2.188
W	1.8	1.665
V	1.8	1.575

Table 2. Preset Timeout Period

PART SUFFIX (_)	RESET TIMEOUT PERIOD (NOMINAL)
D0	35µs
D1	3.125ms
D2	12.5ms
D3	50ms
D4	200ms

Use the following formulas to determine the high/low threshold levels and the hysteresis:

$$V_{L-H} = V_{PFI} \times (1 + R5 / R6 + R5 / R7)$$

$$V_{H-L} = V_{PFI} \times (1 + R5 / R6) + (V_{PFI} - V_{TERM}) [R5 / (R7 + R8)]$$

$$V_{HYS} = V_{PFI} \times (R5 / R7) - (V_{PFI} - V_{TERM}) [R5 / (R7 + R8)]$$

where V_{L-H} is the threshold level for the monitored voltage rising and V_{H-L} is the threshold level for the monitored voltage falling.

Chip Information

PROCESS: BiCMOS

Table 3. ENABLE/ENABLE1 and $\overline{HOLD}$ Truth Table/State Table

OPERATING STATE	ENABLE1 ENABLE	$\overline{HOLD}$	REGULATOR 1 OUTPUT	COMMENT
Initial state	Low	Don't care	Off	ENABLE/ENABLE1 is pulled to GND through internal pulldown. OUT/OUT1 is disabled.
Turn-on state	High	Don't care	On	ENABLE/ENABLE1 is externally driven high turning OUT/OUT1 on. $\overline{HOLD}$ is pulled up to OUT/OUT1.
Hold setup state	High	Low	On	$\overline{HOLD}$ is externally pulled low while ENABLE/ENABLE1 remains high, and the regulator latches on.
Hold state	Low	Low	On	ENABLE/ENABLE1 is driven low (or allowed to float low by an internal pulldown). $\overline{HOLD}$ remains externally pulled low keeping OUT/OUT1 on.
Off state	Low	High	Off	$\overline{HOLD}$ is driven high (or pulled high by the internal pullup) while ENABLE/ENABLE1 is low. OUT/OUT1 is turned off and ENABLE/ENABLE1 and $\overline{HOLD}$ logic returns to the initial state.

Table 4. MIN/MAX Watchdog Setting

WDS0	WDS1	RATIO
0	0	8
0	1	16
1	0	Watchdog disabled
1	1	64

Table 5. Standard Version Part Number

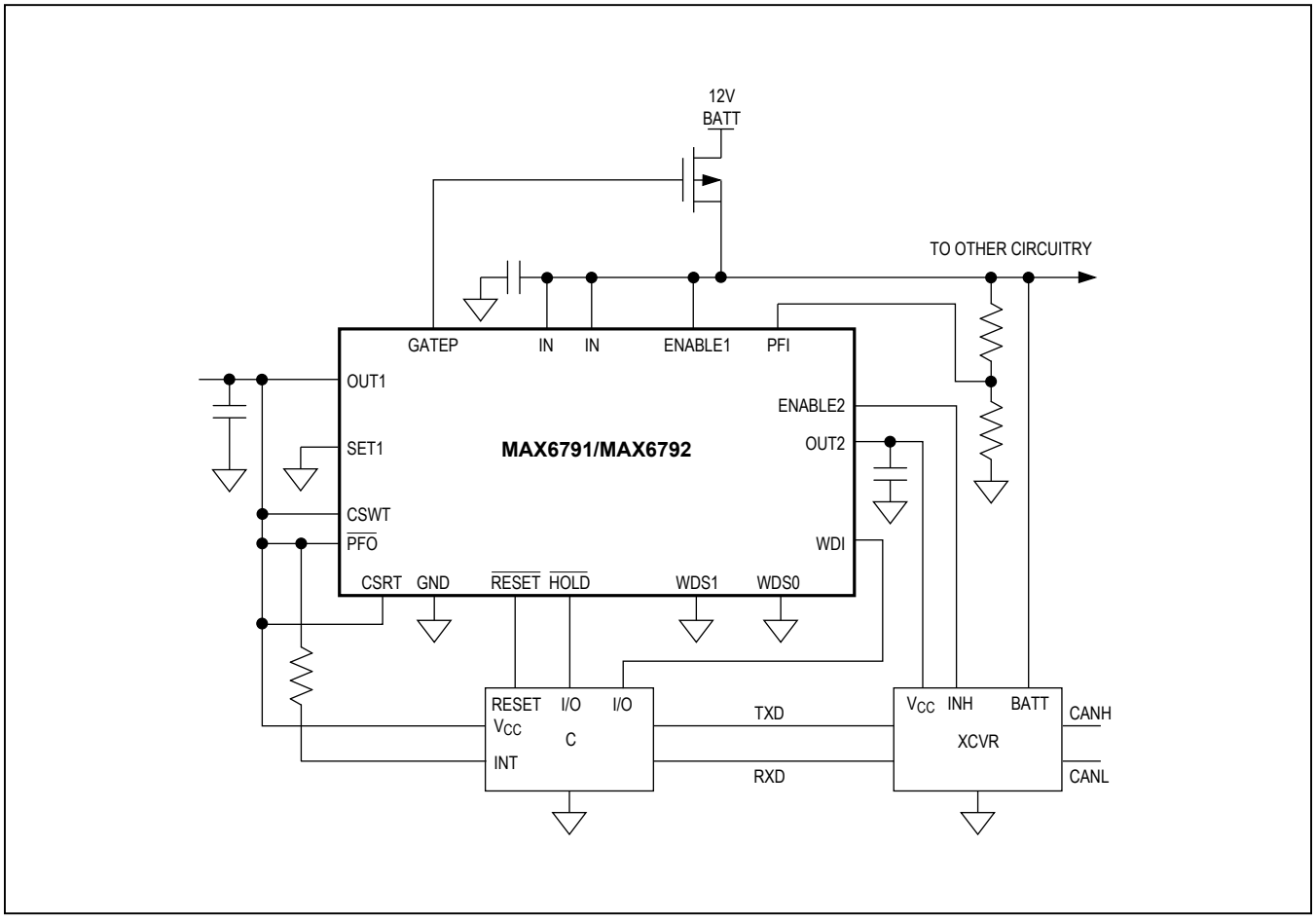
PART NUMBER	OUTPUT VOLTAGE (V)	$\overline{\text{RESET}}$ TIMEOUT PERIOD (ms) (NOMINAL)	RESET THRESHOLD (V) (NOMINAL)
MAX6791TPLD2+	5.0	12.5	4.625
MAX6791TPSD2+	3.3	12.5	2.888
MAX6792TPLD2+	5.0	12.5	4.625
MAX6792TPSD2+	3.3	12.5	2.888
MAX6793TPLD2+	5.0	12.5	4.625
MAX6793TPSD2+	3.3	12.5	2.888
MAX6794TPLD2+	5.0	12.5	4.625
MAX6794TPSD2+	3.3	12.5	2.888
MAX6795TPLD2+	5.0	12.5	4.625
MAX6795TPSD2+	3.3	12.5	2.888
MAX6796TPLD2+	5.0	12.5	4.625
MAX6796TPSD2+	3.3	12.5	2.888

+Denotes lead-free package.

Selector Guide

PART	RESET OUTPUT	NUMBER OF OUTPUTS	WINDOWED WATCHDOG TIMEOUT	ENABLE INPUTS	WATCHDOG DISABLE INPUT
MAX6791TP_D_	Open drain	2	✓	Dual	✓
MAX6792TP_D_	Push-pull	2	✓	Dual	✓
MAX6793TP_D_	Open drain	2	—	Dual	✓
MAX6794TP_D_	Push-pull	2	—	Dual	✓
MAX6795TP_D_	Open drain	1	—	Single	✓
MAX6796TP_D_	Push-pull	1	—	Single	✓

Typical Application Circuit

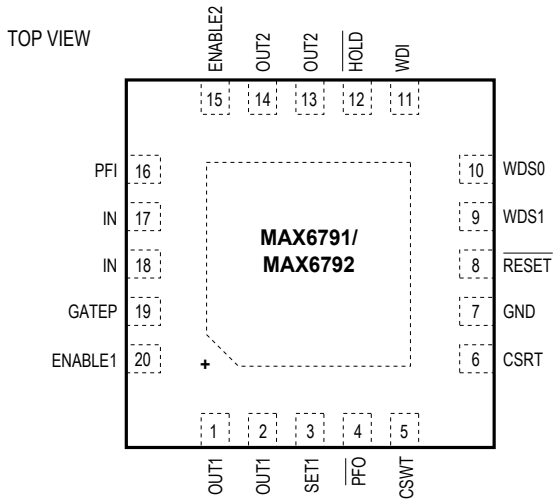


Package Information

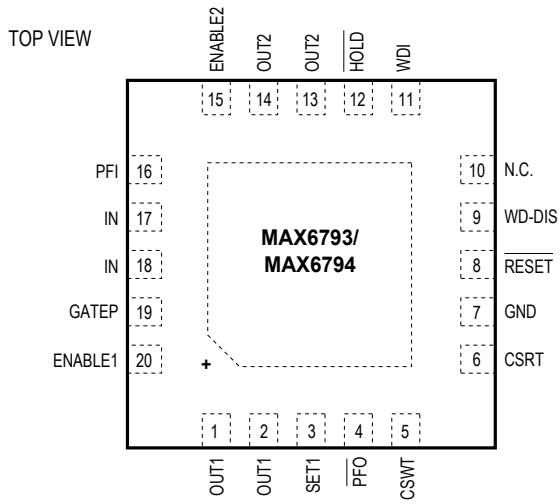
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+4	21-0140	90-0009

Pin Configurations



THIN QFN
5mm x 5mm



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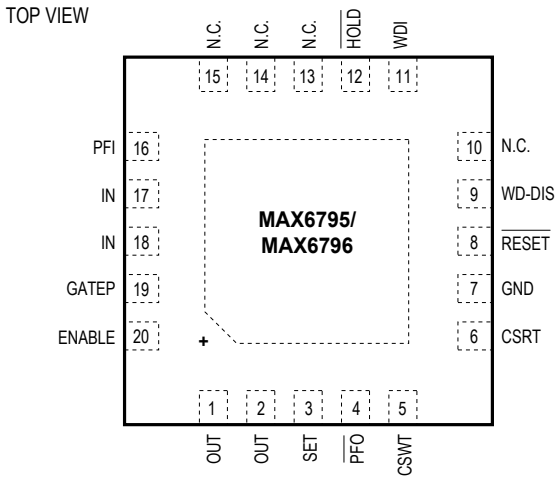

THIN QFN
5mm x 5mm