

Dual-Output (Positive and Negative), DC-DC Converter for CCD and LCD

General Description

The MAX685 DC-DC converter provides low-noise dual outputs for powering CCD imaging devices and LCDs. This device uses a single inductor to provide independently regulated positive and negative outputs. Integrated power switches are included in a small 24-Pin 4mm x 4mm Thin QFN package to save space and reduce cost. A 16-pin QSOP package is also available.

Each output delivers up to 10mA from a +2.7V to +5.5V input voltage range. Output voltages are set independently up to 24V and down to -9V. With a few additional low-cost components, the output voltages can be set at up to 45V and down to -16V. Output ripple magnitude is 30mVp-p. The MAX685 uses a fixed-frequency, pulse-width-modulated (PWM) control scheme at 220kHz or 400kHz to permit output noise filtering and to reduce the size of external components. The frequency can also be synchronized to an external clock signal between 200kHz and 480kHz.

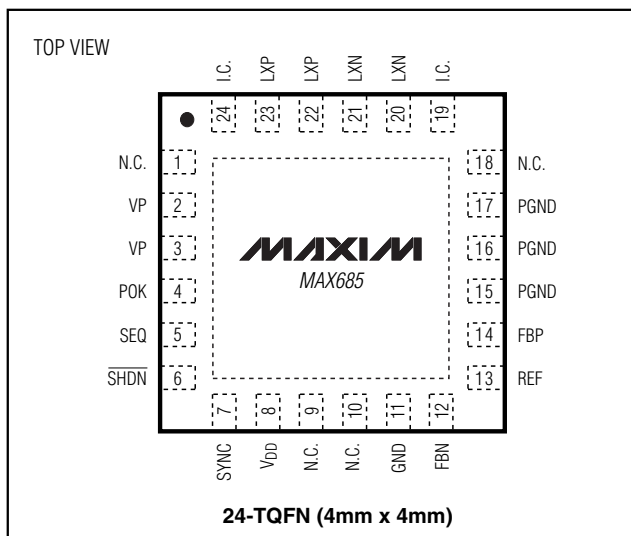
The MAX685 has a power-OK indicator output (POK) that signals when both outputs are within regulation. A logic-controlled shutdown completely turns off both outputs and reduces supply current to 0.1 μ A. The user can also set which output turns on first.

The preassembled MAX685 evaluation kit is available to reduce design time.

Applications

Camcorders LCDs
Digital Cameras CCD Imaging Devices
Notebooks

Pin Configuration



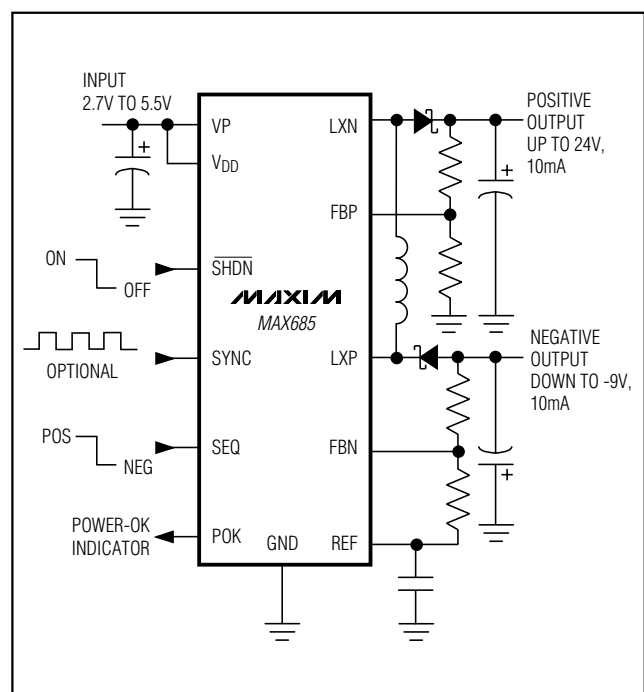
Features

- ◆ Dual Output Using a Single Inductor
- ◆ Low-Noise Output, 30mVp-p Ripple
- ◆ Output Voltages up to 24V and down to -9V (up to 45V and down to -16V with added components)
- ◆ Internal Switches in a Small 24-Pin 4mm x 4mm Thin QFN Package
- ◆ 220kHz/400kHz Fixed-Frequency PWM Operation
- ◆ Frequency Can Be Synchronized to External Clock
- ◆ Power-OK Indicator
- ◆ Selectable Power-On Sequencing
- ◆ 0.1 μ A Logic-Controlled Shutdown

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|-------------|
| MAX685EEE | -40°C to +85°C | 16 QSOP |
| MAX685ETG | -40°C to +85°C | 24 TQFN |

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

| | | | |
|----------------------------------|-----------------------------------|---|-----------------|
| V _{DD} , VP to GND..... | -0.3V to +6V | Continuous Power Dissipation (T _A = +70°C) | |
| PGND to GND | -0.3V to +0.3V | 16-Pin QSOP (derate 8.3mW/°C above +70°C)..... | 667mW |
| V _{DD} to VP..... | -0.3V to +0.3V | 24-Pin TQFN (derate 20.8mW/°C above +70°C) | 1667mW |
| LXN, POK to GND | -0.3V to +30V | Operating Temperature Range | -40°C to +85°C |
| LXP to V _{DD} | -15V to +0.3V | Junction Temperature | +150°C |
| REF, SEQ, SHDN to GND | -0.3V to (V _{DD} + 0.3V) | Storage Temperature Range | -65°C to +165°C |
| FBP, FBN, SYNC to GND | -0.3V to +6V | Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = VP = 5V, T_A = 0°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|-----------------------|-----------------------|-------|-------|
| Input Voltage Range | V _{DD} = VP | 2.7 | | 5.5 | V |
| Positive Output Voltage Range | | VP | | 24 | V |
| Negative Output Voltage Range | V _{DD} = 5.5V (Note 1) | -9 | | -1.27 | V |
| Output Current | V _{DD} = 4.5V, V _{OUT+} ≥ 14.25V, V _{OUT-} ≤ -7.125V, Figure 3 | 10 | | | mA |
| LX Current Limit | T _A = +25°C | | 440 | | mA |
| LXP, LXN On-Resistance | V _{DD} = 4.5V | | 0.6 | 2 | Ω |
| Quiescent Current | SYNC = V _{DD} | | 0.8 | | mA |
| Idle Quiescent Current | V _{FBP} = 1.35V, V _{FBN} = -0.1V | | 300 | 500 | μA |
| Line Regulation | V _{DD} = 4.5V to 5.5V | | 0.2 | | %/V |
| Load Regulation | I _{OUT} = 0 to 10mA, C1 = 10μF | | 0.13 | | %/mA |
| Output Voltage Ripple | C3 = C4 = 10μF, I _{LOAD} = 5mA | | 30 | | mVp-p |
| SHUTDOWN ($\overline{\text{SHDN}}$) | | | | | |
| Shutdown Supply Current | SYNC = SEQ = $\overline{\text{SHDN}}$ = GND | | 0.1 | 10 | μA |
| UNDERVOLTAGE LOCKOUT | | | | | |
| UVLO Threshold | V _{DD} = rising | 2.35 | 2.5 | 2.65 | V |
| UVLO Hysteresis | | | 50 | | mV |
| REFERENCE VOLTAGE | | | | | |
| V _{REF} Output Voltage | No load | 1.23 | 1.250 | 1.27 | V |
| V _{REF} Load Regulation | 0 < I _{REF} < 50μA | | -2 | | mV |
| FB INPUTS | | | | | |
| FBP Threshold Voltage | No load | 1.21 | 1.24 | 1.27 | V |
| FBN Threshold Voltage | No load | -16 | 10 | 36 | mV |
| FBP, FBN Input Leakage Current | | | ±0.01 | ±0.1 | μA |
| LOGIC INPUTS (SEQ, $\overline{\text{SHDN}}$, SYNC) | | | | | |
| Logic-Low Input | 2.7V < V _{DD} < 5.5V | | 0.3 x V _{DD} | | V |
| Logic-High Input | 2.7V < V _{DD} < 5.5V | 0.7 x V _{DD} | | | V |
| Input Bias Current | | | 0.1 | 1 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = V_P = 5V$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|------------------------|-------|-------|-------|---------------|
| SYNC INPUT | | | | | |
| Sync Frequency Range (external) | | 200 | | 480 | kHz |
| Oscillator Frequency (internal) | SYNC = GND | 175 | 220 | 265 | kHz |
| | SYNC = V_{DD} | 320 | 400 | 480 | |
| POK COMPARATORS | | | | | |
| FBP POK Threshold | FBP rising | 1.090 | 1.122 | 1.150 | V |
| FBN POK Threshold | FBN falling | 54 | 79 | 108 | mV |
| POK Output Low Voltage | $I_{POK} = 2\text{mA}$ | | | 0.4 | V |
| POK Output Off Current | $V_{POK} = 10V$ | | | 1 | μA |

ELECTRICAL CHARACTERISTICS

($V_{DD}, V_P = 5V$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|--|--|---------------------|---------------------|---------------|
| Input Voltage Range | $V_{DD} = V_P$ | 2.7 | 5.5 | V |
| Positive Output Voltage Range | | V_P | 24 | V |
| Negative Output Voltage Range | $V_{DD} = 5.5V$ (Note 1) | -9 | -1.27 | V |
| Maximum Output Current | $V_{IN} = 4.5V$, $V_{OUT+} \geq 14.25V$, $V_{OUT-} \leq -7.125V$, Figure 3 | 10 | | mA |
| Idle Quiescent Current | SYNC = GND | | 500 | μA |
| SHUTDOWN | | | | |
| Shutdown Supply Current | SYNC = SEQ = $\overline{\text{SHDN}}$ = GND | | 10 | μA |
| UNDERVOLTAGE LOCKOUT | | | | |
| UVLO Threshold | $V_{DD} = \text{rising}$ | 2.35 | 2.65 | V |
| FB INPUTS AND REFERENCE VOLTAGE | | | | |
| FBP Threshold Voltage | No load | 1.205 | 1.275 | V |
| FBN Threshold Voltage | No load | -20 | 40 | mV |
| VREF Output Voltage | No load | 1.225 | 1.275 | V |
| LOGIC INPUTS (SEQ, $\overline{\text{SHDN}}$, SYNC) | | | | |
| Logic-Low Input | $2.7V < V_{DD} \leq 5.5V$ | | $0.3 \times V_{DD}$ | V |
| Logic-High Input | $2.7V < V_{DD} \leq 5.5V$ | $0.7 \times V_{DD}$ | | V |
| POK COMPARATORS | | | | |
| FBP POK Threshold | FBP rising | 1.090 | 1.150 | V |
| FBN POK Threshold | FBN falling | 54 | 108 | mV |

Note 1: Negative output voltage can be larger magnitude for lower values of V_{DD} . The voltage between V_{DD} and V_{OUT-} must not exceed 14.5V.

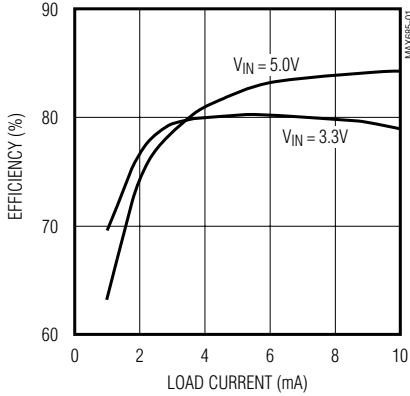
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

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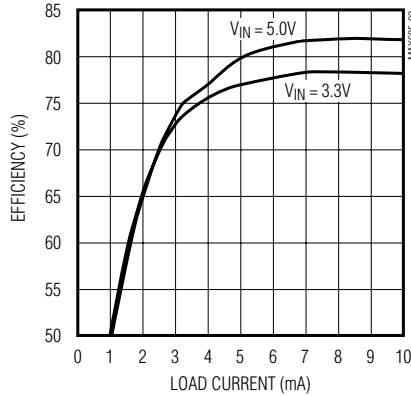
Typical Operating Characteristics

(Circuit of Figure 3, $V_{OUT+} = 15V$, $V_{OUT-} = -7.5V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

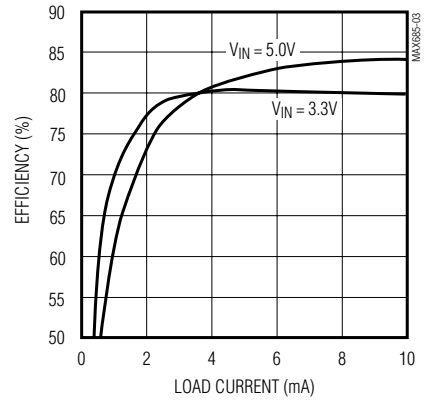
EFFICIENCY vs. LOAD CURRENT (POSITIVE OUTPUT LOADED)



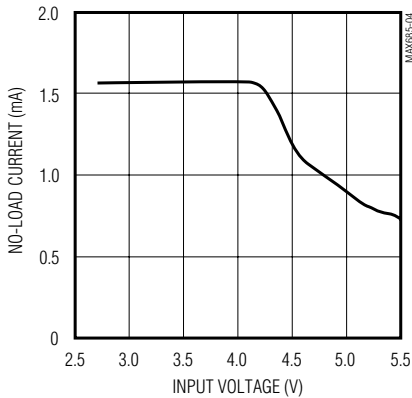
EFFICIENCY vs. LOAD CURRENT (NEGATIVE OUTPUT LOADED)



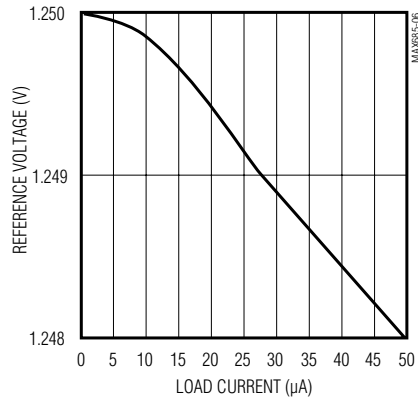
EFFICIENCY vs. LOAD CURRENT (BOTH OUTPUTS LOADED)



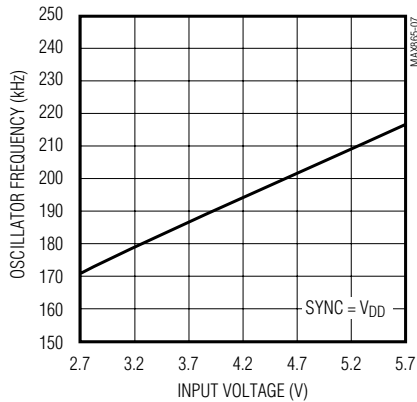
NO-LOAD CURRENT vs. INPUT VOLTAGE



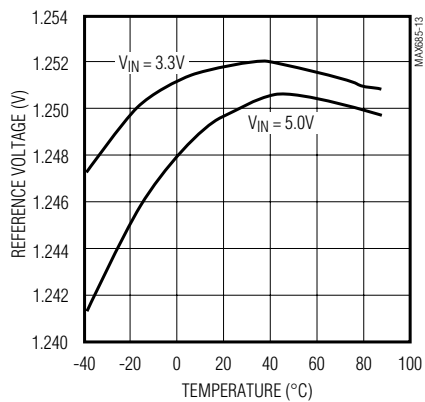
REFERENCE LOAD REGULATION



LX SWITCHING FREQUENCY vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. TEMPERATURE

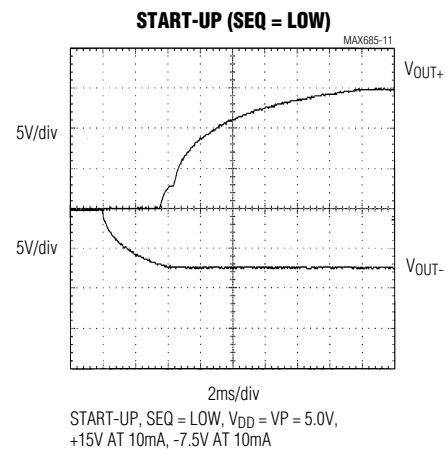
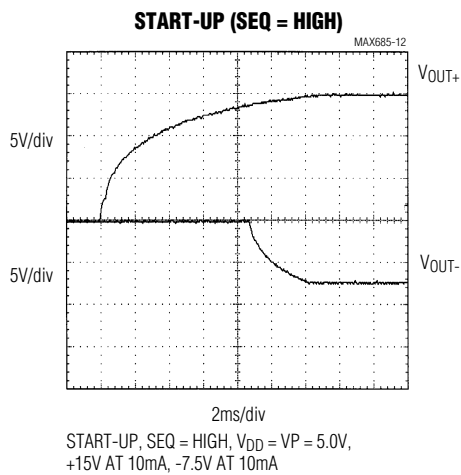
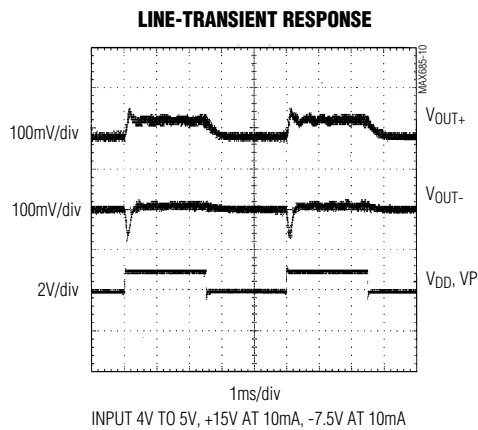
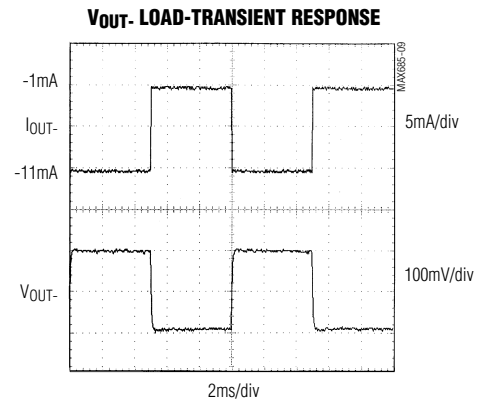
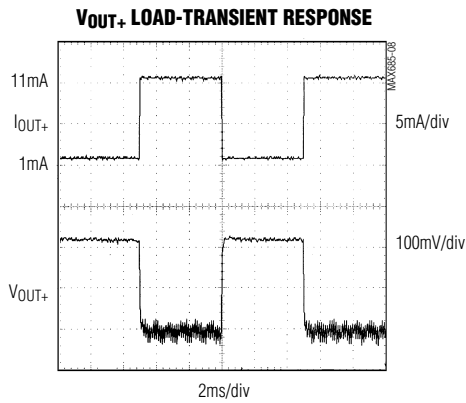


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Typical Operating Characteristics (continued)

(Circuit of Figure 3, $V_{OUT+} = 15V$, $V_{OUT-} = -7.5V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Dual-Output (Positive and Negative), DC-DC Converter for CCD and LCD

Pin Description

| PIN 16-QSOP | PIN 24-TQFN | NAME | FUNCTION |
|----------------|----------------|--------------------------|--|
| 1 | 22, 23 | LXP | P-Channel Switching Inductor Node. LXP turns off when the part enters shutdown. |
| 2, 15 | 19, 24 | I.C. | Internally Connected. Do not externally connect. |
| 3 | 2, 3 | VP | Power Input. Connect to V _{DD} . |
| 4 | 4 | POK | Open-Drain Power-OK Output. POK is high when both outputs are in regulation. Connect POK to V _{DD} with a 100k Ω pull-up resistor to V _{DD} . |
| 5 | 5 | SEQ | Power-Up Sequence Select Input. Connect SEQ to GND to power the negative output voltage first. Connect SEQ to V _{DD} to power the positive output first. |
| 6 | 6 | $\overline{\text{SHDN}}$ | Shutdown Input. Both outputs go to 0V in shutdown. Connect to V _{DD} for automatic startup. |
| 7 | 7 | SYNC | Sync Input. This pin synchronizes the oscillator to an external clock frequency between 200kHz and 480kHz. Connect SYNC to GND (220kHz) or V _{DD} (400kHz) for internal oscillator frequency. |
| 8 | 8 | V _{DD} | Supply Input. Bypass V _{DD} with a 1.0 μ F or greater ceramic capacitor to GND. |
| 9 | 11 | GND | Ground |
| 10 | 12 | FBN | Feedback Input for the Negative Output Voltage. Connect a resistor-divider between the negative output and REF with the center to FBN to set the negative output voltage. |
| 11 | 13 | REF | 1.25V Reference Voltage Output. Bypass with 0.22 μ F to GND. |
| 12 | 14 | FBP | Feedback for the Positive Output Voltage. Connect a resistor-divider between the positive output and GND with the center to FBP to set the positive output voltage. |
| 13, 14 | 15, 16, 17 | PGND | Power Ground. Connect PGND to GND. |
| 16 | 20, 21 | LXN | N-Channel Switching Inductor Node. LXN pulls to GND through the internal transistor when the part is shut down. |
| — | 1, 9, 10, 18 | N.C. | This pin is not internally connected. |

Detailed Description

The MAX685 DC-DC converter accepts an input voltage between +2.7V and +5.5V and generates both a positive and negative voltage, using a single inductor (Figure 1). It alternates between acting as a step-up converter and as an inverting converter on a cycle-by-cycle basis. Both output voltages are independently regulated.

Each output is separately controlled by a pulse-width-modulated (PWM) current mode regulator. This allows the part to operate at a fixed frequency for use in noise-sensitive applications. An internal oscillator runs at 220kHz or 400kHz, or can be synchronized to an external signal. Since switching alternates between the two regulators, each operates at half the oscillator frequency (110kHz, 200kHz, or half the sync frequency). The oscillator can be synchronized to a 200kHz to 480kHz clock.

On the first cycle of operation, the part operates as a step-up converter. LXP connects to V_{DD}, LXN pulls to ground, and the inductor current rises. Once the inductor current rises to a level set by the positive-side error amplifier, LXN releases and the inductor current flows through D2 to the positive output. When the inductor current drops to zero (which happens each cycle under normal, discontinuous operation), LXN returns to the input voltage.

On the second cycle, LXN is held at ground. LXP is pulled up to the input voltage until the current reaches the limit set by the negative error amplifier. Then LXP is released and the inductor current flows through D1 to the negative output. Once the inductor current reaches zero, the voltage at LXP returns to ground. The waveforms at LXN and LXP are shown in Figure 2 for a typical pair of cycles.

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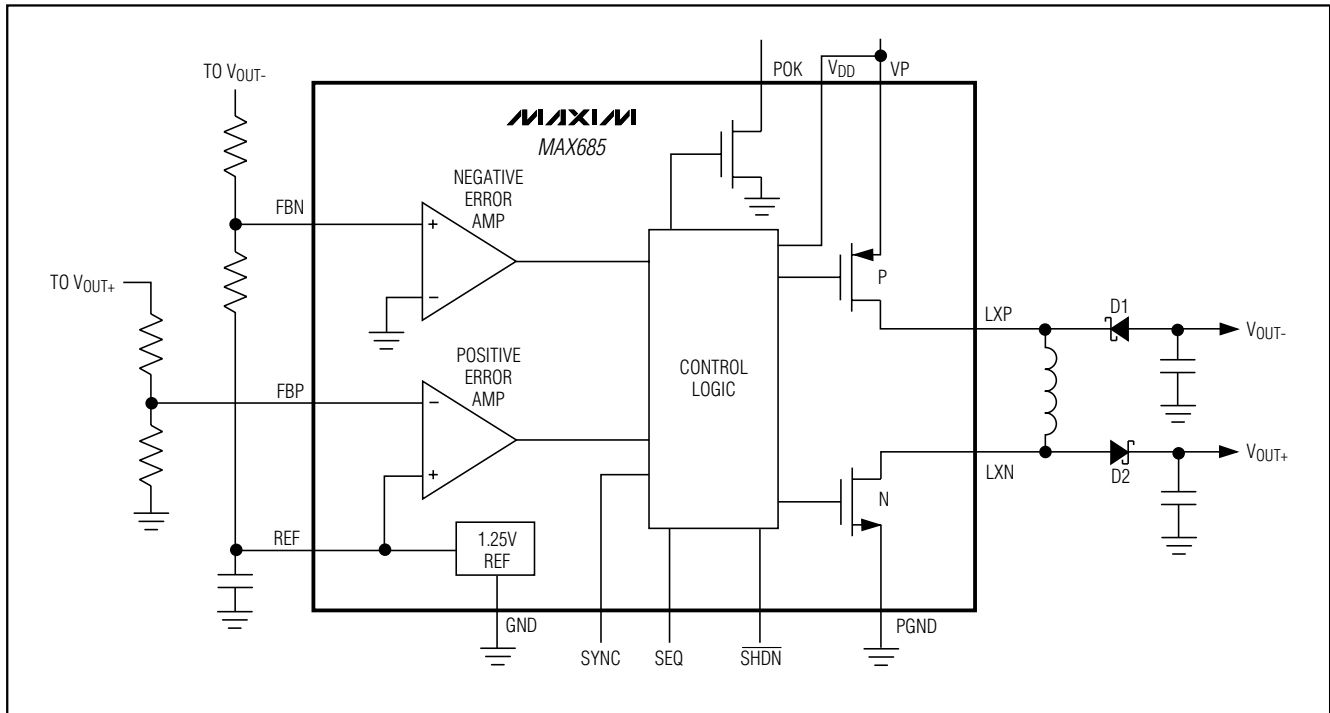


Figure 1. Functional Diagram

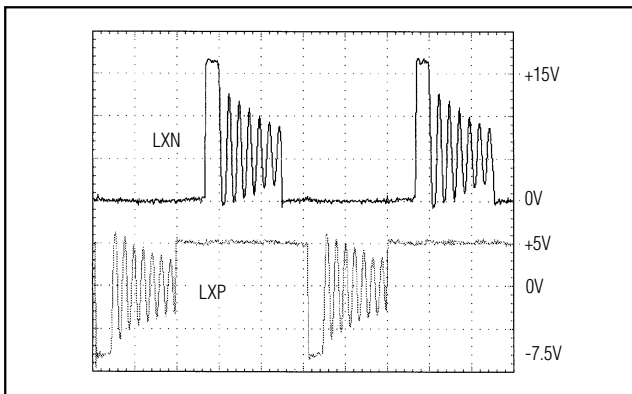


Figure 2. LXN and LXP Waveforms (see also Figure 5)

The current into the LXN pin is sensed to measure the inductor current. The MAX685 controls the inductor current to regulate both the positive and negative output voltages.

SEQ and Power OK (POK)

The SEQ pin controls the power-up sequence. If SEQ is low, the positive output is disabled until the negative output is within 90% of its regulation point. If SEQ is high, the negative output is disabled until the positive

output is within 90% of its regulation point. The power-OK output (POK) indicates that both output voltages are in regulation. When both outputs are within 90% of their regulation points, POK becomes high impedance. Should one or both of the output voltages fall below 90% of their regulation points, POK pulls to ground. POK can sink up to 2mA. To reduce current consumption, POK is high impedance while the part is in shutdown. When coming out of shutdown, POK remains high impedance for 50ns (typ) before going low. Connect POK to V_{DD} through a 100kΩ resistor.

Synchronization/Internal Frequency Selection

The MAX685 operates at a fixed switching frequency. Set the operating frequency using the SYNC pin. If SYNC is grounded, the part operates at the internally set 220kHz frequency. When SYNC is connected to V_{DD}, the part operates at 400kHz. The MAX685 can also be synchronized to signals between 200kHz and 480kHz. Note that each output switches at half the oscillator or synchronized frequency. Since the actual switching frequency is one-half the applied clock signal, drive SYNC at twice the desired switching frequency.

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Applications Information

Figure 3 shows the standard application circuit for the MAX685. The values shown in Table 1 will work well for output currents up to 10mA. However, this circuit can be optimized to a particular application by using different capacitors and a different inductor.

Higher Output Voltages

If the application requires output voltages greater than -7.5V or +24V, use the circuit of Figure 4. This circuit uses a charge pump to increase the output voltage without increasing the voltage stress on the LX_ pin. The maximum output voltages of the circuit in Figure 4 are -15V and +48V.

The voltage rating on D2, D5, and D6 must be 30V or greater. For a larger negative output voltage without a larger positive output (or vice versa), use one-half of the Figure 4 circuit with one-half of the Figure 3 circuit.

Inductor Selection

A 22 μ H inductor is suitable for most applications. Larger inductances will reduce inductor ripple current and output voltage ripple, but they also typically require larger physical size if increased resistance and losses are not also allowed.

Small inductors are typically preferred because of compact design and low cost. Murata LHQ and TDK NLC types are examples of small surface-mount inductors that work for most applications. Because these small-size inductors use thinner wire, they exhibit higher resistance and have greater losses than larger ones. If the application demands higher efficiency, use larger, lower resistance coils such as the Sumida CD43 or CD54, Coilcraft DT1608 or DO1608, or Coiltronics UP1V series.

Filter Capacitor Selection

The output ripple voltage is a function of the peak inductor current, frequency, and type and value of the output capacitors. Capacitors with low equivalent-series resistance (ESR) and large capacitance reduce output ripple. Typically, tantalum or ceramic capacitors are optimal. Tantalum capacitors have higher ESR and higher capacitance than ceramic capacitors. Therefore the ESR of tantalum capacitors determines the output ripple, because at the frequencies used the ESR dominates the impedance of the capacitor. If ceramic capacitors are used, the capacitance determines the output ripple.

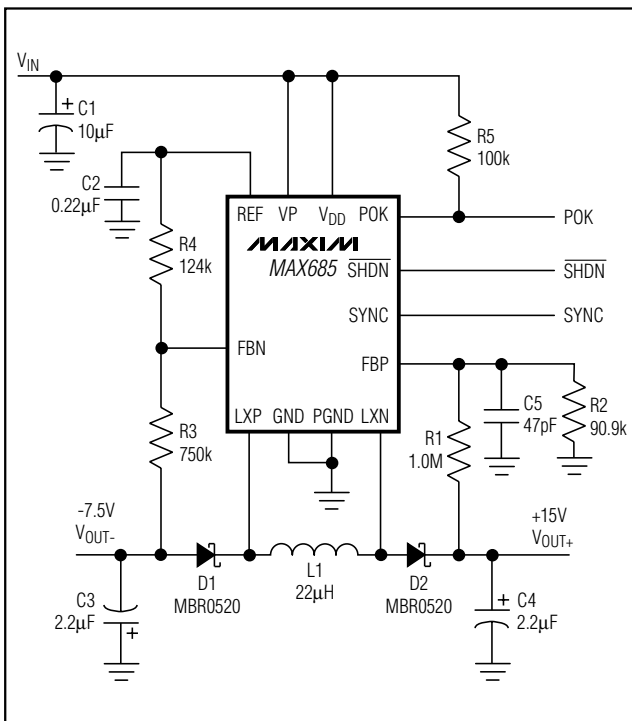


Figure 3. Standard Application Circuit

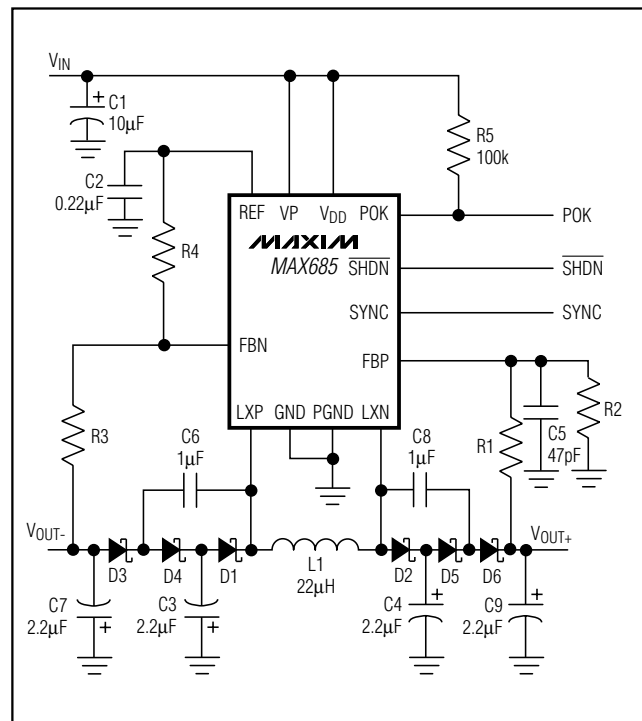


Figure 4. Circuit for Output Voltages <-9V and > +24V

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Table 1. Component Values for the Typical Operating Circuit

| REF | DESCRIPTION | MANUFACTURER PART NUMBER |
|--------|------------------------------|---|
| C1 | 10μF, 10V tantalum cap | Sprague 595D106X0010A2T or AVX TAJA106K010R |
| C2 | 0.22μF ceramic capacitor | Any manufacturer |
| C3, C4 | 2.2μF ceramic capacitor | Any manufacturer |
| C5 | 47pF ceramic cap | Any manufacturer |
| D1, D2 | 0.1A, 20V Schottky rectifier | Motorola MBR0520LT1 (0.5A) or Central Semiconductor CMPSH-3 |
| L1 | 22μH, 0.4A inductor | Murata LHQ4N220J04 or TDK NLC32522T-220K |

Setting the Output Voltage

The resistor-divider formed by R4 and R3 sets the negative output voltage; the resistor-divider formed by R1 and R2 sets the positive output voltage. Let R4 be a value near 100kΩ to set a resistor-divider current of approximately 10μA. Determine the value of R3 by the following:

$$R3 = R4 \frac{|V_{OUT-}|}{1.24V}$$

Let R2 be a value near 100kΩ to set a resistor-divider current of approximately 10μA. Determine the value of R1 with the following formula:

$$R1 = R2 \times (V_{OUT+} - 1.24V) / 1.24$$

Damping LX

LXN and LXP may ring at the conclusion of each switching cycle when the inductor current falls to zero. Typically the ringing waveform appears only on LX_ and has no effect on output ripple and noise. If LX_ ringing is still objectionable, it may be damped by connecting a series RC in parallel with L1. Typically 1kΩ in series with 100pF provides good damping with only 3% efficiency degradation. See Figure 5.

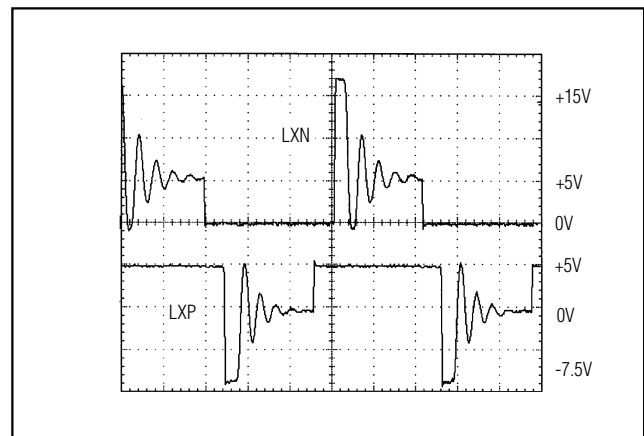


Figure 5. LXN and LXP Waveforms with a Series-Connected 1kΩ Resistor and 100pF Capacitor Connected in Parallel with L1 to Damp Ringing

Chip Information

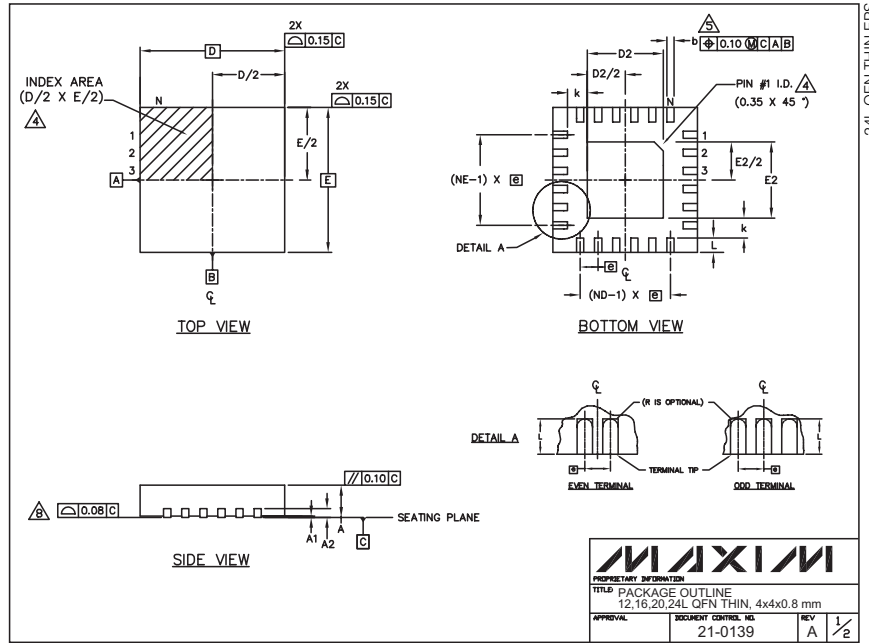
TRANSISTOR COUNT: 902

SUBSTRATE CONNECTED TO GND

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.



| COMMON DIMENSIONS | | | | | | | | | | | | |
|------------------------|------------------|------|------|------------------|------|------|--------------------|------|------|--------------------|------|------|
| PKG REF. | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | |
| | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | |
| V _{gdec} Var. | V _{GGB} | | | V _{GGC} | | | V _{GGD-1} | | | V _{GGD-2} | | |

| EXPOSED PAD VARIATIONS | | | | | | | | | | | | |
|------------------------|------|------|------|------|------|------|------|------|------|------|------|------|
| PKG CODES | D2 | | | E2 | | | | | | | | |
| | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. |
| T1244-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | | | | | | |
| T1644-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | | | | | | |
| T2044-1 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | | | | | | |
| T2444-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | | | | | | |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220.

MAXIM
 PROPRIETARY INFORMATION
 TITLE: PACKAGE OUTLINE
 12,16,20,24L QFN THIN, 4x4x0.8 mm
 APPROVAL: _____ DOCUMENT CONTROL NO: 21-0139 REV: A 2/2