



5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

MAX7426/MAX7427

General Description

The MAX7426/MAX7427 5th-order, lowpass, elliptic, switched-capacitor filters (SCFs) operate from a single +5V (MAX7426) or +3V (MAX7427) supply. The devices draw only 0.8mA of supply current and allow corner frequencies from 1Hz to 12kHz, making them ideal for low-power post-DAC filtering and anti-aliasing applications. They can be put into a low-power mode, reducing supply current to 0.2µA.

Two clocking options are available: self-clocking (through the use of an external capacitor) or external clocking for tighter cutoff-frequency control. An offset-adjust pin allows for adjustment of the DC output level.

The MAX7426/MAX7427 deliver 37dB of stopband rejection and a sharp rolloff with a transition ratio of 1.25. Their fixed response limits the design task to selecting a clock frequency.

Applications

ADC Anti-Aliasing CT2 Base Stations
 Post-DAC Filtering Speech Processing

Selector Guide

| PART | TRANSITION RATIO | OPERATING VOLTAGE (V) |
|---------|------------------|-----------------------|
| MAX7426 | r = 1.25 | +5 |
| MAX7427 | r = 1.25 | +3 |

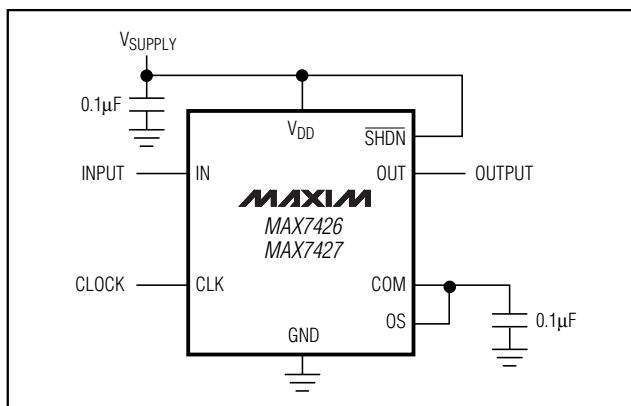
Features

- ◆ 5th-Order, Elliptic Lowpass Filters
- ◆ Low Noise and Distortion: -80dB THD + Noise
- ◆ Clock-Tunable Corner Frequency (1Hz to 12kHz)
- ◆ Single-Supply Operation
 - +5V (MAX7426)
 - +3V (MAX7427)
- ◆ Low Power
 - 0.8mA (Operating Mode)
 - 0.2µA (Shutdown Mode)
- ◆ Available in 8-Pin µMAX/PDIP Packages
- ◆ Low Output Offset: ±4mV

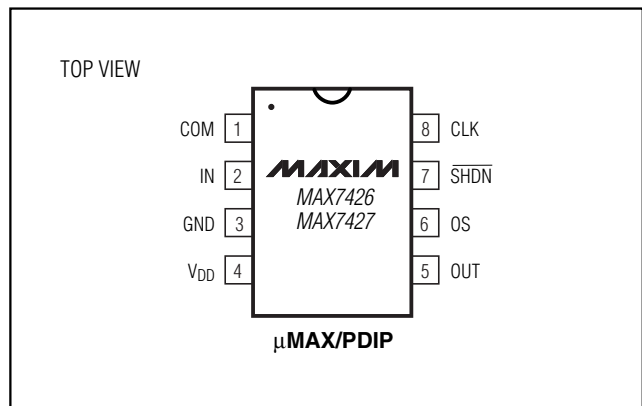
Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|----------------|---------------|
| MAX7426CUA | 0°C to +70°C | 8 µMAX |
| MAX7426CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX7426EUA | -40°C to +85°C | 8 µMAX |
| MAX7426EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX7427CUA | 0°C to +70°C | 8 µMAX |
| MAX7427CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX7427EUA | -40°C to +85°C | 8 µMAX |
| MAX7427EPA | -40°C to +85°C | 8 Plastic DIP |

Typical Operating Circuit



Pin Configuration



5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{DD} to GND | -0.3V to +6V |
| IN, OUT, COM, OS, CLK, $\overline{\text{SHDN}}$ | -0.3V to (V _{DD} + 0.3V) |
| OUT Short-Circuit Duration | 1s |
| Continuous Power Dissipation (T _A = +70°C) | |
| 8-Pin μ MAX (derate 4.1mW/°C above +70°C) | 330mW |
| 8-Pin PDIP (derate 6.90mW/°C above +70°C) | 552mW |

| | |
|-----------------------------------|-----------------|
| Operating Temperature Ranges | |
| MAX742 _C_A | 0°C to +70°C |
| MAX742 _E_A | -40°C to +85°C |
| Storage Temperature Range | -65°C to +160°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7426

(V_{DD} = +5V, filter output measured at OUT, 10k Ω || 50pF load to GND at OUT, $\overline{\text{SHDN}}$ = V_{DD}, OS = COM, 0.1 μ F from COM to GND, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------------------|---|--------------------------|--------------------|--------------------------|------------|
| FILTER | | | | | | |
| Corner-Frequency Range | f _C | (Note 1) | | 0.001 to 9 | | kHz |
| Clock-to-Corner Ratio | f _{CLK} /f _C | | | 100:1 | | |
| Clock-to-Corner Tempco | | | | 10 | | ppm/°C |
| Output Voltage Range | | | 0.25 | | V _{DD} - 0.25 | V |
| Output Offset Voltage | V _{OFFSET} | V _{IN} = V _{COM} = V _{DD} / 2 | | ±4 | ±25 | mV |
| DC Insertion Gain with Output Offset Removed | | V _{COM} = V _{DD} / 2 (Note 2) | 0 | 0.2 | 0.4 | dB |
| Total Harmonic Distortion plus Noise | THD+N | f _{IN} = 200Hz, V _{IN} = 4Vp-p, measurement bandwidth = 22kHz | | -81 | | dB |
| Offset Voltage Gain | A _{OS} | OS to OUT | | +1 | | V/V |
| COM Voltage Range | V _{COM} | Input, COM externally driven | $\frac{V_{DD}}{2} - 0.5$ | $\frac{V_{DD}}{2}$ | $\frac{V_{DD}}{2} + 0.5$ | V |
| | | Output, COM internally driven | $\frac{V_{DD}}{2} - 0.2$ | $\frac{V_{DD}}{2}$ | $\frac{V_{DD}}{2} + 0.2$ | |
| Input Voltage Range at OS | V _{OS} | Measured with respect to COM | | ±0.1 | | V |
| Input Resistance at COM | R _{COM} | | 90 | 130 | | k Ω |
| Clock Feedthrough | | T _A = +25°C | | 5 | | mVp-p |
| Resistive Output Load Drive | R _L | | 10 | 1 | | k Ω |
| Maximum Capacitive Load at OUT | C _L | | 50 | 500 | | pF |
| Input Leakage Current at COM | | $\overline{\text{SHDN}}$ = GND, V _{COM} = 0 to V _{DD} | | ±0.2 | ±10 | μ A |
| Input Leakage Current at OS | | V _{OS} = 0 to V _{DD} | | ±0.2 | ±10 | μ A |
| CLOCK | | | | | | |
| Internal Oscillator Frequency | f _{OSC} | C _{OSC} = 1000pF (Note 3) | 13.5 | 17.5 | 21.5 | kHz |
| Clock Output Current (internal oscillator mode) | I _{CLK} | | | ±8 | ±12.5 | μ A |
| Clock Input High | V _{IH} | | 4.5 | | | V |
| Clock Input Low | V _{IL} | | | | 0.5 | V |

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

MAX7426/MAX7427

ELECTRICAL CHARACTERISTICS—MAX7426 (continued)

($V_{DD} = +5V$, filter output measured at OUT, $10k\Omega \parallel 50pF$ load to GND at OUT, $\overline{SHDN} = V_{DD}$, OS = COM, $0.1\mu F$ from COM to GND, $f_{CLK} = 100kHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------|---------------------------------------|-----|-----------|----------|---------|
| POWER REQUIREMENTS | | | | | | |
| Supply Voltage | V_{DD} | | 4.5 | | 5.5 | V |
| Supply Current | I_{DD} | Operating mode, no load | | 0.8 | 1.0 | mA |
| Shutdown Current | $I_{\overline{SHDN}}$ | $\overline{SHDN} = GND$ | | 0.2 | 1 | μA |
| Power-Supply Rejection Ratio | PSRR | Measured at DC | | 70 | | dB |
| SHUTDOWN | | | | | | |
| \overline{SHDN} Input High | V_{SDH} | | 4.5 | | | V |
| \overline{SHDN} Input Low | V_{SDL} | | | | 0.5 | V |
| \overline{SHDN} Input Leakage Current | | $V_{\overline{SHDN}} = 0$ to V_{DD} | | ± 0.2 | ± 10 | μA |

ELECTRICAL CHARACTERISTICS—MAX7427

($V_{DD} = +3V$, filter output measured at OUT pin, $10k\Omega \parallel 50pF$ load to GND at OUT, $\overline{SHDN} = V_{DD}$, OS = COM, $0.1\mu F$ from COM to GND, $f_{CLK} = 100kHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|---|--------------------------|--------------------|--------------------------|-----------------|
| FILTER CHARACTERISTICS | | | | | | |
| Corner-Frequency Range | f_c | (Note 1) | | 0.001 to 12 | | kHz |
| Clock-to-Corner Ratio | f_{CLK}/f_c | | | 100:1 | | |
| Clock-to-Corner Tempco | | | | 10 | | ppm/ $^\circ C$ |
| Output Voltage Range | | | 0.25 | | $V_{DD} - 0.25$ | V |
| Output Offset Voltage | V_{OFFSET} | $V_{IN} = V_{COM} = V_{DD} / 2$ | | ± 4 | ± 25 | mV |
| DC Insertion Gain with Output Offset Removed | | $V_{COM} = V_{DD} / 2$ (Note 2) | 0 | 0.2 | 0.4 | dB |
| Total Harmonic Distortion plus Noise | THD+N | $f_{IN} = 200Hz$, $V_{IN} = 2.5Vp-p$, measurement bandwidth = 22kHz | | -79 | | dB |
| Offset Voltage Gain | AOS | OS to OUT | | +1 | | V/V |
| COM Voltage Range | V_{COM} | | $\frac{V_{DD}}{2} - 0.1$ | $\frac{V_{DD}}{2}$ | $\frac{V_{DD}}{2} + 0.1$ | V |
| Input Voltage Range at OS | V_{OS} | Measured with respect to COM | | ± 0.1 | | V |
| Input Resistance at COM | R_{COM} | | 90 | 130 | | $k\Omega$ |
| Clock Feedthrough | | $T_A = +25^\circ C$ | | 3 | | mVp-p |
| Resistance Output Load Drive | R_L | | 10 | 1 | | $k\Omega$ |
| Maximum Capacitive Load at OUT | C_L | | 50 | 500 | | pF |
| Input Leakage Current at COM | | $\overline{SHDN} = GND$, $V_{COM} = 0$ to V_{DD} | | ± 0.2 | ± 10 | μA |
| Input Leakage Current at OS | | $V_{OS} = 0$ to V_{DD} | | ± 0.2 | ± 10 | μA |

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ELECTRICAL CHARACTERISTICS—MAX7427 (continued)

($V_{DD} = +3V$, filter output measured at OUT pin, $10k\Omega$ || $50pF$ load to GND at OUT, $\overline{SHDN} = V_{DD}$, OS = COM, $0.1\mu F$ from COM to GND, $f_{CLK} = 100kHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------|---------------------------------------|------|-----------|------------|---------|
| CLOCK | | | | | | |
| Internal Oscillator Frequency | f_{OSC} | $C_{OSC} = 1000pF$ (Note 3) | 13.5 | 17.5 | 21.5 | kHz |
| Clock Output Current (internal oscillator mode) | I_{CLK} | $V_{CLK} = 0$ or $3V$ | | ± 7.5 | ± 12.5 | μA |
| Clock Input High | V_{IH} | | 2.5 | | | V |
| Clock Input Low | V_{IL} | | | | 0.5 | V |
| POWER REQUIREMENTS | | | | | | |
| Supply Voltage | V_{DD} | | 2.7 | | 3.6 | V |
| Supply Current | I_{DD} | Operating mode, no load | | 0.75 | 1.0 | mA |
| Shutdown Current | $I_{\overline{SHDN}}$ | $\overline{SHDN} = GND$ | | 0.2 | 1 | μA |
| Power-Supply Rejection Ratio | PSRR | Measured at DC | | 70 | | dB |
| SHUTDOWN | | | | | | |
| \overline{SHDN} Input High | V_{SDH} | | 2.5 | | | V |
| \overline{SHDN} Input Low | V_{SDL} | | | | 0.5 | V |
| \overline{SHDN} Input Leakage Current | | $V_{\overline{SHDN}} = 0$ to V_{DD} | | ± 0.2 | ± 10 | μA |

ELLIPTIC FILTER CHARACTERISTICS ($r = 1.25$)

($V_{DD} = +5V$ for MAX7426, $V_{DD} = +3V$ for MAX7427, filter output measured at OUT, $10k\Omega$ || $50pF$ load to GND at OUT, $\overline{SHDN} = V_{DD}$, $V_{COM} = V_{OS} = V_{DD} / 2$, $f_{CLK} = 100kHz$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 3)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------------|------|-------|-----|-------|
| Insertion Gain with DC Gain Error Removed (Note 4) | $f_{IN} = 0.38f_C$ | -0.4 | -0.2 | 0.4 | dB |
| | $f_{IN} = 0.68f_C$ | -0.4 | 0.2 | 0.4 | |
| | $f_{IN} = 0.87f_C$ | -0.4 | -0.2 | 0.4 | |
| | $f_{IN} = 0.97f_C$ | -0.4 | 0.2 | 0.4 | |
| | $f_{IN} = f_C$ | -0.7 | -0.2 | 0.2 | |
| | $f_{IN} = 1.25f_C$ | | -38.5 | -34 | |
| | $f_{IN} = 1.43f_C$ | | -37.2 | -35 | |
| | $f_{IN} = 3.25f_C$ | | -37.2 | -35 | |

Note 1: The maximum f_C is defined as the clock frequency $f_{CLK} = 100 \times f_C$ at which the peak SINAD drops to 68dB with a sinusoidal input at $0.2f_C$.

Note 2: DC insertion gain is defined as $\Delta V_{OUT} / \Delta V_{IN}$.

Note 3: f_{OSC} (kHz) $\approx 17.5 \times 10^3 / C_{OSC}$ (C_{OSC} in pF).

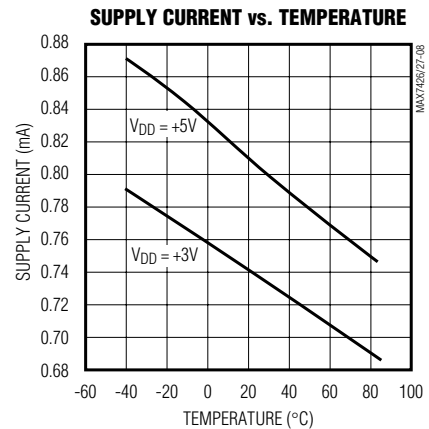
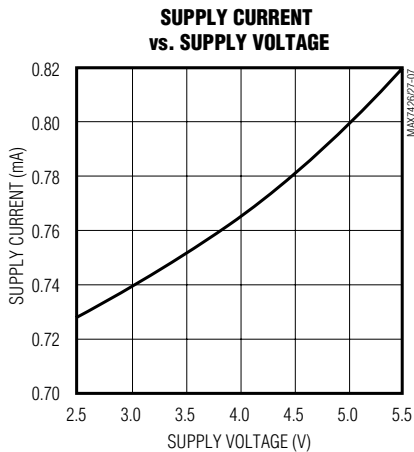
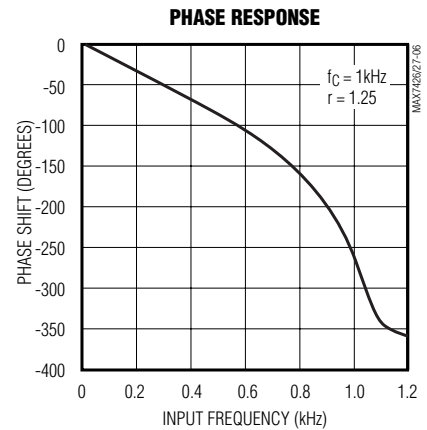
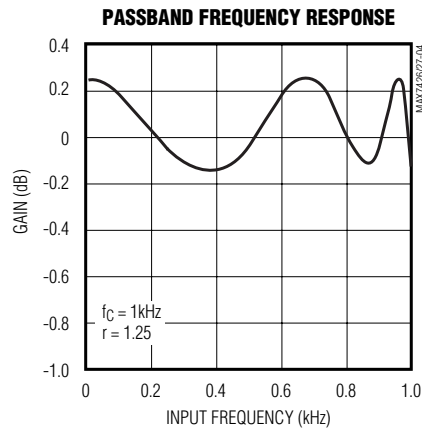
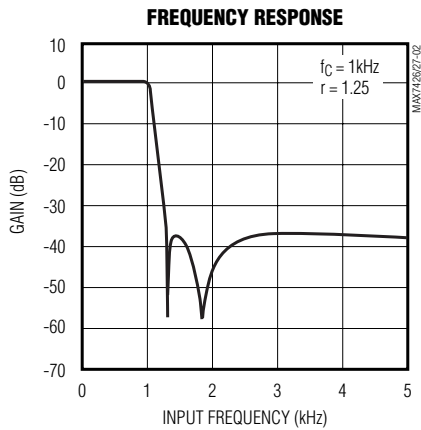
Note 4: The input frequencies, f_{IN} , are selected at the peaks and troughs of the ideal elliptic frequency responses.

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Typical Operating Characteristics

($V_{DD} = +5V$ for MAX7426, $V_{DD} = +3V$ for MAX7427, $f_{CLK} = 100kHz$, $\overline{SHDN} = V_{DD}$, $V_{COM} = V_{OS} = V_{DD} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX7426/MAX7427



5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Typical Operating Characteristics (continued)

($V_{DD} = +5V$ for MAX7426, $V_{DD} = +3V$ for MAX7427, $f_{CLK} = 100kHz$, $\overline{SHDN} = V_{DD}$, $V_{COM} = V_{OS} = V_{DD} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)

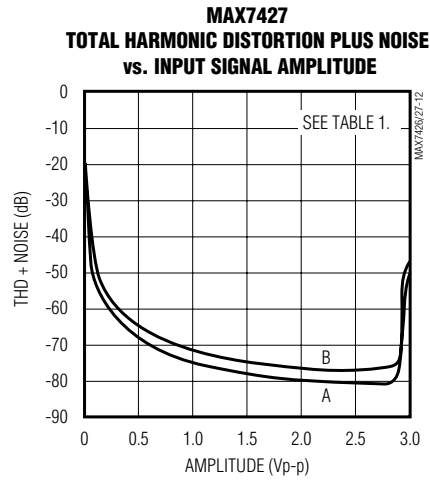
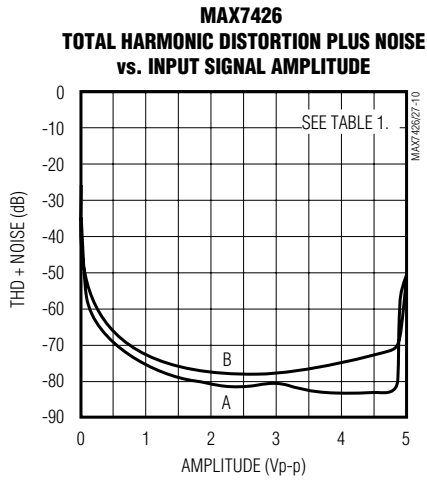


Table 1. THD + Noise Test Conditions

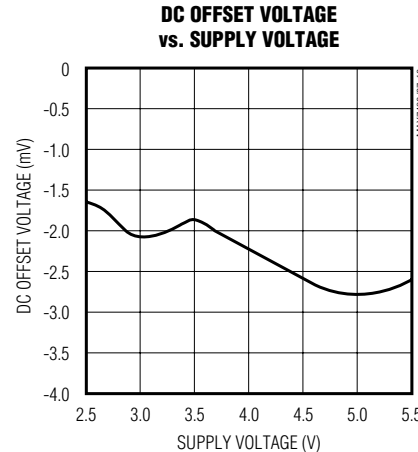
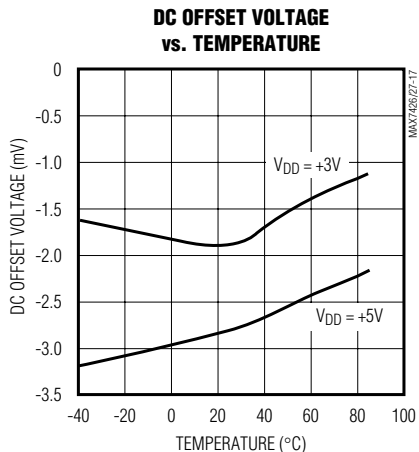
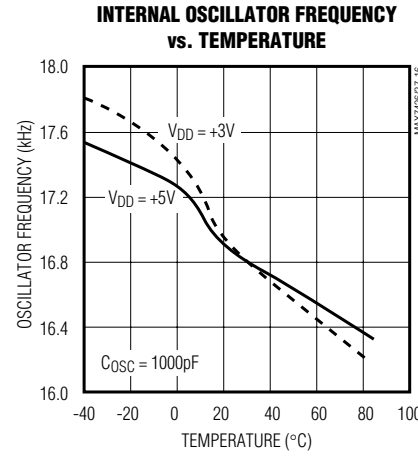
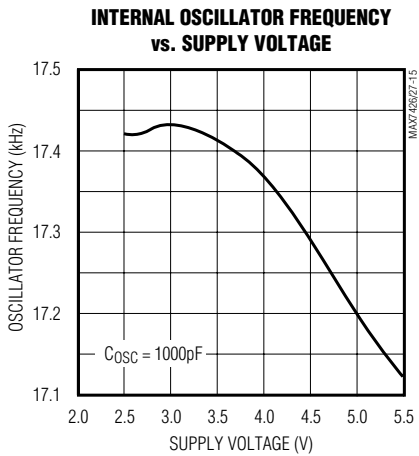
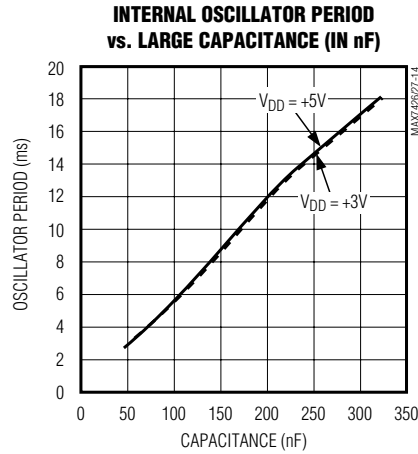
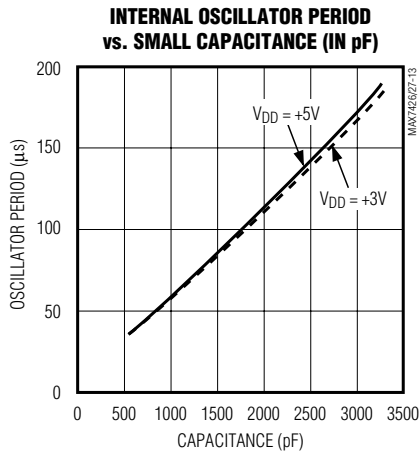
| LABEL | f_{IN} (Hz) | f_c (kHz) | f_{CLK} (kHz) | MEASUREMENT BANDWIDTH (kHz) |
|-------|------------------|----------------|--------------------|--------------------------------|
| A | 200 | 1 | 100 | 22 |
| B | 1k | 5 | 500 | 80 |

5th-Order, Lowpass, Elliptic, Switched-Capacitor

MAX7426/MAX7427

Typical Operating Characteristics (continued)

($V_{DD} = +5V$ for MAX7426, $V_{DD} = +3V$ for MAX7427, $f_{CLK} = 100kHz$, $\overline{SHDN} = V_{DD}$, $V_{COM} = V_{OS} = V_{DD} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)



5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Pin Description

| PIN | NAME | FUNCTION |
|-----|--------------------------|---|
| 1 | COM | Common Input Pin. Biased internally at midsupply. Bypass externally to GND with a 0.1 μ F capacitor. To override internal biasing, drive with an external supply. |
| 2 | IN | Filter Input |
| 3 | GND | Ground |
| 4 | V _{DD} | Positive Supply Input, +5V for MAX7426 or +3V for MAX7427 |
| 5 | OUT | Filter Output |
| 6 | OS | Offset Adjust Input. To adjust output offset, bias OS with a resistive voltage-divider between an external supply and ground. Connect OS to COM if no offset adjustment is needed. |
| 7 | $\overline{\text{SHDN}}$ | Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V _{DD} for normal operation. |
| 8 | CLK | Clock Input. Connect an external capacitor (C _{OSC}) from CLK to GND to set the internal oscillator frequency. To override the internal oscillator, connect to an external clock. |

Detailed Description

The MAX7426/MAX7427 family of 5th-order, elliptic, lowpass filters provides sharp rolloff with good stopband rejection. All parts operate with a 100:1 clock-to-corner frequency ratio.

Most SCFs are designed with biquadratic sections. Each section implements two pole-zero pairs, and the sections can be cascaded to produce higher-order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. The MAX7426/MAX7427 use an alternative approach, which is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network may be synthesized using CAD programs or may be found in many filter books. Figure 1 shows a basic 5th-order ladder elliptic filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of the same advantages. The component sensitivity of a passive ladder filter is low when compared to a cascaded biquadratic design, because each component affects the entire filter shape rather than a single pole-zero pair. In other words, a

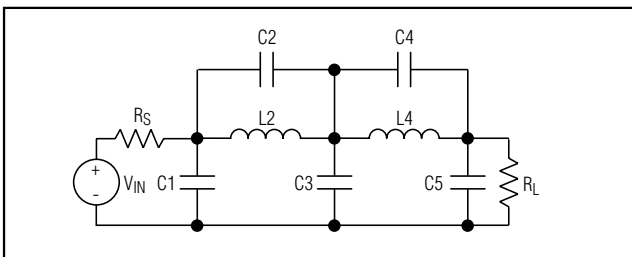


Figure 1. 5th-Order Ladder Elliptic Filter Network

mismatched component in a biquadratic design has a concentrated error on its respective poles, while the same mismatch in a ladder filter design spreads its error over all poles.

Elliptic Characteristics

Lowpass elliptic filters such as the MAX7426/MAX7427 provide the steepest possible rolloff with frequency of the four most common filter types (Butterworth, Bessel, Chebyshev, and elliptic). The high Q value of the poles near the passband edge combined with the stopband zeros allow for the sharp attenuation characteristic of elliptic filters, making these devices ideal for anti-aliasing and post-DAC filtering in single-supply systems (see the *Anti-Aliasing and Post-DAC Filtering* section).

In the frequency domain (Figure 2), the first transmission zero causes the filter's amplitude to drop to a minimum level. Beyond this zero, the response rises as the frequency increases until the next transmission zero. The stopband begins at the stopband frequency, f_s . At frequencies above f_s , the filter's gain does not exceed the gain at f_s . The corner frequency, f_c , is defined as the point where the filter output attenuation falls just below the passband ripple. The transition ratio (r) is defined as the ratio of the stopband frequency to the corner frequency:

$$r = f_s / f_c$$

The MAX7426/MAX7427 have a transition ratio of 1.25 and typically 37dB of stopband rejection.

Clock Signal

External Clock

These SCFs are designed for use with external clocks that have a 40% to 60% duty cycle. When using an external clock, drive the CLK pin with a CMOS gate

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

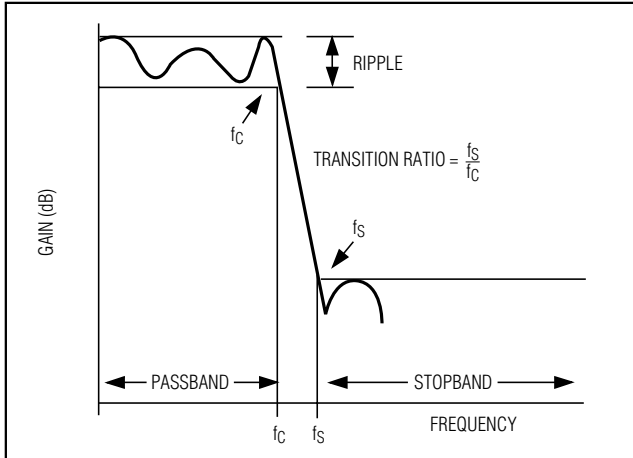


Figure 2. Elliptic Filter Response

powered from 0 to V_{DD} . Varying the rate of the external clock adjusts the corner frequency of the filter:

$$f_c = \frac{f_{CLK}}{100}$$

Internal Clock

When using the internal oscillator, the capacitance (C_{OSC}) on CLK determines the oscillator frequency:

$$f_{OSC}(\text{kHz}) = \frac{17.5 \times 10^3}{C_{OSC}(\text{pF})}$$

Since C_{OSC} is in the low picofarads, minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Varying the rate of the internal oscillator adjusts the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 100kHz produces a nominal corner frequency of 1kHz.

Input Impedance vs. Clock Frequencies

The MAX7426/MAX7427's input impedance is effectively that of a switched-capacitor resistor (see the following equation), and is inversely proportional to frequency. The input impedance values determined by the equation represent the average input impedance, since the input current is not continuous. As a rule, use a driver with an output resistance less than 10% of the filter's input impedance.

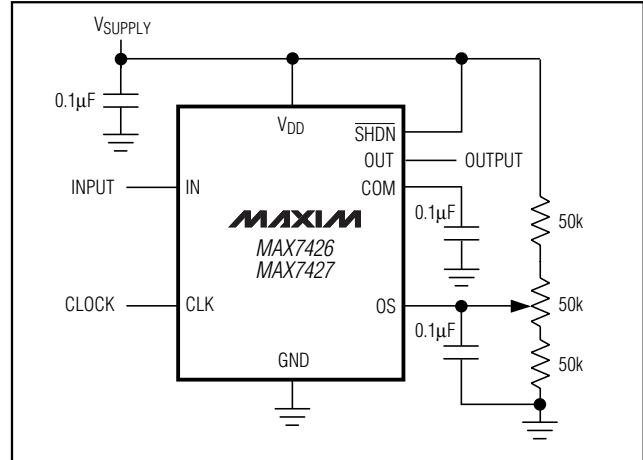


Figure 3. Offset Adjustment Circuit

Estimate the input impedance of the filter by using the following formula:

$$Z_{IN} = \frac{1}{f_{CLK} \times C_{IN}}$$

where f_{CLK} = clock frequency and C_{IN} = 1pF.

Low-Power Shutdown Mode

The MAX7426/MAX7427 have a shutdown mode that is activated by driving \overline{SHDN} low. In shutdown mode, the filter supply current reduces to 0.2µA, and the output of the filter becomes high impedance. For normal operation, drive \overline{SHDN} high or connect to V_{DD} .

Applications Information

Offset (OS) and Common-Mode (COM) Input Adjustment

COM sets the common-mode input voltage and is biased at midsupply with an internal resistor-divider. If the application does not require offset adjustment, connect OS to COM. For applications where offset adjustment is required, apply an external bias voltage through a resistor-divider network to OS, as shown in Figure 3. For applications that require DC level shifting, adjust OS with respect to COM. (**Note:** Do not leave OS unconnected.) The output voltage is represented by these equations:

$$V_{OUT} = (V_{IN} - V_{COM}) + V_{OS}$$

$$V_{COM} = \frac{V_{DD}}{2} \text{ (typical)}$$

where $(V_{IN} - V_{COM})$ is lowpass filtered by the SCF and OS is added at the output stage. See the *Electrical*

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

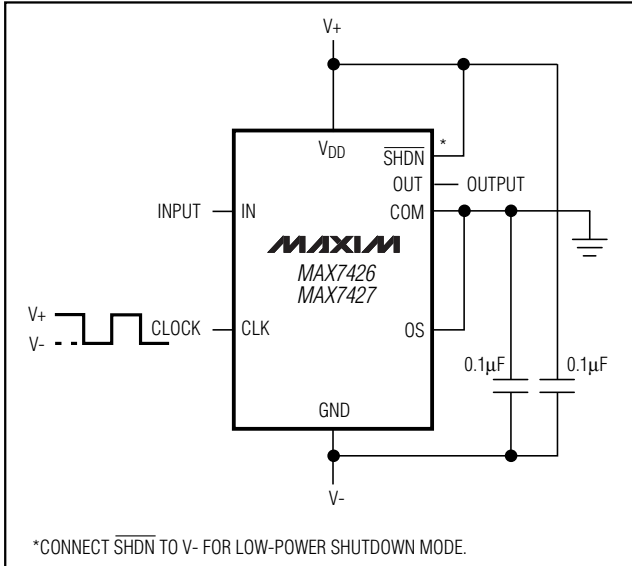


Figure 4. Dual-Supply Operation

Characteristics table for the input voltage range of COM and OS. Changing the voltage on COM or OS significantly from midsupply reduces the dynamic range.

Power Supplies

The MAX7426 operates from a single +5V supply, and the MAX7427 operates from a single +3V supply. Bypass V_{DD} to GND with a 0.1µF capacitor. If dual supplies are required, connect COM to the system ground and GND to the negative supply. Figure 4 shows an example of dual-supply operation. Single-supply and dual-supply performance are equivalent.

For either single-supply or dual-supply operation, drive CLK and SHDN from GND (V₋ in dual-supply operation) to V_{DD}. Use the MAX7427 for ±2.5, and use the MAX7426 for ±1.5V. For ±5V dual-supply applications, refer to the MAX291/MAX292/MAX295/MAX296 and MAX293/MAX294/MAX297 data sheets.

Input Signal Amplitude Range

The optimal input signal range is determined by observing the voltage level at which the signal-to-noise plus distortion (SINAD) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the THD + Noise response as the input signal's peak-to-peak amplitude is varied.

Anti-Aliasing and Post-DAC Filtering

When using the MAX7426/MAX7427 for anti-aliasing or post-DAC filtering, synchronize the DAC (or ADC) and the filter clocks. If the clocks are not synchronized, beat frequencies may alias into the desired passband.

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 2 lists typical harmonic distortion values with a 10kΩ load at T_A = +25°C.

Chip Information

TRANSISTOR COUNT: 1457
PROCESS: BiCMOS

Table 2. Typical Harmonic Distortion

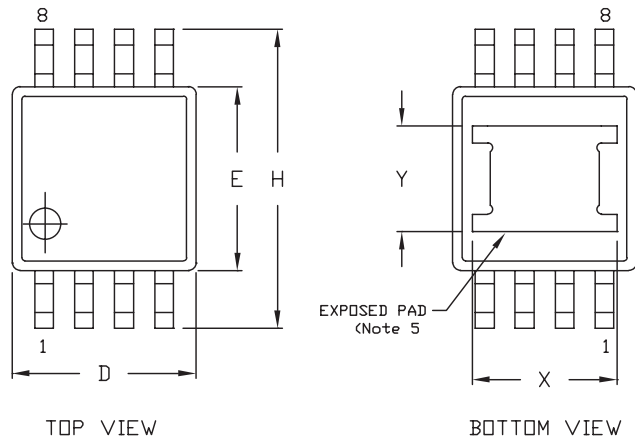
| FILTER | f _{CLK} (kHz) | f _{IN} (Hz) | V _{IN} (V _{p-p}) | TYPICAL HARMONIC DISTORTION (dB) | | | |
|---------|------------------------|----------------------|-------------------------------------|----------------------------------|-----|-----|-----|
| | | | | 2nd | 3rd | 4th | 5th |
| MAX7426 | 500 | 1k | 4 | -71 | -73 | -90 | -82 |
| | 100 | 200 | | -88 | -86 | -92 | -88 |
| MAX7427 | 500 | 1k | 2 | -87 | -86 | -90 | -90 |
| | 100 | 200 | | -90 | -87 | -90 | -90 |

5th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Package Information

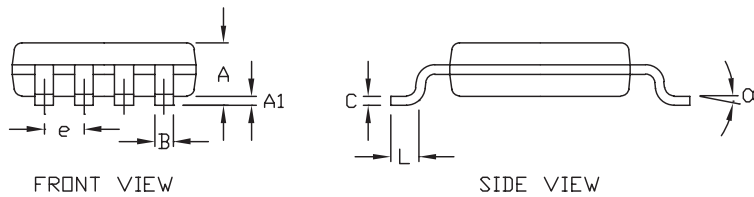
MAX7426/MAX7427

8LUMAXD.EPS



| | INCHES | | MILLIMETERS | | JEDEC | | | |
|----------|------------|-------|-------------|-------|------------|-------|----------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| A | 0.037 | 0.043 | 0.94 | 1.10 | --- | 0.043 | --- | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 |
| B | 0.010 | 0.014 | 0.25 | 0.36 | 0.010 | 0.016 | 0.25 | 0.40 |
| C | 0.005 | 0.007 | 0.13 | 0.18 | 0.005 | 0.009 | 0.13 | 0.23 |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| e | 0.0256 BSC | | 0.65 BSC | | 0.0256 BSC | | 0.64 BSC | |
| E | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| H | 0.188 | 0.198 | 4.78 | 5.03 | 0.193 BSC | | 4.9 BSC | |
| L | 0.016 | 0.026 | 0.41 | 0.66 | 0.016 | 0.027 | 0.40 | 0.70 |
| α | 0° | 6° | 0° | 6° | 0° | 6° | 0° | 6° |
| *X | 0.087 | 0.099 | 2.210 | 2.515 | | | | |
| *Y | 0.062 | 0.074 | 1.575 | 1.880 | | | | |

* EXPOSED PAD (Note 5)



NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

| | | | |
|---|--------------------------------------|--------------------|--------------------|
| MAXIM | | | |
| <small>PROPRIETARY INFORMATION</small> | | | |
| <small>TITLE:</small> | | | |
| PACKAGE OUTLINE, 8L uMAX WITH EP OPTION | | | |
| <small>APPROVAL:</small> | <small>DOCUMENT CONTROL NO.:</small> | <small>REV</small> | <small>1/1</small> |
| | 21-0036 | H | |