MAX77231

2.75V to 4.8V Input, 10mA Output, 35µV_{RMS} Ultra-Low Noise Boost Regulator

General Description

The MAX77231 is optimized for boost applications, requiring very low ripple/noise and small PCB space. Output ripple and noise are suppressed to 35µV_{RMS} (in 1MHz BW) by a PMOS linear post-regulator set 0.5V below the boost regulator output to reject noise while optimizing efficiency.

The boost regulator operates using a 1µH/400mA inductor and 2.2µF (0.22 (min) after derating) output capacitance. Fast transient response and stable operation are guaranteed using a current-limited PFM architecture.

A PMOS low-noise linear post-regulator attenuates boost converter ripple by ~50dB (10MHz BW) before delivering 11.2V to the load. Other output voltages up to 16.2V can be factory set. The LDO also disconnects the load from the boost during shutdown, allowing the output to fall to 0V (true shutdown). Active discharge can also be activated.

The MAX77231 is packaged in a 9-bump wafer-level package (WLP), providing a compact layout when combined with the inductor and external capacitors. Total solution size is less than 7mm^2.

Benefits and Features

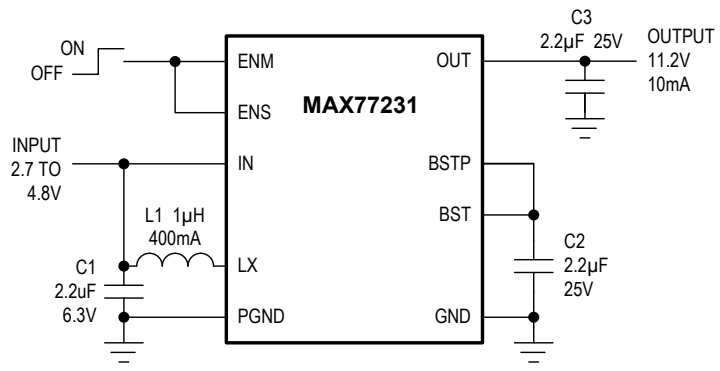
- Ultra-Small Solution Size (< 7mm^2)
- 35µV_{RMS} (typ) Output Ripple/Noise
- 11.2V/10mA Output
- Output Factory Trimmable from 11.2V to 16.2V
- 125µA No Load Supply Current Output on < 1µA Shutdown Supply Current
- True Shutdown Load Disconnect
- Selectable Active Discharge
- 9-Bump, 1.238mm x 1.238mm x 0.35mm WLP

Applications

- Low-Noise Bias Supply
- Sensor Bias Supply

Ordering Information **appears at end of data sheet.**

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

BST, BSTP, OUT to GND .....-0.3V to +22V
BST to BSTP .....-0.3V to +0.3V
BST to OUT .....-0.3V to +6V
IN, ENM, ENS to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
RMS LX_ Current (per bump) 1A

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 6.7mW/°C above +70°C).....533mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Bump Temperature (soldering, reflow).....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = V_{ENM} = V_{ENS} = 3.7V, V_{BSTP} = V_{BST} = 11.7V, V_{OUT} = 11.2V, C_{IN} = C_{BST} = C_{OUT} = 2.2μF, T_A = -40°C to +85°C, Figure 1, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN Operating Range			2.75		4.8	V
IN Undervoltage Threshold	When output is enabled/ disabled	IN rising		2.65	2.75	V
		IN falling	2.4	2.55		
Shutdown Supply Current	Total of I_{IN} and I_{LX}, V_{IN} = V_{LX} = 4.8V, V_{OUT} = V_{ENM} = V_{ENS} = 0V	T_A = +25°C		0.01	1	μA
		T_A = +85°C		0.1		μA
Supply Current	Output regulating, no load			120		μA
IN Supply Current	BST supply current not included			50	100	μA
BST Supply Current	I_{BST} + I_{BSTP}, V_{BST} = 11.7V (not switching)			20	60	μA
BOOST REGULATOR						
BST Regulation Voltage	LDO output voltage is 0.5V less than BST		-3%	11.7	+3%	V
BST Output Range	Factory trimmed		11.7		16.7	V
LX Maximum On-Time				570		ns
LX Minimum Off-Time	VIN = 2.7V to 4.8V	V_{BST} = 11V		35		ns
		V_{BST} = V_{IN} + 3.5V		35		ns
		V_{BST} = V_{IN}		320		ns
LX Peak Current Limit	Static measurement (Note 2)					mA
	V_{IN} = 3.7V, T_A = +25°C		213	225	237	
	V_{IN} = 2.7V to 4.8V, over temperature		170		300	
	Dynamic measurement (Note 2)			350		
LX Inductor Value	±20% tolerance			1.0 to 4.7		μH
LX On Resistance	I_{LX} = 150mA			250	600	mΩ
LX Shutdown Leakage	V_{LX} = 18V	T_A=+25°C		0.05	5	μA
		T_A=+85°C		0.5		μA
Diode Forward Voltage	V_{LX} to V_{BSTP}, V_{LX} = 3.7V, I_{LX} = 150mA			0.4		V
Boost Efficiency	0402 1μH inductor V_{IN} = 3.7V, V_{BST} = 11.7V, 3mA			76		%

Electrical Characteristics (continued)

(V_{IN} = V_{ENM} = V_{ENS} = 3.7V, V_{BSTP} = V_{BST} = 11.7V, V_{OUT} = 11.2V, C_{IN} = C_{BST} = C_{OUT} = 2.2μF, T_A = -40°C to +85°C, Figure 1, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR						
OUT Regulation Voltage	I_{OUT} = 0mA to 6mA		-4%	11.2	+4%	V
OUT Output Range	Factory-trimmed output range (contact factory)		11.2		16.2	V
Output Discharge Current	V_{ENM} = 0V, V_{ENS} = V_{BST} = 3.7V, V_{OUT} = 1V		15			mA
PSRR	BST to OUT, f = 1MHz, I_{OUT} = 5mA			50		dB
OUT Output Capacitance	±20% tolerance, -90% voltage coefficient			2.2		μF
LOGIC (ENM AND ENS)						
Input Threshold	When output is enabled/ disabled	Rising		0.95	1.26	V
		Falling	0.54	0.85		V
ENS Pulldown Resistance	V_{ENS} = 1V, V_{ENM} = 0V			500		kΩ
ENM Input Leakage	V_{ENM} = 0V to 4.8V, V_{ENS} = 0V	T_A = +25°C		0.001	1	μA
		T_A = +85°C		0.01		μA
TRANSIENT/NOISE						
Total Output Noise and Ripple	Circuit of Figure 1, I_{LOAD} = 0mA to 6mA, f = 100Hz to 10MHz (-3dB corners, first order roll off)			35		μV_{RMS}
Transient Load Regulation	Circuit of Figure 1, I_{OUT} = 0 to 6mA			20		mV_{P-P}
Transient Line Regulation	Circuit of Figure 2, at 16V load, V_{IN} = 2.7V to 4.8V, V_{IN} = 500mV step, t_R = t_F = 100mV/μs			5		mV_{P-P}
Startup Time	Circuit of Figure 2, at 16V load, from V_{ENM} and V_{ENS} high to V_{OUT} = 16V			2		ms
Output Active Discharge Time	Circuit of Figure 2, at 16V load, from V_{ENM} low to V_{OUT} < 0.1V			5		ms
Short-Circuit Output Current	V_{OUT} = 0V			40		mA

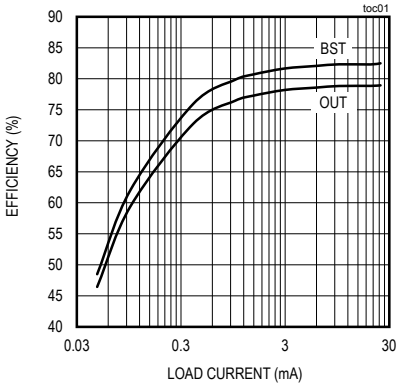
Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods. Static LX current limits test.

Note 3: In-circuit limit with 1μH inductor is approximately 125mA higher than listed values due to current comparator delay. Dynamic (in circuit) peak limit is typically 350mA.

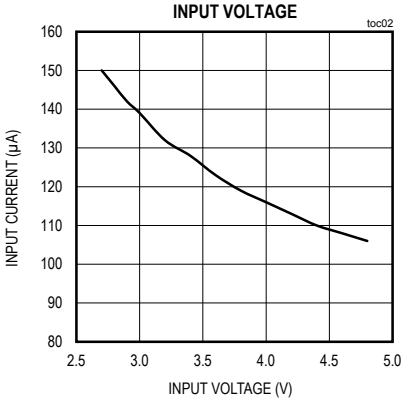
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

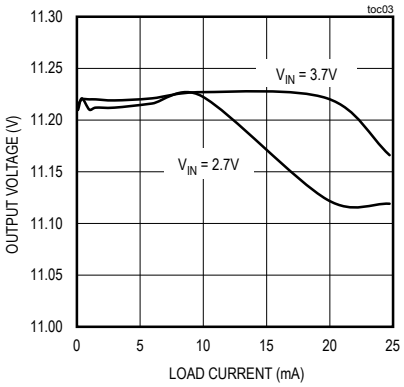
EFFICIENCY vs. LOAD CURRENT



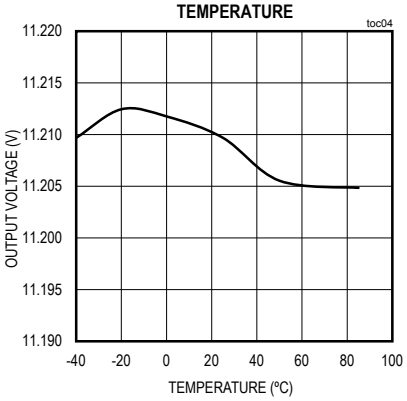
NO-LOAD INPUT CURRENT vs. INPUT VOLTAGE



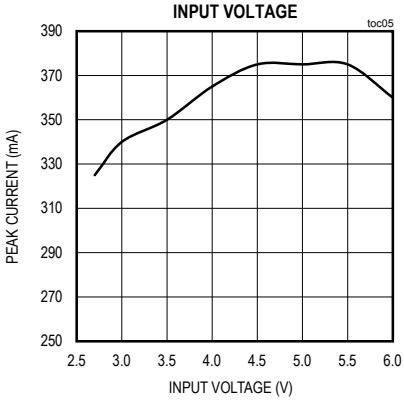
OUTPUT VOLTAGE vs. LOAD CURRENT



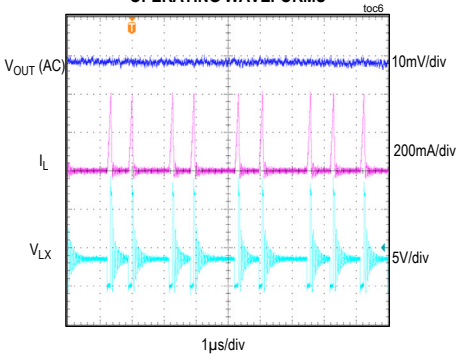
OUTPUT VOLTAGE vs. TEMPERATURE



PEAK LX CURRENT vs. INPUT VOLTAGE



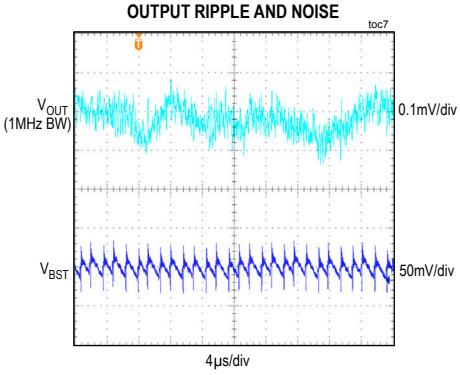
TYPICAL OPERATING WAVEFORMS



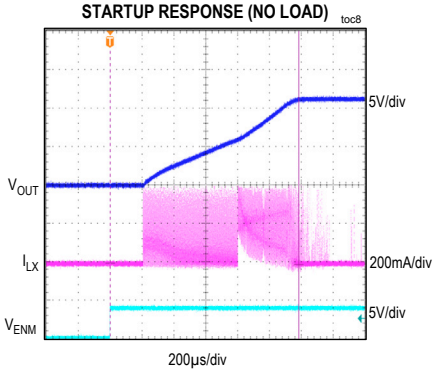
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

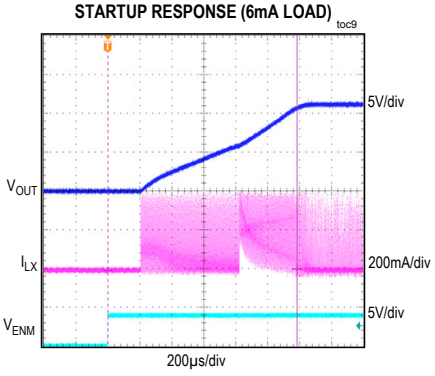
OUTPUT RIPPLE AND NOISE



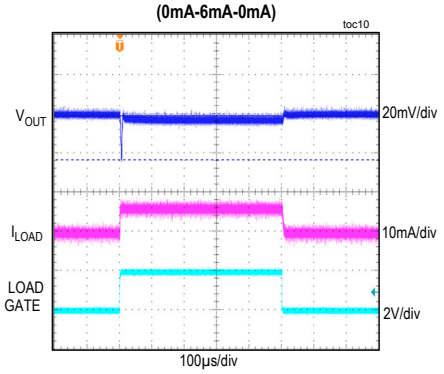
STARTUP RESPONSE (NO LOAD)



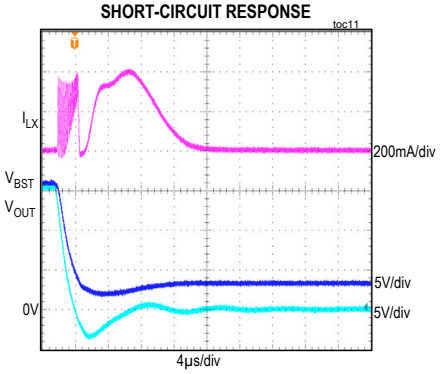
STARTUP RESPONSE (6mA LOAD)



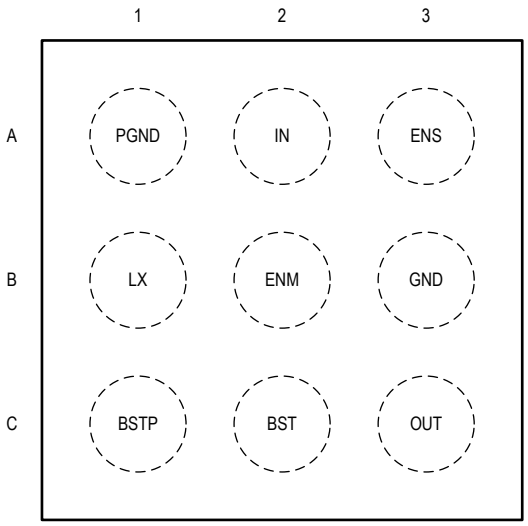
LOAD TRANSIENT RESPONSE
(0mA-6mA-0mA)



SHORT-CIRCUIT RESPONSE



Bump Configuration



(VIEW FROM TOP OF PACKAGE, PINS DOWN)

Bump Description

NAME	LOCATION	FUNCTION
PGND	A1	Power Ground. Connect to ground through a low-inductance trace. Low side of internal LX switch.
IN	A2	Input Supply Voltage. Connect this pin to the 2.5V to 4.8V input power source. Connect a 2.2μF/6.3V ceramic capacitor from IN to ground.
ENS	A3	Slave Enable Input. Logic-high enables the output. Logic-low turns it off. Typically, a 0.9V logic threshold with ±50mV hysteresis.
LX	B1	Inductor Pin. Connect a 1.0μH inductor from this pin to the input voltage source.
ENM	B2	Master Enable Input. A logic-high on both ENM and ENS enables the output. Logic-low turns the output off, while also enabling a 15mA (min) output discharge current. Typically, a 0.9V logic threshold with ±50mV hysteresis.
AGND	B3	Analog Ground
BSTP	C1	Boost Power Output. Output of internal Schottky diode. Delivers up to 400mA current pulses at high switching speeds. Bypass to ground through a low-inductance trace with a 2.2μF/25V ceramic capacitor at BST/BSTP. BSTP should be connected to the linear regulator input at BST.
BST	C2	Linear Regulator Input. Connect this pin to the boost output, BSTP, to supply the linear regulator when the part is enabled. Connect a 2.2μF/25V ceramic capacitor from BST/BSTP to AGND to ensure proper operation.
OUT	C3	Linear Regulator Low-Noise/Ripple Output (When MAX77321 is Enabled). OUT falls to 0V when disabled. Connect a 2.2μF/25V ceramic capacitor from OUT to ground.

Detailed Description

The MAX77231 is a low-noise boost regulator designed to occupy minimal PCB board space. A high-frequency PFM boost regulator creates an 11.7V supply, which is then post-regulated to 11.2V with a low-noise, high PSRR PMOS linear regulator (see Figure 1). Other output voltages up to 16.2V are available on request.

Boost Converter

An 11.7V (or other factory trimmed) output is generated by a current-limited, maximum on-time, minimum off-time, PFM boost converter. When the output drops below 11.7V, an internal NMOS switch forces the input voltage across the inductor. The switch turns off when the inductor current reaches 350mA, and the LX pin is driven high by the inductor until the internal Schottky diode, D1, turns on. Inductor current is delivered to the boost output through the diode until the reverse inductor voltage causes the current to drop to 0mA, and the LX voltage drops.

A maximum on-time timer prevents the LX switch from staying on longer than 570ns if resistive, or other, losses prevent the inductor current from reaching 350mA.

If the inductor discharge time exceeds the 35ns minimum off time, and the BST output is still less than 11.7V, LX switches back down to 0V, and the current builds back up to 350mA. Under this condition, the inductor current ramps back up before reaching 0mA, causing the boost to operate in continuous conduction mode. This mode is typically reached only during startup, when the BST output is much less than 11.7V.

The typical switching frequency is:

$$f_{SW} = (1/t_{OFF})(2\ I_{OUT}/I_{LPK})/Eff$$

where: I_{OUT} = load current, Eff = estimated boost efficiency (0.75), I_{LPK} = inductor peak current (350mA), and t_{OFF} is time needed to discharge the inductor. The expression for t_{OFF} is:

$$t_{OFF} = L \times I_{LPK}/(V_{BST} + V_{DIODE} - V_{IN})$$

For the typical application circuit:

$$t_{OFF} = 1\mu H \times 350mA/(11.7V + 0.4V - 3.7V) = 41.7ns$$

where: L = 1μH, I_{LPK} = 350mA, V_{BST} = 11.7V, V_{DIODE} = 0.4V, and V_{IN} = 3.7V, and t_{OFF} = 41.7ns:

$$f_{SW(mA)} = 183kHz/mA \text{ of load current}$$

The MAX77231 maximum operating frequency (and hence available output current) is governed by the charge (t_{ON}) and discharge time (t_{OFF}) of the inductor. t_{OFF} is calculated above, but is limited to at least 35ns by an internal timer. t_{ON} is calculated below:

$$t_{ON} = L \times I_{LPK}/V_{IN}$$

The maximum possible frequency is:

$$f_{SW(MAX)} = 1/(t_{ON} + t_{OFF})$$

and consequently, typical available output current is:

$$I_{OUT(MAX)} = f_{SW(MAX)}/f_{SW(mA)}$$

For a typical scenario with V_{IN} = 3.7V, L_{IPK} = 350mA, and a 1μH inductor:

$$t_{ON} = L \times I_{LPK}/V_{IN} = 1\mu H \times 350mA/3.7V = 94.6ns$$

$$f_{SW(MAX)} = 1/(t_{ON} + t_{OFF}) = 1/(94.6ns + 41.7ns) = 7.33MHz$$

Typical available output current for an 11.2V output (at OUT) and a 3.7V input is then:

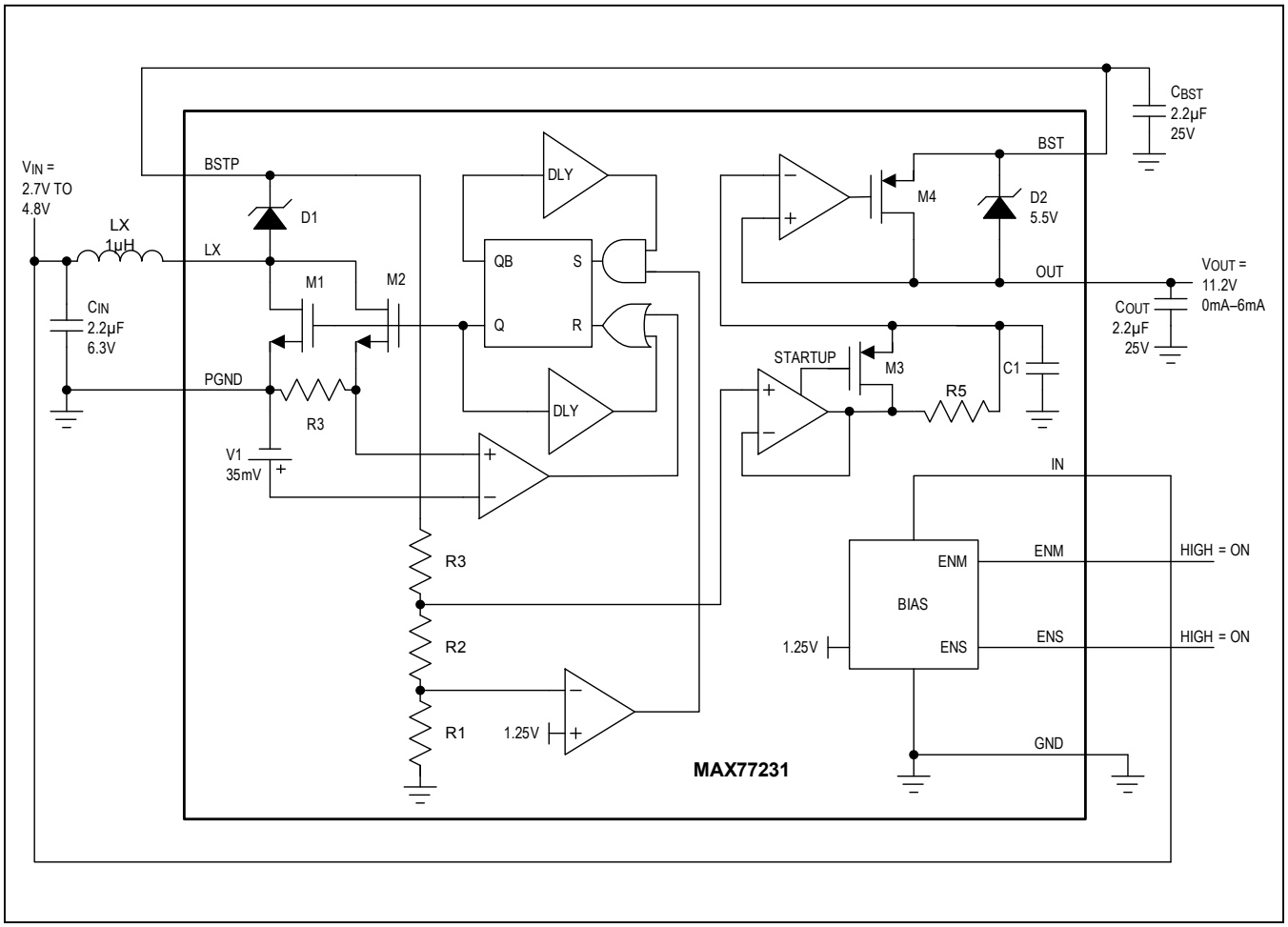
$$I_{OUT(MAX)} = f_{SW(MAX)}/f_{SW(mA)} = 7.33/0.183 = 40mA$$

Linear Regulator

The boost is followed by an 11.2V linear regulator. This regulator passes the boost output current to the load, while rejecting the unwanted ripple and reducing noise. The linear regulator can deliver 10mA of output current and provides 50dB of ripple rejection at 1MHz.

The linear regulator is fed from an internal low-noise reference. The reference voltage is filtered to remove unwanted thermal, shot, and 1/f noise generated in the preceding circuitry. Using this low-noise reference, the linear regulator output is able to achieve 35μV_{RMS} noise in a 100kHz bandwidth.

Block Diagram (FPO)



Enable/Active Discharge

The MAX77231 has two enable inputs: ENM and ENS. To turn on the device, both ENM and ENS must be high. A logic-low on ENM disables the device with a 15mA active discharge current. A logic-low on ENS disables the device without active discharge. ENM and EMS functionality is outlined in Table 1.

Overload and Short-Circuit Protection

The MAX77231 is fully protected against output short circuits. In the case of a short circuit, off time is lengthened to prevent inductor current from climbing. The MAX77231 sources current into the short indefinitely, without damage, until the short is removed.

Note, however, that only OUT, not BST, is protected. A short of V_{BST} can cause inductor and LX current to rise above guaranteed operating levels.

Component Selection
Input and Output Capacitance

The MAX77231 operates with small ceramic capacitors. X5R or X7R dielectrics are recommended. C_{IN} should be 2.2μF 6.3V, while C_{OUT} and C_{BST} should be 2.2μF 25V rated. It is expected that the elevated voltage on C_{OUT} and C_{BST} significantly derate the realized capacitance value at these nodes. The MAX77231 is designed with this expectation and can tolerate a minimum of 0.22μF at C_{OUT} and C_{BST} after derating.

Inductors

The MAX77231 is designed to operate with a 1μH 400mH rated inductor. Other values up to 10μH can be used, but it is expected that in the space-constrained applications for which the MAX77231 is likely to chosen, smaller values are preferred. Inductance less than 1μH is not recommended because the accompanying higher dI/dt can exceed the current comparator's ability to effectively limit current.

Table 1. MAX77231 Enable Truth Table

ENM	ENS	POWER STATE	ACTIVE DISCHARGE
0	X	Power-down	On
1	0	Power-down	Off
1	1	Active	Off

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77231EZL+	-40°C to +85°C	9 WLP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 Ultra-Thin WLP	Z91A1+1	**21-0691**	**Refer to Application Note 1891**