Click here for production status of specific part numbers.

MAX77650/MAX77651

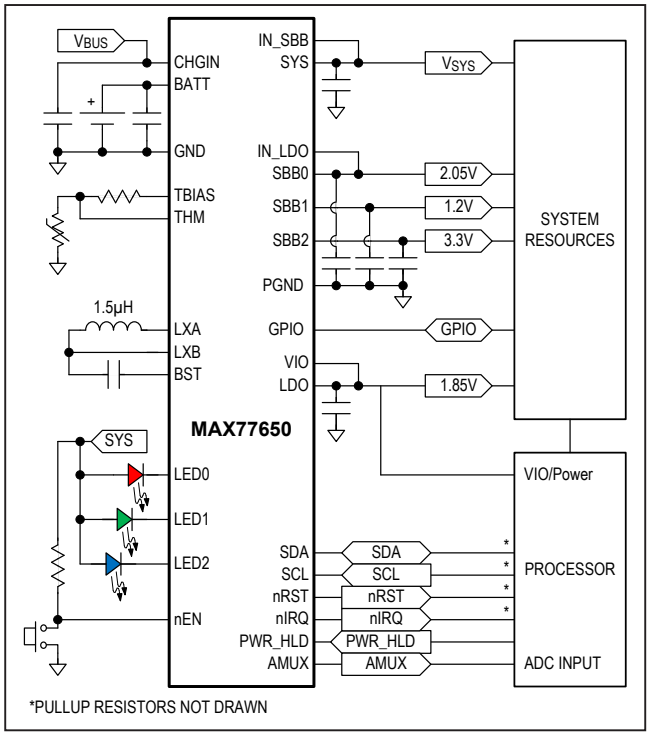
Ultra-Low Power PMIC with 3-Output SIMO and Power Path Charger for Small Li+

General Description

The MAX77650/MAX77651 provide highly-integrated battery charging and power supply solutions for low-power wearable applications where size and efficiency are critical. Both devices feature a SIMO buck-boost regulator that provides three independently programmable power rails from a single inductor to minimize total solution size. A 150mA LDO provides ripple rejection for audio and other noise-sensitive applications. A highly configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA).

The devices include other features such as current sinks for driving LED indicators and an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I²C interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality when the devices are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Simplified Application Circuit



Benefits and Features

- Highly Integrated
  - Smart Power Selector™ Li+/Li-Poly Charger
  - 3 Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
  - 150mA LDO
  - 3-Channel Current Sink Driver
  - Analog MUX Output for Power Monitoring
- Low Power
  - 0.3µA Shutdown Current
  - 5.6µA Operating Current (3 SIMO Channels + LDO)
- Charger Optimized for Small Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Flexible and Configurable
  - I²C Compatible Interface and GPIO
  - Factory OTP Options Available
- Small Size
  - 2.75mm x 2.15mm x 0.7mm WLP Package
  - 30-Bump, 0.4mm-Pitch WLP, 6x5 Array
  - Small Total Solution Size (19.2mm²)

Applications

- Bluetooth Headphones/Hearables
- Fitness, Health, and Activity Monitors
- Portable Devices
- Internet of Things (IoT)

***Ordering Information* appears at end of data sheet.**

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

19-8550; Rev 7; 9/18

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TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

nEN, PWR_HLD, nIRQ, nRST to GND .....-0.3V to V_{SYS} + 0.3V
SCL, SDA, GPIO to GND .....-0.3V to V_{IO} + 0.3V
CHGIN to GND .....-0.3V to +30.0V
SYS, BATT to GND .....-0.3V to +6.0V
SYS to IN_SBB .....-0.3V to +0.3V
V_L to GND .....-0.3V to +6.0V
AMUX, THM, TBIAS to GND .....-0.3V to +6.0V
nIRQ, nRST, SDA, AMUX, GPIO Continous Current .....±20mA
CHGIN Continuous Current .....$1.2A_{RMS}$
SYS Continuous Current .....$1.2A_{RMS}$
BATT Continuous Current (Note 1) .....$1.2A_{RMS}$
LDO to GND (Note 2) .....-0.3V to V_{IN_LDO} + 0.3V
IN_LDO, V_{IO} to GND ..... -0.3V to the lower of (V_{SYS} + 0.3V) and +6.0V
LED0, LED1, LED2 to LGND .....-0.3V to +6.0V
IN_SBB to PGND .....-0.3V to +6.0V
LXA Continuous Current (Note 3) .....$1.2A_{RMS}$
LXB Continuous Current (Note 4) .....$1.2A_{RMS}$
SBB0, SBB1, SBB2 to PGND (Note 2) .....-0.3V to +6.0V
BST to IN_SBB .....-0.3V to +6.0V
BST to LXB .....-0.3V to +6.0V
SBB0, SBB1, SBB2 Short-Circuit Duration .....Continuous
PGND to GND .....-0.3V to +0.3V
LGND to GND .....-0.3V to +0.3V
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C
Continuous Power Dissipation (Multilayer Board)
(T_A = +70°C, derate 20.4mW/°C above +70°C) 1632mW

Note 1: Do not repeatedly hot-plug a source to the BATT terminal at a rate greater than 10Hz. Hot plugging low-impedance sources results in an ~8A momentary (~2µs) current spike.
Note 2: When the active discharge resistor is engaged, limit its power dissipation to an average of 10mW.
Note 3: LXA has internal clamping diodes to PGND and IN_SBB. It is normal for these diodes to briefly conduct during switching events. Avoid steady-state conduction of these diodes.
Note 4: Do not externally bias LXB. LXB has an internal low-side clamping diode to PGND, and an internal high-side clamping diode that dynamically shifts to the selected SIMO output. It is normal for these internal clamping diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} + 0.3V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

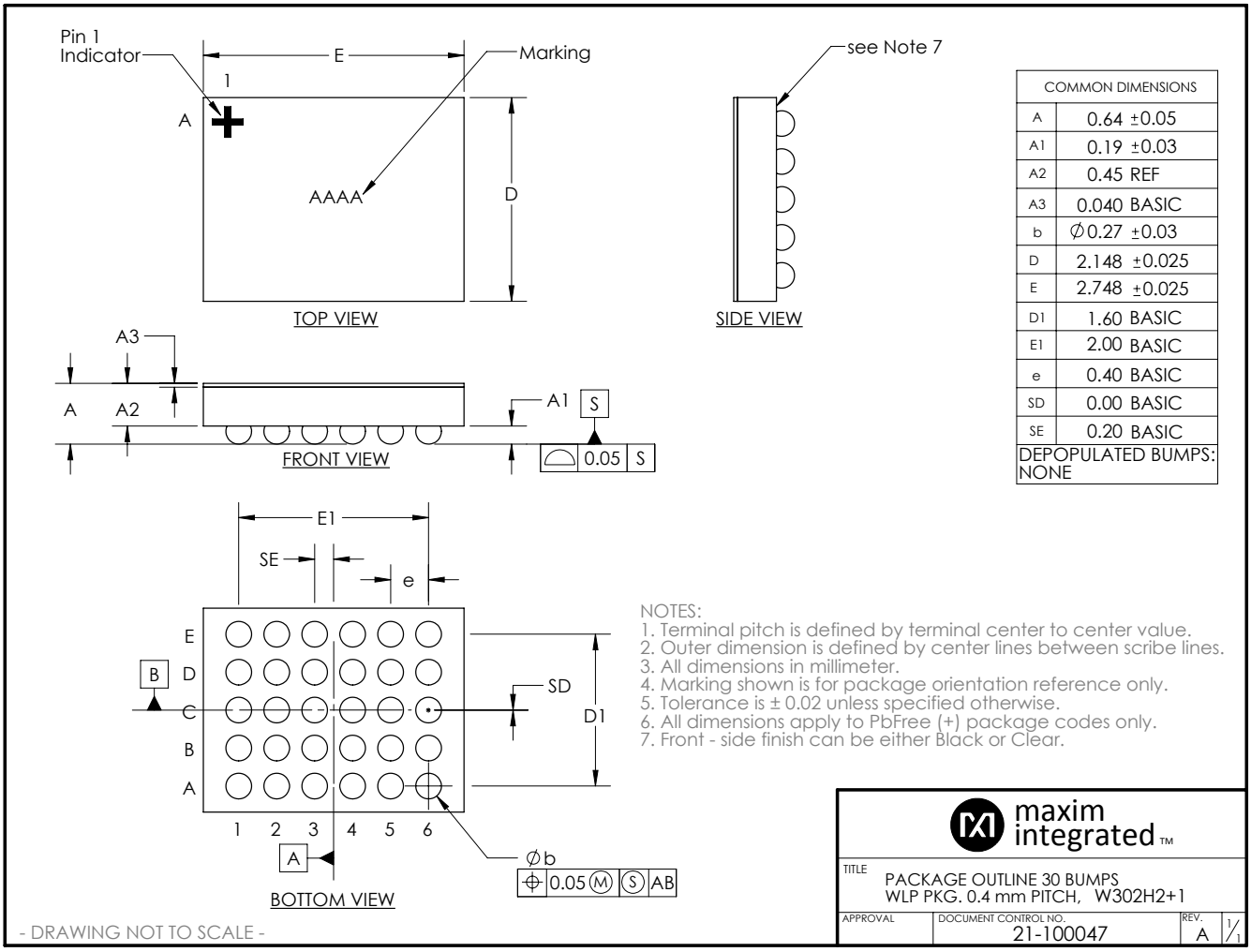
Package Information

PACKAGE CHARACTERISTICS	VALUES
Package Code	W302H2+1
Outline Number	**21-100047**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	49°C/W (2s2p board)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Package Information (continued)



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.040 BASIC
b	∅0.27 ±0.03
D	2.148 ±0.025
E	2.748 ±0.025
D1	1.60 BASIC
E1	2.00 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

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TITLE: PACKAGE OUTLINE 30 BUMPS WLP PKG. 0.4 mm PITCH, W302H2+1

APPROVAL | DOCUMENT CONTROL NO. 21-100047 | REV. A | 1/1

Electrical Characteristics—Top Level

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{IN_SBB} = V_{IN_LDO} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{SYS}			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Current measured into BATT and SYS and IN_SBB and IN_LDO, all resources are off (LDO, SBB0, SBB1, SBB2, LED0, LED1, LED2), T_A = 25°C	Main bias is off (SBIA_EN = 0). This is the standby state		0.3	1	µA
			Main bias is on in low-power mode (SBIA_EN = 1, SBIA_LPM = 1)		1		
			Main bias is on in normal-power mode (SBIA_EN = 1, SBIA_LPM = 0)		28		
Quiescent Supply Current	I_Q	Current measured into BATT and SYS and IN_SBB and IN_LDO. LDO, SBB0, SBB1, and SBB2 are enabled with no load. LED0, LED1, and LED2 are disabled	Main bias is in low-power mode (SBIA_LPM = 1)		5.6	13	µA
			Main bias is in normal-power mode (SBIA_LPM = 0)		40	60	

Electrical Characteristics—Global Resources

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{SYS} falling		1.6	1.9	2.1	V
POR Threshold Hysteresis					100		mV
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling, UVLO_F[3:0] = 0xA		2.5	2.6	2.7	V
		V_{SYS} falling, UVLO_F[3:0] = 0xF		2.75	2.85	2.95	
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	UVLO_H[3:0] = 0x5			300		mV
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising		5.70	5.85	6.00	V
THERMAL MONITORS							
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising			165		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			100		°C
Thermal Alarm Temperature Hysteresis					15		°C
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{SYS} = 5.5V, V_{nEN} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN falling		V_{SYS} - 1.4	V_{SYS} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_F}$	nEN falling			V_{SYS} - 0.9	V_{SYS} - 0.6	V
Debounce Time	t_{DBNC_nEN}	DBEN_nEN = 0			100		µs
		DBEN_nEN = 1			30		ms
Manual Reset Time	t_{MRST}	MRT_OTP = 0		14	16	20	s
		MRT_OTP = 1		7	8	10.5	
POWER HOLD INPUT (PWR_HLD)							
PWR_HLD Input Leakage Current	$I_{PWR\_HLD\_LKG}$	V_{SYS} = V_{IO} = 5.5V, V_{PWR_HLD} = 0V, and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
PWR_HLD Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
PWR_HLD Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
PWR_HLD Input Hysteresis	V_{HYS}	V_{IO} = 1.8V			50		mV
PWR_HLD Glitch Filter	$t_{PWR\_HLD\_GF}$	Both rising and falling edges are filtered			100		µs
PWR_HLD Wait Time	$t_{PWR\_HLD\_WAIT}$	Maximum time for PWR_HLD input to assert after nRST deasserts during the power-up sequence		3.5	4.0	5.0	s
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	C_{IRQ} = 25pF			2		ns
Leakage Current	I_{nIRQ_LKG}	V_{SYS} = V_{IO} = 5.5V, nIRQ set to be high impedance (i.e., no interrupts), VnIRQ = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 5 and Figure 7 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}	See Figure 5 for more information			10.24		ms
Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V, nRST set to be high impedance (i.e., not reset), V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
Input Leakage Current	I_{GPI_LKG}	DIR = 1, V_{IO} = 5.5V, V_{GPIO} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DBNC_GPI}	DBEN_GPI = 1			30		ms
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See Figure 6			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 6			2.56		ms

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC INPUT						
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging	4.10		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC rising		28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising	7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis				100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	3.9	4.0	4.1	V
CHGIN Undervoltage Lockout Hysteresis				500		mV
Input Current Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with VCHGIN_MIN[2:0].	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms
SUPPLY AND QUIESCENT CURRENTS						
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		5		µA
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (USBS = 0), Charging is finished (CHG_DTLS indicate done), I_{SYS} = 0mA		1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0A			50	µA
CHGIN Suspend Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger in USB suspend (USBS = 1)			50	µA
PREQUALIFICATIONS						
Charge Current Soft-Start Slew Time		Zero to full scale		1		ms
Input Current Soft-Start Slew Time		Zero to full scale		1		ms
Prequalification Voltage Threshold Range	V_{PQ}	Charger is in prequalification mode when V_{BATT} < V_{PQ}, this threshold has 100mV of hysteresis, programmable in 100mV steps with CHG_PQ[2:0]	2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V	-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 0		10		%
		V_{BATT} = 2.5V, V_{PQ} = 3.0V, expressed as a percentage of $I_{FAST-CHG}$, I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V	27	30	33	minutes

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST CHARGE						
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CHG_CV[5:0]	3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5	±0.15	+0.5	%
		I_{BATT} = 0mA, $V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CHG_CC[5:0]	7.5		300	mA
Fast-Charge Current Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-1.5		+1.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-1.5		+1.5	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV	-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with T_FAST_CHG[1:0], from prequal done to timer fault	3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours	-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, loading conditions and/or a weak charging source caused charge current to drop below this threshold, expressed as a percentage of $I_{FAST-CHG}$		20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with TJ_REG[2:0]	60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise		-5.4		%/°C
TERMINATION AND TOPOFF						
End-of-Charge Termination Current	I_{TERM}	I_TERM = 0b00 (expressed as a percentage of $I_{FAST-CHG}$)		5		%
		I_TERM = 0b01 (expressed as a percentage of $I_{FAST-CHG}$)		7.5		
		I_TERM = 0b10 (expressed as a percentage of $I_{FAST-CHG}$)		10		
		I_TERM = 0b11 (expressed as a percentage of $I_{FAST-CHG}$)		15		

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C	1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C	27	30	33	
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with T_TOPOFF[2:0]	0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes	-10		+10	%
Charge Restart Threshold	$V_{RESTART}$	CHG = 0 (charging done), charging resumes when V_{BATT} < $V_{FAST-CHG}$ - $V_{RESTART}$	65	150		mV
DEVICE ON-RESISTANCE AND LEAKAGE						
BATT to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS		100		mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = 25°C, charger disabled		0.1	1.0	µA
		V_{SYS} = 4.5V, V_{BATT} = 0V, T_A = 85°C, charger disabled		1		
CHGIN to SYS On-Resistance		V_{CHGIN} = 4.65V		600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +25°C, body-switched diode reverse biased		0.1	1.0	µA
		V_{CHGIN} = 0V, V_{SYS} = 4.2V, T_A = +85°C, body-switched diode is reverse biased		1		
SYSTEM NODE						
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 25mV steps with VSYS_REG[4:0]	4.1		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = +25°C	4.41	4.50	4.59	V
		$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA, T_A = -40°C to +85°C	4.365	4.500	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, V_{SYS} < $V_{SYS-REG}$ due to I_{CHGIN} = $I_{CHGIN-LIM}$ (input in current-limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)	4.34	4.4	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA		V_{BATT} - 0.15V		V

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
TBIAS Voltage	V_{TBIAS}	THM_EN = 1, V_{CHGIN} = 5V		1.25		V
JEITA Cold Threshold Range	V_{COLD}	Voltage rising threshold, programmable with THM_COLD[1:0] in 5ºC increments when using an NTC β = 3380K	0.867		1.024	V
JEITA Cool Threshold Range	V_{COOL}	Voltage rising threshold, programmable with THM_COOL[1:0] in 5ºC increments when using an NTC β = 3380K	0.747		0.923	V
JEITA Warm Threshold Range	V_{WARM}	Voltage falling threshold, programmable with THM_WARM[1:0] in 5ºC increments when using an NTC β = 3380K	0.367		0.511	V
JEITA Hot Threshold Range	V_{HOT}	Voltage falling threshold, programmable with THM_HOT[1:0] in 5ºC increments when using an NTC β = 3380K	0.291		0.411	V
Temperature Threshold Accuracy		Voltage threshold accuracy expressed as temperature for an NTC β = 3380K		±3		°C
Temperature Threshold Hysteresis		Temperature hysteresis set on each voltage threshold for an NTC β = 3380K		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER AND POWER MONITOR AFEs						
Full-Scale Voltage	V_{FS}			1.25		V
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting		0.26		V/V
CHGIN POWER						
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting		2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}		0.167		V/V
BATT MONITOR						
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CHG_CC[5:0])		12.5		mV/%

Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = 25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA		-0.5		+0.65	mA
Battery Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V
ANALOG MULTIPLEXER							
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +85°C		1		µA
THM AND TBIAS							
THM Voltage Monitor Gain	G_{VTHM}				1		V/V
TBIAS Voltage Monitor Gain	G_{VTBIAS}				1		V/V

Electrical Characteristics—SIMO Buck-Boost

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE RANGE (SBB0)							
Minimum Output Voltage					0.8		V
Maximum Output Voltage					2.375		V
Output DAC Bits					6		bits
Output DAC LSB Size					25		mV
OUTPUT VOLTAGE RANGE (SBB1)							
Minimum Output Voltage		MAX77650			0.8		V
		MAX77651			2.4		
Maximum Output Voltage		MAX77650			1.5875		V
		MAX77651			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size		MAX77650			12.5		mV
		MAX77651			50		
OUTPUT VOLTAGE RANGE (SBB2)							
Minimum Output Voltage		MAX77650			0.8		V
		MAX77651			2.4		
Maximum Output Voltage		MAX77650			3.95		V
		MAX77651			5.25		
Output DAC Bits					6		bits
Output DAC LSB Size					50		mV
OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage (Note 3)	T_A = +25°C	-2.5		+2.5	%
			T_A = -40°C to +85°C	-4.0		+4.0	
TIMING CHARACTERISTICS							
Enable Delay		Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output.			60		µs
Soft-Start Slew Rate	dV/dt_{SS}			3.3	5.0	6.6	mV/µs

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{SYS} = 3.7V, V_{IN_SBB} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +85°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V	T_A = +25°C		+0.01	+1.0	µA
			T_A = +85°C		+0.1		
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V	T_A = +25°C		+0.1	+1.0	µA
			T_A = +85°C		+0.2		
Active Discharge Impedance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω
CONTROL SCHEME							
Peak Current Limit (Note 4)	I_{P_SBB}	IP_SBBx = 0b11		0.414	0.500	0.586	A
		IP_SBBx = 0b10		0.589	0.707	0.806	
		IP_SBBx = 0b01		0.713	0.866	0.947	
		IP_SBBx = 0b00		0.892	1.000	1.108	

Note 3: Measured in an open-loop test that determines the output voltage falling threshold where LXA switches high.

Note 4: Typical values align with bench observations using the stated conditions. Minimum and maximum values are tested in production with DC currents. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Electrical Characteristics—LDO

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage	V_{IN_LDO}	IN_LDO cannot exceed SYS voltage (Note 5)		1.8		5.5	V
LDO Shutdown Current	I_{IN_LDO}	Current measured into IN_LDO, LDO output disabled (Note 6)			0.1	1	µA
LDO Quiescent Supply Current (Note 6)	I_{IN_LDO}	Current measured into IN_LDO, I_{LDO} = 0mA	LDO output enabled and in regulation, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V		1.7	5.15	µA
			LDO output enabled and in dropout, V_{IN_LDO} = 1.8V, V_{LDO} target is 1.85V		2.3		
Maximum Output Current	I_{OUT}			150			mA
Current Limit		V_{LDO} externally forced to 1.3V		165	255	375	mA
OUTPUT VOLTAGE RANGE							
Output Voltage Range		Programmable with TV_LDO[6:0] in 12.5mV steps		1.3500		2.9375	V
Output DAC Bits					7		bits
Output DAC LSB Size					12.5		mV
STATIC CHARACTERISTICS							
Initial Output Voltage Accuracy		I_{LDO} = 75mA, T_A = +25°C		-2.5		+2.5	%
Output Voltage Accuracy		V_{LDO} programmed from 1.35V to 2.9375V, V_{IN_LDO} = 1.8V to 5.5V, LDO not in drop-out, I_{LDO} = 0mA to 150mA, T_A = -5°C to +85°C		-3		+3	%
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 15mA, V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V	Main bias circuits are in normal-power mode (SBIA_LPM = 0)		550		μV_{RMS}
			Main bias circuits are in low-power mode (SBIA_LPM = 1)		800		

Electrical Characteristics—LDO (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 2.05V, V_{LDO} = 1.85V, C_{LDO} = 10µF, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Enable Delay		T_A = +25°C			0.6	1.25	ms
Soft-Start Slew Rate	dV/dt_{SS}	V_{LDO} from 10% to 90% of final value. T_A = +25°C		0.5	1.25	2.50	mV/µs
POWER STAGE CHARACTERISTICS							
Dropout Voltage	V_{LDO_DO}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.8V, I_{LDO} = 150mA (Note 5)			90	180	mV
Active-Discharge Impedance	R_{AD_LDO}	Regulator disabled, active discharge enabled (ADE_LDO = 1)		50	100	200	Ω
Disabled Output Leakage Current		Regulator disabled, active discharge disabled (ADE_LDO = 0), V_{SYS} = V_{IN_LDO} = 5.5V, V_{LDO} = 5.5V and 0V	T_A = +25°C (Note 7)		+0.1	+1.0	µA
			T_A = +85°C		+1.0		
Dropout On-Resistance	R_{DSON}	V_{SYS} = 3.7V, 1.85V programmed output voltage (TV_LDO[6:0] = 0x20), V_{IN_LDO} = 1.8V, I_{LDO} = I_{MAX}, (Note 5)	T_A = +25°C		0.6	0.9	Ω
			T_A = +85°C			1.2	

Note 5: Dropout is the condition where the input voltage is in its valid input range but the output cannot be properly regulated because the input voltage is not sufficiently higher than the output voltage. The dropout voltage is the difference between the input voltage and the output voltage when the regulator is in dropout. The dropout on-resistance is the resistance of the power MOSFET between the input and the output when the regulator is in dropout. Generally speaking, applications should avoid dropout by having sufficient input voltage. A dropout detection interrupt is available (DOD_R; see the *Programmer's Guide* for more information). For example, applications with the output voltage target of 1.85V and the maximum load current is 80mA (ILDO_MAX), has a dropout voltage of 96mV (V_{LDO_DO} = ILDO_MAX x RDSON_LDO = 80mA x 1.2Ω = 96mV). To avoid dropout, the input voltage should be 1.95V (V_{IN_LDO} = V_{LDO} + V_{LDO_DO}).

Note 6: Guaranteed by design and characterization but not directly production tested. Production test coverage is provided by the shutdown supply current and quiescent supply current specification in the *Electrical Characteristics—Top Level* table.

Note 7: Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

Electrical Characteristics—Current Sinks

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Current Sink Quiescent Current	I_Q	Change in supply current at SYS when one channel is enabled and delivering 12.8mA, V_{LEDx} = 0.2V			6	12	µA
Current Sink Leakage		All current sink drivers combined, outputs disabled, V_{LEDx} = 5.5V	T_A = +25ºC		+0.1	+1.0	µA
			T_A = +85ºC		+1.0		
3.2mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b01, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.1		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			3.2		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.1		mA
Current Sink Accuracy		T_A = +25ºC		3.10	3.20	3.25	mA
		T_A = -40ºC to +85ºC		3.03	3.20	3.36	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 2.9mA			35	70	mV
6.4mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b10, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.2		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			6.4		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.2		mA
Current Sink Accuracy		T_A = +25ºC		6.30	6.40	6.50	mA
		T_A = -40ºC to +85ºC		6.06	6.40	6.72	
Dropout Voltage	V_{DO}	LED_FSx[1:0] = 0b11, BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 5.75mA			35	70	mV
12.8mA CURRENT SINK RANGE (LED_FSx[1:0] = 0b11, VLEDx = 0.2V)							
Minimum Sink Current		BRT_LEDx[4:0] = 0b00000			0.4		mA
Maximum Sink Current		BRT_LEDx[4:0] = 0b11111			12.8		mA
Current Sink DAC Bits					5		bits
Current Sink DAC LSB					0.4		mA
Current Sink Accuracy		T_A = +25ºC		12.6	12.8	13.0	mA
		T_A = -40ºC to +85ºC		12.16	12.80	13.44	
Dropout Voltage	V_{DO}	BRT_LEDx[4:0] = 0b11111, I_{LEDx} = 11.5mA			35	70	mV
TIMING CHARACTERISTICS							
Root Clock Frequency				25.6	32.0	38.4	Hz

Electrical Characteristics—Current Sinks (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS/BLINK PERIOD SETTINGS						
Minimum Blink Period				0.5		s
				16		clocks
Maximum Blink Period				8		s
				256		clocks
Blink Period LSB				0.5		s
				16		clocks
TIMING CHARACTERISTICS/BLINK DUTY CYCLE						
Minimum Blink Duty Cycle		D_LEDx[3:0] = 0b0000		6.25		%
Maximum Blink Duty Cycle		D_LEDx[3:0] = 0b1111		100		%
Blink Duty Cycle LSB				6.25		%

Electrical Characteristics—I²C Serial Interface

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 2)	t_{OF}				120	ns

Electrical Characteristics—I²C (continued)

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST MODE PLUS) (Note 8)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 100pF) (Note 8)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Electrical Characteristics—I²C (continued)

(V_{SYS} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

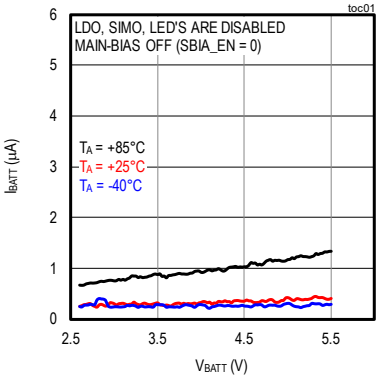
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (Note 8)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 8: Design guidance only. Not production tested.

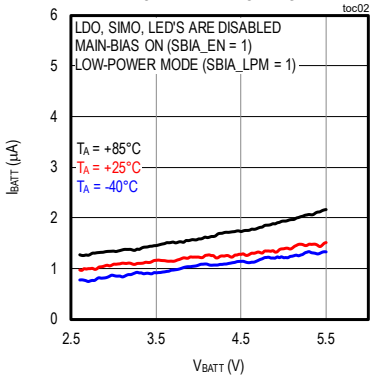
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, unless otherwise noted.)

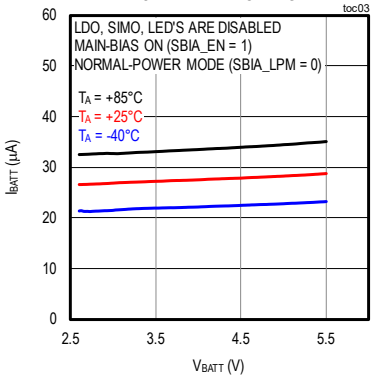
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



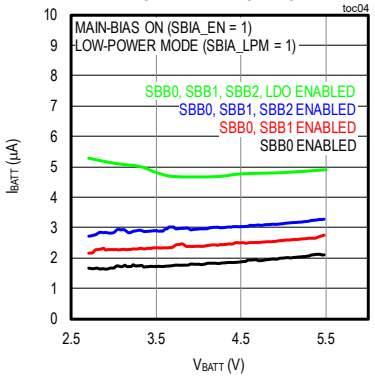
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



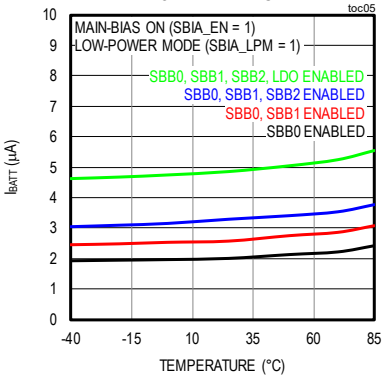
SHUTDOWN SUPPLY CURRENT vs. BATTERY VOLTAGE



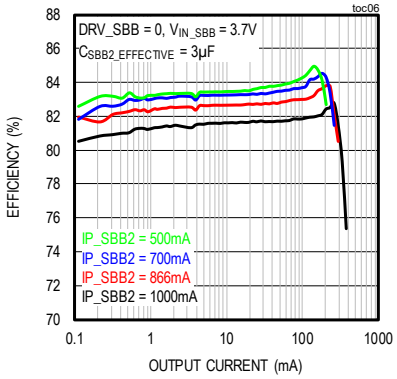
QUIESCENT SUPPLY CURRENT vs. BATTERY VOLTAGE



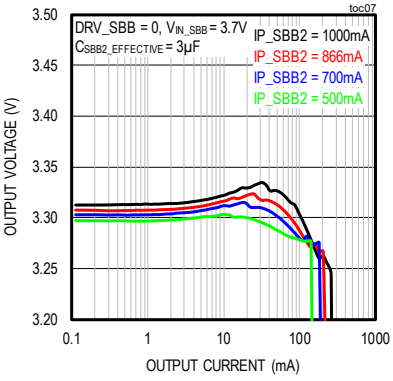
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



SBB2 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB2} = 3.3V, PER PEAK CURRENT LIMIT)



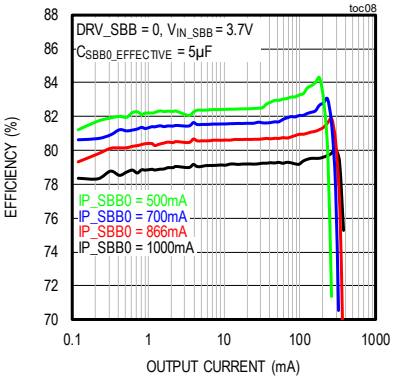
SBB2 LOAD REGULATION (V_{SBB2} = 3.3V, PER PEAK CURRENT LIMIT)



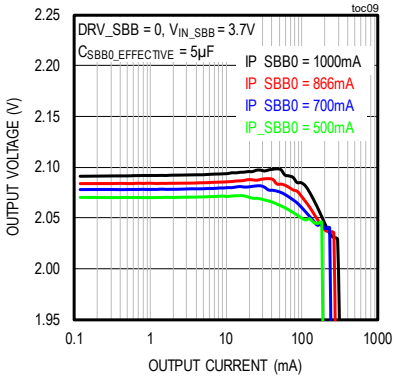
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 2.2µF (TOKO DFE201210S-2R2M, 127mΩ, 2.0mm x 1.2mm x 1.0mm), T_A = +25°C, unless otherwise noted.)

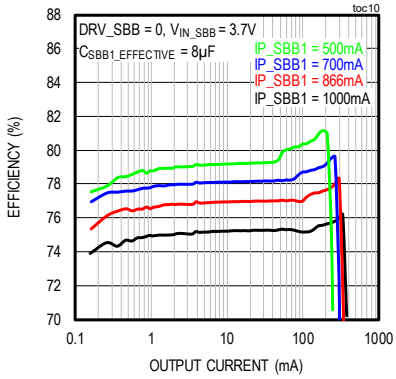
SBB0 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB0} = 2.05V, PER PEAK CURRENT LIMIT)



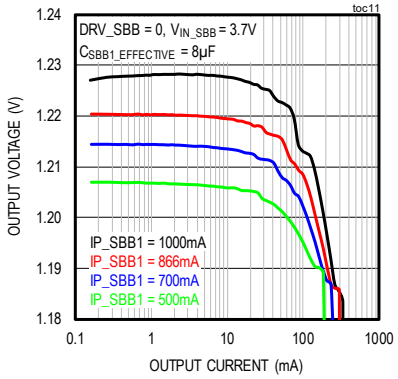
SBB0 LOAD REGULATION (V_{SBB0} = 2.05V, PER PEAK CURRENT LIMIT)



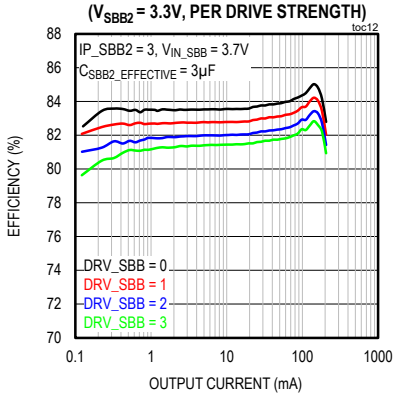
SBB1 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB1} = 1.2V, PER PEAK CURRENT LIMIT)



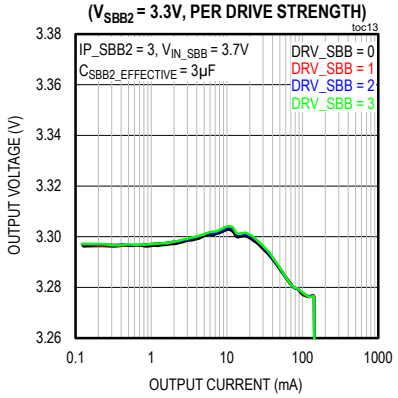
SBB1 LOAD REGULATION (V_{SBB1} = 1.2V, PER PEAK CURRENT LIMIT)



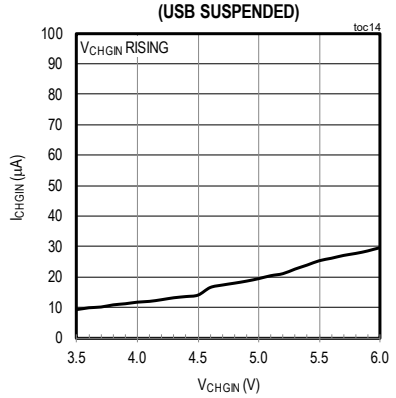
SBB2 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB2} = 3.3V, PER DRIVE STRENGTH)



SBB2 LOAD REGULATION (V_{SBB2} = 3.3V, PER DRIVE STRENGTH)



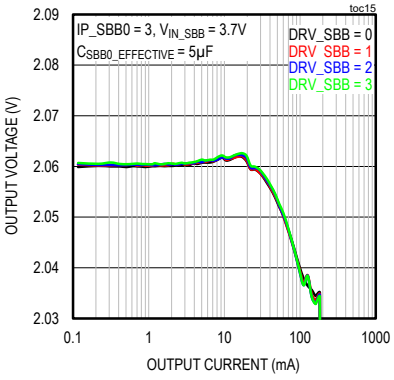
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE (USB SUSPENDED)



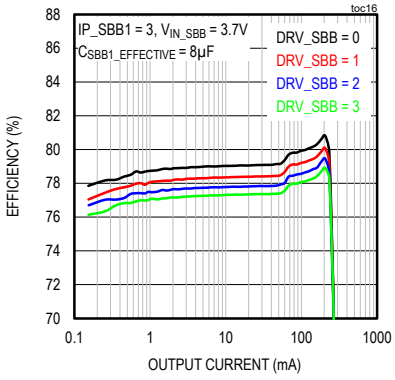
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 2.2µF (TOKO DFE201210S-2R2M, 127mΩ, 2.0mm x 1.2mm x 1.0mm), T_A = +25°C, unless otherwise noted.)

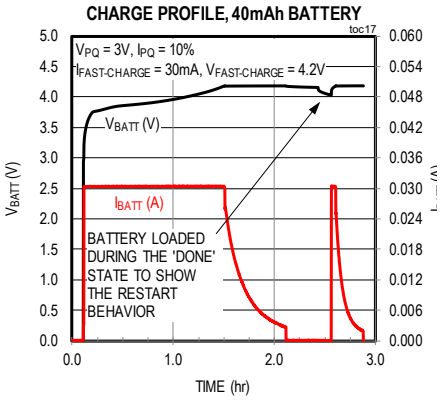
SBB0 LOAD REGULATION
(V_{SBB0} = 2.05V, PER DRIVE STRENGTH)



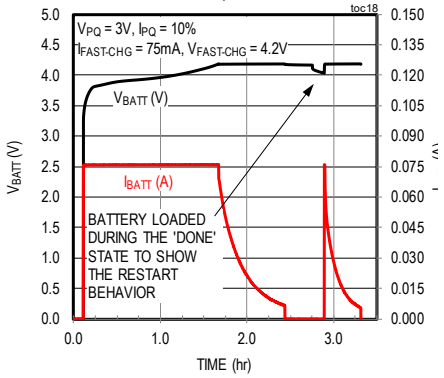
SBB1 EFFICIENCY vs. OUTPUT CURRENT
(V_{SBB1} = 1.2V, PER DRIVE STRENGTH)



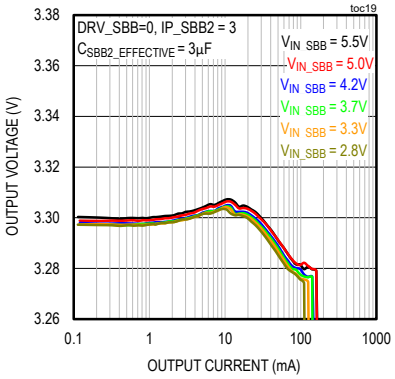
CHARGE PROFILE, 40mAh BATTERY



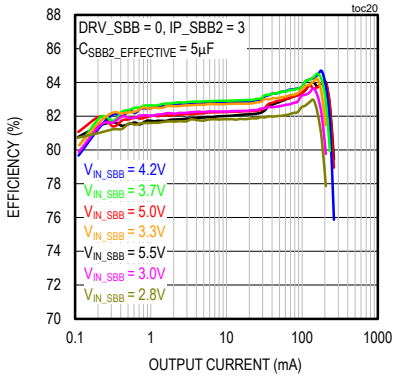
CHARGE PROFILE, 110mAh BATTERY



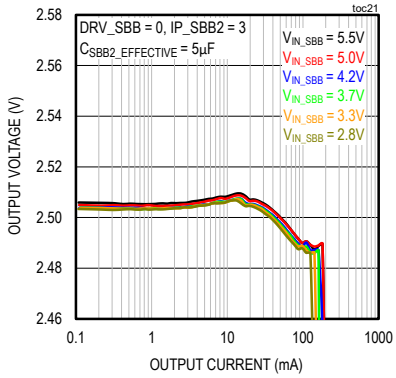
SBB2 LOAD REGULATION
(V_{SBB2} = 3.3V, PER INPUT VOLTAGE)



SBB2 EFFICIENCY vs. OUTPUT CURRENT
(V_{SBB2} = 2.5V, PER INPUT VOLTAGE)



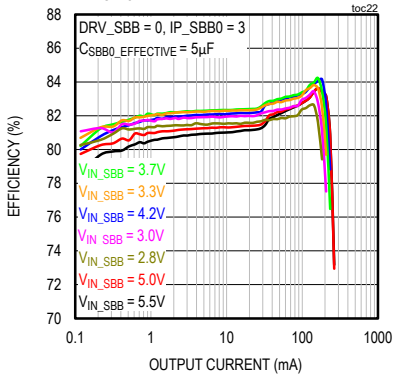
SBB2 LOAD REGULATION
(V_{SBB2} = 2.5V, PER INPUT VOLTAGE)



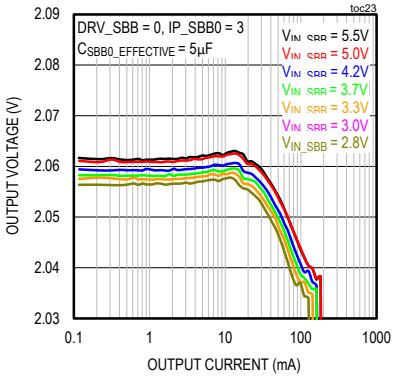
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 2.2µF (TOKO DFE201210S-2R2M, 127mΩ, 2.0mm x 1.2mm x 1.0mm), T_A = +25°C, unless otherwise noted.)

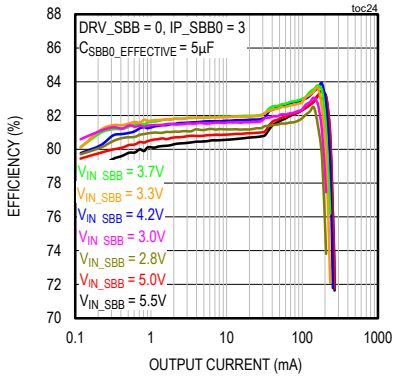
SBB0 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB0} = 2.05V, PER INPUT VOLTAGE)



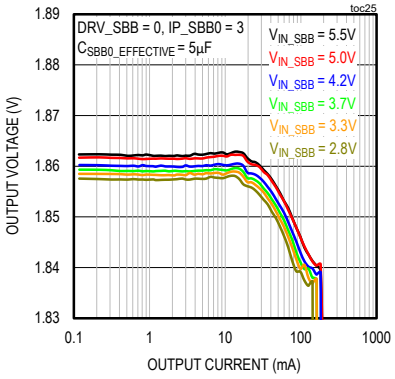
SBB0 LOAD REGULATION (V_{SBB0} = 2.05V, PER INPUT VOLTAGE)



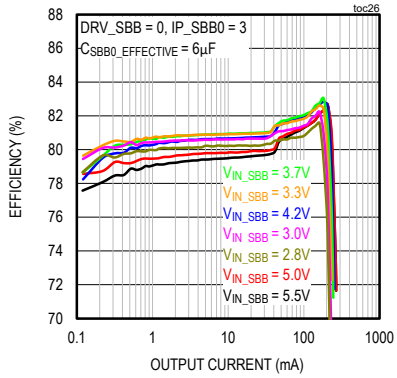
SBB0 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB0} = 1.85V, PER INPUT VOLTAGE)



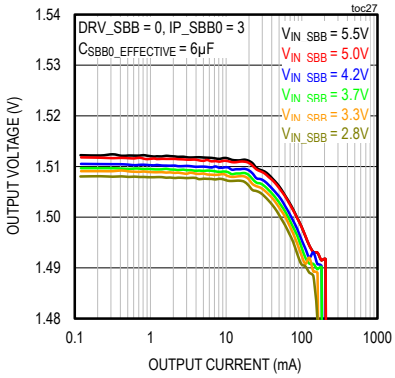
SBB0 LOAD REGULATION (V_{SBB0} = 1.85V, PER INPUT VOLTAGE)



SBB0 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB0} = 1.5V, PER INPUT VOLTAGE)



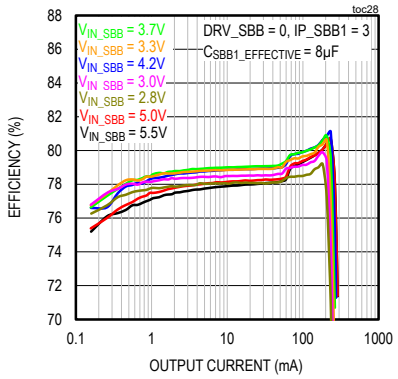
SBB0 LOAD REGULATION (V_{SBB0} = 1.5V, PER INPUT VOLTAGE)



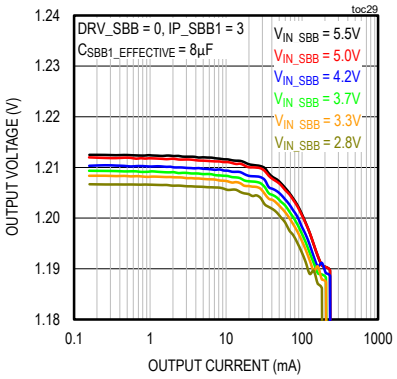
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 2.2µF (TOKO DFE201210S-2R2M, 127mΩ, 2.0mm x 1.2mm x 1.0mm), T_A = +25°C, unless otherwise noted.)

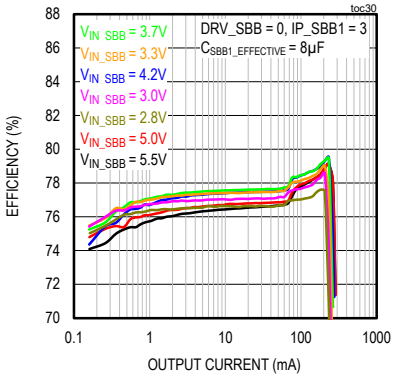
SBB1 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB1} = 1.2V, PER INPUT VOLTAGE)



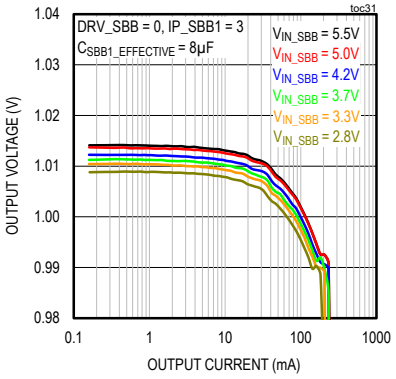
SBB1 LOAD REGULATION (V_{SBB1} = 1.2V, PER INPUT VOLTAGE)



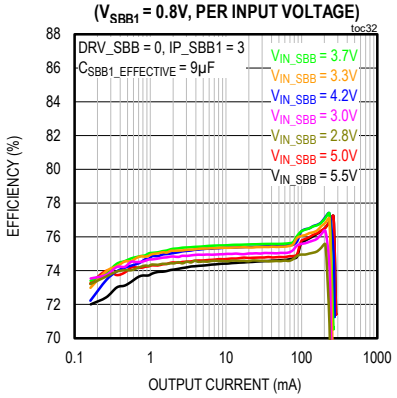
SBB1 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB1} = 1.0V, PER INPUT VOLTAGE)



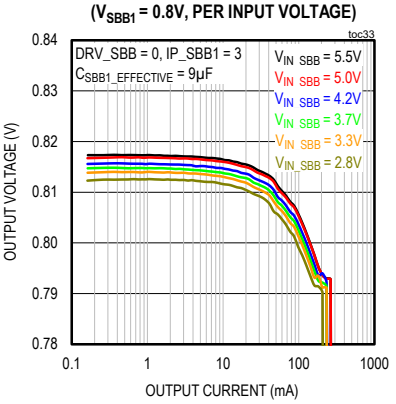
SBB1 LOAD REGULATION (V_{SBB1} = 1.0V, PER INPUT VOLTAGE)



SBB1 EFFICIENCY vs. OUTPUT CURRENT (V_{SBB1} = 0.8V, PER INPUT VOLTAGE)



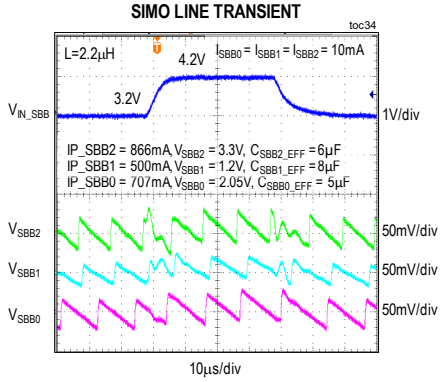
SBB1 LOAD REGULATION (V_{SBB1} = 0.8V, PER INPUT VOLTAGE)



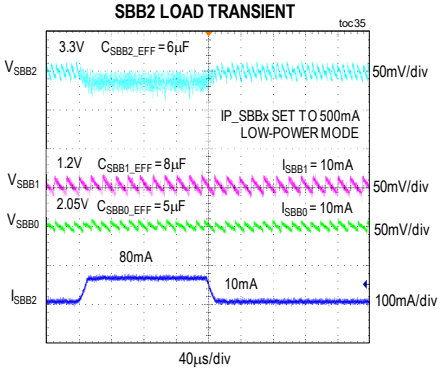
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 1.5µF, T_A = +25°C, unless otherwise noted.)

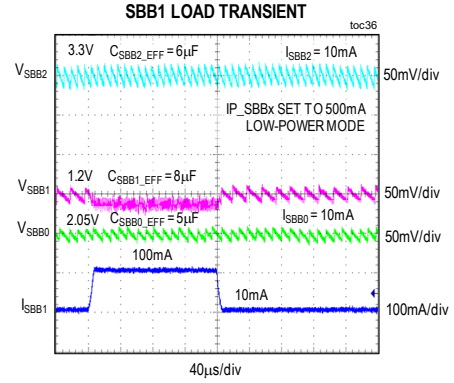
SIMO LINE TRANSIENT



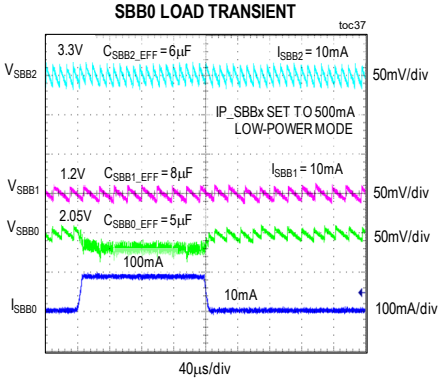
SBB2 LOAD TRANSIENT



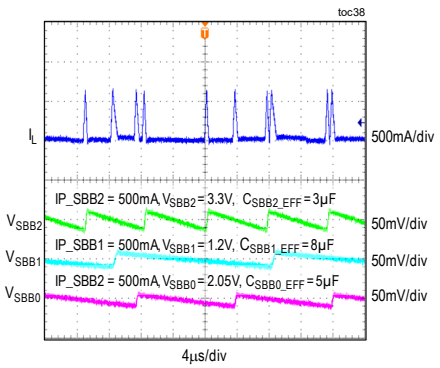
SBB1 LOAD TRANSIENT



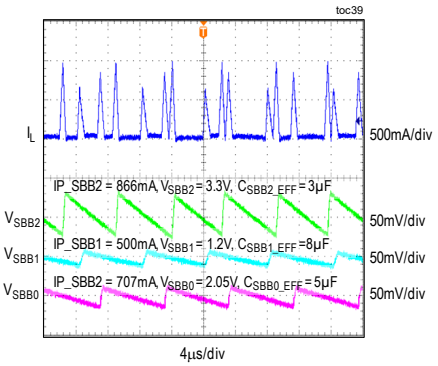
SBB0 LOAD TRANSIENT



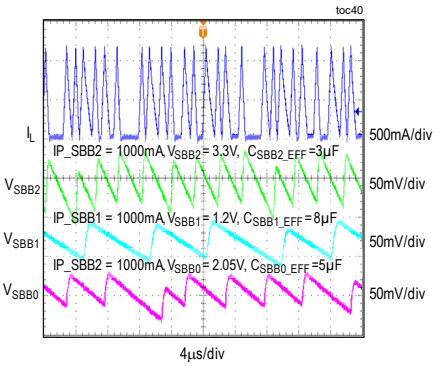
SIMO SWITCHING WAVEFORMS LIGHT UTILIZATION 10mA PER CHANNEL



SIMO SWITCHING WAVEFORMS MEDIUM UTILIZATION 25mA PER CHANNEL



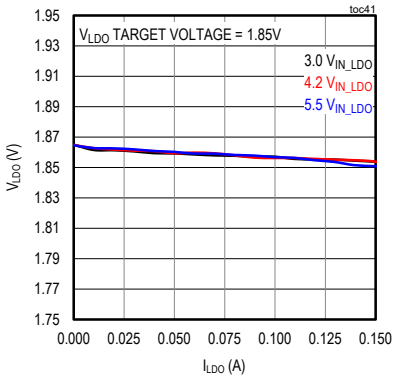
SIMO SWITCHING WAVEFORMS HEAVY UTILIZATION 75mA PER CHANNEL



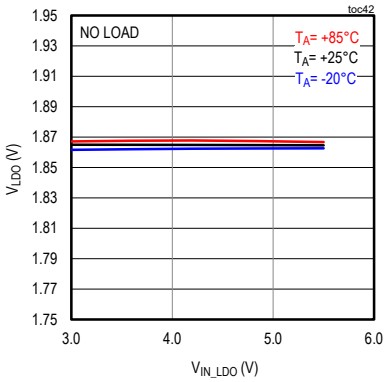
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 1.5µF, T_A = +25°C, unless otherwise noted.)

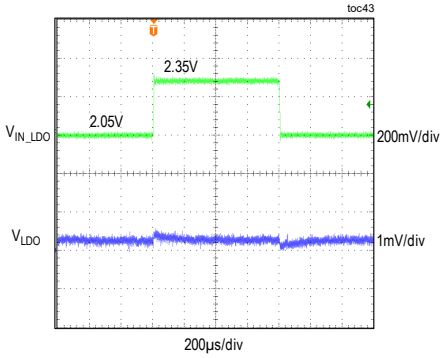
LDO LOAD REGULATION



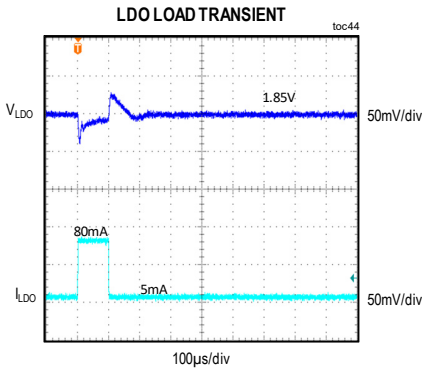
LDO LINE REGULATION



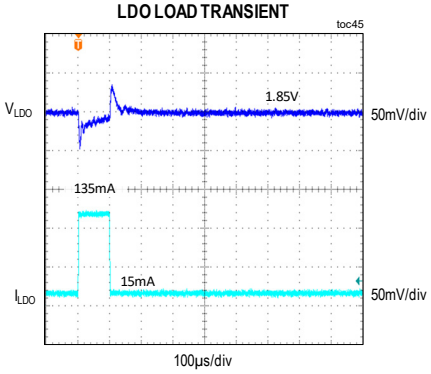
LDO LINE TRANSIENT



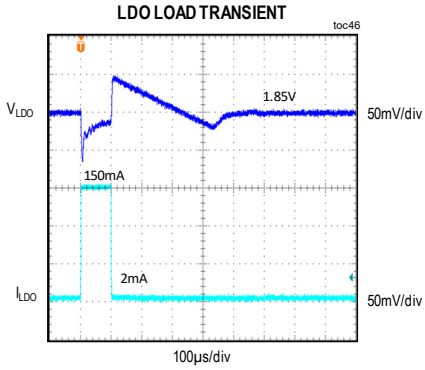
LDO LOAD TRANSIENT



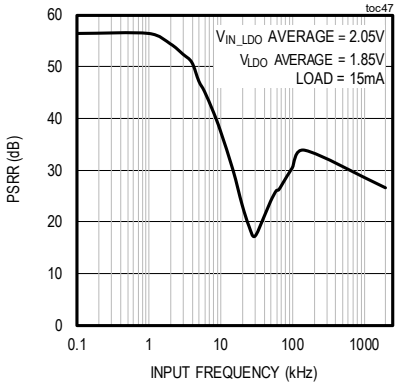
LDO LOAD TRANSIENT



LDO LOAD TRANSIENT



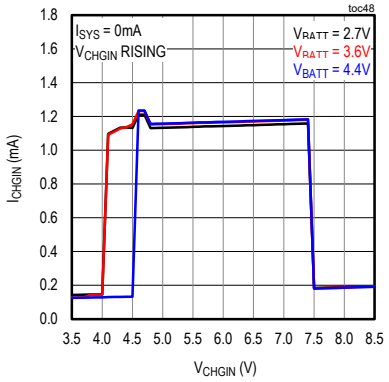
LDO POWER-SUPPLY REJECTION RATIO



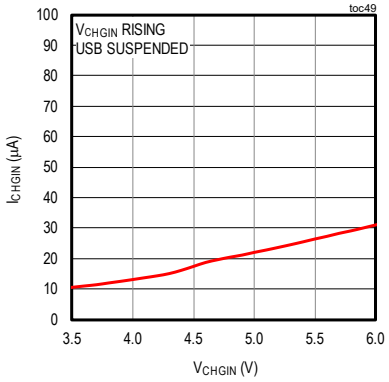
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 1.5µF, T_A = +25°C, unless otherwise noted.)

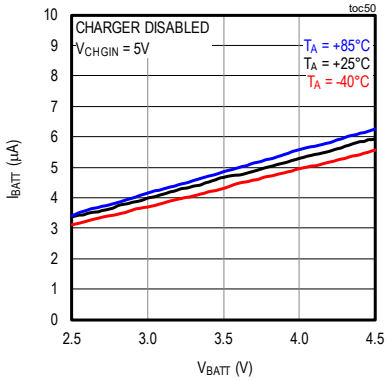
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE



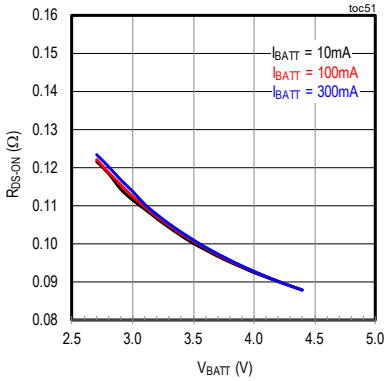
CHGIN SUPPLY CURRENT vs. CHGIN VOLTAGE



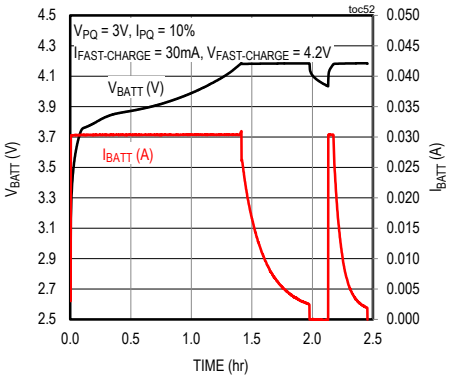
BATT BIAS CURRENT vs. BATT



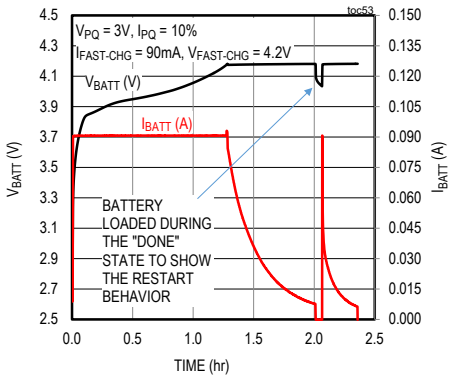
SYS TO BATT IMPEDANCE



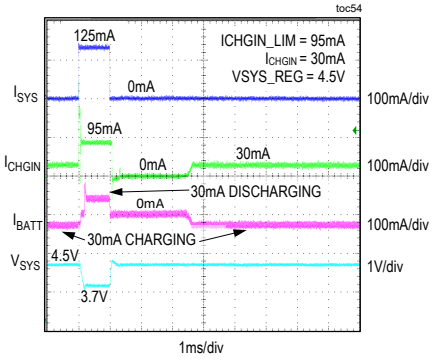
CHARGE PROFILE, 40mAh BATTERY



CHARGE PROFILE, 110mAh BATTERY



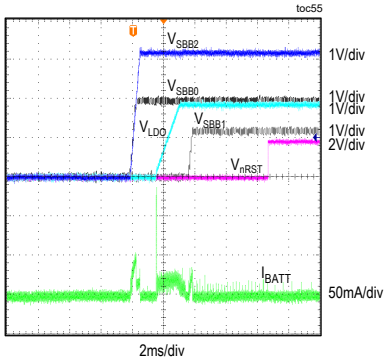
SYS LOAD TRANSIENT CAUSING BATTERY SUPPLEMENT



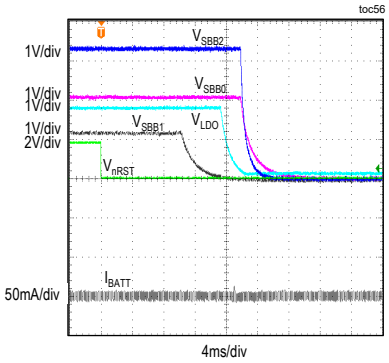
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = 3.7V, V_{BATT} = 3.7V, V_{IO} = 1.8V, L = 1.5µF, T_A = +25°C, unless otherwise noted.)

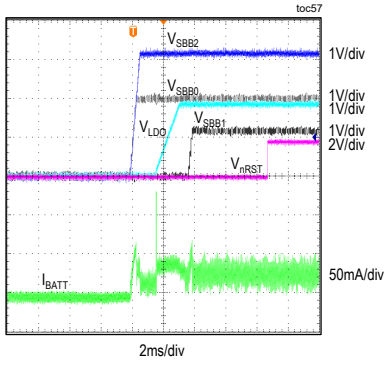
POWER UP
NO LOAD



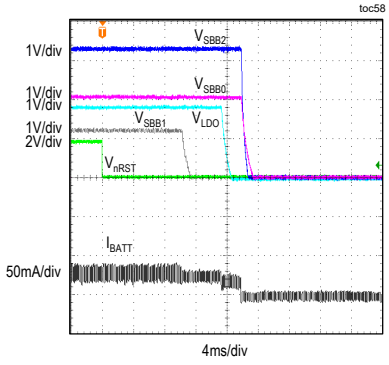
POWER DOWN
NO LOAD



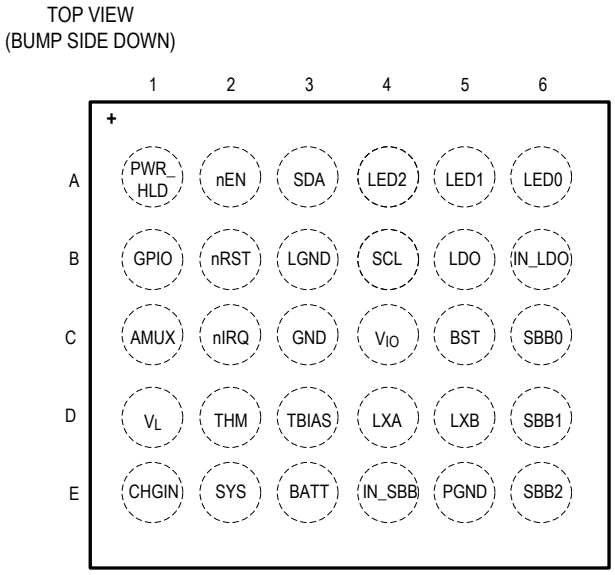
POWER UP
10mA LOAD PER CHANNEL



POWER DOWN
10mA LOAD PER CHANNEL



Pin Configuration



WLP
(2.75mm x 2.15mm)

Bump Description

PIN	NAME	FUNCTION	TYPE
TOP LEVEL			
A2	nEN	Active-Low Enable Input. nEN supports push-button or slide-switch configurations. An external pullup resistor (10kΩ to 100kΩ) to SYS is required.	digital input
C2	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between nIRQ and a voltage equal to or less than V_{SYS}.	digital output
B2	nRST	Active-Low, Open-Drain Reset Output. Connect a 100kΩ pullup resistor between nRST and a voltage equal to or less than V_{SYS}.	digital output
A1	PWR_HLD	Active-High Power Hold Input. Assert PWR_HLD to keep the on/off controller in its on through on/off controller state. If PWR_HLD is not needed, connect it to SYS and use the SFT_RST bits to power down the device.	digital input
B1	GPIO	General-Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}.	digital I/O
C4	V_{IO}	I^2C Interface and GPIO Driver Power	power input
B4	SCL	I^2C Clock	digital input
A3	SDA	I^2C Data	digital I/O
C3	GND	Quiet Ground. Connect GND to PGND, LGND, and the low-impedance ground plane of the PCB.	ground

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
CHARGER			
E1	CHGIN	Charger Input. Connect to a DC charging source. Bypass to GND with a 4.7µF ceramic capacitor.	power input
E2	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the device. Connect SYS to IN_SBB and bypass to GND with a 22µF ceramic capacitor.	power output
E3	BATT	Li+ Battery Connection. Connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.	power I/O
D1	V_L	Internal Charger 3V Logic Supply Powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load V_L externally.	power
D3	TBIAS	Thermistor Bias Supply. Connect a resistor equal to the NTC's room temperature resistance between TBIAS and THM. Do not load TBIAS with any other external circuitry.	analog
D2	THM	Thermistor Monitor. Thermally couple an NTC to the battery and connect between THM and GND.	analog input
C1	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals.	analog output
LDO			
B5	LDO	Linear Regulator Output	power output
B6	IN_LDO	Linear Regulator Input	power input
RGB LED DRIVER			
A6	LED0	Current Sink Port 0. LED0 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
A5	LED1	Current Sink Port 1. LED1 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
A4	LED2	Current Sink Port 2. LED2 is typically connected to the cathode of an LED and is capable of sinking up to 12.5mA. Connect to ground if unused.	power
B3	LGND	Current Sink Ground. Connect LGND to GND, PGND, and the low-impedance ground plane of the PCB.	ground
SIMO BUCK BOOST			
E4	IN_SBB	SIMO Power Input. Connect IN_SBB to SYS and bypass to PGND with a 10uF ceramic capacitor as close as possible to the IN_SBB pin.	power input
C6	SBB0	SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 10µF ceramic capacitor.	power output
D6	SBB1	SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 10µF ceramic capacitor.	power output
E6	SBB2	SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck-boost. Bypass SBB2 to PGND with a 10µF ceramic capacitor.	power output
C5	BST	SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 3300pF ceramic capacitor between BST and LXB.	power input
D4	LXA	Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power I/O
D5	LXB	Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	power I/O
E5	PGND	Power ground for the SIMO low-side FETs. Connect PGND to GND, LGND, and the low-impedance ground plane of the PCB.	ground

Detailed Description

The MAX77650/MAX77651 provide a highly-integrated battery charging and power management solution for low-power applications. The linear charger provides a wide range of charge current and charger termination voltage options to charge various Li+ batteries. Temperature monitoring and JEITA compliance settings add additional functionality and safety to the charger. Four regulators are integrated within this device (see Table 1). A single-inductor, multiple output (SIMO) buck-boost regulator efficiently provides three independently programmable power rails. A 150mA LDO provides ripple rejection for audio and other low-noise applications.

The system includes other features such as current sinks for driving LED indicators and an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I^2C serial interface allows for configuring and checking the status of the device. An internal on/off controller provides regulator sequencing and supervisory functionality for the device.

Support Materials

Support materials are available to assist engineering teams in designing with this device. For example, a full description of the register bits along with software advice is available in the *Programmer's Guide*. Visit the product page at **www.maximintegrated.com/MAX77650** and/or *contact Maxim* for more information on support documents.

Top-Level Interconnect Simplified Diagram

Figure 1 shows the same major blocks as the *Typical Application Circuit* with an increased emphasis on the routing between each block. This diagram is intended to familiarize the user with the landscape of the device. Many of the details associated with these signals are discussed throughout the data sheet. At this stage of the data sheet, note the addition of the main bias and clock block that are not shown in the *Typical Applications Circuit*. The main bias and clock block provides voltage, current, and clock references for other blocks as well as many resources for the top-level digital control.

Table 1. Regulator Summary

REGULATOR NAME	REGULATOR TOPOLOGY	MAXIMUM I_{OUT} (mA)	V_{IN} RANGE (V)	MAX77650 V_{OUT} RANGE/ RESOLUTION	MAX77651 V_{OUT} RANGE/ RESOLUTION
SBB0	SIMO	Up to 300*	2.7 to 5.5	0.8V to 2.375V in 25mV steps	0.8 to 2.375V in 25mV steps
SBB1	SIMO	Up to 300*	2.7 to 5.5	0.8V to 1.5875V in 12.5mV steps	2.4 to 5.25V in 50mV steps
SBB2	SIMO	Up to 300*	2.7 to 5.5	0.8V to 3.95V in 50mV steps	2.4 to 5.25V in 50mV steps
LDO	PMOS LDO	150	1.8 to 5.5	1.35V to 2.9375V in 12.5mV steps	1.35 to 2.9375V in 12.5mV steps

**Shared capacity with other SBBx channels. See the SIMO Available Output Current section for more information.*

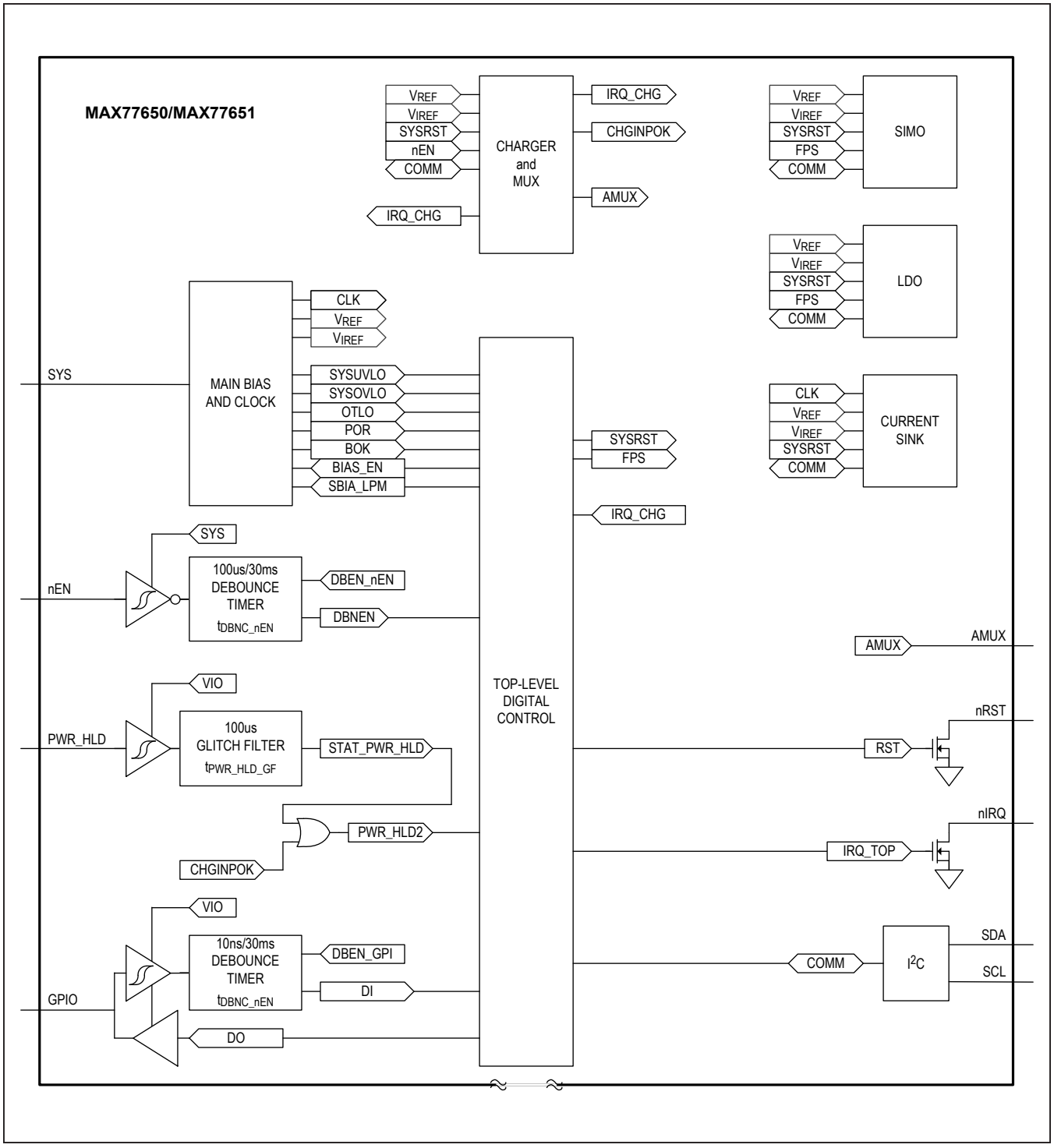


Figure 1. Top-Level Interconnect Simplified Diagram

Global Resources

The global resources encompass a set of circuits that serve the entire device and ensure safe, consistent, and reliable operation.

Features and Benefits

- Voltage Monitors
  - SYS POR (power-on-reset) comparator generates a reset signal upon power-up
  - SYS undervoltage ensures repeatable behavior when power is applied to and removed from the device
  - SYS overvoltage monitor inhibits operation with overvoltage power sources to ensure reliability in faulty environments
- Thermal Monitors
  - 165°C junction temperature shutdown
- Manual Reset
  - 8s or 16s period
- Wakeup Events
  - Charger insertion (with 120ms debounce)
  - nEN input assertion
- Interrupt Handler
  - Interrupt output (nIRQ)
  - All interrupts are maskable
- Push-button/Slide-Switch Onkey (nEN)
  - Configurable push-button/slide-switch functionality
  - 100µs or 30ms debounce timer interfaces directly with mechanical switches
- On/Off Controller
  - Startup/shut-down sequencing
  - Programable sequencing delay
- PWR_HLD, GPIO, RST Digital I/Os

Voltage Monitors

The device monitors the system voltage (V_{SYS}) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

SYS POR Comparator

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

SYS Undervoltage Lockout Comparator

The SYS undervoltage lockout (UVLO) comparator monitors V_{SYS} and generates a SYSUVLO signal when the V_{SYS} falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See Figure 4 and Table 2 for additional information regarding the UVLO comparator:

- When the device is in the STANDBY state, the UVLO comparator is disabled.
- When transitioning out of the STANDBY state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If the device has sufficient input voltage, it can transition to the on state; if there is insufficient input voltage, the device transitions back to the STANDBY state.

SYS Overvoltage Lockout Comparator

The device is rated for 5.5V maximum operating voltage (V_{SYS}) with an absolute maximum input voltage of 6.0V. An overvoltage lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than $V_{SYSOVLO}$. See Figure 4 and Table 2 for additional information regarding the OVLO comparator:

- When the device is in the STANDBY state, the OVLO comparator is disabled.

nEN Enable Input

nEN is an active-low internally debounced digital input that typically comes from the system's on key. The debounce time is programmable with DBEN_nEN. The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the regulators. Maskable rising/falling interrupts are available for nEN (nEN_R and nEN_F) for alternate functionality. nEN requires an external pullup resistor (10kΩ to 100kΩ) to SYS.

The nEN input can be configured to work either with a push-button (nEN_MODE = 0) or a slide-switch (nEN_MODE = 1). See Figure 2 for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

nEN Manual Reset

nEN works as a manual reset input when the on/off controller is in the on via on/off controller state. The manual reset function is useful for forcing a power-down in case the communication with the processor fails. When nEN is configured for a push-button mode and the input is asserted (nEN = low) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode. When nEN is configured for a slide-switch mode and the input is deasserted (nEN = high) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to standby mode.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_nEN}) and 16s (t_{MRST}) timers for nEN. Whenever the device is actively counting either of these times, the

supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away.

nEN Dual-functionality: Push-Button vs. Slide-Switch

The nEN digital input can be configured to work with a push-button switch or a slide-switch. The timing diagram below shows nEN's dual functionality for power-on sequencing and manual reset. The default configuration of the device is push-button mode (nEN_MODE = 0) and no additional programming is necessary. Applications that use a slide-switch on-key configuration must set nEN_MODE = 1 within t_{MRST}.

Interrupts (nIRQ)

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in the device's status. Refer to the *Programmer's Guide* for a comprehensive list of all interrupt bits and status registers.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node. nIRQ is the logical NOR of all unmasked interrupt bits in the register map

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

Reset Output (nRST)

nRST is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t_{RSTODD}). During a power-down sequence, the nRST output asserts before any regulator is powered down (t_{RSTOAD}). See Figure 5 for nRST timing.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node.

Power Hold Input (PWR_HLD)

PWR_HLD is an active-high digital input. PWR_HLD has a 100µs glitch filter ($t_{PWR\_HLD\_GF}$). As shown in Figure 1, the output of this glitch filter is logically ORed with the wakeup signal coming from the charger to create a signal called PWR_HLD2 that drives the top-level digital control.

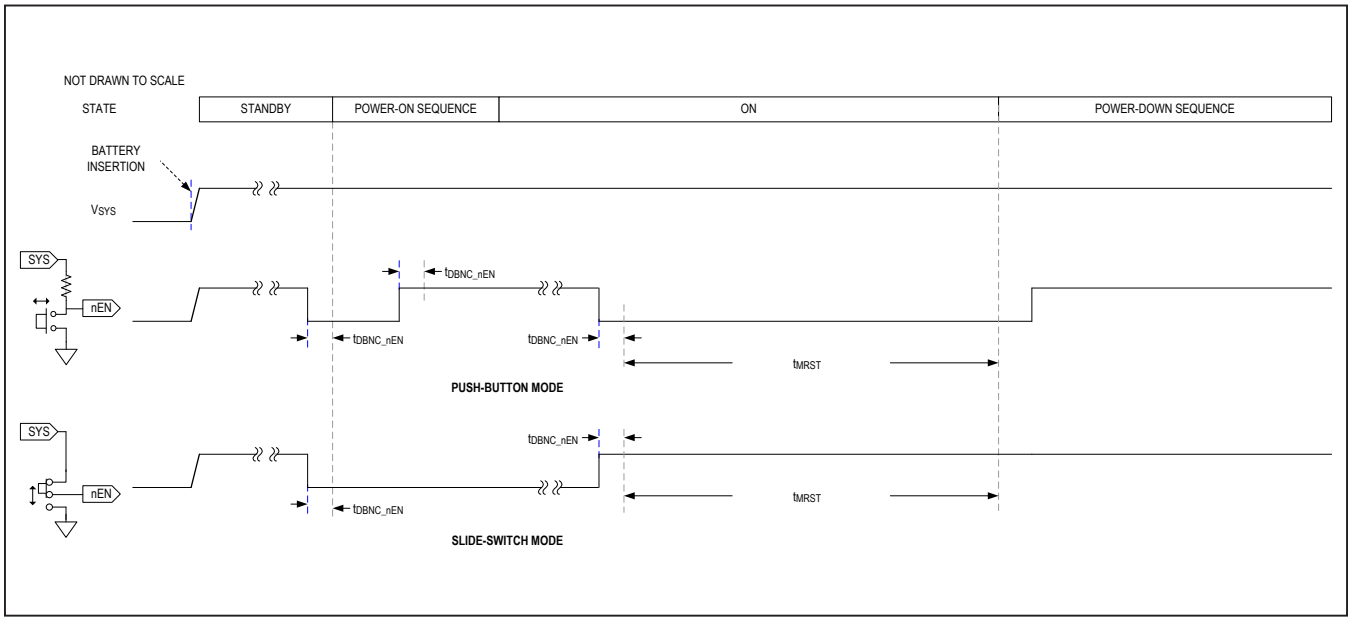


Figure 2. nEN Usage Timing Diagram

- When there is no valid charge voltage at CHGIN (CHGINPOK = 0):
  - After the power-up sequence, the system processor must assert PWR_HLD within the PWR_HLD wait time ($t_{PWR\_HLD\_WAIT}$) to hold the power supply in the on state. If the PWR_HLD input is not asserted within the $t_{PWR\_HLD\_WAIT}$ period, a power-down sequence is initiated.
  - While in the on state, the system processor must assert PWR_HLD as long as power is required. If the system processor wants to turn off, it can either pull PWR_HLD low or it can write the SFT_RST bits to execute the SFT_CRST or SFT_OFF functions to execute the power-down sequence.
- If there is a valid charge voltage at CHGIN (CHGINPOK = 1):
  - The charger sends a wakeup signal to the on/off controller which is also logically ORed with PWR_HLD to assert PWR_HLD2. PWR_HLD2 being asserted satisfies the on/off controller such that the PWR_HLD signal is a don't care.

See the Figure 7, *Top-Level On/Off Controller* section, and Table 2 for additional information regarding PWR_HLD. If the power hold function is not used, connect PWR_HLD to SYS and then use the SFT_RST bits to power the device down.

General-Purpose Input Output (GPIO)

A general-purpose input/output (GPIO) is provided to increase system flexibility. See Figure 3 for the GPIO Block Diagram.

Clear DIR to configure GPIO as a general-purpose output (GPO). The GPO can either be in push-pull mode (DRV = 1) or open-drain mode (DRV = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to V_{IO}.
  - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 1.8V logic domain (V_{IO} = 1.8V) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).

The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the DI (input status) bit still functions properly and does not collide with the state of the DIR bit.

Set DIR to disable the output drivers associated with the GPO and have the device function as a GPI. The GPI features a 30ms debounce timer (t_{DBNC_GPI}) that can be enabled or disabled with DBEN_GPI.

- Enable the debounce timer (DBEN_GPI = 1) if the GPI is connected to a device that can bounce or chatter (like a mechanical switch).
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (DBEN_GPI = 0) to eliminate unnecessary logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_GPI}) debounce timer. Whenever the device is actively counting this time, the supply current increases by the oscillator's supply current (65µA when the battery voltage is at 3.7V). As soon as the event driving the timer goes away or is fulfilled, the oscillator automatically turns off and its supply current goes away.

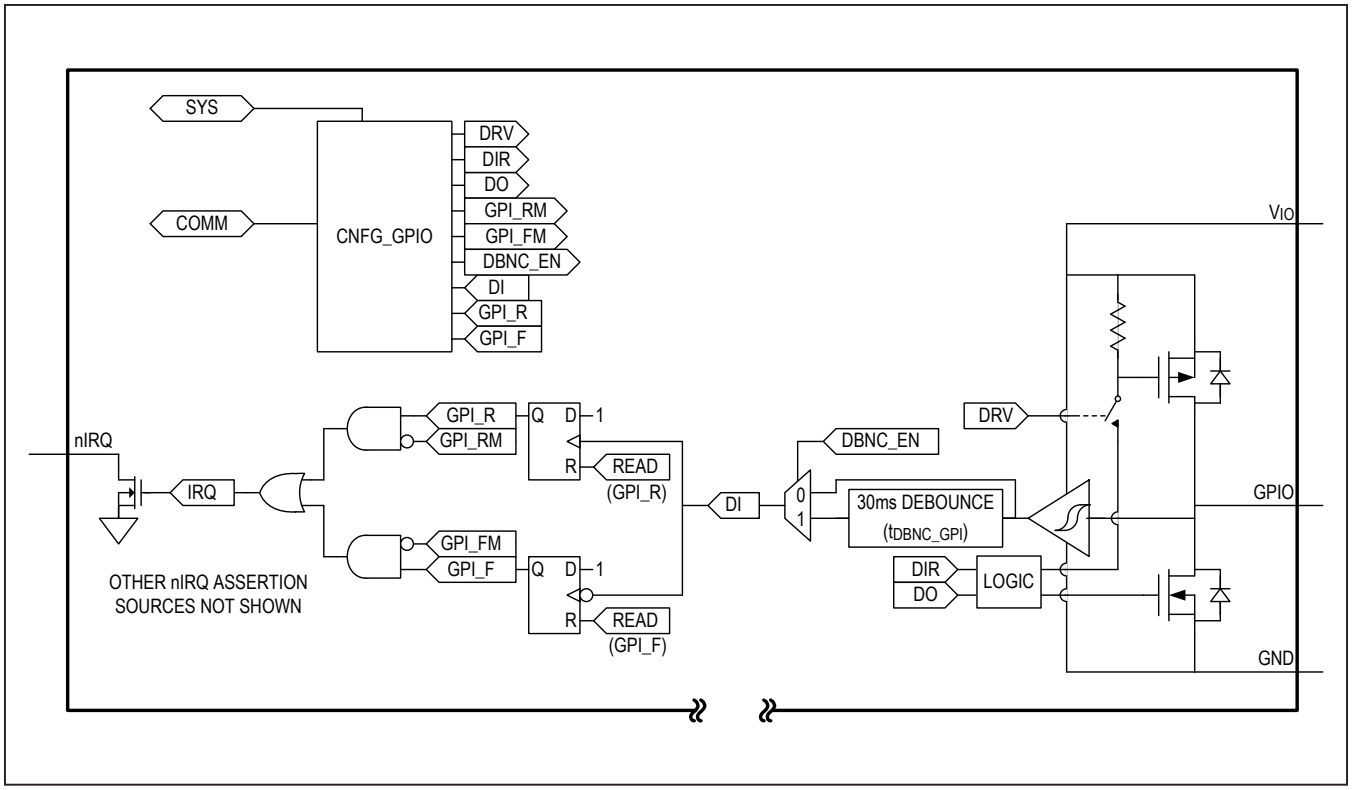


Figure 3. GPIO Block Diagram

Maskable rising and falling interrupts (GPI_R and GPI_F) are available to signal a change in the GPI's status.

- To interrupt on a rising edge only: unmask the rising edge interrupt and mask the falling edge interrupt (GPI_RM = 0, GPI_FM = 1).
- To interrupt on a falling edge only: unmask the falling edge interrupt and mask the rising edge interrupt (GPI_RM = 1, GPI_FM = 0).
- To interrupt on either rising or falling edge: unmask both rising and falling edge interrupts (GPI_RM = 0, GPI_FM = 0). Consult the *Register Map* for more details.

On/Off Controller

The on/off controller monitors multiple power-up (wakeup) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power management controller and one processor and rely on the on/off controller to be the master controller. In this case, the on/off controller receives the wakeup events and enables some or all of the regulators in order to power up a processor. That processor then manages the system. To conceptualize this master operation see Figure 4 and Table 2. A typical path through the on/off controller in master mode is:

- Start in the no power state.
- Apply a battery to the system and transition through path 1 and 2 to the standby state.
- Press the system's on key (nEN = low) and transition through path 3A and 4 to the "PWR_HLD?" state.
- The processor boots up and drives PWR_HLD high, which drives the transition through path 4C to the on through the on/off controller state.
- The device performs its desired functions in the on through on/off controller state. When it is ready to turn off, the processor drives PWR_HLD low that drives the transition through path 5B and 8 to the standby state.

Some systems have several power management blocks, a main processor, and subprocessors. These systems can use this device as a subpower management block for a peripheral portion of circuitry as long as there is an I2C port available from a higher level processor. To conceptualize this slave operation, see Figure 4 and Table 2. A typical path through the on/off controller in slave mode is:

- Start in the no power state.
- Apply a battery to the system and transition through path 1 and 2 to the standby state.
- When the higher level processor wants to turn on this device's resources, it enables the main bias circuits through I2C (SBIA_EN = 1) to transition along path 2A to the on through software state.
- The higher level processor can now control this device's resources with I2C commands (i.e., turn on/off regulators).
- When the higher level processor is ready to turn this device off, it turns off everything through I2C and then disables the main bias circuits through I2C (SBIA_EN = 0) to transition along path 2B to the standby state.

Note that in this slave style of operation, the SFT_RST bits should not be used to turn the device off. The SFT_RST bits establish directives to the on/off controller itself that does not make sense in slave mode. In slave mode, since the I2C commands enable the device's resources, they should also disable them.

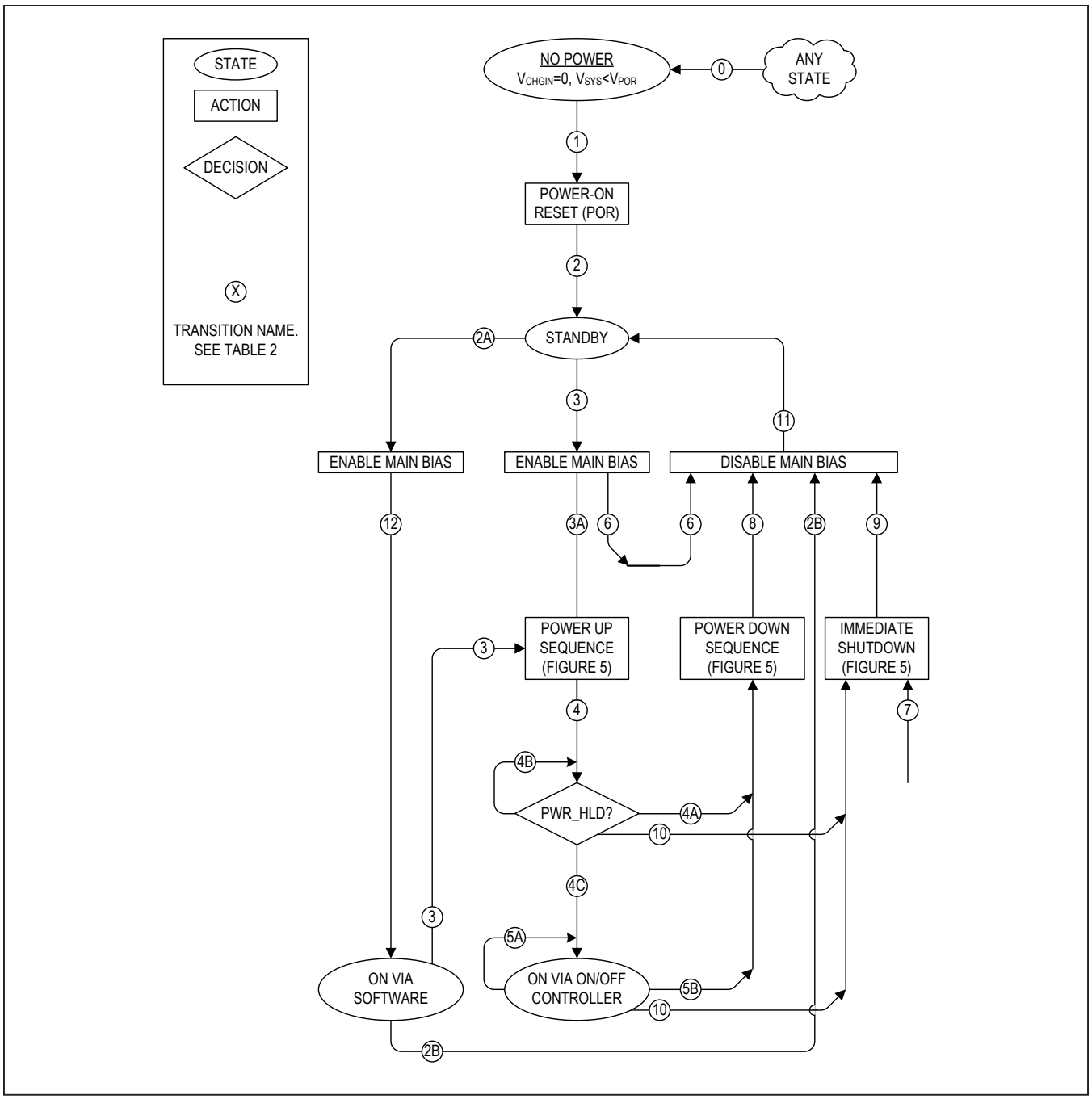


Figure 4. Top-Level On/Off Controller

Table 2. On/Off Controller Transition/State

TRANSITION/STATE	CONDITION
0	System voltage is below the POR threshold (V_{SYS} < V_{POR}).
1	System voltage is above the POR threshold (V_{SYS} > V_{POR}).
2	Internal signals and on-chip memory stabilize and the device is released from reset.
STANDBY	The device is waiting for a wake-up signal or an I²C command to enable the main bias circuits. * This is the lowest current state of the device (I_Q ~0.3µA). * Main bias circuits are off, POR comparator is on. * I²C is on when V_{IO} is valid. * Peripheral functions (LDO, SIMO, LEDs, AMUX) do not operate in this state because the main bias circuits are off. To utilize a function enter the on through software or on through on/off controller states.
2A	Main bias circuits enabled through I²C (SBIA_EN = 1).
2B	Main bias circuits disabled through I²C (SBIA_EN = 0).
ON VIA SOFTWARE*	The main bias circuits are enabled through software and all peripheral functions (LDO, SIMO, LEDs, AMUX) can be manually enabled or disabled through I²C.
3	A wake-up signal has been received. * A debounced onkey (nEN) falling edge has been detected (DBNEN = 1) or * A charge source has been applied and a rising edge on CHGIN has been detected and debounced ($t_{CHGIN-DB}$ ~120ms) or * Internal wake-up flag has been set due to SFT_RST = 0b01 (WKUP = 1)
3A	Main bias circuits are OK (BOK = 1)
4	Power-up sequence complete.
4A	PWR_HLD wait time has expired and PWR_HLD2 is low (t > $t_{PWR\_HLD\_WAIT}$ && PWR_HLD2 = 0).
4B	PWR_HLD wait time has not expired and PWR_HLD2 is low (t < $t_{PWR\_HLD\_WAIT}$ && PWR_HLD2 = 0).
4C	PWR_HLD2 = 1
ON VIA ON/OFF CONTROLLER*	On state. * All flexible power sequencers (FPS) are on. * The main bias circuits are enabled. * I_Q ~5.6µA (typ) with all regulators enabled (no load) and the main bias circuits in low power mode.
5A	PWR_HLD2 = 1
5B	PWR_HLD2 = 0 OR System overtemperature lockout (T_J >T_{OTLO}) or Software cold reset (SFT_RST[1:0] = 0b01) or Software power off (SFT_RST[1:0] = 0b10) or Manual reset occurred. See the *nEN Manual Reset* section for more information.
6	System overtemperature lockout (T_J >T_{OTLO}) or System undervoltage lockout (V_{SYS} < $V_{SYSUVLO}$ + $V_{SYSUVLO\_HYS}$) or System overvoltage lockout (V_{SYS} > $V_{SYSOVLO}$)
7	System undervoltage lockout (V_{SYS} < $V_{SYSUVLO}$) or System overvoltage lockout (V_{SYS} > $V_{SYSOVLO}$) Note: The overvoltage lockout transition does not apply to the ON VIA SOFTWARE state.
8	Finished with the power-down sequence.
9	Finished with immediate shutdown.
10	System overtemperature lockout (T_J > T_{OTLO}).
11	Done disabling main bias.
12	Done enabling main bias.

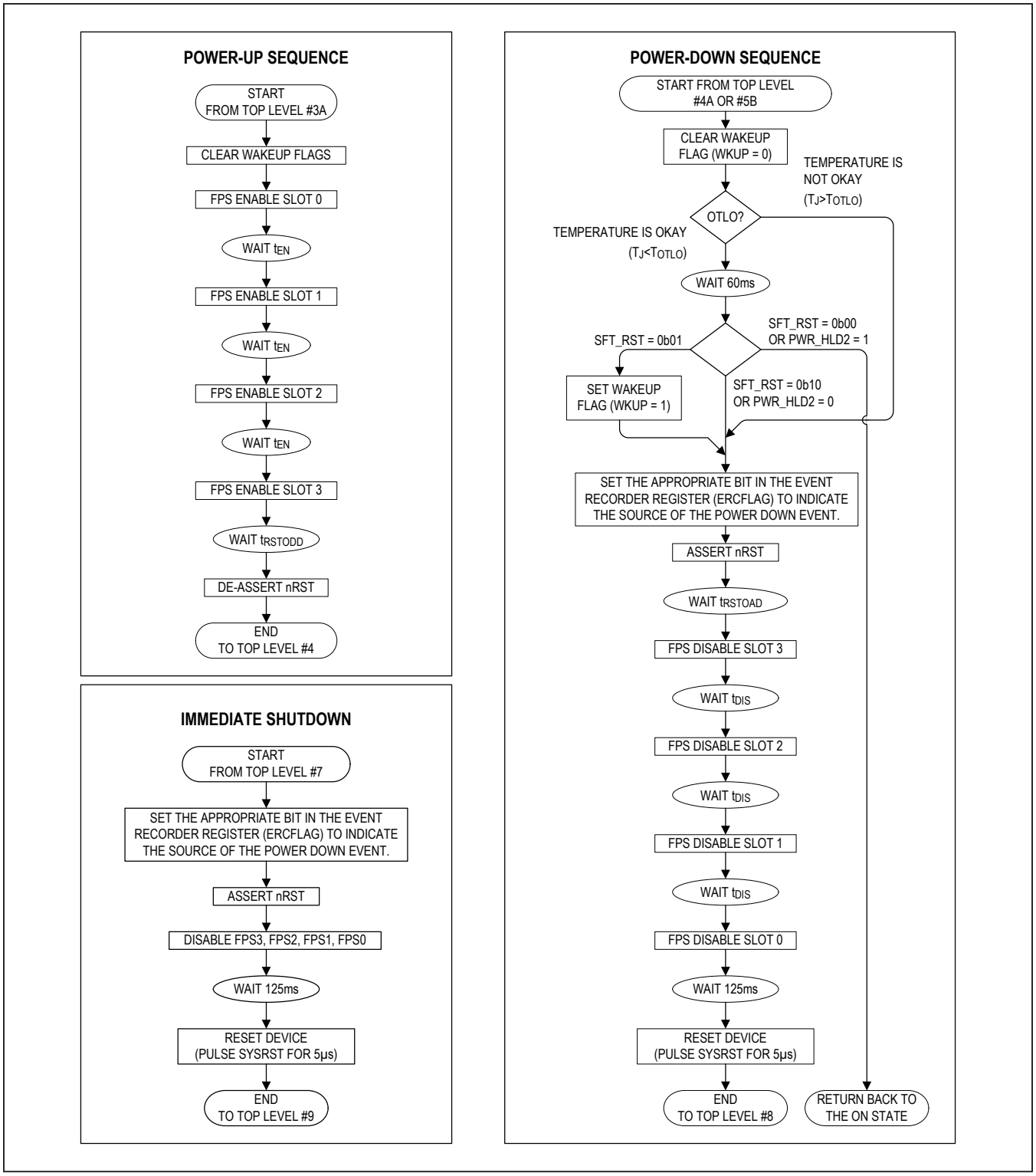


Figure 5. Power-Up/Power-Down Sequence

Flexible Power Sequencer

The flexible power sequencer (FPS) allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up and power-down delays (sequencing). Figure 6 shows four resources powering up under the control of flexible power sequencer.

The flexible sequencing structure consists of 1 master sequencing timer and 4 slave resources (SBB0, SBB1, SBB2, and LDO). When the FPS is enabled, a master timer generates four sequencing events for device power-up and power-down.

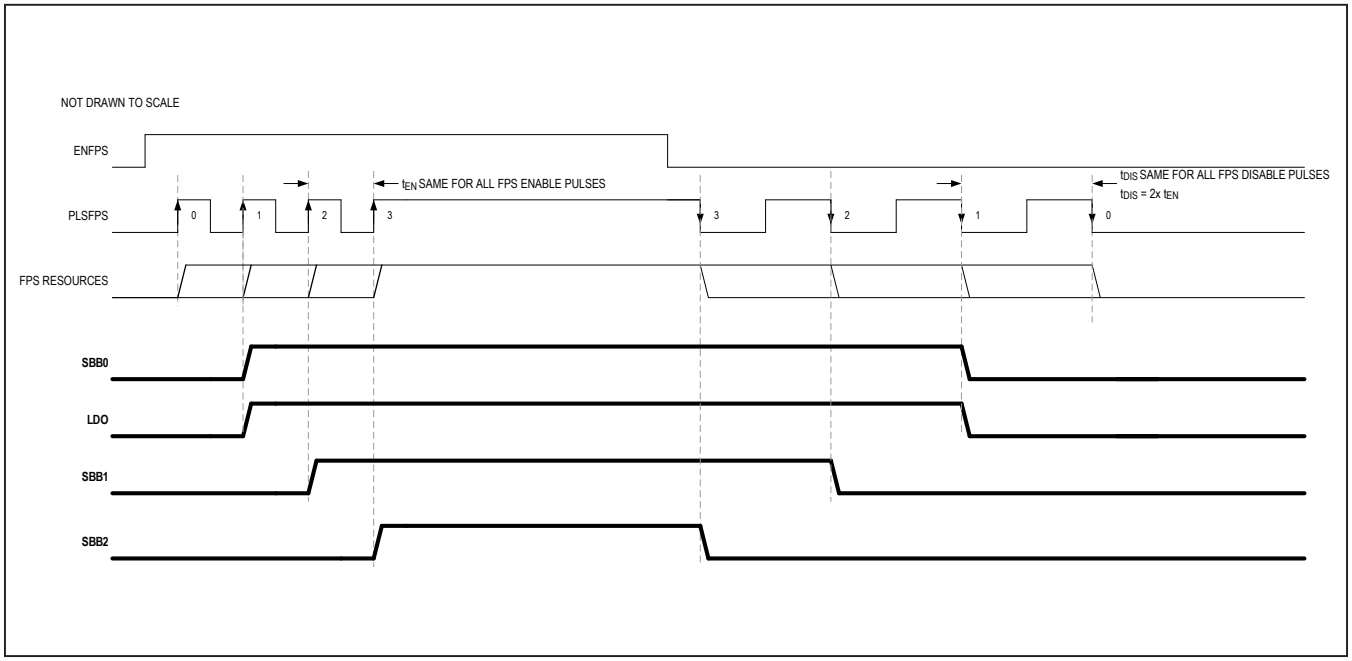


Figure 6. Flexible Power Sequencer Basic Timing Diagram

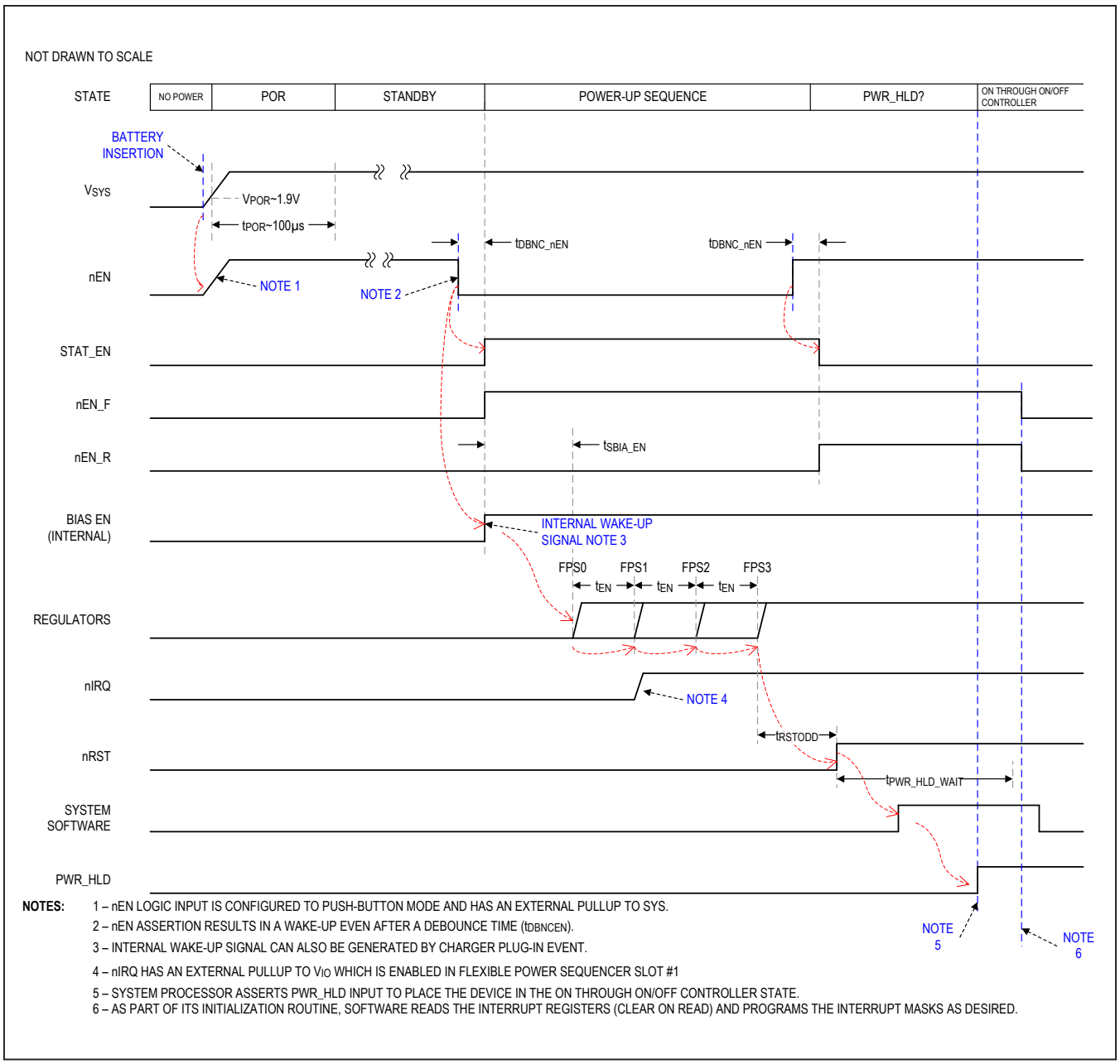


Figure 7. Startup Timing Diagram Due to nEN

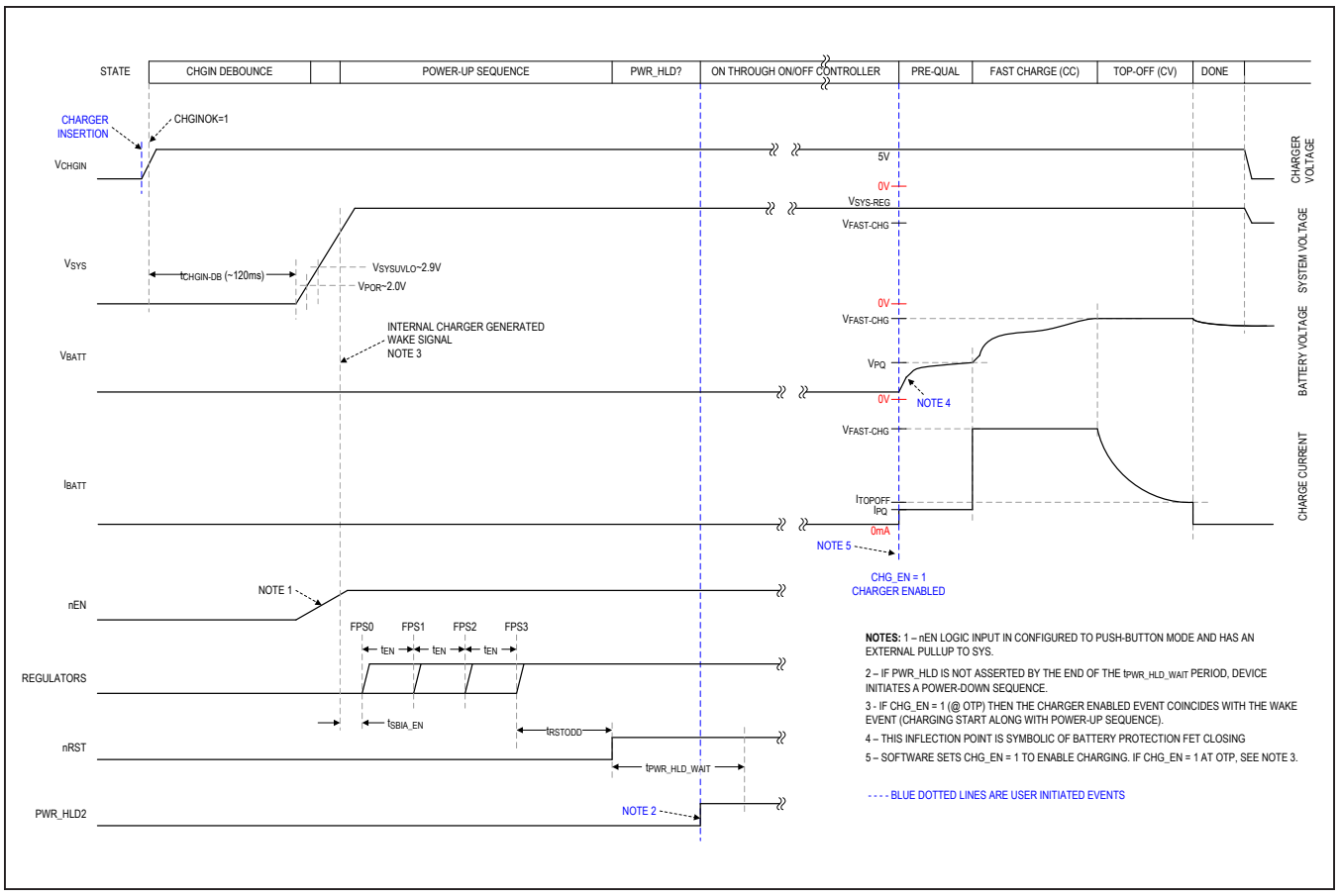


Figure 8. Startup Timing Diagram Due to Charge Source Insertion

Debounced Inputs (nEN, GPI, CHGIN)

nEN, CHGIN, and GPIO (when operating as an input), are debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. Figure 9 shows an example timing diagram for the nEN debounce.

Thermal Alarms and Protection

The device has thermal alarms to monitor if the junction temperature rises above 80°C (T_{JAL1}) and 100ºC (T_{JAL2}).

Over-temperature lockout (OTLO) is entered if the junction temperature exceeds T_{OTLO} (approximately 165°C, typ). OTLO causes transition 10 in Figure 4 which causes resources to immediately shutdown from the on via on/off controller state. Resources may not enable until the temperature falls below T_{OTLO} by approximately 15°C.

The TJAL1_S and TJAL2_S status bits continuously indicate the junction temperature alarm status. Maskable interrupts are available to signal a change in either of these bits. Refer to the *Programmer's Guide* for details.

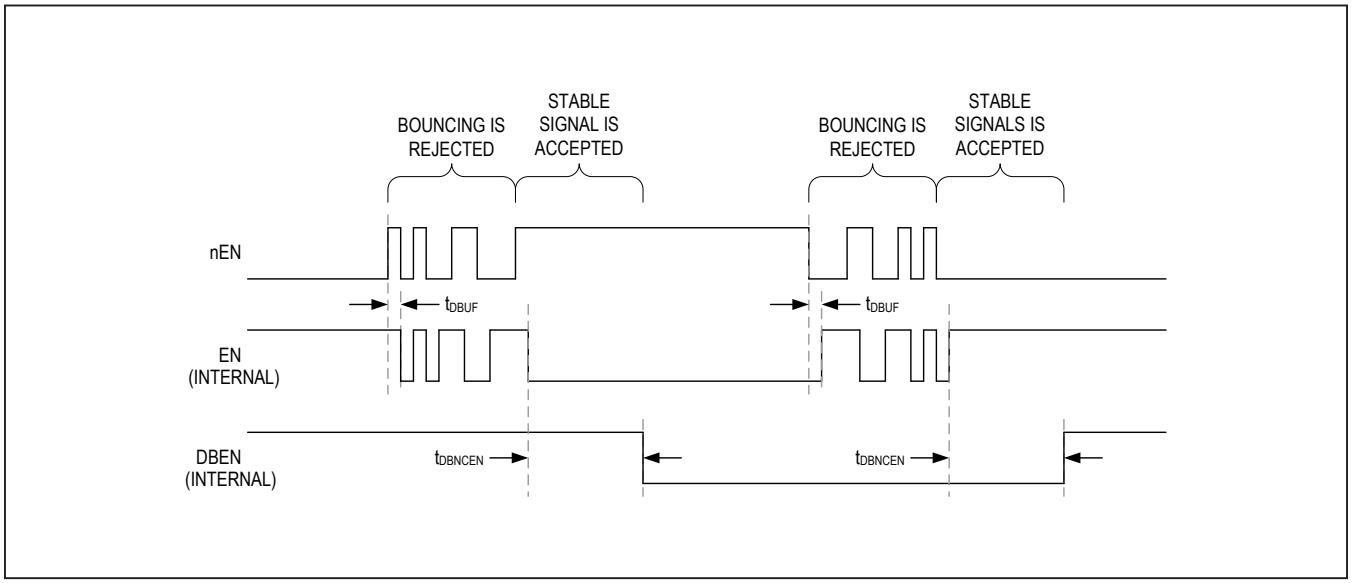


Figure 9. Debounced Inputs

Smart Power Selector Charger

The linear Li+ charger implements power path with Maxim's smart power selector. This allows separate input current limit and battery charge current settings. Batteries charge faster under the supervision of the smart power selector because charge current is independently regulated and not shared with variable system loads. See the *Smart Power Selector* section for more information.

The programmable constant-current charge rate (7.5mA to 300mA) supports a wide range of battery capacities. The programmable input current limit (0mA to 475mA) supports a range of charge sources, including USB. The charger's programmable battery regulation voltage range (3.6V–4.6V) supports a wide variety of cell chemistries. Small battery capacities are supported; the charger accurately terminates charging by detecting battery currents as low as 0.375mA.

Additionally, the robust charger input withstands overvoltages up to 28V. To enhance charger safety, an NTC thermistor provides temperature monitoring in accordance with the JEITA recommendations. See the *Adjustable Thermistor Temperature Monitors* section for more information.

Features

- 7.25V maximum operating input voltage with 28V input standoff
- 7.5mA to 300mA programmable fast-charge current
- Programmable termination current from 0.375mA to 45mA
- Programmable battery regulation voltage from 3.6V to 4.6V
- < 1µA battery-only supply current
- Instant-on functionality
- Analog multiplexer enables power monitoring
- JEITA battery temperature monitor adjusts current and battery regulation voltage for safe charging
- Programmable die temperature regulation

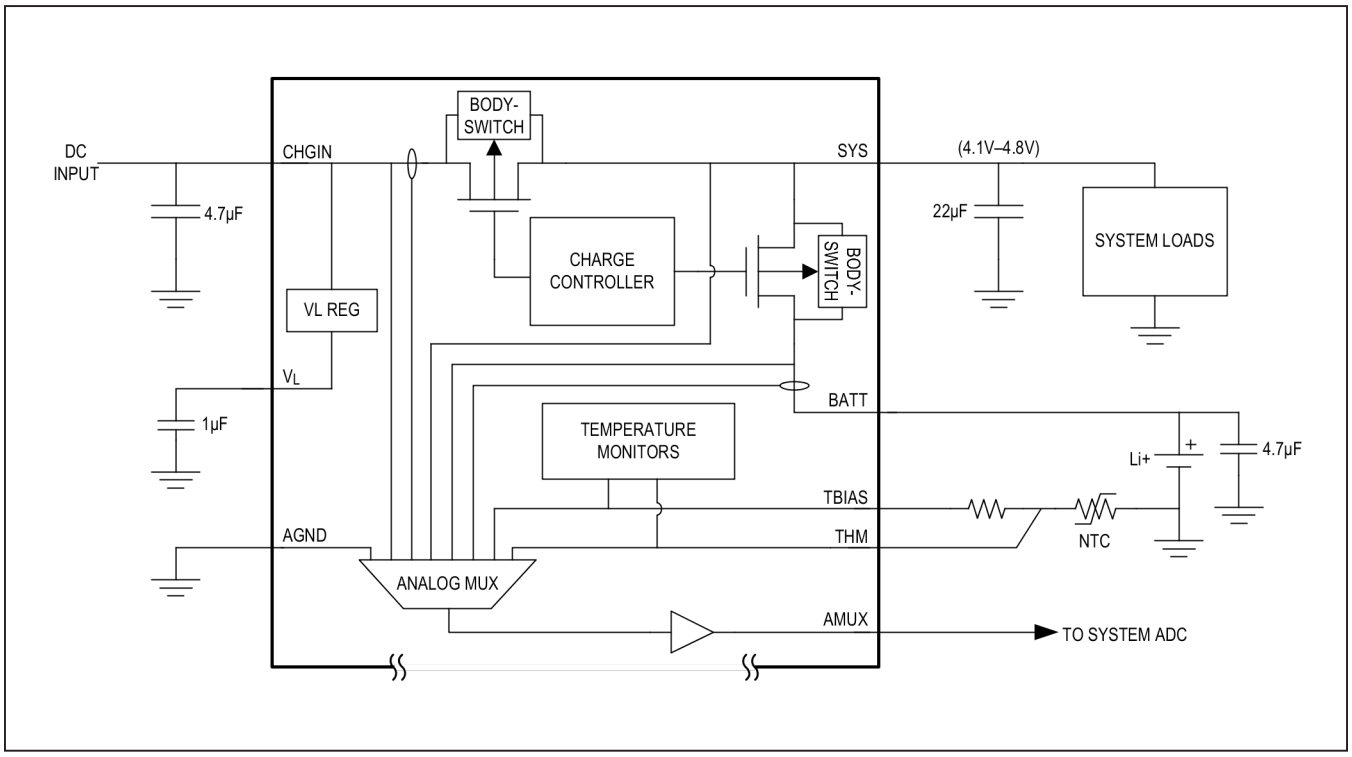


Figure 10. Linear Charger Simplified Block Diagram

Charger Symbol Reference Guide

Table 3 lists the names and functions of charger-specific signals and if they can be programmed through I2C. Consult the *Electrical Characteristics* and *Programmer's Guide* for more information.

Figure 11 indicates the high-level functions of each control circuit within the linear charger.

Table 3. Charger Quick Symbol Reference Guide

SYMBOL	NAME	I2C PROGRAMMABLE?
V_{CHGIN_OVP}	CHGIN overvoltage threshold	No
V_{CHGIN_UVLO}	CHGIN undervoltage lockout threshold	No
$V_{CHGIN-MIN}$	Minimum CHGIN voltage regulation setpoint	Yes, through VCHGIN_MIN[2:0]
$I_{CHGIN-LIM}$	CHGIN input current limit	Yes, through ICHGIN_LIM[2:0]
$V_{SYS-REG}$	SYS voltage regulation target	Yes, through VSYS_REG[4:0]
$V_{SYS-MIN}$	Minimum SYS voltage regulation setpoint	No, tracks $V_{SYS-REG}$
$V_{FAST-CHG}$	Fast-charge constant-voltage level	Yes, through CHG_CV[5:0]
$I_{FAST-CHG}$	Fast-charge constant-current level	Yes, through CHG_CC[5:0]
I_{PQ}	Prequalification current level	Yes, through I_PQ
V_{PQ}	Prequalification voltage threshold	Yes, through CHG_PQ[2:0]
I_{TERM}	Termination current level	Yes, through I_TERM[1:0]
T_{J-REG}	Die temperature regulation setpoint	Yes, through TJ_REG[2:0]
t_{PQ}	Prequalification safety timer	No
t_{FC}	Fast-charge safety timer	Yes, through T_FAST_CHG[1:0]
t_{TO}	Top-off timer	Yes, through T_TOPOFF[2:0]

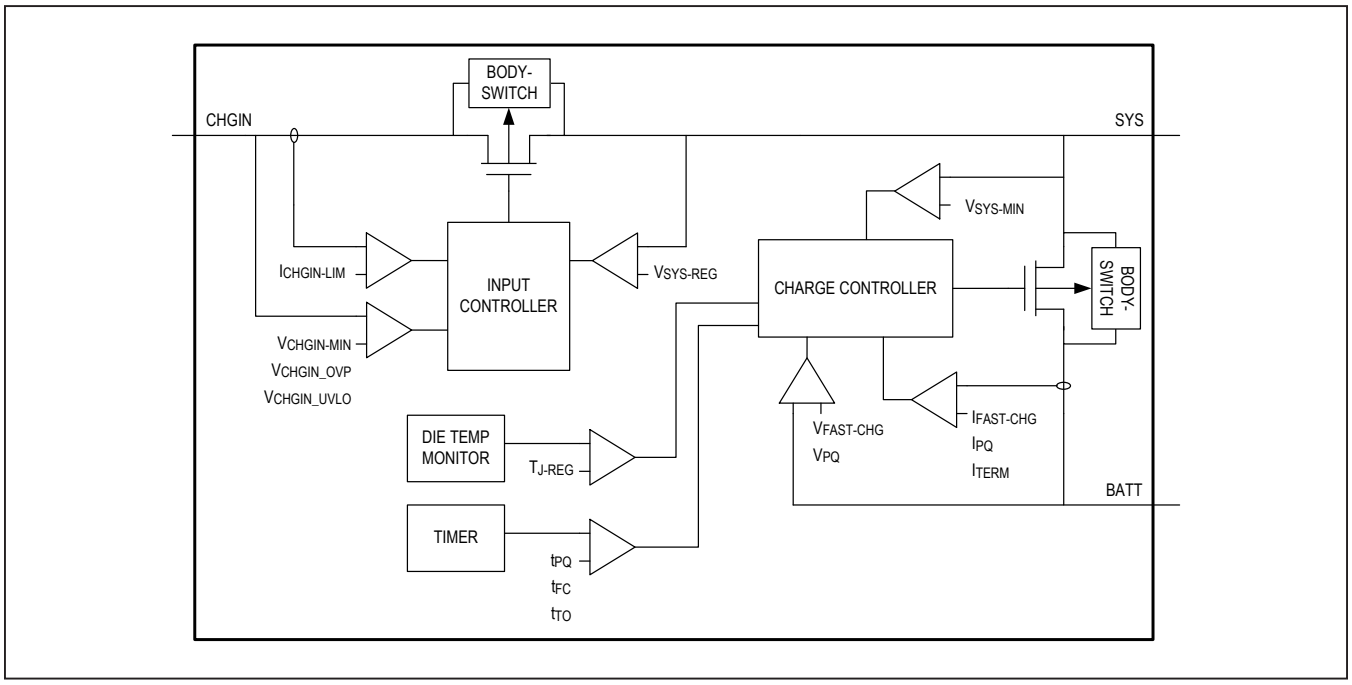


Figure 11. Charger Simplified Control Loops

Smart Power Selector

The smart power selector seamlessly distributes power from the input (CHGIN) to the battery (BATT) and the system (SYS). The smart power selector basic functions are:

- When the system load current is less than the input current limit, the battery is charged with residual power from the input.
- When a valid input source is connected, the system regulates to $V_{SYS-REG}$ to power system loads regardless of the battery's voltage (instant on).
- When the system load current exceeds the input current limit, the battery provides additional current to the system (supplement mode).
- When the battery is finished charging and an input source is present to power the system, the battery remains disconnected from the system.
- When the battery is connected and there is no input power, the system is powered from the battery.

Input Current Limiter

The input current limiter limits CHGIN current so as not to exceed $I_{CHGIN-LIM}$ (programmed by I_{CHGIN_LIM}[2:0]). A maskable interrupt (CHGIN_CTRL_I) is available to signal when the input current limit engages. The state of this loop is reflected by the ICHGIN_LIM_STAT bit.

The input circuit is capable of standing off 28V from ground. CHGIN suspends power delivery to the system and battery when V_{CHGIN} exceeds V_{CHGIN_OVP} (7.5V typical). The input circuit also suspends when V_{CHGIN} falls below V_{CHGIN_UVLO} minus 500mV of hysteresis (3.5V typical). While in OVP or UVLO, the charger remains off, and the battery provides power to the system.

When an valid charge source is connected to CHGIN, SYS begins delivering power to the system after a 120ms debounce timer ($t_{CHGIN-DB}$).

A maskable interrupt (CHGIN_I) signals changes in the state of CHGIN's voltage quality. The state of CHGIN is reflected by CHGIN_DTLS[1:0].

Minimum Input Voltage Regulation

In the event of a poor-quality charge source, the minimum input voltage regulation loop works to reduce input current if V_{CHGIN} falls below $V_{CHGIN-MIN}$ (programmed by VCHGIN_MIN[2:0]). This is important because many commonly used charge adapters feature foldback protection mechanisms where the adapter completely shuts off if its output droops too low. The minimum input voltage regulation loop also prevents V_{CHGIN} from dropping below V_{CHGIN_UVLO} if the cable between the charge source and the charger's input is long or highly resistive.

The input voltage regulation loop improves performance with current limited adapters. If the charger's input current limit is programmed above the current limit of the given adapter, the input voltage loop allows the input to regulate at the current limit of the adapter. The input voltage regulation loop also allows the charger to perform well with adapters that have poor transient load response times.

A maskable interrupt (CHGIN_CTRL_I) signals when the minimum input voltage regulation loop engages. The state of this loop is reflected by VCHGIN_MIN_STAT.

Minimum System Voltage Regulation

The minimum system voltage regulation loop ensures that the system rail remains close to the programmed SYS regulation voltage ($V_{SYS-REG}$) regardless of system loading. The loop engages when the combined battery charge current and system load current causes the CHGIN input to current-limit at $I_{CHGIN-LIM}$. When this happens, the minimum system voltage loop reduces charge current in an attempt to keep the input out of current limit, thereby keeping the system voltage above $V_{SYS-MIN}$ ($V_{SYS-REG}$ - 100mV typical). If this loop reduces battery current to 0 and the system is in need of more current than the input can provide, then the smart power selector overrides the minimum system voltage regulation loop and allows SYS to collapse to BATT for the battery to provide supplement current to the system. The smart power selector automatically reenables the minimum system voltage loop when the supplement event has ended.

A maskable interrupt (SYS_CTRL_I) asserts to signal a change in VSYS_MIN_STAT. This status bit asserts when the minimum system voltage regulation loop is active.

Die Temperature Regulation

In case the die temperature exceeds T_{J-REG} (programmed by TJ_REG[2:0]) the charger attempts to limit the temperature increase by reducing battery charge current. The TJ_REG_STAT bit asserts whenever charge current is reduced due to this loop. The charger's current sourcing capability to SYS remains unaffected when TJ_REG_STAT is high. A maskable interrupt (TJ_REG_I) asserts to signal a change in TJ_REG_STAT. It is advisable that the TJ_REG_I interrupt be used to signal the system processor to reduce loads on SYS to reduce total system temperature.

Charger State Machine

The battery charger follows a strict state-to-state progression to ensure that a battery is charged safely. The status bitfield, CHG_DTLS[3:0], reflects the charger's current operational state. A maskable interrupt (CHG_I) is available to signal a change in CHG_DTLS[3:0].

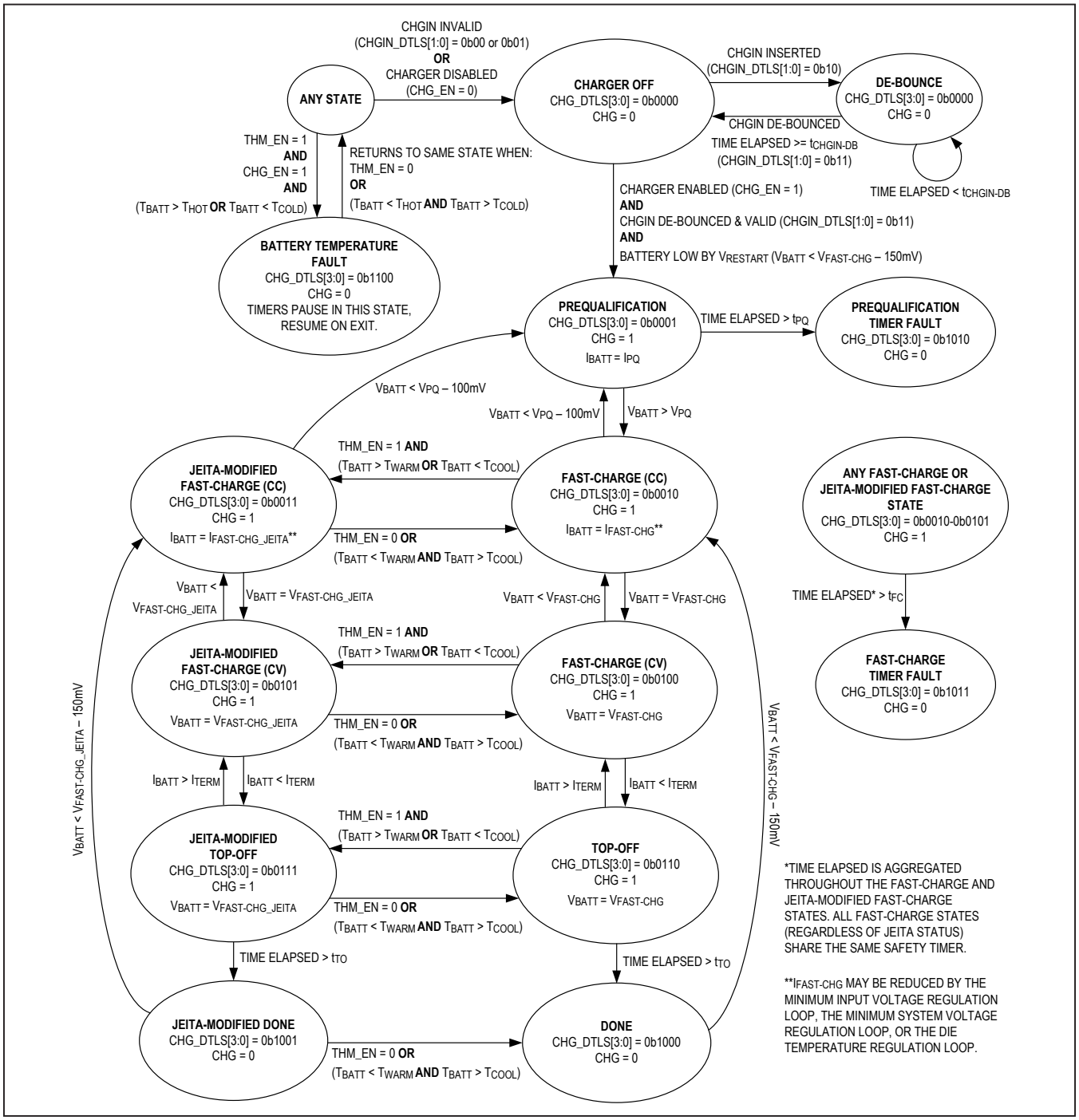


Figure 12. Charger State Diagram

Charger Off State

The charger is off when CHGIN is invalid, the charger is disabled, or the battery is fresh.

CHGIN is invalid when the CHGIN input is invalid ($V_{CHGIN} < V_{CHGIN\_UVLO}$ or $V_{CHGIN} > V_{CHGIN\_OVP}$). While CHGIN is invalid, the battery is connected to the system. CHGIN voltage quality can be separately monitored by the CHGIN_DTLS[1:0] status bitfield. Refer to the *Programmer's Guide* for details.

The charger is disabled when the charger enable bit is 0 (CHG_EN = 0). The battery is connected or disconnected to the system depending on the validity of V_{CHGIN} while CHG_EN = 0. See the *Smart Power Selector* section.

The battery is fresh when CHGIN is valid and the charger is enabled (CHG_EN = 1) and the battery is not low by $V_{RESTART}$ ($V_{BATT} > V_{FAST\text{-}CHG} - V_{RESTART}$). The battery is disconnected from the system and not charged while the battery is fresh. The charger state machine exits this state and begin charging when the battery becomes low by $V_{RESTART}$ (150mV typical). This condition is functionally similar to done state. See *Done State* section.

Prequalification State

The prequalification state is intended to assess a low-voltage battery's health by charging at a reduced rate. If the battery voltage is less than the V_{PQ} threshold, the charger is automatically in prequalification. If the cell voltage does not exceed V_{PQ} in 30 minutes (t_{PQ}), the charger faults. The prequalification charge rate is a percentage of $I_{FAST\text{-}CHG}$ and is programmable with I_PQ. The prequalification voltage threshold (V_{PQ}) is programmable through CHG_PQ[2:0].

Fast-Charge States

When the battery voltage is above V_{PQ}, the charger transitions to the fast-charge (CC) state. In this state, the charger delivers a constant current ($I_{FAST\text{-}CHG}$) to the cell. The constant current level is programmable from 7.5mA to 300mA by CHG_CC[5:0].

When the cell voltage reaches $V_{FAST\text{-}CHG}$, the charger state machine transitions to fast-charge (CV). $V_{FAST\text{-}CHG}$ is programmable with CHG_CV[5:0] from 3.6V to 4.6V. The charger holds the battery's voltage constant at $V_{FAST\text{-}CHG}$ while in the fast-charge (CV) state. As the battery approaches full, the current accepted by the battery reduces. When the charger detects that battery charge current has fallen below I_{TERM}, the charger state machine enters the top-off state.

A fast-charge safety timer starts when the state machine enters fast-charge (CC) or JEITA-modified fast-charge (CC) from a non-fast-charge state. The timer continues to run through all fast-charge states regardless of JEITA status. The timer length (t_{FC}) is programmable from 3 hours to 7 hours in 2 hour increments with T_FAST_CHG[1:0]. If it is desired to charge without a safety timer, program T_FAST_CHG[1:0] with 0b00 to disable the feature. If the timer expires before the fast-charge states are exited, the charger faults. See the *Fast-Charge Timer Fault State* section for more information.

If the charge current falls below 20% of the programmed value during fast-charge (CC), the safety timer pauses. The timer also pauses for the duration of supplement mode events. The TIME_SUS bit indicates the status of the fast-charge safety timer. Refer to the *Programmer's Guide* for more details.

Top-Off State

Top-off state is entered when the battery charge current falls below I_{TERM} during the fast-charge (CV) state. I_{TERM} is a percentage of $I_{FAST\text{-}CHG}$ and is programmable through I_TERM[1:0]. While in the top-off state, the battery charger continues to hold the battery's voltage at $V_{FAST\text{-}CHG}$. A programmable top-off timer starts when the charger state machine enters the top-off state. When the timer expires, the charger enters the done state. The top-off timer value (t_{TO}) is programmable from 0 minutes to 35 minutes with T_TOPOFF[2:0]. If it is desired to stop charging as soon as battery current falls below I_{TERM}, program t_{TO} to 0 minutes.

Done State

The charger enters the done state when the top-off timer expires. The battery remains disconnected from the system during done. The charger restarts if the battery voltage falls more than $V_{RESTART}$ (150mV typ) below the programmed $V_{FAST\text{-}CHG}$ value.

Prequalification Timer Fault State

The prequalification timer fault state is entered when the battery's voltage fails to rise above V_{PQ} in t_{TO} (30 minutes typical) from when the prequalification state was first entered. If a battery is too deeply discharged, damaged, or internally shorted, the prequalification timer fault state can occur. During the timer fault state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the prequalification timer fault state, toggle the charger enable (CHG_EN) bit or unplug and replug the external voltage source connected to CHGIN.

Fast-Charge Timer Fault State

The charger enters the fast-charge timer fault state if the fast-charge safety timer expires. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the fast-charge timer fault state, toggle the charger enable bit (CHG_EN) or unplug and replug the external voltage source connected to CHGIN.

Battery Temperature Fault State

If the thermistor monitoring circuit reports that the battery is either too hot or too cold to charge (as programmed by THM_HOT[1:0] and THM_COLD[1:0]), the state machine enters the battery temperature fault state. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. This state can only be entered if the thermistor is enabled (THM_EN = 1). Battery temperature fault state has priority over any other fault state, and can be exited when the thermistor is disabled (THM_EN = 0) or when the battery returns to an acceptable temperature. When this fault state is exited, the state machine returns to the last state it was in before battery temperature fault state was entered.

All active charger timers (fast-charge safety timer, prequalification timer, or top-off timer) are paused in this state. Active timers resume when the state is exited.

The THM_DTLS[2:0] bitfield reports battery temperature status. See the *Adjustable Thermistor Temperature Monitors* section and refer to the *Programmer's Guide* for more information.

JEITA-Modified States

If the thermistor is enabled (THM_EN = 1), then the charger state machine is allowed to enter the JEITA-modified states. These states are entered if the charger's temperature monitors indicate that the battery temperature is either warm (greater than T_{WARM}) or cool (lesser than T_{COOL}). See the *Adjustable Thermistor Temperature Monitors* section for more information about setting the temperature thresholds.

The charger's current and voltage parameters change from $I_{FAST-CHG}$ and $V_{FAST-CHG}$ to $I_{FAST-CHG\_JEITA}$ and $V_{FAST-CHG\_JEITA}$ while in the JEITA-modified states. The JEITA modified parameters can be independently set to lower voltage and current values so that the battery can charge safely over a wide range of ambient temperatures. If the battery temperature returns to normal, or the thermistor is disabled (THM_EN = 0) the charger exits the JEITA-modified states.

Typical Charge Profile

A typical battery charge profile (and state progression) is illustrated in Figure 13.

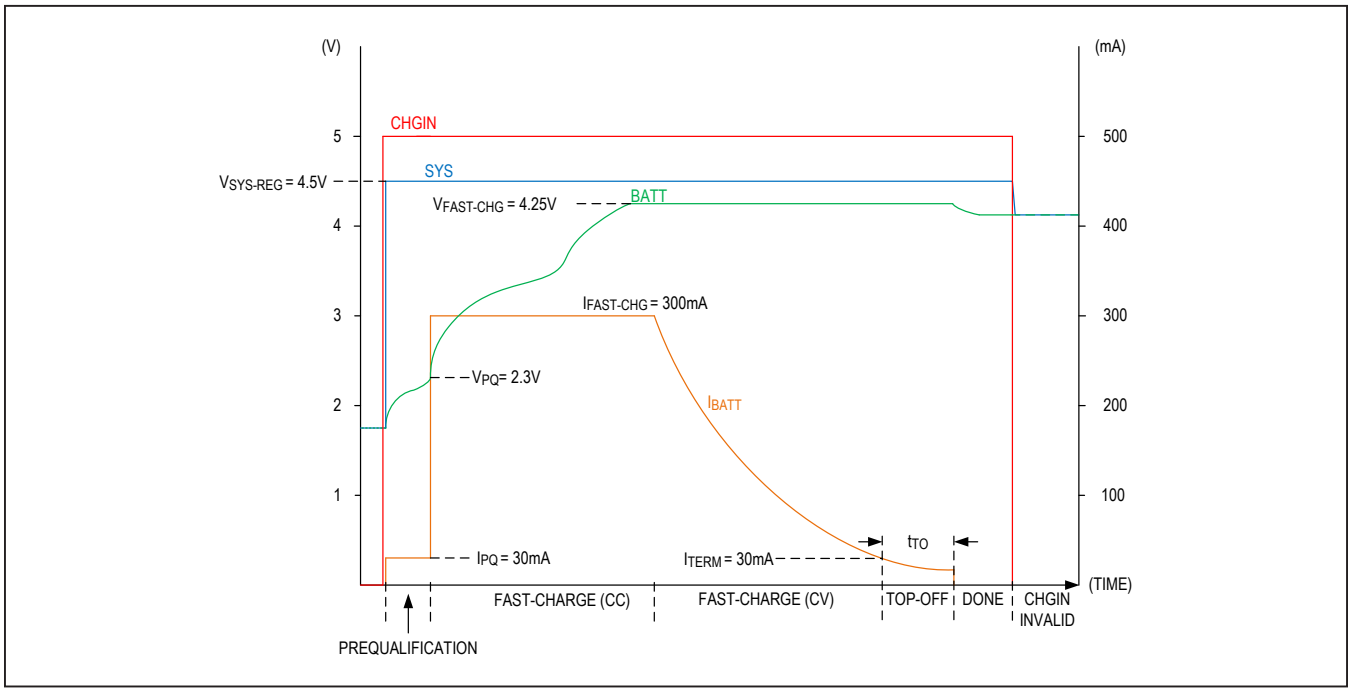


Figure 13. Example Battery Charge Profile

Charger Applications Information

Configuring a Valid System Voltage

The smart power selector begins to regulate SYS to $V_{SYS-REG}$ when CHGIN is connected to a valid source. To ensure the charger's accuracy specified in the *Electrical Characteristics* table, the system voltage must always be programmed at least 200mV above the charger's constant-voltage level ($V_{FAST-CHG}$). If this condition is not met, then the charger's internal configuration logic forces $V_{FAST-CHG}$ to reduce to satisfy the 200mV requirement. If this happens, the charger asserts the SYS_CNFG_I interrupt to alert the user that a configuration error has been made and that the bits in CHG_CV[5:0] have changed to reduce $V_{FAST-CHG}$.

CHGIN/SYS/BATT Capacitor Selection

Bypass CHGIN to GND with a 4.7µF ceramic capacitor to minimize inductive kick caused by long cables between the DC charge source and the device. Larger values increase decoupling for the linear charger, but increase inrush current from the DC charge source when the device is first connected to a source through a cable/plug. If the DC charging source is an upstream USB device, limit the maximum CHGIN input capacitance based on the appropriate USB specification (typically no more than 10µF). The effective value of the CHGIN capacitor must be greater than 1µF when biased with 5V.

Bypass SYS to GND with a 22µF ceramic capacitor. This capacitor is needed to ensure stability of SYS while it is being regulated from CHGIN. Since SYS must be connected to IN_SBB, then one capacitor can be used to bypass this node as long as it is physically close to the device. Larger values of SYS capacitance increase decoupling for all SYS loads. When biased with 4.5V, the effective value of the SYS capacitor must be greater than 4µF and no more than 100µF.

Bypass BATT to GND with a 4.7µF ceramic capacitor. This capacitor is required to ensure stability of the BATT voltage regulation loop. When biased with 4.5V, the effective value of the BATT capacitor must be greater than 1µF.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Adjustable Thermistor Temperature Monitors

The optional use of a negative temperature coefficient (NTC) thermistor (thermally coupled to the battery) enables the charger to operate safely over the JEITA temperature range. When the thermistor is enabled (THM_EN = 1), the charger continuously monitors the voltage at the THM pin in order to sense the temperature of the battery being charged.

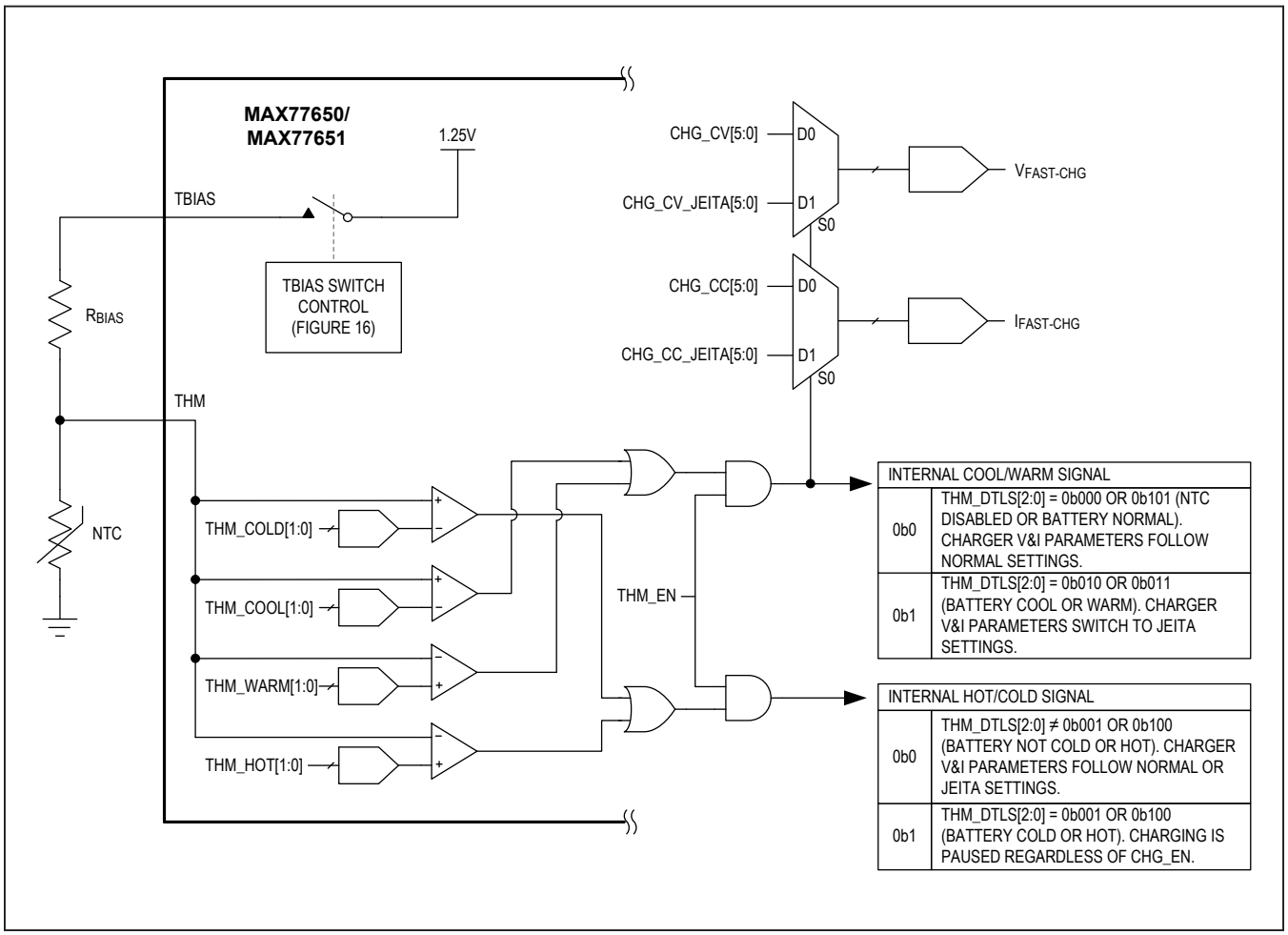


Figure 14. Thermistor Logic Functional Diagram

See Figure 15 for a visual example of what is described here in text.

- If the battery temperature is higher than T_{COOL} and lower than T_{WARM}, the battery charges normally with the normal values for $V_{FAST-CHG}$ and $I_{FAST-CHG}$. The charger state machine does not enter JEITA-modified states while the battery temperature is normal.
- If the battery temperature is either above T_{WARM} but below T_{HOT}, or, below T_{COOL} but above T_{COLD}, the battery charges with the JEITA-modified voltage and current values. These modified values, $V_{FAST-CHG\_JEITA}$ and $I_{FAST-CHG\_JEITA}$, are programmable through CHG_CV_JEITA[5:0] and CHG_CC_JEITA[5:0], respectively. These values are independently programmable from the nonmodified $V_{FAST-CHG}$ and $I_{FAST-CHG}$ values and can even be programmed to the same values if an automatic response to a warm or cool battery is not desired. The charger state machine enters JEITA-modified states while the battery temperature is outside of normal.
- If the battery temperature is either above T_{HOT} or below T_{COLD}, the charger follows the JEITA recommendation and pauses charging. The charger state machine enters battery temperature fault state while charging is paused due to extreme high or low temperatures.

The battery's temperature status is reflected by the THM_DTLS[2:0] status bitfield. A maskable interrupt (THM_I) signals a change in THM_DTLS[2:0]. Refer to the *Programmer's Guide* for more information. To completely disable the charger's automatic response to battery temperature, disable the feature by programming THM_EN = 0.

The voltage thresholds corresponding to the JEITA temperature thresholds are independently programmable through THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0]. Each threshold can be programmed to one of four voltage options spanning 15°C for an NTC beta of 3380K. See the *Configurable Temperature Thresholds* section and refer to the *Programmer's Guide* for more information.

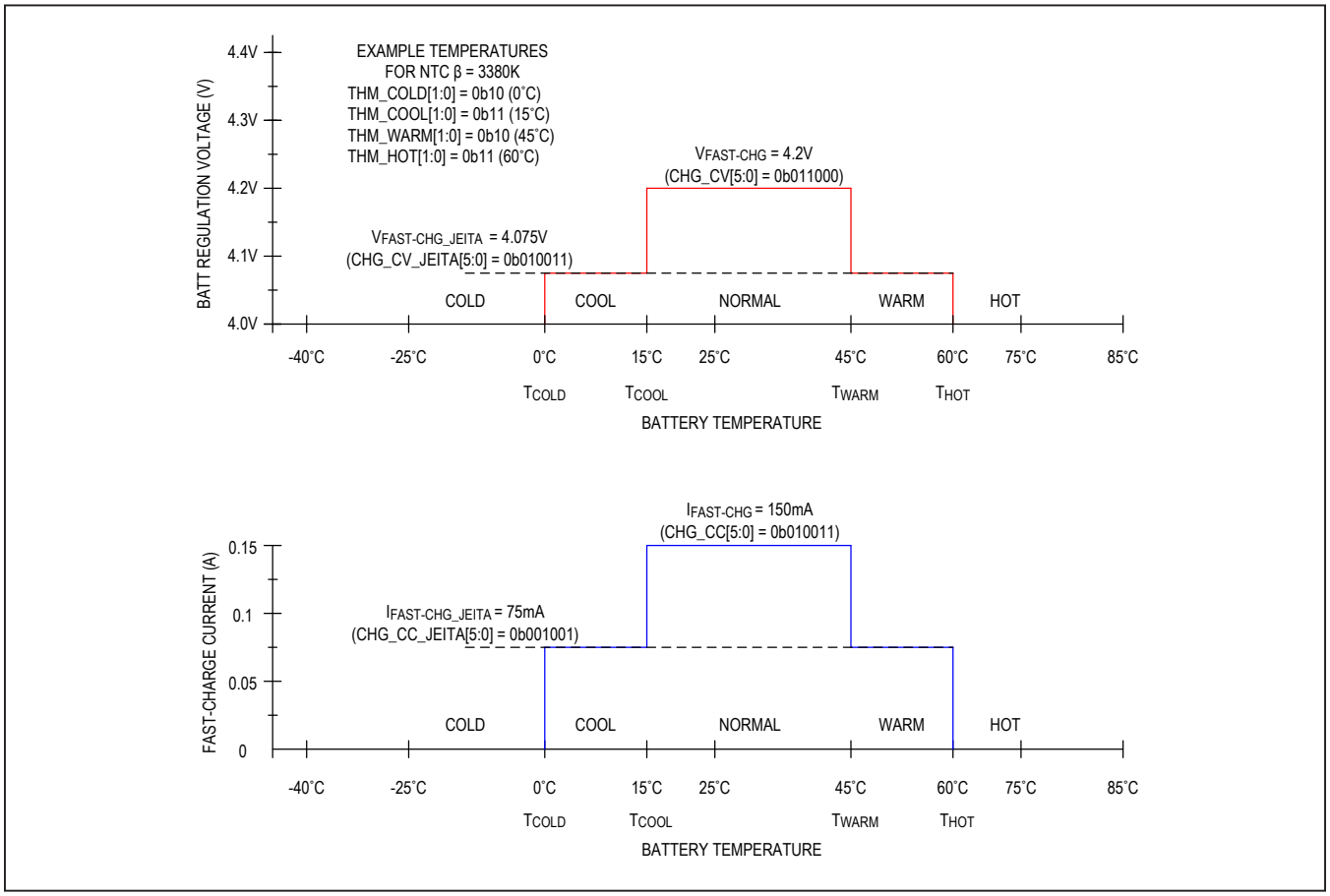


Figure 15. Safe-Charging Profile Example

Thermistor Bias

An external ADC can optionally perform conversions on the THM and TBIAS pins to measure the battery's temperature. An on-chip analog multiplexer is used to route these nodes to the AMUX pin. The operation of the analog multiplexer does not interfere with the charger's temperature monitoring comparators or the charger's automatic JEITA response. See the *Analog Multiplexer & Power Monitor AFEs* section for more information.

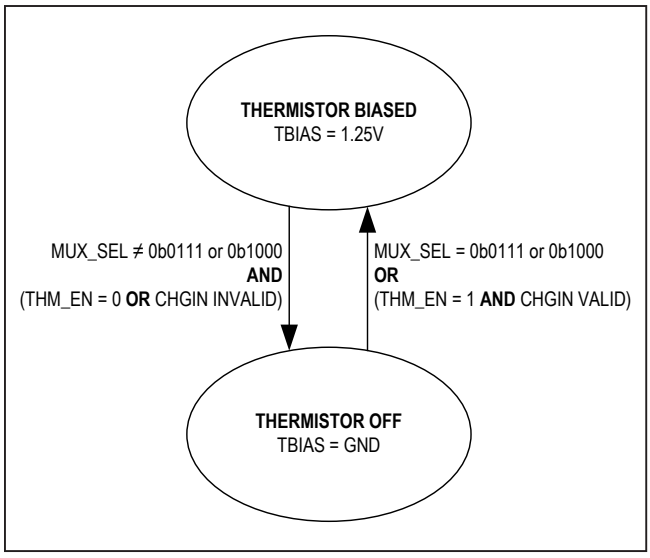


Figure 16. Thermistor Bias State Diagram

The NTC thermistor's bias source (TBIAS) follows the simple operation outlined below:

- If CHGIN is valid and the thermistor is enabled (THM_EN = 1), then the thermistor is biased so the charger can automatically respond to battery temperature changes.
- If the analog multiplexer is connecting THM or TBIAS to AMUX, then the thermistor is biased so an external ADC can perform a meaningful temperature conversion.

The AMUX pin is a buffered output. The operation of the analog multiplexer and external ADC does not collide with the function of the on-chip temperature monitors. Both functions may be used simultaneously with no ill effect.

Configurable Temperature Thresholds

Temperature thresholds for different NTC thermistor beta values are listed in Table 4. The largest possible programmable temperature range can be realized by using an NTC with a beta of 3380K. Using a larger beta compresses the temperature range. The trip voltage thresholds are programmable with the THM_HOT[1:0], THM_WARM[1:0], THM_COOL[1:0], and THM_COLD[1:0] bitfields. All possible programmable trip voltages are listed in Table 4.

These are theoretical values computed by a formula. Refer to the particular NTC's data sheet for more accurate measured data. In all cases, select the value of R_{BIAS} to be equal to the NTC's effective resistance at +25°C.

Table 4. Trip Temperatures vs. Trip Voltages for Different NTC β

TRIP VOLTAGE (V)	TRIP TEMPERATURES (°C)					
	3380K	3435K	3940K	4050K	4100K	4250K
1.024	-10.0	-9.5	-5.6	-4.8	-4.5	-3.5
0.976	-5.0	-4.6	-1.1	-0.5	-0.2	0.6
0.923	0.0	0.3	3.3	3.8	4.1	4.8
0.867	5.0	5.3	7.7	8.1	8.3	8.9
0.807	10.0	10.2	12.0	12.4	12.5	12.9
0.747	15.0	15.1	16.4	16.6	16.7	17.0
0.511	35.0	34.8	33.5	33.3	33.2	32.9
0.459	40.0	39.8	37.8	37.4	37.3	36.8
0.411	45.0	44.7	42.0	41.5	41.3	40.7
0.367	50.0	49.6	46.2	45.6	45.3	44.6
0.327	55.0	54.5	50.4	49.7	49.3	48.4
0.291	60.0	59.4	54.6	53.7	53.3	52.2

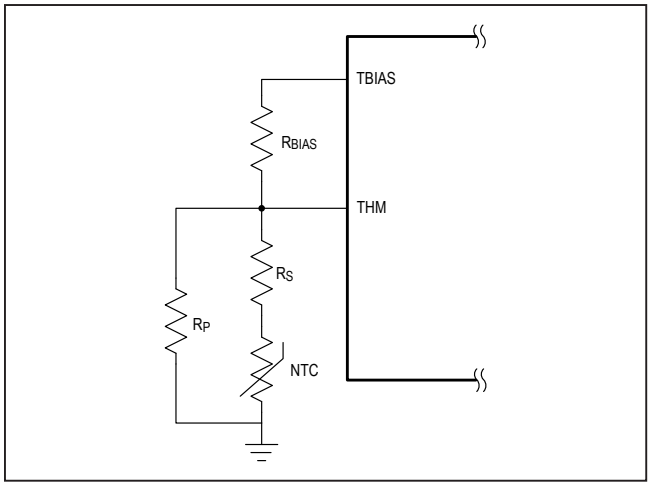


Figure 17. Thermistor Circuit with Adjusting Series and Parallel Resistors

Thermistor Applications Information

Using Different Thermistor β

If an NTC with a beta larger than 3380K is used and the resulting available programmable temperature range is undesirably small, then two adjusting resistors can be used to expand the temperature range. R_S and R_P can be optionally added to the NTC thermistor circuit shown in Figure 17 to expand the range of programmable temperature thresholds.

Select values for R_S and R_P based on the information shown in Table 5.

NTC Thermistor Selection

Popular NTC thermistor options are listed in Table 6.

Table 5. Example R_S and R_P Correcting Values for NTC β Above 3380K

PARAMETER	UNIT	DESIGN TARGET CASE	CASE 1		CASE 2		CASE 3	
NTC thermistor beta	K	3380	3940		4050		4250	
25°C NTC resistance	kΩ	10	10		47		100	
R_{BIAS}		10	10		47		100	
Adjusting parallel resistor, R_P		open	open	200	open	680	open	1300
Adjusting series resistor, R_S		short	short	0.62	short	3.3	short	9.1
R_{NTC} at $1.024V_{COLD}$ threshold		45.24	45.24	578.5	212.6	306.1	452.4	684.8
R_{NTC} at $0.867V_{COOL}$ threshold		22.61	22.61	248.8	106.3	122.7	226.1	264.7
R_{NTC} at $0.459V_{WARM}$ threshold		5.81	5.81	5.36	27.3	25.1	58.1	51.7
R_{NTC} at $0.291V_{HOT}$ threshold		3.04	3.04	2.46	14.3	112.7	30.4	22.0
T_{ACTUAL} at V_{COLD} (-10°C expected)	°C	-10.03	-5.56	-9.96	-4.82	-11.14	-3.55	-10.46
T_{ACTUAL} at V_{COOL} (5°C expected)		4.98	7.66	5.76	8.10	5.33	8.86	5.94
T_{ACTUAL} at V_{WARM} (40°C expected)		40.02	37.79	39.76	37.43	39.40	36.82	39.48
T_{ACTUAL} at V_{HOT} (60°C expected)		60.04	54.56	60.37	53.68	60.02	52.21	60.4

Table 6. NTC Thermistors

MANUFACTURER	PART	B-CONSTANT (25°C/50°C)	R (Ω) AT 25°C	CASE SIZE
TDK	NTCG063JF223HTBX	3380K	22k	0201
Murata	NCP03XH103F05RL	3380K	10k	0201
Murata	NCP15XH103F03RC	3380K	10k	0402
TDK	NTCG103JX103DT1	3380K	10k	0402
Cantherm	CMFX3435103JNT	3435K	10k	0402
Murata	NCP15XV103J03RC	3900K	10k	0402
Panasonic	ERT-JZEP473J	4050K	47k	0201
Panasonic	ABNTC-0402-473J-4100F-T	4100K	47k	0402
Murata	NCP15WF104F03RC	4250K	100k	0402

Analog Multiplexer & Power Monitor AFEs

An external ADC can be used to measure the chip's various signals for general functionality or on-the-fly power monitoring. The MUX_SEL[3:0] bitfield controls the internal analog multiplexer responsible for connecting the proper channel to the AMUX pin. Each measurable signal is listed below with its appropriate multiplexer channel. The voltage on the AMUX pin is a buffered output that ranges from 0V to V_{FS} (1.25V typ). The buffer has a 50µA quiescent current draw and is only active when the device's main bias is active and a channel is selected (MUX_SEL[3:0] ≠ 0b0000). Disable the buffer by programming to MUX_SEL[3:0] to 0b0000 when not actively converting the voltage on AMUX.

Table 7 shows how to translate the voltage signal on the AMUX pin to the value of the parameter being measured.

See the *Electrical Characteristics—Analog Multiplexer and Power Monitor AFEs* table and refer to the *Programmer's Guide* for more details.

Table 7. AMUX Signal Transfer Functions

SIGNAL	MUX_SEL [3:0]	TRANSFER FUNCTION	FULL-SCALE SIGNAL MEANING (V_{AMUX} = 1.25V)	ZERO-SCALE SIGNAL MEANING (V_{AMUX} = 0V)
CHGIN pin voltage	0b0001	$V_{CHGIN} = \frac{V_{AMUX}}{G_{VCHGIN}}$	7.5V	0V
CHGIN pin current	0b0010	$I_{CHGIN} = \frac{V_{AMUX}}{G_{ICHGIN}}$	0.475A	0A
BATT pin voltage	0b0011	$V_{BATT} = \frac{V_{AMUX}}{G_{VBATT}}$	4.6V	0V
BATT pin charging current	0b0100	$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$	100% of $I_{FAST-CHG}$ (CHG_CC[5:0])	0% of $I_{FAST-CHG}$
BATT pin discharge current	0b0101	$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$	100% of $I_{DISCHG-SCALE}$ (IMON_DISCHG_SCALE[3:0])	0% of $I_{DISCHG-SCALE}$
BATT pin discharge current NULL	0b0110	$V_{NULL} = V_{AMUX}$	1.25V	0V
THM pin voltage	0b0111	$V_{THM} = V_{AMUX}$	1.25V	0V
TBIAS pin voltage	0b1000	$V_{TBIAS} = V_{AMUX}$	1.25V	0V
AGND pin voltage*	0b1001	$V_{AGND} = V_{AMUX}$	1.25V	0V
SYS pin voltage	0b1010	$V_{SYS} = \frac{V_{AMUX}}{G_{VSYS}}$	4.8V	0V

**AGND pin voltage is accessed through a 100Ω (typ) pulldown resistor. Setting MUX_SEL[3:0] to 0b0000 disables the multiplexer and changes the AMUX pin to a high-impedance state.*

Measuring Battery Current

It is possible to sample the current in the BATT pin at any time or in any mode with an external ADC. For improved accuracy, the analog circuitry used for monitoring battery discharge current is different from the circuitry monitoring battery charge current. Table 8 outlines how to determine the direction of battery current.

Method for Measuring Discharging Current

- Program the multiplexer to switch to the discharge NULL measurement by changing MUX_SEL[3:0] to 0b0110. A NULL conversion must always be performed first to cancel offsets.
- Wait the appropriate channel switching time (0.3µs typ).
- Convert the voltage on the AMUX pin and store as V_{NULL}.
- Program the multiplexer to switch to the battery discharge current measurement by changing MUX_SEL[3:0] to 0b0101. A nonnulling conversion should be done immediately after a NULL conversion.
- Wait the appropriate channel switching time (0.3µs typ).
- Convert the voltage on AMUX pin and use the following transfer function to determine the discharge current.

$$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$$

V_{FS} is 1.25V (typ). $I_{DISCHG-SCALE}$ is programmable through IMON_DISCHG_SCALE[3:0]. The default value is 300mA. If smaller currents are anticipated, then $I_{DISCHG-SCALE}$ can be reduced for improved measurement accuracy.

Method for Measuring Charging Current

- Program the multiplexer to switch to the charge current measurement by changing MUX_SEL[3:0] to 0b0100.
- Wait the appropriate channel switching time (0.3µs typ).
- Convert the voltage on the AMUX pin and use the following transfer function to determine charging current.

$$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$$

V_{FS} is 1.25V (typ). $I_{FAST-CHG}$ the charger's fast-charge constant-current setting and is programmable through CHG_CC[5:0].

Table 8. Battery Current Direction Decode

MEASUREMENT	CHARGING OR DISCHARGING INDICATORS		
	CHG BIT	CHG_DTLS[3:0]	CHGIN_DTLS[1:0]
Discharging Battery Current (Positive Battery Terminal Sourcing Current into the BATT pin of MAX77650/MAX77651)	Don't care	Don't care	0b00 0b01 0b10
Charging Battery Current (Positive Battery Terminal Sinking Current from the BATT pin of MAX77650/MAX77651)	1	0b0001–0b0111	0b11

SIMO Buck-Boost

The device has a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The SIMO configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

SIMO Benefits and Features

- 3 Output Channels
- Ideal for Low-Power Designs
  - Delivers > 300mA at 1.8V from a 3.7V Input
  - ±3% Accurate Output Voltage
- Small Solution Size
  - Multiple Outputs from a Single 1.5µH (0603) Inductor
  - Small 10µF (0402) Output Capacitors
- Flexible and Easy to Use
  - Single Mode of Operation
  - Programmable Peak Inductor Current
  - Programmable On-Chip Active Discharge
- Long Battery Life
  - High Efficiency, > 87% at 3.3V Output
  - Better Total System Efficient than Buck + LDOs
  - Low Quiescent Current, 1µA per Output
  - Low Input Operating Voltage, 2.7V (min)

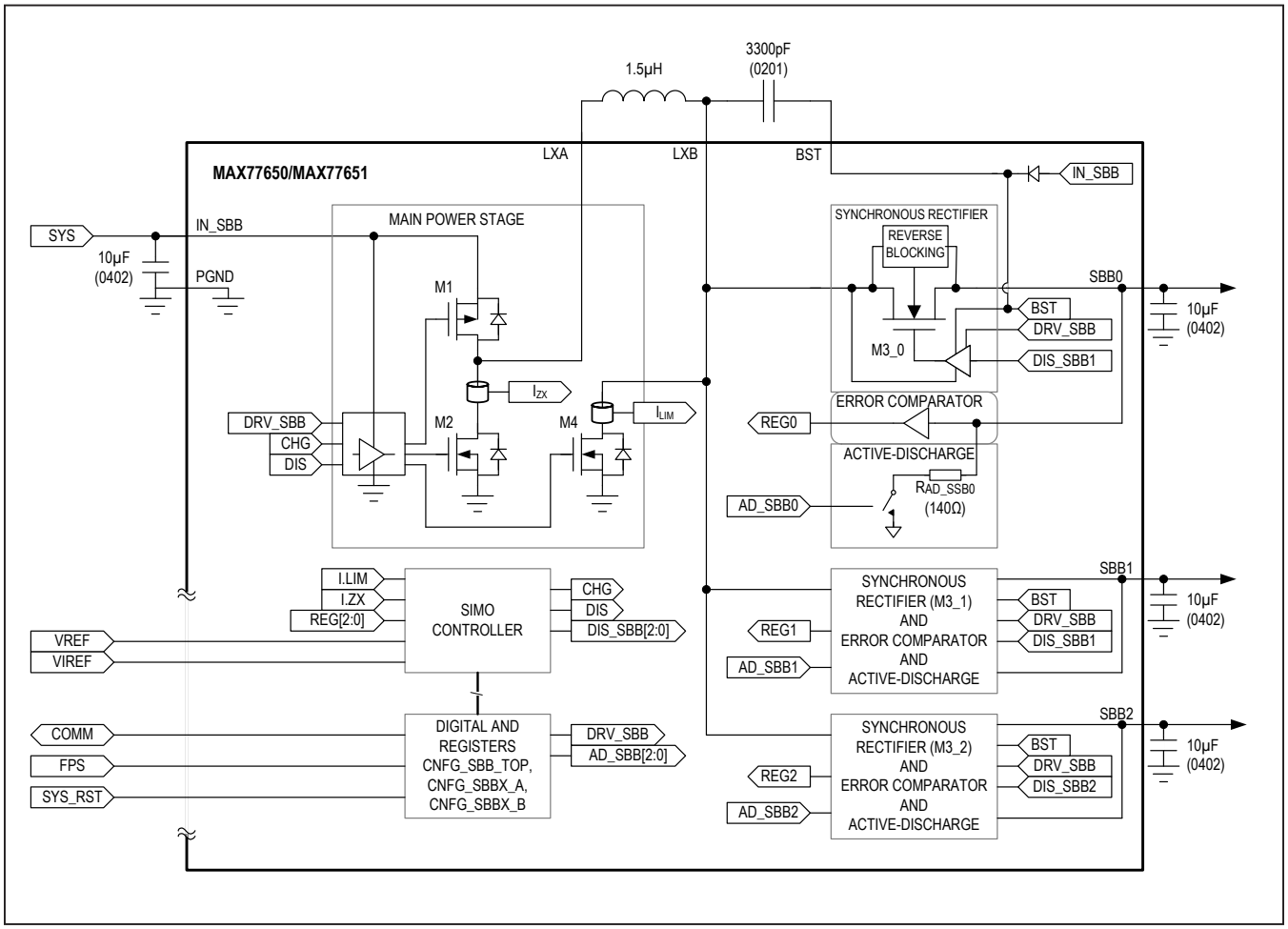


Figure 18. SIMO Detailed Block Diagram

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

When the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached (I_{LIM} = I_{P_SBB}). The inductor energy then discharges (M2 + M3_x) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup to dV/dt_{SS} (5mV/µs typ).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

The current into the output capacitor (I_{CSBB}) during soft-start is:

$$I_{CSBB} = C_{SBB}\frac{dV}{dt_{SS}} \quad \text{(Equation 1)}$$

where C_{SBB} is the capacitance on the output of the regulator, and dV/dt_{SS} is the voltage change rate of the output.

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{\left(I_{CSBB} + I_{LOAD}\right)\frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \text{(Equation 2)}$$

where I_{CSBB} is from the calculation above, I_{LOAD} is current consumed from the external load, V_{SBBx} is the output voltage, and V_{IN} is the input voltage, ξ is the efficiency of the regulator.

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- V_{SBB2} is 3.3V
- C_{SBB2} = 10µF
- dV/dt_{SS} = 5mV/µs
- R_{LOAD2} = 330Ω (I_{LOAD2} = 3.3V/330Ω = 10mA)
- ξ is 80%

Calculation:

- I_{CSBB} = 10µF x 5mV/µs (from Equation 1)
- I_{CSBB} = 50mA
- $I_{IN} = \frac{(50mA + 10mA)\frac{3.3V}{3.5V}}{0.85}$ (from Equation1)
- I_{IN} ~ 71mA

SIMO Registers

Each SIMO buck-boost channel has a dedicated register to program its target output voltage (TV_SBBx) and its peak current limit (IP_SBBx). Additional controls are available for enabling/disabling the active discharge resistors (ADE_SBBx), as well as enabling/disabling the SIMO buck-boost channels (EN_SBBx). For a full description of bits, registers, default values, and reset conditions, refer to the *Programmer's Guide*.

SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on a ADE_SBBx and the status of the SIMO regulator. The active discharge feature can be enabled (ADE_SBBx = 1) or disabled (ADE_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever V_{SYS} is below $V_{SYSUVLO}$ and above V_{POR}.

These resistors discharge the output when ADE_SBBx = 1, and their respective SIMO channel is off. Note if the regulator is forced on through EN_SBBx = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when V_{SYS} is less than 1.0V, the NMOS transistors that control the active discharge resistors lose their gate drive and become open.

SIMO Applications Information

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, peak current limit setting, and the output current of the other SIMO channels. Maxim offers a SIMO calculator that outlines the available capacity for specific conditions. See *Support Materials* for more information on this and other engineering resources. Table 9 is an extraction from the calculator.

Inductor Selection

Choose an inductance from 1.0µH to 2.2uH; 1.5µH inductors work best for most designs. Larger inductances transfer more energy to the output for each cycle and typically result in larger output voltage ripple and better efficiency. See the *Output Capacitor Selection* section for more information on how to size your output capacitor in order to control ripple.

Table 9. SIMO Available Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3
V.IN.MIN	2.7V	3.2V	3.4V
R.L.DCR	0.1Ω	0.1Ω	0.12Ω
SBB1	1V at 100mA	1.2V at 50mA	1.2V at 20mA
SBB0	1.2V at 75mA	2.05V at 100mA	2.05V at 80mA
SBB2	1.8V at 50mA	3.3V at 30mA	3.3V at 10mA
I.PEAK.0	1A	0.866A	0.5A
I.PEAK.1	1A	0.707A	0.5A
I.PEAK.2	1A	1A	0.5A
Utilized Capacity	73	79	73

**R.C.IN = R.C.OUT = 5mΩ, L = 1.5µH*

Choose the inductor saturation current to be greater than or equal to the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I_{P_SBB}). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.866A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1.0A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system. For systems where the expected load currents are not well known, be conservative and choose the RMS current to be greater than or equal to the half of higher maximum peak current limit setting [I_{RMS}>=MAX(IP_SBB0, IP_SBB1, IP_SBB2)/2]. This is a safe/conservative choice because the SIMO buck-boost regulator implements a discontinuous conduction mode (DCM) control scheme, which returns the inductor current to zero each cycle.

Consider the DC-resistance (DCR), AC-resistance (ACR) and solution size of the inductor. Typically, smaller sized inductors have larger DC-resistance and larger AC-resistance that reduces efficiency and the available output current. Note that many inductor manufacturers have inductor families which contain different versions of core material in order to balance trade-offs between DCR, ACR (i.e., core losses), and component cost. For this SIMO regulator, inductors with the lowest ACR in the 1.0MHz to 2.0MHz region tend to provide the best efficiency.

See Table 10 for examples of inductors that work well with this device. This table was created in 2016. Inductor technology advances rapidly. Always consider the most current inductor technology for new designs to achieve the best possible performance.

Table 10. Example Inductors

MANUFACTURER	PART	L (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (Ω)	X (mm)	Y (mm)	Z (mm)
Samsung	CIGT201610EH2R2MN	2.2	2.9	2.7	0.073	2.0	1.6	1.0
Murata	DFE201610E-2R2M	2.2	2.6	1.9	0.117	2.0	1.6	1.0
Murata	DFE201610E-1R5M	1.5	2.4	3.2	0.076	2.0	1.6	1.0
Murata	DFE201210S-2R2M	2.2	2.3	1.80	0.127	2.0	1.2	1.0
Murata	DFE201210S-1R5M	1.5	2.2	2.6	0.086	2.0	1.2	1.0
Samsung	CIGT201208EH2R2MN	2.2	2.0	1.8	0.095	2.0	1.25	0.8
Murata	DFE201208S-1R5M	1.5	2.4	2.0	0.110	2.0	1.2	0.8
Murata	DFE201208S-2R2M	2.2	2.0	1.6	0.170	2.0	1.2	0.8

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN_SBB}) to be 10µF. Larger values of C_{IN_SBB} improve the decoupling for the SIMO regulator.

C_{IN_SBB} reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V max), use a 6.3V capacitor voltage rating.

IN_SBB is a critical discontinuous current path that requires careful bypassing. When the SIMO detects that an output is below its regulation threshold, a switching cycle begins and the IN_SBB current ramps up as a function of the input voltage and inductor ($di/dt = V_{IN\_SBB}/L$) until it reaches the peak current limit (I_{P_SBB}). Once I_{P_SBB} is reached, the IN_SBB current falls to zero rapidly (~5ns). This rapid current decrease makes the parasitic inductance in the PGND to input capacitor to IN_SBB path critical. In the PCB layout, place C_{IN_SBB} as close as possible to the power pins (IN_SBB and PGND) to minimize parasitic inductance. If making connections to the input capacitor through vias, ensure that the vias are rated for the expected input current so they do not contribute excess inductance and resistance between the bypass capacitor and the power pins.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 3.3nF. Smaller values of C_{BST} (< 1nF) result in insufficient gate drive for M3. Larger values of C_{BST} (> 10nF) have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitance (C_{SBBx}) based on the desired output voltage ripple; typical values are 10µF. Larger values of C_{SBBx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance, the output voltage, and the peak current limit setting. Maxim offers a SIMO calculator to aid in the selection of the output capacitance. See *Support Materials* for more information on this and other engineering resources.

Note that most designs concern themselves with having enough capacitance on the output but there is also a maximum capacitance limitation that is calculated within the SIMO Calculator; take care not to exceed the maximum capacitance.

C_{SBBx} is required to keep the output voltage ripple small. The impedance of the output capacitor (ESR, ESL) should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for an 0603 case size capacitor to perform well, while an 0402 case size capacitor of the same value performs poorly. The SIMO regulator is stable with low output capacitance (1µF) but the output voltage ripple would be large; consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

SBBx is a critical discontinuous current path that requires careful bypassing. When the SIMO detects that an output is below its target, it charges the inductor to a peak current limit (I_{P_SBB}) and then discharges that inductor into the output. At the moment the charge is applied to the output, the current increases rapidly and then decays relatively slowly ($dt/dt = V_{OUT}/L$). This rapid current increase is a function of the drive strength setting (DRV_SBB) and makes the parasitic inductance in the SBBx to output capacitor to PGND path critical. In the PCB layout, place C_{SBBx} as close as possible to SBBx and PGND to minimize parasitic inductance. If making connections to the output capacitor through vias, ensure that the vias are rated for the expected output current so they do not contribute excess inductance and resistance.

SIMO Switching Frequency

The SIMO buck-boost regulator utilizes a pulse frequency modulation (PFM) control scheme. The switching frequency for each output is a function of the input voltage, output voltage, load current, and inductance. Maxim offers a SIMO calculator to aid in the understanding of the switching frequency.

At no load, switching frequencies can be as low as 10Hz. It is possible to get SIMO switching frequencies that are high (5.7MHz) with all of the worst-case conditions: high input voltage (4.5V), low inductance (1.0µH), high output voltage (5.0V), low peak current limit (0.5A), and high utilization (80% which is 90mA with these conditions). With these high switching frequencies, the SIMO efficiency is poor. The maximum switching frequencies for designs should be no more than 3MHz. For example, in the 5.7MHz example above if we change the inductance to peak current limit from 0.5A to 0.707A while leaving the load current at 90mA, then the switching frequency drops to 2.4MHz. If we put the peak current limit at 0.866A and change the inductance to 1.5µH, then the switching frequency drops to 1MHz which provides a “nice” efficiency.

Unused Outputs

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, inductor current dumps into an open pin, and the output voltage can soar above the absolute maximum rating, potentially causing damage to the device. If the unused output is always disabled (EN_SBBx = 0x4 or 0x5), connect that output to ground. If an unused output can be enabled at any point during operation (such as startup or accidental software access), then implement one of the following:

- Bypass the unused output with a 1µF ceramic capacitor to ground.
- Connect the unused output to the power input (IN_SBB). This connection is beneficial because it does not require an external component for the unused output. The power input and its capacitance receives the energy packets when the regulator is enabled and V_{IN_SBB} is below the target output voltage of the unused output. Circulating the energy back to the power input ensures that the unused output voltage does not fly high.
  - Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx) such that connecting an unused output SBBx to IN_SBB creates a 140Ω (R_{AD_SBBx}) to ground until software can be ran to disable the active-discharge resistor. **Connecting an unused SBBx to IN_SBB is not recommended if the regulator's active-discharge resistor is enabled by default.**
- Connect the unused output to another power output that is above the target voltage of the unused output. In the same way as the option listed above, this connection is beneficial because it does not require an external component for the unused output. Unlike the option above, this connection is preferred in cases where the unused output voltage bias level is always above the unused output voltage target because no energy packages are provided to the unused output.
  - Note that some OTP options of the device have the active-discharge resistors enabled by default (ADE_SBBx). If the other power output used to bias the unused output is normally off, then the active-discharge resistor of the unused output does not create a continuous current draw. Remember that once the system is enabled, it should turn off the unused output's active-discharge resistor (ADE_SBBx = 0).

LDO

The device includes one on-chip low-dropout linear regulator (LDO). This LDO is optimized to have low-quiescent current and low dropout voltage. The input voltage range of this LDO (V_{IN_LDO}) allows it to be powered directly from the main energy source such as a Li-Poly battery or from an intermediate regulator. The linear regulator delivers up to 150mA.

Features

- 150mA LDO
- 1.8V to 5.5V Input Voltage Range
- Adjustable Output Voltage
- 180mV Maximum Dropout Voltage
- Programmable On-Chip Active Discharge

LDO Simplified Block Diagram

The LDO has one input (IN_LDO) and one output (LDO) and several ports that exchange information with the rest of the device (VREF, EN_LDO, ADE_LDO). VREF comes from the main bias circuits. EN_LDO and ADE_LDO are register bits for controlling the enable and active-discharge feature of the LDO. Refer to the *Programmer’s Guide* for more information.

LDO Active Discharge Resistor

The LDO has an active-discharge resistor (R_{AD_LDO}) that automatically enables/disables based on a configuration bit (ADE_LDO) and the status of the LDO regulator. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever V_{SYS} is above V_{POR} and V_{IN_LDO} is above 1.0V, the LDO active discharge resistor is turned on. Note that when V_{IN_LDO} is less than 1.0V, the NMOS transistor that controls the LDO active discharge resistor loses its gate drive and becomes open.

LDO Soft-Start

The soft-start feature of the LDO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The equation and example describes the input current surge phenomenon during startup.

The input current (I_{IN}) during soft-start is:

$$I_{IN} = C_{LDO}\frac{dV}{dt_{SS}} + I_{LDO}$$

where C_{LDO} is the capacitance on the output of the regulator, and dV/dt_{SS} is the voltage change rate of the output. For example, given the following conditions, the input current (I_{IN}) during soft-start is 22.5mA:

Given:

- C_{LDO} = 10µF
- dV/dt_{SS} = 1.25mV/µs
- R_{LDO} = 185Ω (I_{LDO} = 1.85V/185Ω = 10mA)

Calculation:

- I_{IN} = 10µF x 1.25mV/µs + 10mA
- I_{IN} = 22.5mA

LDO Applications Information

Input and Output Capacitor Selection

Sufficient input bypass capacitance (C_{IN_LDO}) and output capacitance (C_{LDO}) is required for stable operation of the LDO. Figure 19 provides guidance on capacitor selection and refers to required effective capacitance, which is the actual value of capacitance seen by the LDO during operation. Effective capacitance is almost always lower than the nominal capacitance and is a commonly overlooked design parameter. Determine the effective capacitance by assessing the capacitor's initial tolerance, variation with temperature, and variation with DC bias. Consult the capacitor manufacturer for specific details of derating.

Choose the input capacitor (C_{IN_LDO}) so that the effective capacitance is equal to or greater than the value found in Figure 19, based on expected load conditions for the application. A single 10µF, 1005/0402 (mm/inch) capacitor, is recommended for typical applications but ensure that the load current and derated capacitance does not compromise the stability curve in Figure 19. Larger values of C_{IN_LDO} improve stability and decoupling for the LDO regulator. The floorplan of the device is such that SBB0 is adjacent to IN_LDO, and if SBB0 powers the input of the LDO, then the two nodes can share the SBB0 output capacitor (C_{SBB0}). C_{IN_LDO} reduces the current peaks drawn from the battery or input power source during LDO regulator operation.

Choose the output capacitor (C_{LDO}) so that the effective capacitance is equal to or greater than the value found in Figure 19, based on expected load conditions for the application. A single 10µF, 1005/0402 (mm/inch) capacitor is recommended for typical applications, but ensure that the load current and derated capacitance does not compromise the stability curve in Figure 19. Larger values of C_{LDO} improve stability and output PSRR, but increases the input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed 100µF to maintain LDO stability.

For example, consider the case of the MAX77650A where:

1. Size is very important.
2. The LDO input is powered by SBB0, which is 2.05V.
3. The LDO output is 1.85V.
4. The LDO output current is ≤80mA.

A small 1005/0402 (mm/inch) capacitor such as the GRM155R60J106ME15 (Murata, 10µF, 6.3V X5R) gives 5.7µF at 60°C and 5.4µF at -20°C with the 1.85V bias voltage and has a ± 20% tolerance, so the worst-case effective capacitance is 4.3µF (5.4µF derated by 20% tolerance). With just 4.3µF of capacitance at the output, Figure 19 shows the LDO is stable with load currents of ≤35mA. To get stability at 80mA, 6µF is required. There are a few options to consider:

- Add more capacitors to the design.
- Replace the 1005/0402 (mm/inch) capacitor with a 1608/0603 (mm/inch) capacitor.
- Consider point-of-load capacitance in your assessment of effective capacitance. For example, if there is a point-of-load capacitor downstream from the LDO that is sufficiently close to the local LDO output capacitor, it can cover the gap. The capacitor can be considered "sufficiently close" if the PCB does not add more than 25nH and 25mΩ of extra ESR and ESL (more or less within 1").

Note the impedance of either the input or output capacitor (ESR, ESL) should be very low (i.e., ≤ 50mΩ + ≤ 5nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

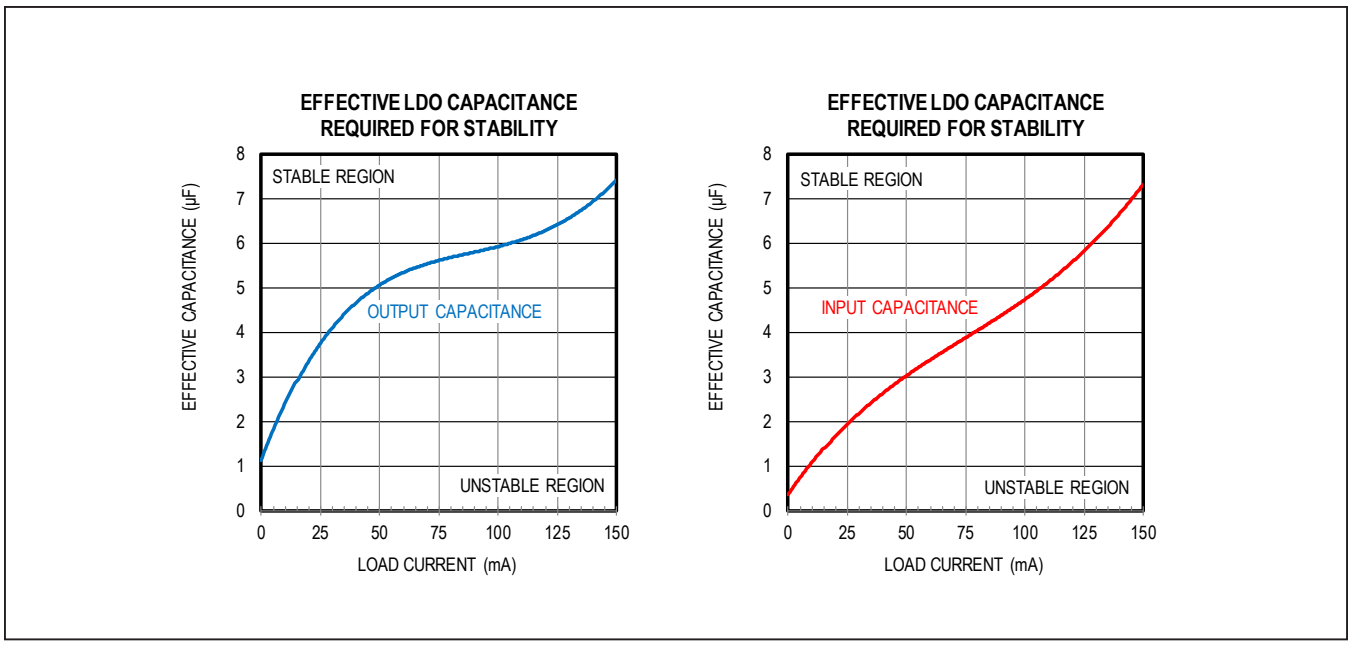


Figure 19. LDO Capacitance for Stability

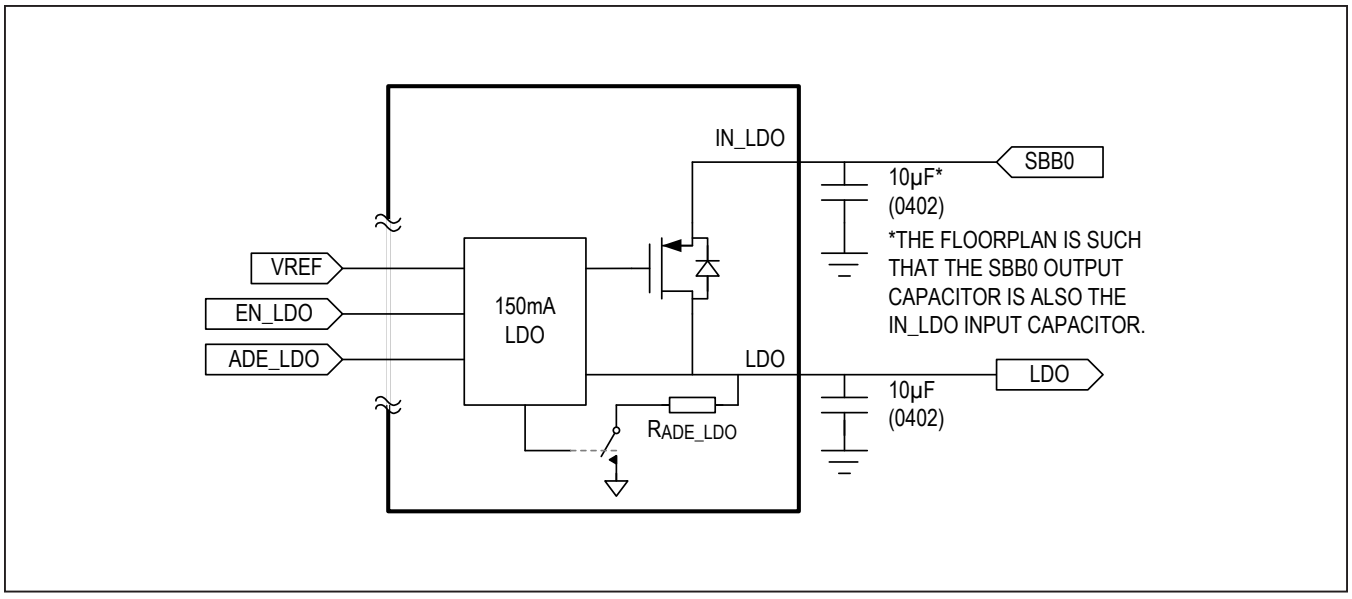


Figure 20. LDO Simplified Block Diagram

Current Sinks

The device has a 3-channel current sink driver designed to drive LED's in portable devices. This block can also be used as a general-purpose current sink driver for other applications. The driver's on-time and frequency are independently programmable for each output to achieve a desired blink pattern. Alternatively, the LEDs can be continuously on (i.e., not blinking). The blink period is programmable from 0.5s to 8s,with an on-time duty cycle from 6.25% to 100%.

Figure 21 utilizes a common set of clock dividers to drive three identical current sink modules. Refer to the *Programmer's Guide* for more information.

Current Sink Applications Information

LED Assignment

The three current sinks (LED0, LED1, LED2) are identical. In a typical application where a red, green, blue LED cluster is used (RGB), the assignment of the RGB elements to the LED0/1/2 pins should be done in whatever way makes the PCB layout the easiest.

Unused Current Sink Ports

If a current sink port is not utilized in a given application, connect that port to ground. Additionally, software should ensure that the unused current sink is not enabled (EN_LEDx = 0).

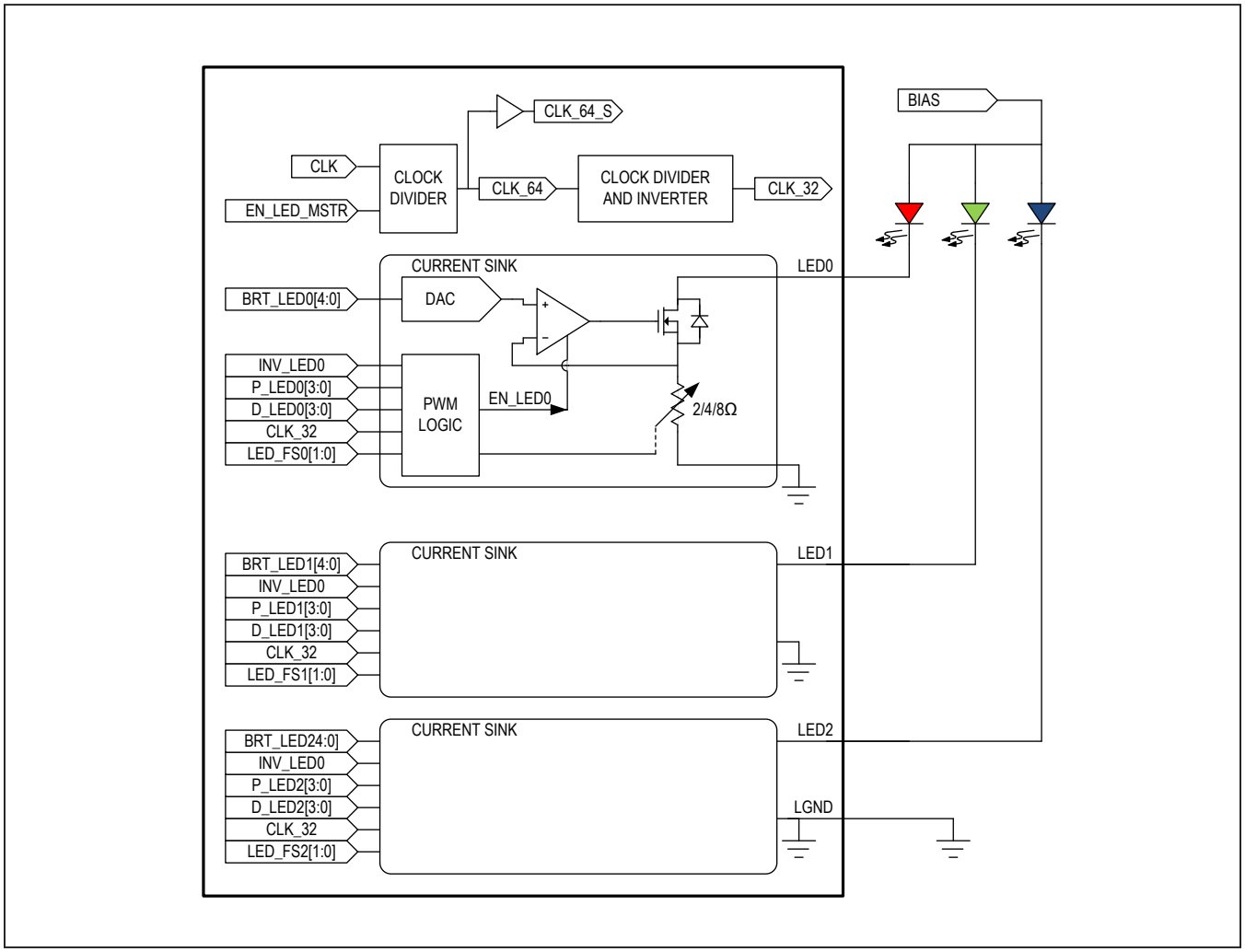


Figure 21. Current Sink Block Diagram

I²C Serial Interface

The MAX77650 features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77650/MAX77651 act as slave-only devices where they rely on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported. I²C is an open-drain bus, and therefore, SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals. Figure 22 shows the functional diagram for the I²C based communications controller. For additional information on I²C, refer to the *I²C Bus Specification and User Manual* that is available for free on the Internet.

Features

- I²C Revision 3 Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I²C Clock Stretching

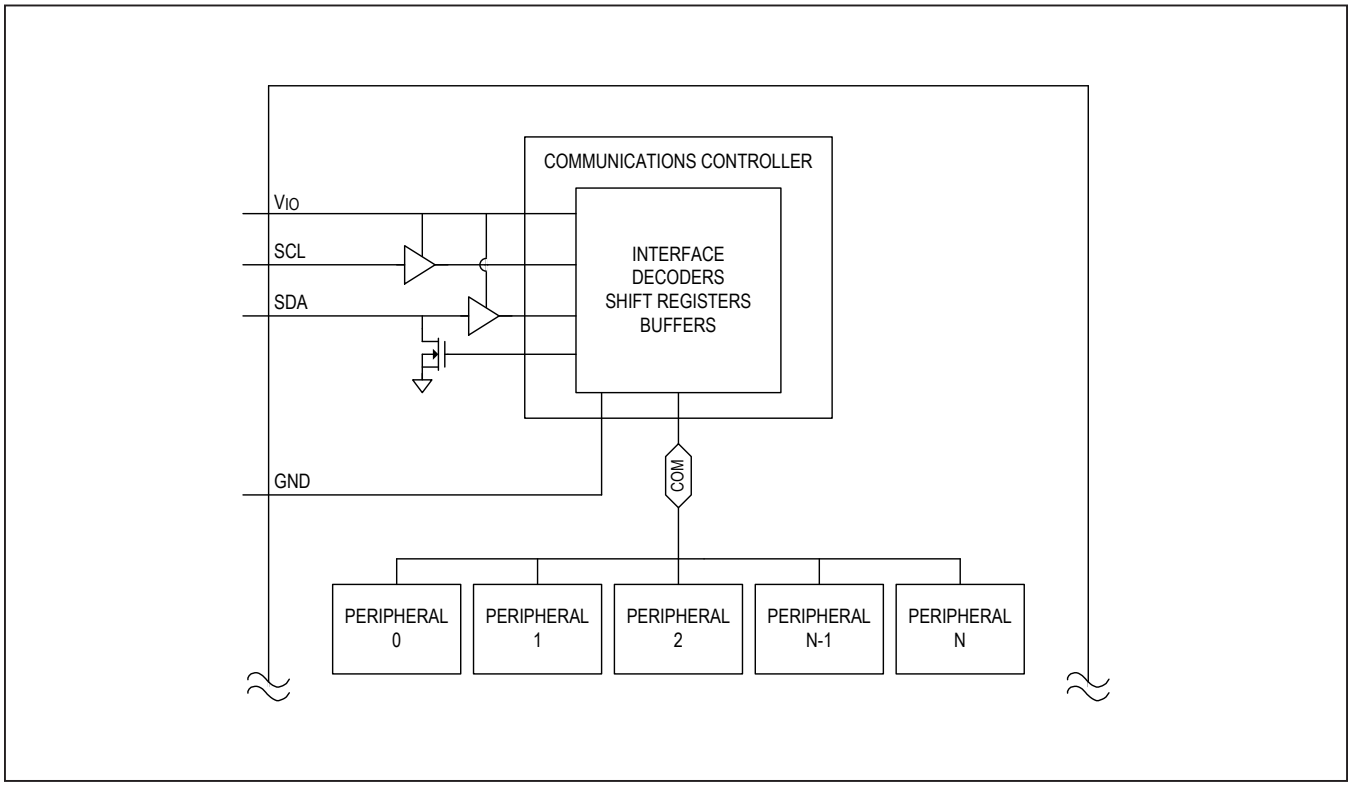


Figure 22. I²C Simplified Block Diagram

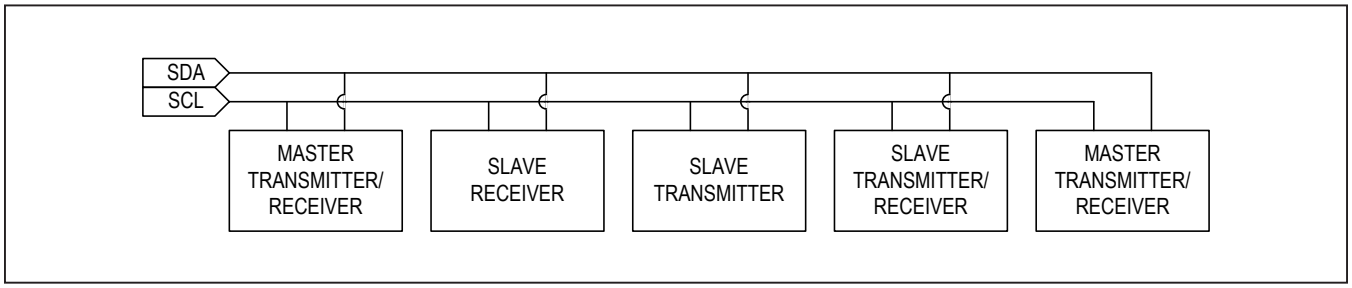


Figure 23. I²C System Configuration

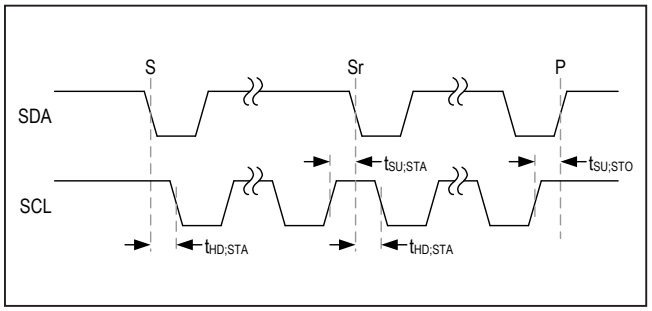


Figure 24. I²C Start and Stop Conditions

I²C System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The MAX77650/MAX77651 I²C compatible interface operates as a slave on the I²C bus with transmit and receive capabilities.

I²C Interface Power

The MAX77650/MAX77651 I²C interface derives its power from V_{IO}. Typically a power input such as V_{IO} would require a local 0.1µF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I²C registers. When V_{IO} is less than V_{IOUVLO} and V_{SYS} is less than $V_{SYSUVLO}$, SDA and SCL are high impedance.

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I²C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 24.

A START condition from the master signals the beginning of a transmission to the MAX77650/MAX77651. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition. See the *I²C Acknowledge Bit* section for information on the not-acknowledge. The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the MAX77650/MAX77651 internally disconnect SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

I²C Acknowledge Bit

Both the I²C bus master and the MAX77650/MAX77651 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 25. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

The MAX77650/MAX77651 issue an ACK for all register addresses in the possible address space even if the particular register does not exist.

I²C Slave Address

The I²C controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 26. The slave address is factory programmable to one of two options. See Table 11. All slave addresses not mentioned in the Table 11 are not acknowledged.

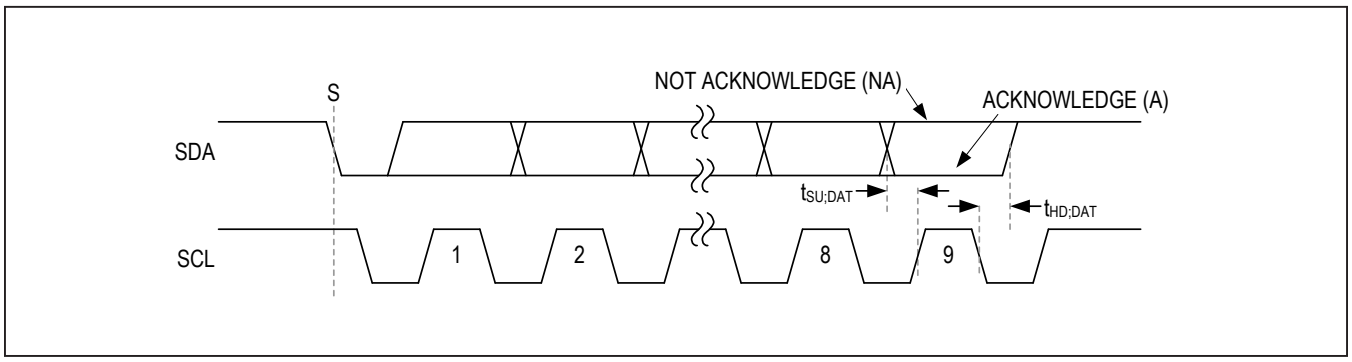


Figure 25. Acknowledge Bit

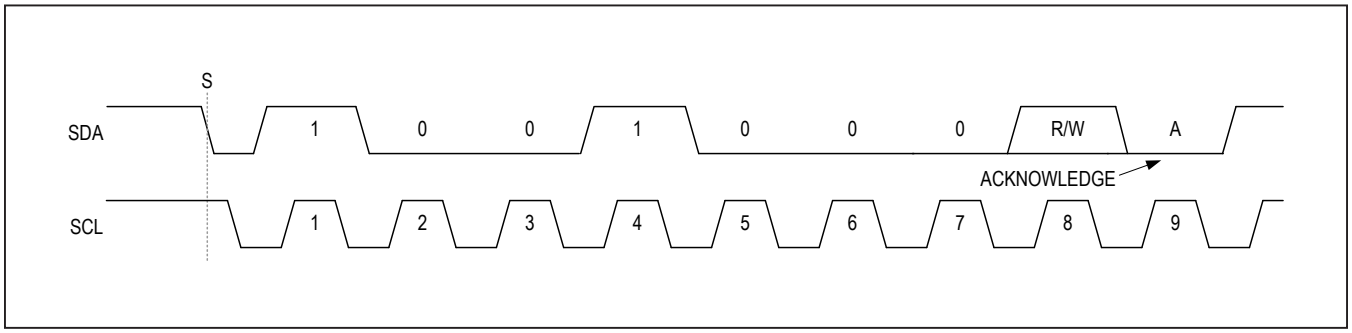


Figure 26. Slave Address Example

Table 11. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

**Perform all reads and writes on the Main Address. ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict. Contact Maxim for more information.*

***When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.*

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77650/MAX77651 do not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX77650/MAX77651 do not implement the I²C specifications general call address. If the MAX77650/MAX77651 see the general call address (0b0000_0000), they do not issue an acknowledge.

I²C Device ID

The MAX77650/MAX77651 do not support the I²C Device ID feature.

I²C Communication Speed

The MAX77650/MAX77651 are compatible with all 4 communication speed ranges as defined by the Revision 3 I²C specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the *I²C Bus Specification and User Manual* that is available for free on the Internet for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, lower value pullup resistors dissipate more power (V2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the *I²C Communication Speed* section. The major considerations with respect to the MAX77650/MAX77651:

- The I²C bus master use current source pull-ups to shorten the signal rise.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the MAX77650/MAX77651 input filters are set for standard mode, fast mode, and fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I²C Communication Protocols* section.

I²C Communication Protocols

The MAX77650/MAX77651 supports both writing and reading from its registers.

Writing to a Single Register

Figure 27 shows the protocol for the I²C master device to write one byte of data to the MAX77650/MAX77651. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a data byte.
- The slave updates with the new data
- The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

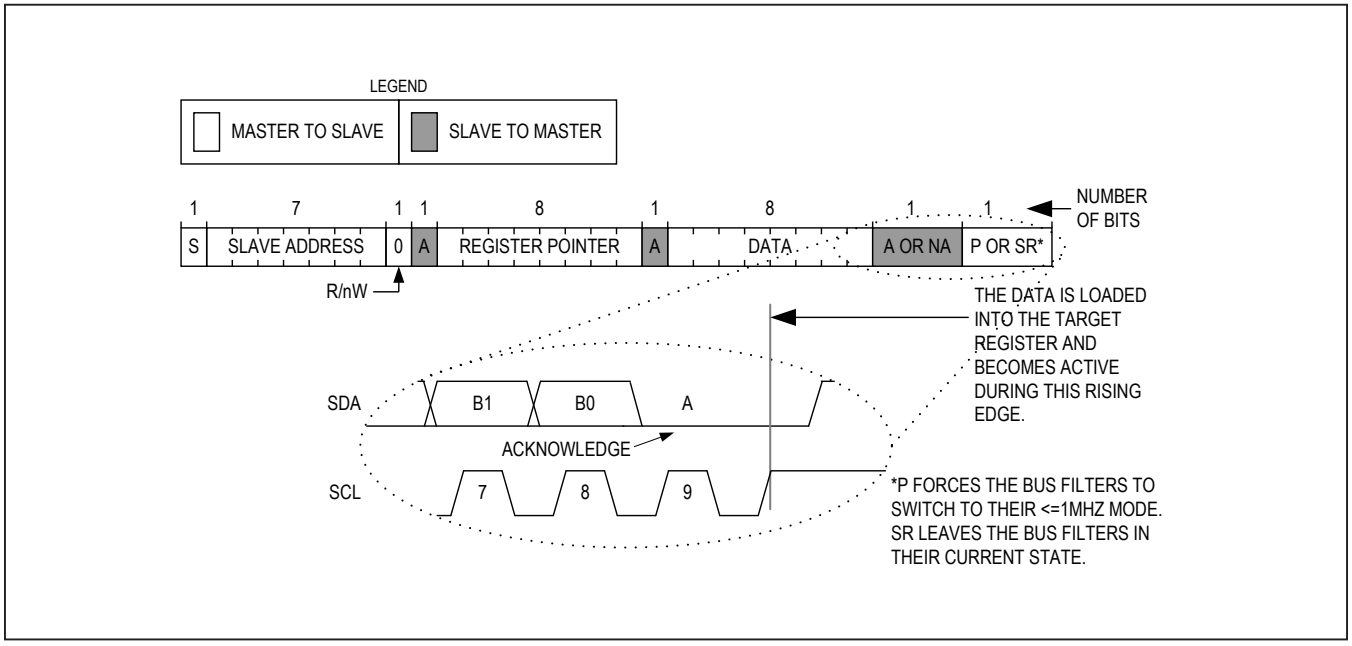


Figure 27. Writing to a Single Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 28 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a data byte.
- The slave acknowledges the data byte. The next rising edge on SDA load the data byte into its target register and the data will become active.
- Steps 6 to 7 are repeated as many times as the master requires.
- During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

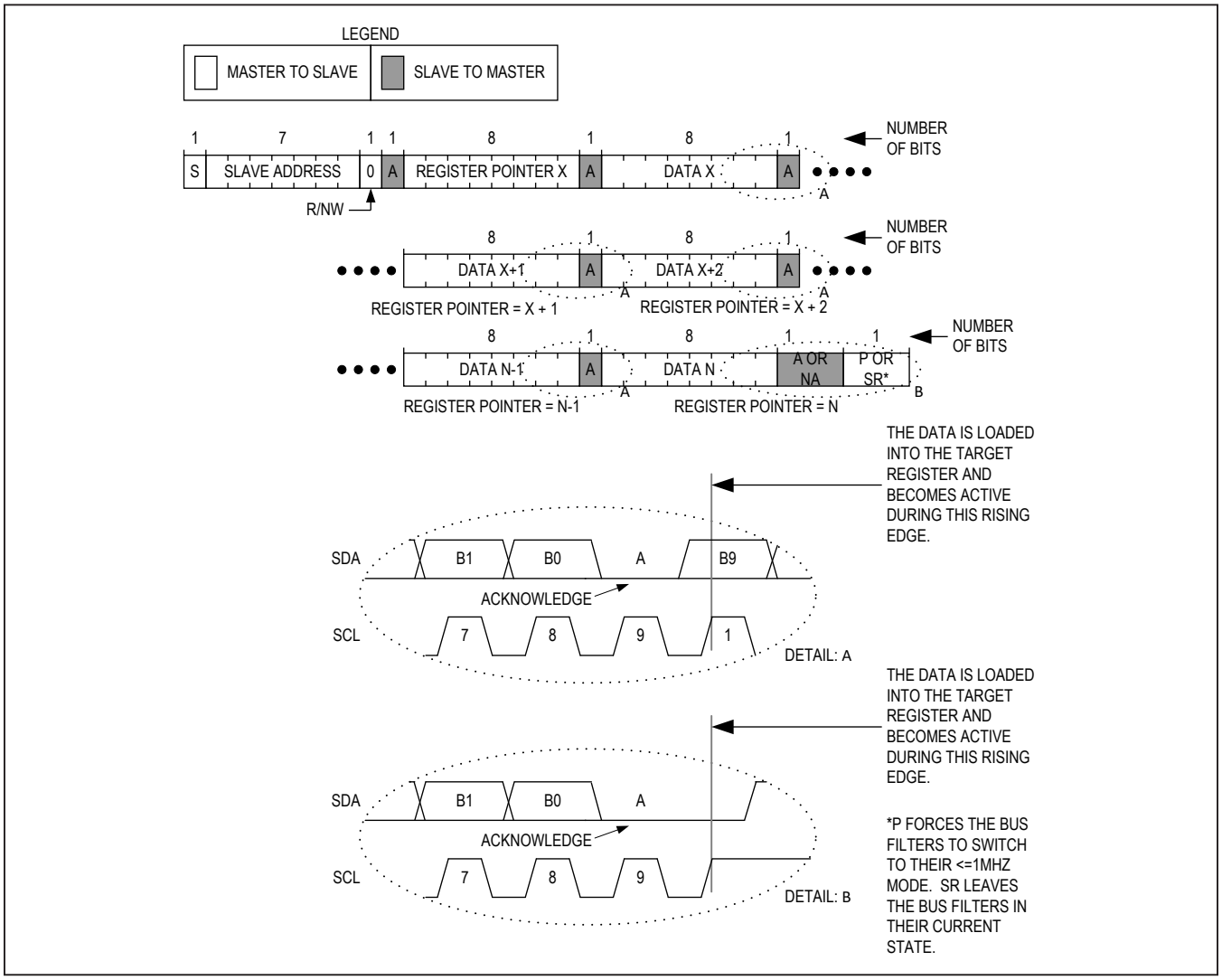


Figure 28. Writing to Sequential registers X to N

Reading from a Single Register

Figure 29 shows the protocol for the I2C master device to read one byte of data to the MAX77650/MAX77651. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a repeated start command (Sr).
- The master sends the 7-bit slave address followed by a read bit (R/W = 1).
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- The master issues a not acknowledge (nA).
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the MAX77650/MAX77651 receive a stop they do not modify their register pointer.

Reading from Sequential Registers

Figure 30 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

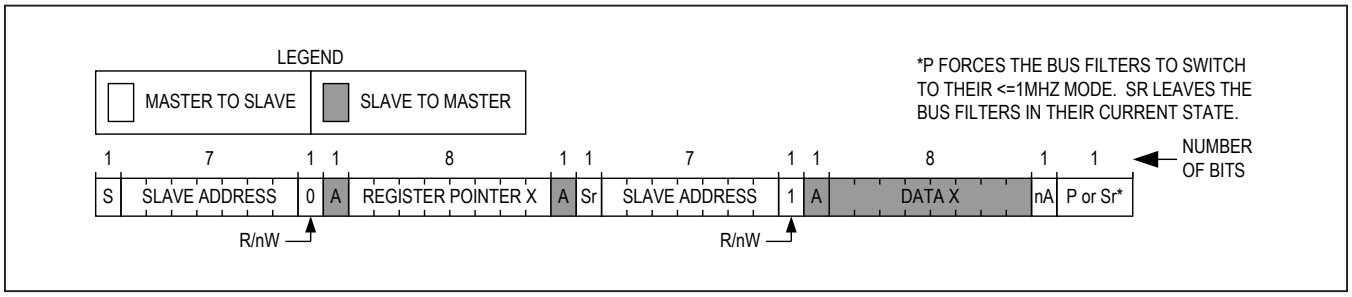


Figure 29. Reading from a Single Register with the Read Byte Protocol

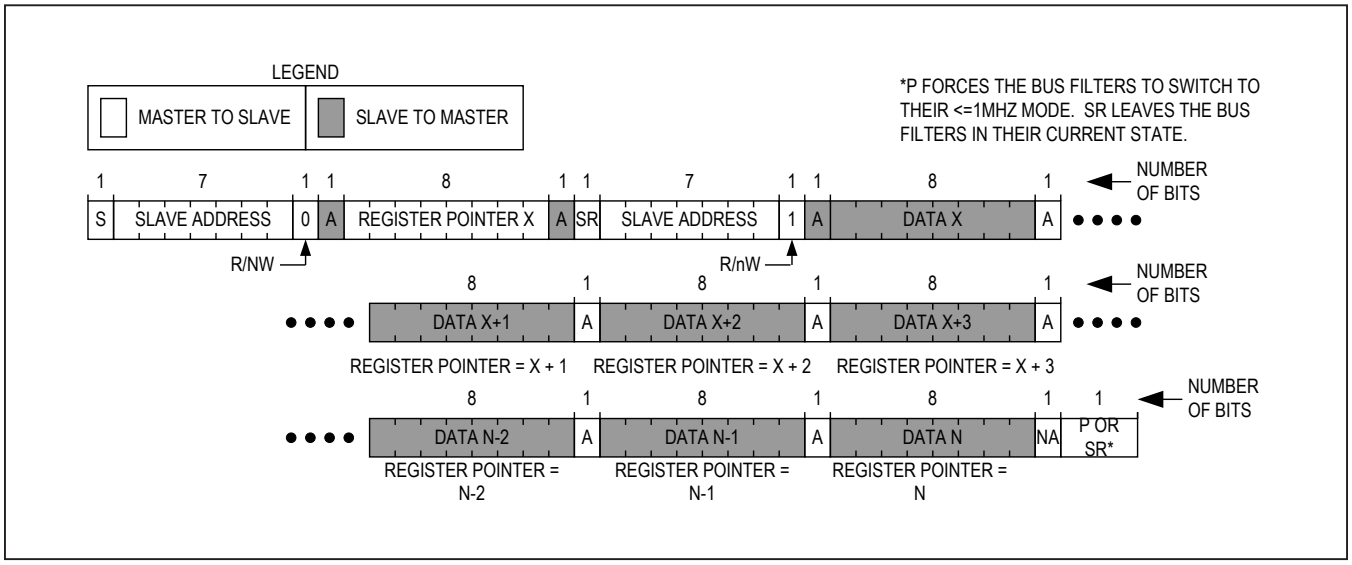


Figure 30. Reading Continuously from Sequential Registers X to N

The continuous read from sequential registers protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a repeated start command (Sr).
- The master sends the 7-bit slave address followed by a read bit (R/W = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
- Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the MAX77650/MAX77651 receive a stop, they do not modify their register pointers.

Engaging HS-mode for operation up to 3.4MHz

Figure 31 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

- Begin the protocol while operating at a bus speed of 1MHz or lower
- The master sends a start command (S).
- The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
- The addressed slave issues a not acknowledge (nA).
- The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high speed mode, use repeated start (Sr).

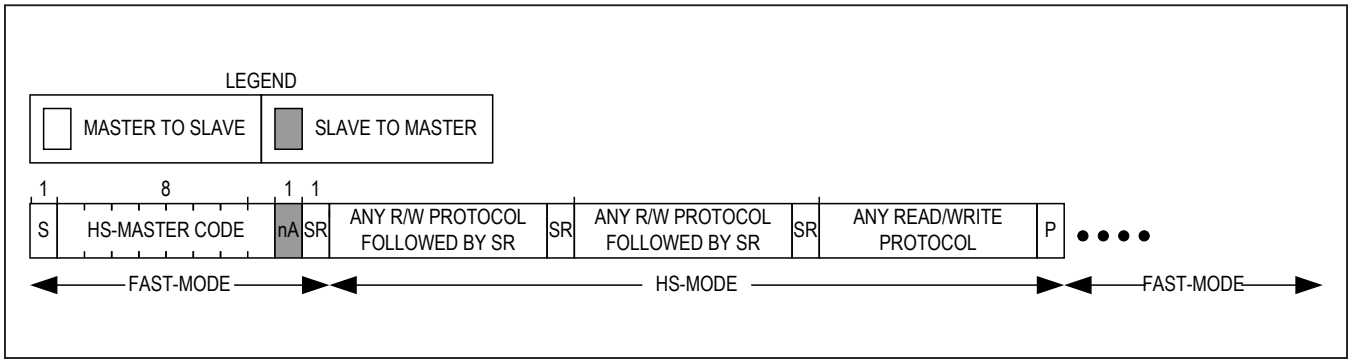
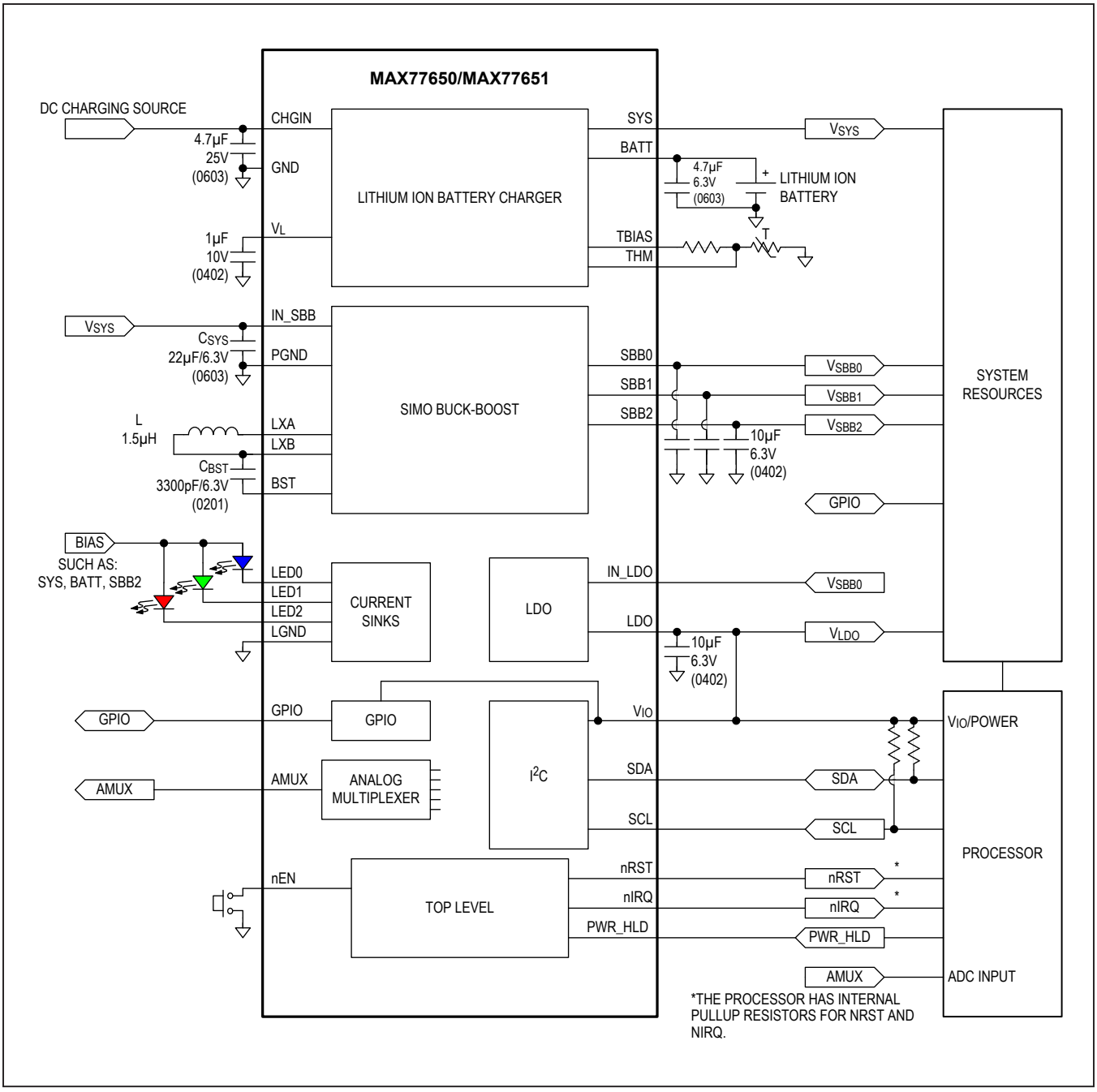


Figure 31. Engaging HS Mode

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OPTIONS
MAX77650EWV+T*	-40°C to +85°C	30 WLP	Samples with various OTP options
MAX77650AEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 2.05V/1.2V/3.3V, production device, DIDM = 0b00, CID = 0b0011**
MAX77650BEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 1.8V/1.2V/3.15V, production device, DIDM = 0b00, CID = 0b1110**
MAX77650CEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 1.8V/1.0V/1.2V, production device, DIDM = 0b00, CID = 0b1010**
MAX77650MEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 1.8V/1.2V/3.15V, production device, DIDM = 0b00, CID = 0b1000**
MAX77651EWV+T*	-40°C to +85°C	30 WLP	Samples with various OTP options
MAX77651AEWV+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 1.8V/4.6V/3.6V, production device, DIDM = 0b01, CID = 0b0110**
MAX77651BEWVA+T	-40°C to +85°C	30 WLP	SBB0/SBB1/SBB2 values 1.9V/3.2V/5.2V, production device, DIDM = 0b01, CID = 0b1000**

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Custom samples only. Not for production or stock. Contact factory for more information.*

***See the Programmer's Guide for the options associated with a specified DIDM and CID.*