

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## General Description

The MAX8563/MAX8564/MAX8564A ultra-low-output dual and triple LDO controllers allow flexible and inexpensive point-of-load voltage conversion in motherboards, desknotes, notebooks, and other applications.

These parts feature a 0.5V reference voltage with ±1% accuracy providing tight regulation of the output voltage. The MAX8563 has three n-channel MOSFET controller outputs, and the MAX8564/MAX8564A has two controller outputs.

Each controller output is adjustable from 0.5V to 3.3V when  $V_{DD} = 12V$  and between 0.5V and 1.8V when  $V_{DD} = 5V$ . Each output is independently enabled and asserts a POK signal when the output reaches 94% of the set value. Each output is protected against a soft short-circuit condition by an undervoltage comparator that disables the output when it drops to under 80% of the set voltage for more than 50 $\mu$ s. For a catastrophic short condition, the regulators are shut down immediately if the output drops below 60% of the set voltage.

The MAX8563 is available in a 16-pin QSOP package, and the MAX8564/MAX8564A are available in a 10-pin  $\mu$ MAX<sup>®</sup> package.

## Applications

|                            |                                |
|----------------------------|--------------------------------|
| Motherboards               | Ultra-Low-Dropout              |
| Dual/Triple Power Supplies | Voltage Regulators             |
| Desknotes and Notebooks    | Low-Voltage DSP, $\mu$ P, and  |
| Graphic Cards              | Microcontroller Power Supplies |

## Features

- ◆ MAX8563: 3 Outputs
- ◆ MAX8564/MAX8564A: 2 Outputs
- ◆ ±1% Feedback Regulation
- ◆ Adjustable Output Voltage Down to 0.5V
- ◆ Can Use Ceramic Output Capacitors
- ◆ Wide Supply Voltage Range Permits Operation from 5V or 12V Rails
- ◆ Individual Enable Control and POK Signal Allows Sequencing
- ◆ Overload Protection Against Soft Short-Circuit Condition
- ◆ Undervoltage Short-Circuit Protection
- ◆ Drive n-Channel MOSFETs

## Ordering Information

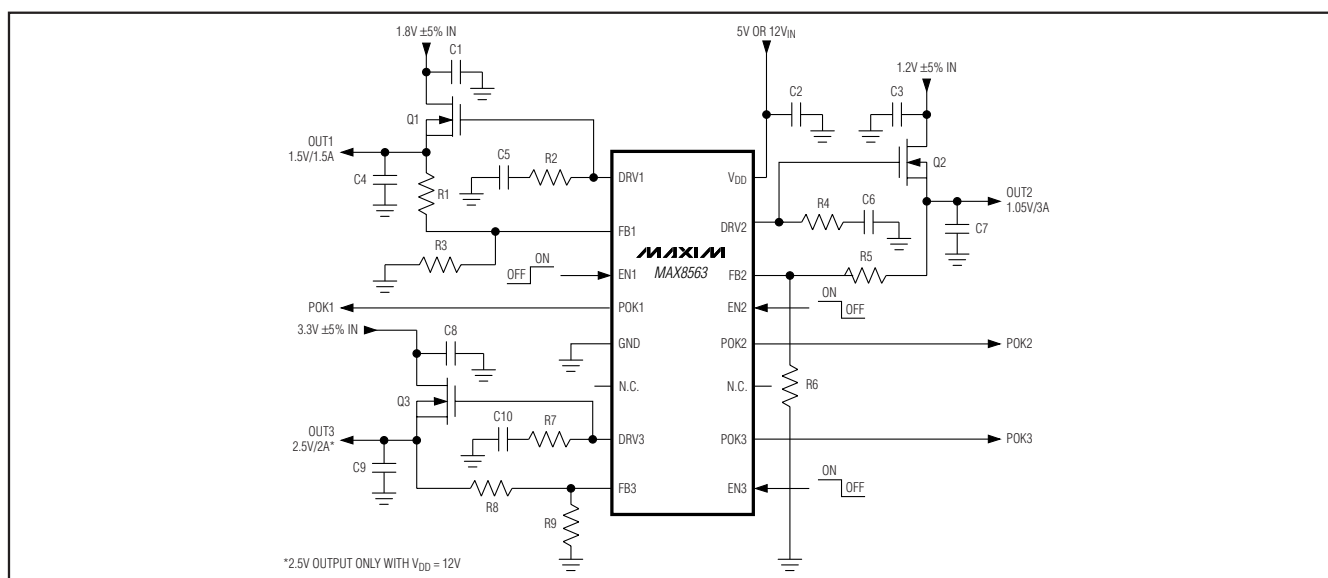
| PART         | TEMP RANGE     | PIN-PACKAGE  | PKG CODE |
|--------------|----------------|--------------|----------|
| MAX8563EEE   | -40°C to +85°C | 16 QSOP      | E16-1    |
| MAX8564EUB   | -40°C to +85°C | 10 $\mu$ MAX | U10-2    |
| MAX8564AEUB+ | -40°C to +85°C | 10 $\mu$ MAX | U10-2    |

+Denotes lead-free package.

Pin Configurations appear at end of data sheet.

$\mu$ MAX is a registered trademark of Maxim Integrated Products, Inc.

## Typical Operating Circuit



# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub> to GND .....-0.3V to +14V  
 DRV1, DRV2, DRV3, EN1, EN2,  
 EN3 to GND .....-0.3V to (V<sub>DD</sub> + 0.3V)  
 FB1, FB2, FB3, POK1, POK2, POK3 to GND .....-0.3V to +6V  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 10-Pin μMAX (derate 5.6mW/°C above +70°C) .....444.4mW  
 16-Pin QSOP (derate 8.3mW/°C above +70°C) .....666.7mW

Operating Temperature Range .....-40°C to +85°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = V<sub>EN1</sub> = V<sub>EN2</sub> = V<sub>EN3</sub> = 5V, V<sub>GND</sub> = 0V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                                      | CONDITIONS  |                                 | MIN   | TYP   | MAX   | UNITS |
|--|---|---------------------------------|-------|-------|-------|-------|
| <b>GENERAL</b>                                 |   |                                 |       |       |       |       |
| V <sub>DD</sub> Voltage Range                  |   |                                 | 4.5   |       | 13.2  | V     |
| V <sub>DD</sub> Undervoltage-Lockout Threshold | Rising, 200mV hysteresis (typ)  |                                 | 3.56  | 3.76  | 4.00  | V     |
| V <sub>DD</sub> Quiescent Current              | V <sub>EN_</sub> = V <sub>DD</sub> = 12V (MAX8563)                    |                                 |       | 930   | 1600  | μA    |
|  | V <sub>EN_</sub> = V <sub>DD</sub> = 12V (MAX8564/MAX8564A)           |                                 |       | 660   | 1200  |       |
| V <sub>DD</sub> Shutdown Current               | EN1 = EN2 = EN3 = GND, V <sub>DD</sub> = 12V                          |                                 |       |       | 25    | μA    |
| <b>LDOs</b>                                    |   |                                 |       |       |       |       |
| FB_ Accuracy                                   | T <sub>A</sub> = 0°C to +85°C   |                                 | 0.494 | 0.5   | 0.504 | V     |
|  | T <sub>A</sub> = -40°C to +85°C                                       |                                 | 0.489 |       | 0.509 |       |
| FB_ Input Bias Current                         | T <sub>A</sub> = +25°C  |                                 | -100  |       | +100  | nA    |
|  | T <sub>A</sub> = +85°C  |                                 |       | -8    |       |       |
| DRV_ Soft-Start Charging Current               | MAX8563, MAX8564  |                                 |       | 100   |       | μA    |
|  | MAX8564A  |                                 |       | 10    |       |       |
| DRV_ Max Sourcing Current                      | V <sub>FB_</sub> = 0.45V  | T <sub>A</sub> = 0°C to +85°C   | 4     |       |       | mA    |
|  |   | T <sub>A</sub> = -40°C to +85°C | 3     | 7     |       |       |
| DRV_ Max Sinking Current                       | V <sub>FB_</sub> = 0.6V   | T <sub>A</sub> = 0°C to +85°C   | 3     |       |       | mA    |
|  |   | T <sub>A</sub> = -40°C to +85°C | 1.8   | 7     |       |       |
| DRV_ Max Voltage                               | V <sub>DD</sub> = 5V, V <sub>FB_</sub> = 0.46V                        |                                 | 4.7   |       |       | V     |
|  | V <sub>DD</sub> = 13.2V, V <sub>FB_</sub> = 0.46V                     |                                 | 8.0   |       | 10.9  |       |
| FB_ Slow Short-Circuit Threshold               | Measured at FB_ (falling)   |                                 |       | 400   |       | mV    |
| FB_ Fast Short-Circuit Threshold               | Measured at FB_ (falling)   |                                 |       | 300   |       | mV    |
| Slow Short-Circuit Timer                       |   |                                 |       | 50    |       | μs    |
| FB_ to DRV_ Transconductance                   |   |                                 | 0.115 | 0.24  | 0.460 | Mho   |
| <b>LOGIC</b>                                   |   |                                 |       |       |       |       |
| EN_ Input Low Level                            |   |                                 |       |       | 0.7   | V     |
| EN_ Input High Level                           |   |                                 | 1.3   |       |       | V     |
| EN_ Input Leakage Current                      | V <sub>EN_</sub> = 0 and V <sub>DD</sub> ,<br>V <sub>DD</sub> = 13.2V | T <sub>A</sub> = +25°C          | -0.1  |       | +0.1  | μA    |
|  |   | T <sub>A</sub> = +85°C          |       | 0.001 |       |       |

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## ELECTRICAL CHARACTERISTICS (continued)

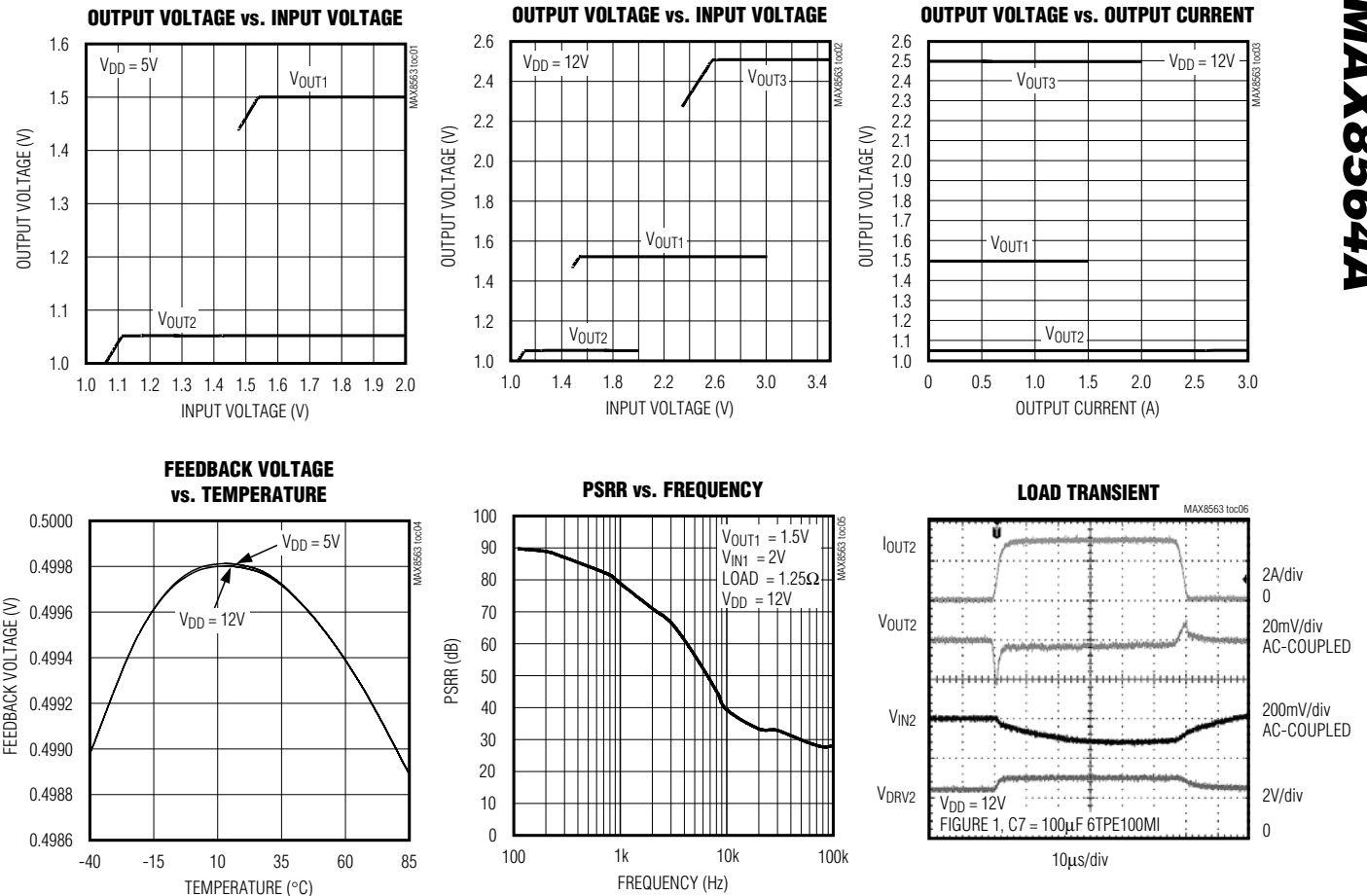
( $V_{DD} = V_{EN1} = V_{EN2} = V_{EN3} = 5V$ ,  $V_{GND} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

| PARAMETER                        | CONDITIONS                                       | MIN                  | TYP | MAX   | UNITS   |
|----------------------------------|--|----------------------|-----|-------|---------|
| POK_ Threshold Falling           | Measured at FB_ (falling)                        | 425                  | 440 | 455   | mV      |
| POK_ Threshold Rising at Startup | Measured at FB_ (rising)                         | 455                  | 470 | 485   | mV      |
| POK_ Output Low Level            | Sinking 1mA, $V_{DD} = 4.5V$ , $V_{FB\_} = 0.4V$ |                      |     | 0.1   | V       |
| POK_ Output High Leakage         | $V_{DD} = 5.5V$                                  | $T_A = +25^{\circ}C$ |     | 0.1   | $\mu A$ |
|                                  |  | $T_A = +85^{\circ}C$ |     | 0.001 |         |

**Note 1:** Specifications are production tested at  $T_A = +25^{\circ}C$ . Maximum and minimum specifications over temperature are guaranteed by design.

## Typical Operating Characteristics

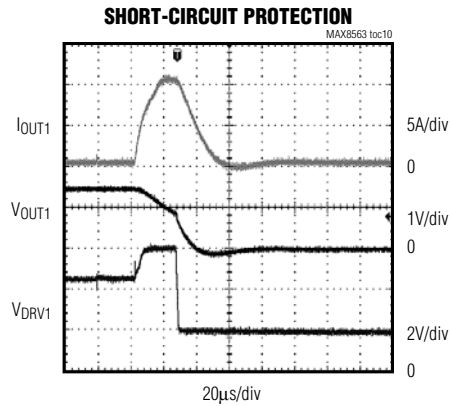
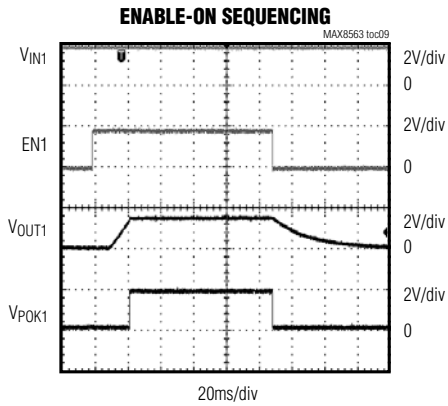
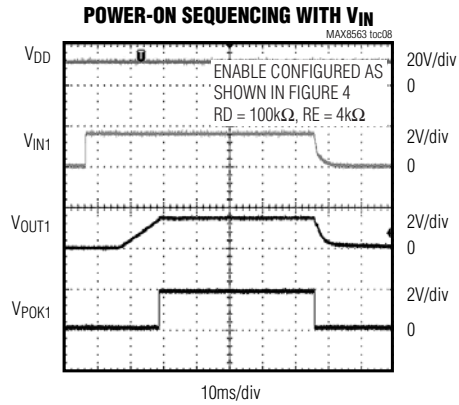
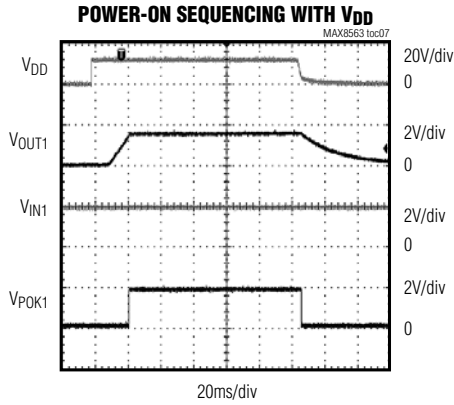
(Circuit of Figure 1,  $T_A = +25^{\circ}C$ .)



# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

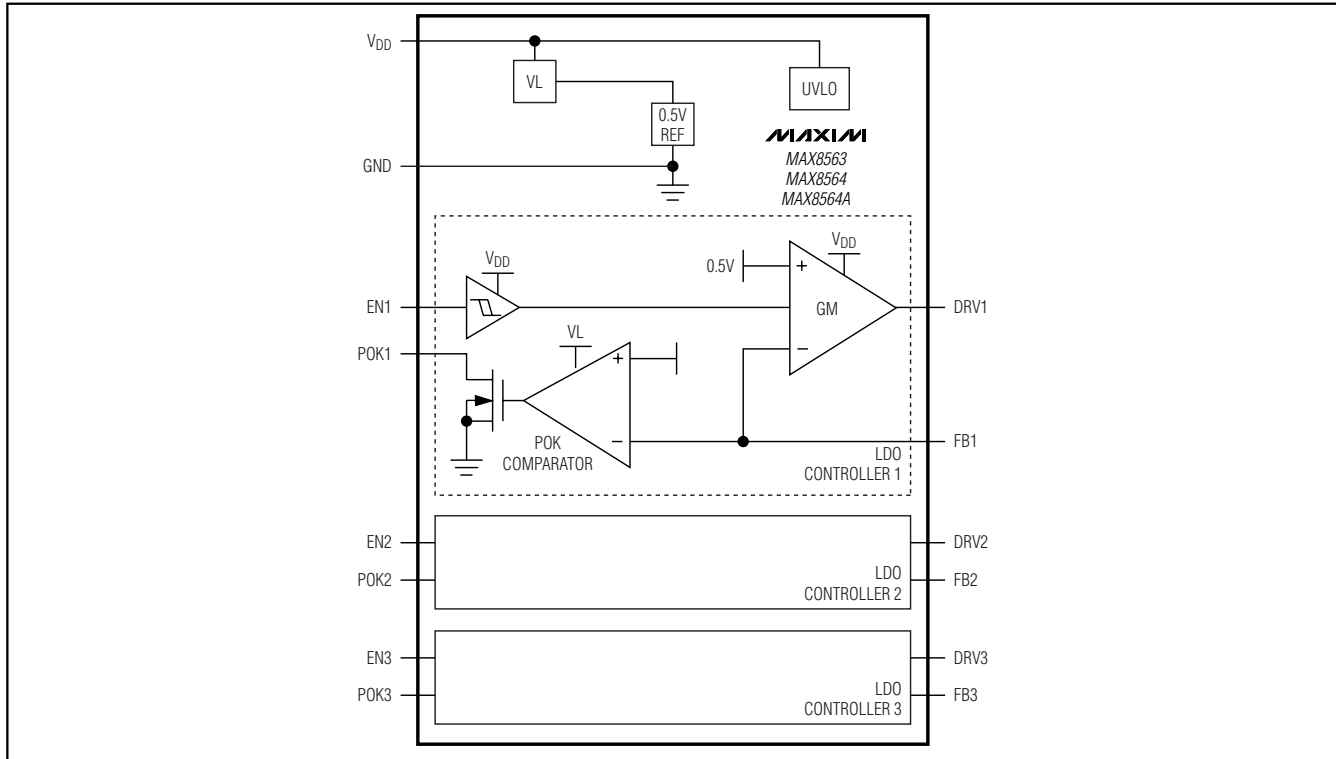
## Typical Operating Characteristics (continued)

(Circuit of Figure 1, T<sub>A</sub> = +25°C.)



# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Functional Diagram



## Pin Description

| PIN | NAME    |                      | FUNCTION   |
|-----|---------|----------------------|--|
|     | MAX8563 | MAX8564/<br>MAX8564A |  |
| 1   | DRV1    | DRV1                 | Output n-MOSFET Drive. Drives the gate of an external n-channel MOSFET to regulate output 1. DRV1 is internally pulled to ground when EN1 is logic low. Connect an external series RC circuit for compensation. See the <i>Stability Compensation</i> section. |
| 2   | FB1     | FB1                  | Feedback Input for Output 1. Connect to the center of a resistor-divider between output 1 and GND to set the output voltage of output 1. The feedback regulation voltage is 0.500V. See the <i>Output Voltage Setting</i> section.                             |
| 3   | EN1     | EN1                  | Enable Control for Output 1. Drive logic high to enable output 1, or logic low to disable the output. Connect to VDD for always-on operation.  |
| 4   | POK1    | POK1                 | Output 1 Power-Good Signal. Open-drain output pulls low when output 1 is 12% below the nominal regulated voltage.  |
| 5   | GND     | GND                  | Ground   |
| 6   | —       | POK2                 | Output 2 Power-Good Signal. Open-drain output pulls low when output 2 is 12% below the nominal regulated voltage.  |
|     | N.C.    | —                    | No Internal Connection   |

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Pin Description (continued)

| PIN | NAME            |                      | FUNCTION  |
|-----|-----------------|----------------------|---|
|     | MAX8563         | MAX8564/<br>MAX8564A |   |
| 7   | —               | EN2                  | Enable Control for Output 2. Drive logic high to enable output 2, or logic low to disable the output. Connect to V <sub>DD</sub> for always-on operation.   |
|     | DRV3            | —                    | Output 3 n-MOSFET Drive. Drives the gate of an external n-channel MOSFET to regulate output 3. DRV3 is internally pulled to ground when EN3 is logic low. Connect an external series RC circuit for compensation. See the <i>Stability Compensation</i> section.  |
| 8   | —               | FB2                  | Feedback Input for Output 2. Connect to the center of a resistor-divider between output 2 and GND to set the output voltage of output 2. The feedback regulation voltage is 0.500V. See the <i>Output Voltage Setting</i> section.                                |
|     | FB3             | —                    | Feedback Input for Output 3. Connect to the center of a resistor-divider between output 3 and GND to set the output voltage of output 3. The feedback regulation voltage is 0.500V. See the <i>Output Voltage Setting</i> section.                                |
| 9   | —               | DRV2                 | Output 2 n-MOSFET Drive. Drives the gate of the external n-channel MOSFET to regulate output 2. DRV2 is internally pulled to ground when EN2 is logic low. Connect an external series RC circuit for compensation. See the <i>Stability Compensation</i> section. |
|     | EN3             | —                    | Enable Control for Output 3. Drive logic high to enable output 3, or logic low to disable the output. Connect to V <sub>DD</sub> for always-on operation.   |
| 10  | —               | V <sub>DD</sub>      | +5V or +12V Supply Input. Connect to external +5V or +12V supply rail. Bypass with a 0.1μF ceramic or larger capacitor.   |
|     | POK3            | —                    | Output 3 Power-Good Signal. Open-drain output pulls low when output 3 is 12% below the nominal regulated voltage.   |
| 11  | N.C.            | —                    | No Internal Connection  |
| 12  | POK2            | —                    | Output 2 Power-Good Signal. Open-drain output pulls low when output 2 is 12% below the nominal regulated voltage.   |
| 13  | EN2             | —                    | Enable Control for Output 2. Drive logic high to enable output 2, or logic low to disable the output. Connect to a V <sub>DD</sub> for always-on operation.   |
| 14  | FB2             | —                    | Feedback Input for Output 2. Connect to the center of a resistor-divider between output 2 and GND to set the output voltage of output 2. The feedback regulation voltage is 0.500V. See the <i>Output Voltage Setting</i> section.                                |
| 15  | DRV2            | —                    | Output 2 n-MOSFET Drive. Drives the gate of the external n-channel MOSFET to regulate output 2. DRV2 is internally pulled to ground when EN2 is logic low. Connect an external series RC circuit for compensation. See the <i>Stability Compensation</i> section. |
| 16  | V <sub>DD</sub> | —                    | +5V or +12V Supply Input. Connect to an external +5V or +12V supply rail. Bypass with a 0.1μF ceramic or larger capacitor.  |

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Typical Application Circuits

### MAX8563: Triple Output

MAX8563/MAX8564/MAX8564A

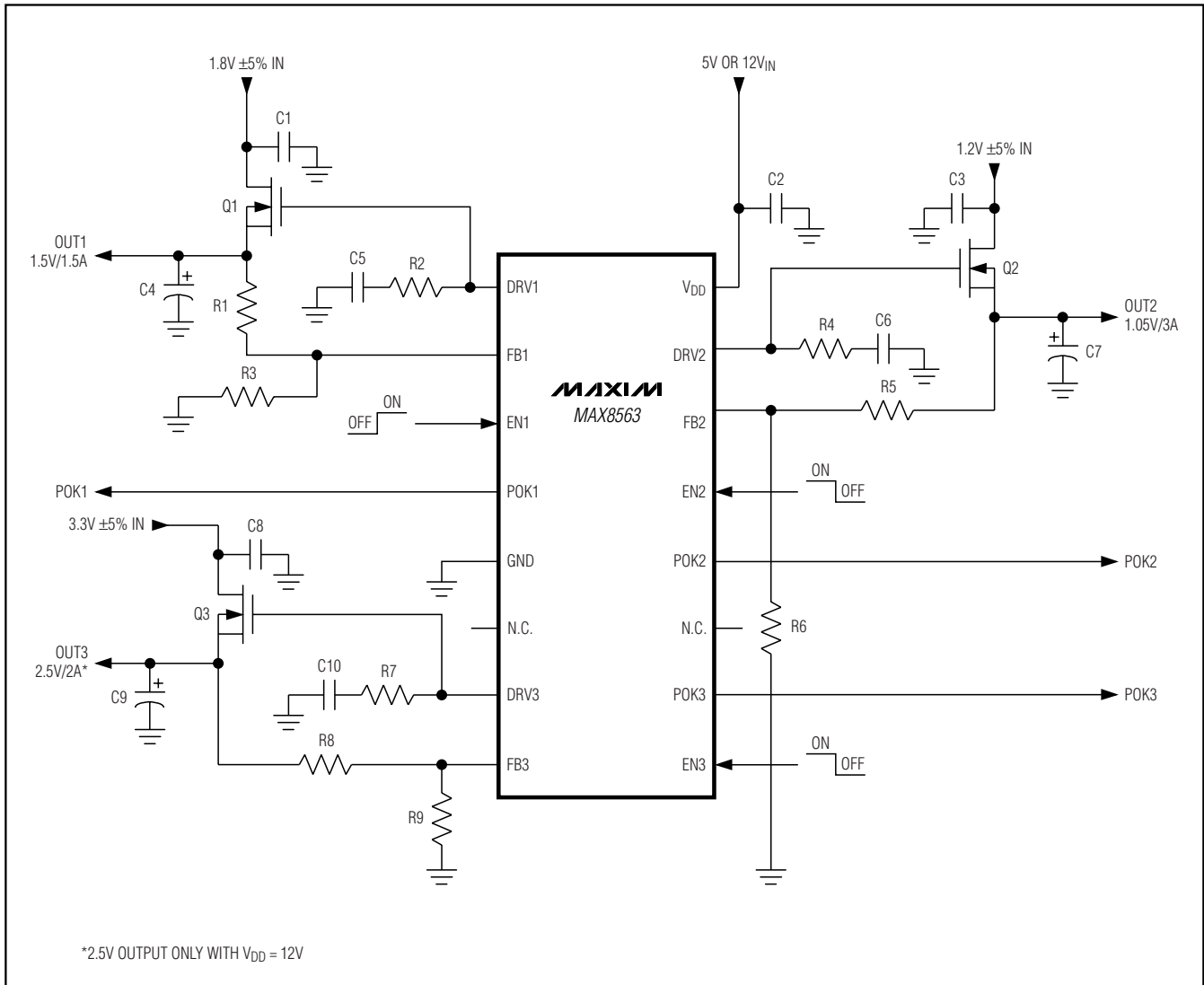


Figure 1. MAX8563 Typical Application Circuit

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Typical Application Circuits (continued)

### MAX8564/MAX8564A: Dual Output

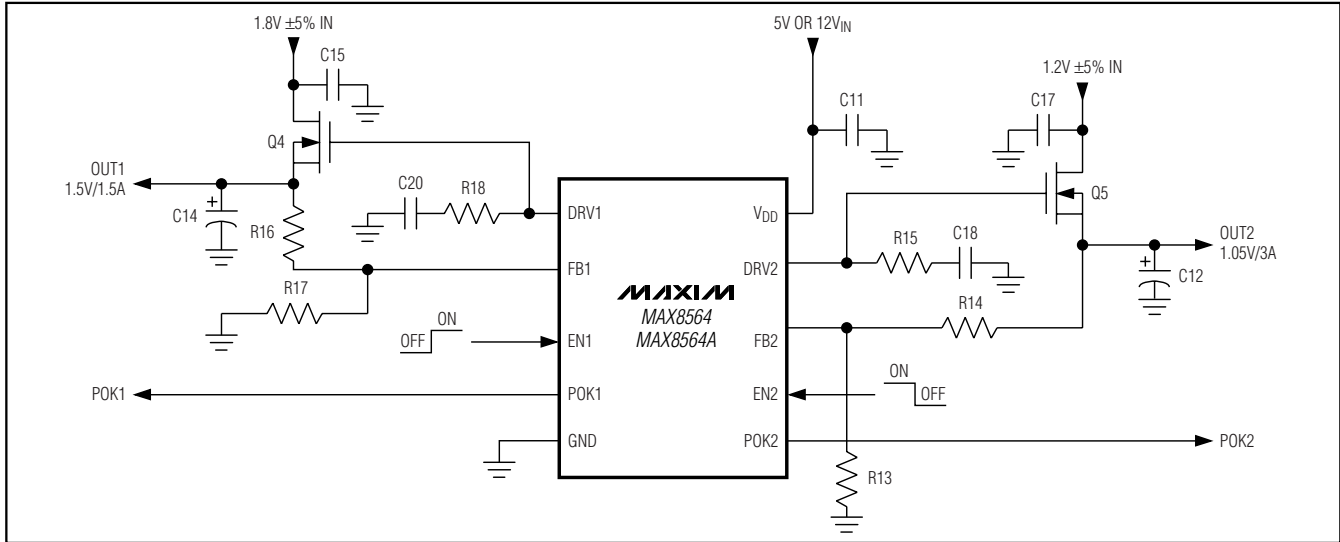


Figure 2. MAX8564/MAX8564A Typical Application Circuit

### MAX8563 External Component List

| COMPONENTS   | QTY | DESCRIPTION   |
|--------------|-----|---|
| C1, C3, C8   | 3   | 2.2µF, 10V X5R ceramic capacitors (optional 100µF, 18mΩ, 6.3V aluminum electrolytic, Sanyo GTPE100MI in parallel) |
| C2           | 1   | 0.1µF, 16V X7R ceramic capacitor  |
| C4, C7, C9   | 3   | 100µF, 18mΩ, 6.3V aluminum electrolytic capacitors Sanyo GTPE100MI  |
| C5, C6, C10  | 3   | 1µF, 16V X7R ceramic capacitors   |
| Q1/Q2 (dual) | 1   | Dual n-channel MOSFETs, 30V, 18mΩ Vishay Si4922DY   |
| Q3           | 1   | n-channel MOSFET, 30V, 50mΩ Fairchild Semiconductor FDD6630A  |
| R1           | 1   | 665Ω ±1% resistor   |
| R2           | 1   | 620Ω ±5% resistor   |
| R3           | 1   | 332Ω ±1% resistor   |
| R4           | 1   | 390Ω ±5% resistor   |
| R5           | 1   | 182Ω ±1% resistor   |
| R6           | 1   | 165Ω ±1% resistor   |
| R7           | 1   | 910Ω ±5% resistor   |
| R8           | 1   | 1kΩ ±1% resistor  |
| R9           | 1   | 249Ω ±1% resistor   |

### MAX8564/MAX8564A External Component List

| COMPONENTS   | QTY | DESCRIPTION   |
|--------------|-----|---|
| C11          | 1   | 0.1µF, 16V X7R ceramic capacitor  |
| C12, C14     | 2   | 100µF, 18mΩ, 6.3V aluminum electrolytic capacitors Sanyo GTPE100MI  |
| C15, C17     | 2   | 2.2µF, 10V X5R ceramic capacitors (optional 100µF, 18mΩ, 6.3V aluminum electrolytic, Sanyo GTPE100MI in parallel) |
| C18, C20     | 2   | 1µF, 16V X7R ceramic capacitors   |
| Q4/Q5 (dual) | 1   | Dual n-channel MOSFETs, 30V, 18mΩ Vishay Si4922DY   |
| R13          | 1   | 165Ω ±1% resistor   |
| R14          | 1   | 182Ω ±1% resistor   |
| R15          | 1   | 390Ω ±5% resistor   |
| R16          | 1   | 665Ω ±1% resistor   |
| R17          | 1   | 332Ω ±1% resistor   |
| R18          | 1   | 620Ω ±5% resistor   |



# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Detailed Description

The MAX8563/MAX8564/MAX8564A triple and dual LDO controllers allow flexible and inexpensive voltage conversion by controlling the gate of an external n-MOSFET in a source-follower configuration. The MAX8563/MAX8564/MAX8564A consist of multiple identical LDO controllers. Each LDO controller features an enable input (EN\_) and a power-OK output (POK\_). The MAX8563/MAX8564/MAX8564A also include a 0.5V reference, an internal regulator, and an undervoltage lockout (UVLO). The transconductance amplifier measures the feedback voltage on FB\_ and compares it to an internal 0.5V reference connected to the positive input. If the voltage on FB\_ is lower than 0.5V, the current output on the gate-drive output DRV\_ is increased. If the voltage on FB\_ is higher than 0.5V, the current output on the gate-drive output is decreased.

### Bias Voltage (V<sub>DD</sub>), UVLO, and Soft-Start

The MAX8563/MAX8564/MAX8564A bias current for internal circuitry is supplied by V<sub>DD</sub>. The V<sub>DD</sub> voltage range is from 4.5V to 13.2V. If V<sub>DD</sub> drops below 3.76V (typ), the MAX8563/MAX8564/MAX8564A assume that the supply and reference voltages are too low and activate the UVLO circuitry. During UVLO, the internal regulator (VL) and the internal bandgap reference are forced off, DRV\_ is pulled to GND, and POK\_ is pulled low.

Before any internal startup circuitry is activated, V<sub>DD</sub> must be above the UVLO threshold. After UVLO indicates that V<sub>DD</sub> is high enough, the internal VL regulator, the internal bandgap reference, and the bias currents are activated. If EN\_ is logic-high after the internal reference and bias currents are activated, then the corresponding DRV\_ output initiates operation in soft-start mode. Once the voltage on FB\_ reaches 94% of the regulation threshold, the full output current of the LDO controller is permitted.

When an LDO is activated, the respective DRV\_ is pulled up from GND with a typical soft-start current of DRV\_ soft-start. The soft-start current limits the slew of the output voltage and limits the initial spike of current that the drain of the external n-MOSFET receives. The size of the compensation capacitor (C<sub>C</sub>) limits the slew rate (see Figure 3). This output voltage slew rate is equal to (DRV\_<sub>soft-start</sub>/C<sub>C</sub>)mV/ms, where C<sub>C</sub> is in μF. The maximum startup drain current is the ratio of C<sub>OUT</sub> to C<sub>C</sub> multiplied by the soft-start current.

### Input Voltage (Drain Voltage of the External n-MOSFET)

The minimum input voltage to the drain of the n-MOSFET is a function of the desired output voltage and the dropout voltage of the n-MOSFET. Details on calculating

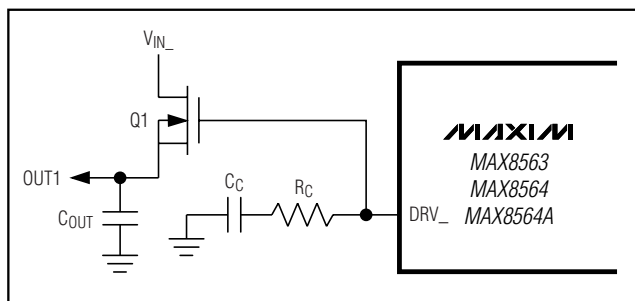


Figure 3. Soft-Start and Compensation Schematic

this value are covered in the *Power MOSFET Selection* section.

The maximum input voltage to the drain of the n-MOSFET is a function of the breakdown voltage and the thermal conditions during operation. The breakdown voltage from drain to source is normally provided in the MOSFET data sheet. The theoretical maximum input voltage is the set output voltage plus the breakdown voltage. The thermal constraint is usually the largest concern when discussing maximum input voltage. Details on calculating this value are covered in the *Power MOSFET Selection* section. The MOSFET package and thermal relief on the board are the largest contributors to removing heat from the n-MOSFET. Since output voltage is normally set and maximum output current is fixed, the input voltage becomes the only variable that determines the maximum power dissipated. Thus, the maximum input voltage is limited by the power capability of the n-MOSFET, if it is less than the breakdown voltage, which is most often the case. Ensure input capacitors handle the maximum input voltage.

During a power-up sequence where V<sub>DD</sub> and EN\_ rise before the input to the drain of the n-MOSFET, the MAX8563/MAX8564/MAX8564A drive DRV\_ high but the output does not rise. As DRV\_ rails and V<sub>FB</sub> is still below 80% of the regulation voltage, the MAX8563/MAX8564/MAX8564A assume that an output short-circuit fault is present and shut down that regulator. To avoid this error condition, connect a resistor-divider from V<sub>DD</sub> to IN\_ with the middle node connected to the respective EN\_ (see Figure 4). Use the following equations to calculate the resistor values.

When V<sub>IN\_</sub> is off or at a low-voltage state:

$$0.7 > \left( \frac{R_E}{R_E + R_D} \right) \times (V_{DD} - V_{IN\_}) + V_{IN\_}$$

When V<sub>IN\_</sub> is on or at a high-voltage state:

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

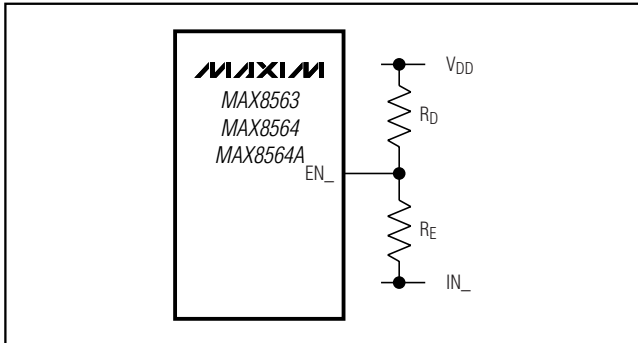


Figure 4. Voltage-Divider on EN\_

$$1.3 < \left( \frac{R_E}{R_E + R_D} \right) \times (V_{DD} - V_{IN\_}) + V_{IN\_}$$

Set  $R_D = 100\text{k}\Omega$ . The above equations also assume that  $V_{DD} > V_{IN\_} > 1\text{V}$  when  $V_{IN\_}$  is on or at a high-voltage state, and that  $V_{DD} > 3\text{V}$ .

Example: Connect  $100\text{k}\Omega$  from EN\_ to  $V_{DD}$  and  $4\text{k}\Omega$  from EN\_ to  $IN_$ . Thus, when  $V_{DD} = 12\text{V}$  and  $V_{IN\_} = 0\text{V}$ , then  $V_{EN\_} = 0.46\text{V}$ . When  $V_{DD} = 12\text{V}$  and  $V_{IN\_} = 1.2\text{V}$ , then  $V_{EN\_} = 1.6\text{V}$ .

Alternately, to avoid fault shutdown due to the delay of  $V_{IN}$  relative to  $V_{DD}$ , pull EN\_ low with a separate control logic and only drive high when  $V_{IN}$  reaches a steady-state value.

## Output Voltage

The output voltage range at the source of the n-MOSFET is from 0.5V to 3.3V when  $V_{DD}$  is 12V and from 0.5V to 1.8V when  $V_{DD}$  is 5V. The maximum output voltage is a function of the minimum gate-to-source voltage ( $V_{GS}$ ) of the MOSFET and  $V_{DD}$ .

The external n-MOSFET contains a parasitic diode from source to drain. If the output is ever anticipated to exceed the input, current flows from source to drain. If this is undesirable, external protection is needed. A simple solution is the placement of a diode in series, from  $IN_$  to the drain of the n-MOSFET, so that reverse current is not possible. Due to the forward-voltage drop of the diode, the maximum output voltage is reduced and additional power is consumed in the diode.

## Enable and POK

The MAX8563/MAX8564/MAX8564A have independent enable control inputs (EN1, EN2, and EN3). Drive EN1 high to enable output 1. Drive EN2 high to enable output 2. Drive EN3 high to enable output 3. When EN\_ is driven low, the corresponding  $DRV_$  is internally pulled to GND and POK\_ is internally pulled low.

The POK\_ is an open-drain output that provides the status of the output voltage and pulls low depending upon circuit conditions. During startup, once the  $FB_$  reaches the POK\_ threshold, the POK\_ signal goes high. The POK\_ threshold has 30mV of hysteresis. When the output voltage drops 12% below the nominal regulated voltage, POK\_ pulls low. All POK\_ outputs pull low when UVLO is activated or when the internal VL regulator and reference are not ready.

## Output Undervoltage and Overload Protection

When an overload event or short circuit occurs, the device that is most vulnerable is the external n-MOSFET. The MAX8563/MAX8564/MAX8564A monitor the output voltage to protect the MOSFET. When  $DRV_$  is at its maximum voltage and the output voltage drops below 80% but is still greater than 60% of its nominal voltage for more than  $50\mu\text{s}$ , the MAX8563/MAX8564/MAX8564A shut down that particular regulator output by pulling  $DRV_$  to GND. Note that there is an additional inherent delay in turning off the MOSFET. The delay is a function of the compensation capacitor and the MOSFET. If the output recovers to greater than 80% within  $50\mu\text{s}$ , it is not considered to be in overload and no action is taken. When the output voltage drops below 60% of its nominal voltage, the MAX8563/MAX8564/MAX8564A immediately shut down that particular regulator output by pulling  $DRV_$  to GND. To restart that particular LDO,  $V_{DD}$  must be recycled below the UVLO or the corresponding EN\_ must be recycled. The overload protection is shown in the *Typical Operating Characteristics*.

## Design Procedure

### Output Voltage Setting

The minimum output voltage for each controller of the MAX8563/MAX8564/MAX8564A is typically 0.5V. The maximum output voltage is adjustable up to 3.3V with  $V_{DD} = 12\text{V}$ , and up to 1.8V with  $V_{DD} = 5\text{V}$ . To set the output voltage, connect the  $FB_$  pin to the center of a voltage-divider between  $OUT_$  and GND (Figure 5). The resistor-divider current should be at least 1mA per 1A of maximum output current; i.e., for a 3A maximum output current, set the resistor-divider bias current to  $\geq 3\text{mA}$ :

$$I_{OUT(MIN)} \geq \frac{I_{OUT(MAX)}}{1000}$$

$$R_B \leq \frac{V_{FB}}{I_{OUT(MIN)}} = 1000 \times \frac{V_{FB}}{I_{OUT(MAX)}} = \frac{500}{I_{OUT(MAX)}}$$

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

$$R_A = R_B \times \left[ \left( \frac{V_{OUT}}{V_{FB}} \right) - 1 \right] = R_B \times (2 \times V_{OUT} - 1)$$

To set the output voltage to 0.5V, disconnect  $R_B$  from  $FB_-$  and connect it to  $OUT_-$ ; this change maintains the minimum load requirement on the output. In this case,  $R_A$  can vary from 1kΩ to 10kΩ.

### Input and Output Capacitor Selection

The input filter capacitor aids in providing low input impedance to the regulator and also reduces peak currents drawn from the power source during transient conditions. Use a minimum 2.2μF ceramic capacitor from  $IN_-$  (drain of the external pass n-MOSFET) to GND (see Figures 1 and 2). If large line transients or load transients are expected, increase the input capacitance to help minimize output voltage changes.

The output filter capacitor and its equivalent series resistance (ESR) contribute to the stability of the regulator (see the *Stability Compensation* section) and affect the load-transient response. If large step loads (no load to full load) are expected, and a very fast response (less than a few microseconds) is required, use a 100μF, 18mΩ POSCAP for the output capacitor. If a larger capacitance is desired, keep the capacitance ESR product ( $C_{OUT} \times R_{ESR}$ ) in the 1μs to 5μs range.

If the application expects smaller load steps (less than 50% of full load), then use a 6.8μF ceramic capacitor or larger per ampere of maximum output current. This option reduces the size and cost of the regulator circuit. Note that some ceramic dielectrics exhibit large capacitance variation with temperature. Use X7R or X5R dielectrics to ensure sufficient capacitance at all operating temperatures. Tantalum and aluminum capacitors are not recommended.

### Power MOSFET Selection

The MAX8563/MAX8564/MAX8564A use an n-channel MOSFET as the series pass transistor instead of a p-channel MOSFET to reduce cost. The selected MOSFET must have a gate threshold voltage that meets the following criteria:

$$V_{GS\_MAX} \leq V_{DD} - V_{OUT\_}$$

where  $V_{DD}$  is the controller bias voltage, and  $V_{GS\_MAX}$  is the maximum gate voltage required to yield the on-resistance ( $R_{DS\_ON}$ ) specified by the manufacturer's data sheet.  $R_{DS\_ON}$  multiplied by the maximum output

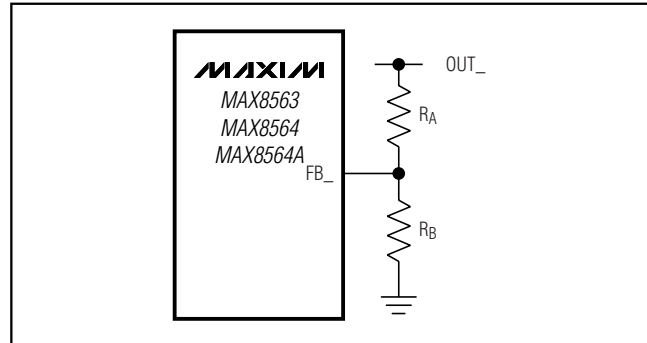


Figure 5. Adjustable Output Voltage

current (load current) is the maximum voltage dropout across the MOSFET,  $V_{DS\_MIN}$ . Make sure that  $V_{DS\_MIN}$  meets the condition below to avoid entering dropout, where output voltage starts to decrease and any ripple on the input also passes through to the output:

$$V_{IN\_MIN} > V_{DS\_MIN} + V_{OUT}$$

where  $V_{IN\_MIN}$  is the minimum input voltage at the drain of the MOSFET.  $V_{DS\_MIN}$  has a positive temperature coefficient; therefore, the value of  $V_{DS\_MIN}$  at the highest operating junction temperature should be used.

For thermal management, the maximum power dissipation in the MOSFET is calculated by:

$$P_D = (V_{IN\_MAX} - V_{OUT}) \times I_{OUT\_MAX}$$

The MOSFET is typically in an SMT package. Refer to the MOSFET data sheet for the PC board area needed to meet the maximum operating junction temperature required.

### Stability Compensation

Connect a resistor,  $R_C$ , and a capacitor,  $C_C$ , in series from the  $DRV_-$  pin to GND. The values of the compensation network depend upon the external MOSFET characteristics, the output current range, and the programmed output voltage. The following parameters are needed from the MOSFET data sheet: the input capacitance ( $C_{ISS}$  at  $V_{DS} = 1V$ ), the typical forward transconductance ( $g_{FS}$ ), and the current at which  $g_{FS}$  was measured ( $I_{DFS}$ ). Calculate the transconductance of the FET at the maximum load current ( $I_{OUT\_MAX}$ ):

$$g_{C(MAX)} = g_{FS} \times \sqrt{\frac{I_{OUT\_MAX}}{I_{DFS}}}$$

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

For the best transient response in applications with large step loads (see the *Input and Output Capacitor Selection* section for output capacitance requirements), use the following equations to select the compensation components:

$$C_C = \frac{\left[ 0.16 \times V_{OUT} \times C_{OUT} \times \left( g_{C(MAX)} \times (g_{C(MAX)} \times R_{ESR} + 1) \right) \right]}{\left( g_{C(MAX)} \times V_{OUT} + I_{OUT\_MAX} \right)^2} - C_{ISS}$$

$$R_C = 59 \times \frac{V_{OUT} \times C_{OUT} (g_{C(MAX)} \times R_{ESR} + 1)}{C_C \times (g_{C(MAX)} \times V_{OUT} + I_{OUT\_MAX})}$$

where  $C_{OUT}$  is the output capacitance and  $R_{ESR}$  is the ESR of  $C_{OUT}$ .

To use a low-cost ceramic capacitor (see the *Input and Output Capacitor Selection* section for load-transient response characteristics), use the following equations to select the compensation components:

$$C_C = \frac{C_{OUT} \times g_{C(MAX)}}{\left( g_{C(MAX)} \times V_{OUT} + I_{OUT\_MAX} \right)} - C_{ISS}$$

$$R_C = 15 \times \frac{C_{OUT}}{C_C \times g_{C(MAX)}}$$

### Example

OUTPUT 1 of Figure 1 is used in this example. Table 1 shows the values required to calculate the compensation. The values were taken from the appropriate data sheets and Figure 1.

**Table 1. Parameters Required to Calculate Compensation**

| PARAMETER        | CONDITIONS       | VALUE | UNITS |
|------------------|------------------|-------|-------|
| MOSFET $C_{ISS}$ | $V_{DS} = 1V$    | 2500  | pF    |
| MOSFET $G_{FS}$  | $I_{DFS} = 8.8A$ | 30    | S     |
| $V_{OUT1}$       | Figure 1         | 1.5   | V     |
| $I_{OUT\_MAX}$   | Figure 1         | 1.5   | A     |
| $C_{OUT1}$       | Figure 1         | 100   | μF    |
| $R_{ESR}$        | Figure 1         | 18    | mΩ    |

$$g_{C(MAX)} = 30S \times \sqrt{\frac{1.5A}{8.8A}} = 12.4S$$

$$C_C = 0.16 \times \frac{1.5V \times 100\mu F \times 12.4S \times \left( \frac{12.4S \times 18m\Omega}{1} + 1 \right)}{\left( 12.4S \times 1.5V + 1.5A \right)^2} - C_{ISS}$$

$$2500pF = 0.90\mu F, \text{ use } 1\mu F.$$

$$R_C = 59 \times \frac{1.5V \times 100\mu F \times (12.4S \times 18m\Omega + 1)}{1\mu F (12.4S \times 1.5V + 1.5A)} = 599.4\Omega, \text{ use } 620\Omega.$$

### PC Board Layout Guidelines

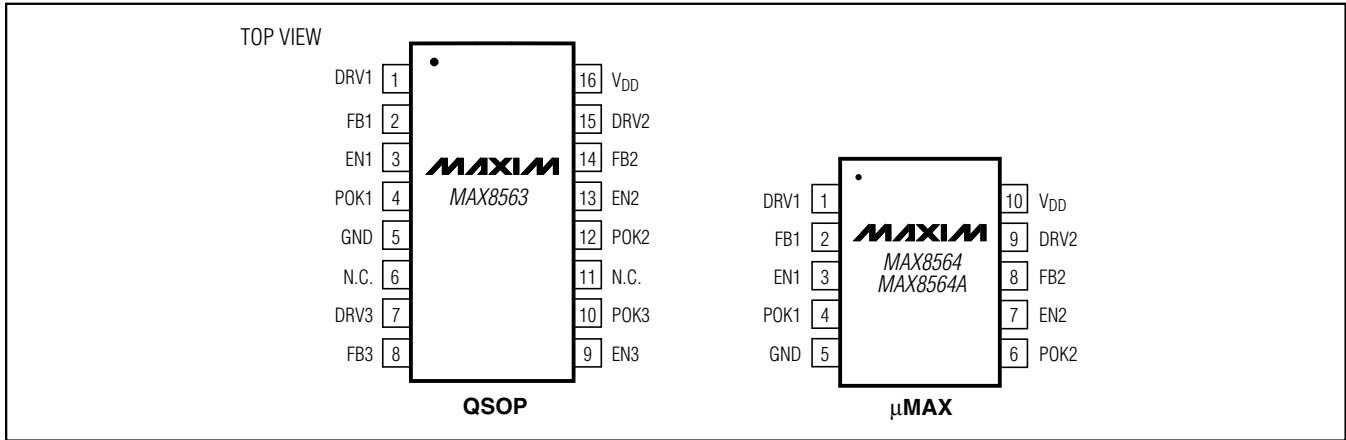
Due to the high-current paths and tight output accuracy required by most applications, careful PC board layout is required. An evaluation kit (MAX8563EVKIT) is available to speed design.

It is important to keep all traces as short as possible to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. The MOSFET dissipates a fair amount of heat due to the high currents involved, especially during large input-to-output voltage differences. To dissipate the heat generated by the MOSFET, make power traces very wide with a large amount of copper area. An efficient way to achieve good power dissipation on a surface-mount package is to lay out copper areas directly under the MOSFET package on multiple layers and connect the areas through vias. Use a ground plane to minimize impedance and inductance. In addition to the usual high-power considerations, here are four tips to ensure high output accuracy:

- Ensure that the feedback connection to  $C_{OUT\_}$  is short and direct.
- Place the feedback resistors next to the FB pin.
- Place  $R_C$  and  $C_C$  next to the  $DRV\_$  pin.
- Ensure  $FB\_$  and  $DRV\_$  traces are away from noisy sources to ensure tight accuracy.

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Pin Configurations



## Chip Information

TRANSISTOR COUNT: 1801

PROCESS: BICMOS

MAX8563/MAX8564/MAX8564A

# ±1%, Ultra-Low Output Voltage, Dual and Triple Linear n-FET Controllers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

| DIM | INCHES         |       | MILLIMETERS |       |
|-----|----------------|-------|-------------|-------|
|     | MIN            | MAX   | MIN         | MAX   |
| A   | .053           | .069  | 1.35        | 1.75  |
| A1  | .004           | .010  | .102        | .254  |
| A2  | .049           | .065  | 1.245       | 1.651 |
| B   | .008           | .012  | 0.20        | 0.30  |
| C   | .0075          | .0098 | 0.191       | 0.249 |
| D   | SEE VARIATIONS |       |             |       |
| E   | .150           | .157  | 3.81        | 3.99  |
| e   | .025 BSC       |       | 0.635 BSC   |       |
| H   | .230           | .244  | 5.84        | 6.20  |
| h   | .010           | .016  | 0.25        | 0.41  |
| L   | .016           | .035  | 0.41        | 0.89  |
| N   | SEE VARIATIONS |       |             |       |
| α   | 0°             | 8°    | 0°          | 8°    |

| DIM | INCHES |       | MILLIMETERS |       | N     |
|-----|--------|-------|-------------|-------|-------|
|     | MIN.   | MAX.  | MIN.        | MAX.  |       |
| D   | .189   | .196  | 4.80        | 4.98  | 16 AB |
| S   | .0020  | .0070 | 0.05        | 0.18  |       |
| D   | .337   | .344  | 8.56        | 8.74  | 20 AD |
| S   | .0500  | .0550 | 1.270       | 1.397 |       |
| D   | .337   | .344  | 8.56        | 8.74  | 24 AE |
| S   | .0250  | .0300 | 0.635       | 0.762 |       |
| D   | .386   | .393  | 9.80        | 9.98  | 28 AF |
| S   | .0250  | .0300 | 0.635       | 0.762 |       |

NOTES:

- 1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
- 2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
- 3). CONTROLLING DIMENSIONS: INCHES.
- 4). MEETS JEDEC MO137.

VARIATIONS:

DALLAS SEMICONDUCTOR  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH  
 APPROVAL: DOCUMENT CONTROL NO. 21-0055 REV. F 1/1

QSOP-EPS