19-2213; Rev 0; 10/01

MAXIM

Low-Jitter, Low-Noise LVDS Repeater in an SC70 Package

General Description

The MAX9155 is a low-voltage differential signaling (LVDS) repeater, which accepts a single LVDS input and duplicates the signal at a single LVDS output. Its low-jitter, low-noise performance makes it ideal for buffering LVDS signals sent over long distances or noisy environments, such as cables and backplanes.

The MAX9155's tiny size makes it especially suitable for minimizing stub lengths in multidrop backplane applications. The SC70 package (half the size of a SOT23) allows the MAX9155 to be placed close to the connector, thereby minimizing stub lengths and reflections on the bus. The point-to-point connection between the MAX9155 output and the destination IC, such as an FPGA or ASIC, allows the destination IC to be located at greater distances from the bus connector.

Ultra-low, $23ps_{p-p}$ added deterministic jitter and $0.6ps_{RMS}$ added random jitter ensure reliable communication in high-speed links that are highly sensitive to timing errors, especially those incorporating clock-and-data recovery, PLLs, serializers, or deserializers. The MAX9155's switching performance guarantees a 200Mbps data rate, but minimizes radiated noise by guaranteeing 0.5ns minimum output transition time.

The MAX9155 has fail-safe circuitry that sets the output high for undriven open, short, or terminated inputs.

The MAX9155 operates from a single +3.3V supply and consumes only 10mA over a -40°C to +85°C temperature range. Refer to the MAX9129 data sheet for a quad bus LVDS driver, and to the MAX9156 data sheet for a low-jitter, low-noise LVPECL-to-LVDS level translator in an SC70 package.

Applications

Cellular Phone Base Stations

DSLAMs

Digital Cross-Connects

Add/Drop Muxes

Network Switches/Routers

Multidrop Buses

Cable Repeaters

Typical Operating Circuit appears at end of data sheet.

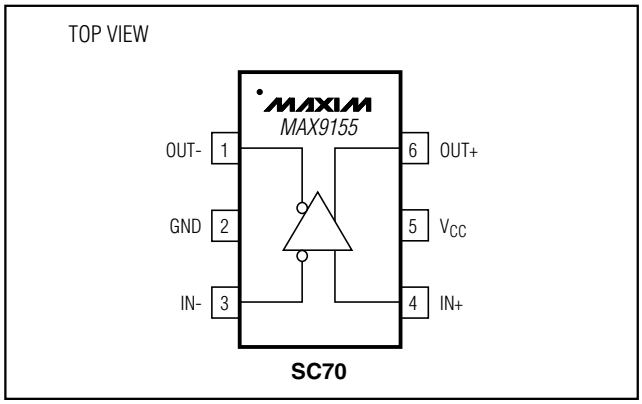
Features

- **Tiny SC70 Package**
- **Ultra-Low Jitter**
  - **$23ps_{p-p}$ Added Deterministic Jitter (2^{23}-1 PRBS)**
  - **$0.6ps_{RMS}$ Added Random Jitter**
- **0.5ns (min) Transition Time Minimizes Radiated Noise**
- **200Mbps Guaranteed Data Rate**
- **Fail-Safe Circuit Sets Output High for Undriven Inputs (Open, Terminated, or Shorted)**
- **Low 10mA Supply Current**
- **Low 6mA Supply Current in Fail-Safe**
- **Conforms to ANSI/EIA/TIA-644 LVDS Standard**
- **High-Impedance Inputs and Outputs in Power-Down Mode**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9155EXT-T	-40°C to +85°C	6 SC70-6	ABC

Pin Configuration



SC70

Low-Jitter, Low-Noise LVDS Repeater in an SC70 Package

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN+, IN- to GND .....-0.3V to +4.0V
OUT+, OUT- to GND .....-0.3V to +4.0V
Short-Circuit Duration (OUT+, OUT-) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
ESD Protection
Human Body Model, IN+, IN-, OUT+, OUT- .....±8kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $|V_{ID}|$ = 0.05V to 1.2V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUT							
Differential Input High Threshold	V_{TH}				7	50	mV
Differential Input Low Threshold	V_{TL}			-50	-7		mV
Input Current	I_{IN+}, I_{IN-}	0.05V ≤ $\|V_{ID}\|$ ≤ 0.6V		-15	-2.5	15	µA
		0.6V< $\|V_{ID}\|$ ≤ 1.2V,		-20	-3.5	20	
Power-Off Input Current	I_{IN+}, I_{IN-}	0.05V ≤ $\|V_{ID}\|$ ≤0.6V, V_{CC} = 0		-15	1.3	15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, V_{CC} = 0		-20	2.6	20	
Input Resistor 1	R_{IN1}	V_{CC} = +3.6V or 0, Figure 1		67	232		kΩ
Input Resistor 2	R_{IN2}	V_{CC} = +3.6V or 0, Figure 1		267	1174		kΩ
LVDS OUTPUT							
Differential Output Voltage	V_{OD}	Figure 2		250	360	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 2			0.008	25	mV
Offset (Common-Mode) Voltage	V_{OS}	Figure 2		1.125	1.25	1.375	V
Change in V_{OS} for Complementary Output States	ΔV_{OS}	Figure 2			0.005	25	mV
Output High Voltage	V_{OH}				1.44	1.6	V
Output Low Voltage	V_{OL}			0.9	1.08		V
Fail-Safe Differential Output Voltage	V_{OD+}	IN+, IN- shorted, open, or parallel terminated		+250	+360	+450	mV
Power-Off Output Leakage Current	IO_{OFF}	V_{CC} = 0	OUT+ = 3.6V, other output open	-10	0.02	10	µA
			OUT- = 3.6V, other output open	-10	0.02	10	
Differential Output Resistance	RO_{DIFF}	V_{CC} = +3.6V or 0		100	260	400	Ω
Output Short Current	I_{SC}	V_{ID} = +50mV, OUT+ = GND			-5	-15	mA
		V_{ID} = -50mV, OUT- = GND			-5	-15	
POWER SUPPLY							
Supply Current	I_{CC}	Output loaded			10	15	mA
Supply Current in Fail-Safe	I_{CCF}	Output loaded, input undriven			6	8	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 10pF, $|V_{ID}|$ = 0.15V to 1.2V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 3, 4, 5) (Figures 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}		1.3	2.0	2.8	ns
Differential Propagation Delay Low to High	t_{PLHD}		1.3	2.0	2.8	ns
Added Deterministic Jitter (Notes 6, 11)	t_{DJ}	200Mbps 2^{23}-1 PRBS data pattern		23	100	ps_{p-p}
Added Random Jitter (Notes 7, 11)	t_{RJ}	f_{IN} = 100MHz		0.6	2.9	ps_{RMS}
Differential Part-to-Part Skew (Note 8)	t_{SKPP1}			0.17	0.6	ns
Differential Part-to-Part Skew (Note 9)	t_{SKPP2}				1.5	ns
Switching Supply Current	I_{CCSW}			11.3	18	mA
Rise Time	t_{TLH}		0.5	0.66	1.0	ns
Fall Time	t_{THL}		0.5	0.64	1.0	ns
Input Frequency (Note 10)	f_{MAX}		100			MHz

Note 1: All devices are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design and characterization.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, V_{OD}, and ΔV_{OD}.

Note 3: Guaranteed by design and characterization.

Note 4: Signal generator output (unless otherwise noted): frequency = 100MHz, 50% duty cycle, R_O = 50Ω, t_R = 1.5ns, and t_F = 1.5ns (0% to 100%).

Note 5: C_L includes scope probe and test jig capacitance.

Note 6: Signal generator output for t_{DJ}: V_{OD} = 150mV, V_{OS} = 1.2V, t_{DJ} includes pulse (duty-cycle) skew.

Note 7: Signal generator output for t_{RJ}: V_{OD} = 150mV, V_{OS} = 1.2V.

Note 8: t_{SKPP1} is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same supply voltage, input common-mode voltage, and ambient temperature.

Note 9: t_{SKPP2} is the magnitude difference of any differential propagation delays between devices operating over rated conditions.

Note 10: Device meets V_{OD} DC specification and AC specifications while operating at f_{MAX}.

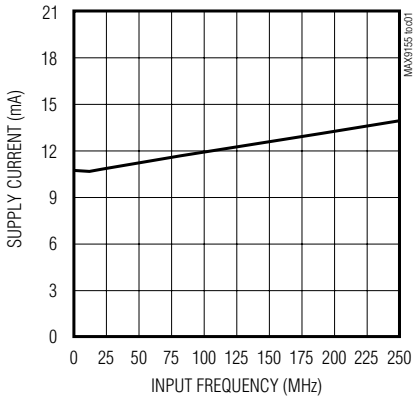
Note 11: Jitter added to the input signal.

Low-Jitter, Low-Noise LVDS Repeater in an SC70 Package

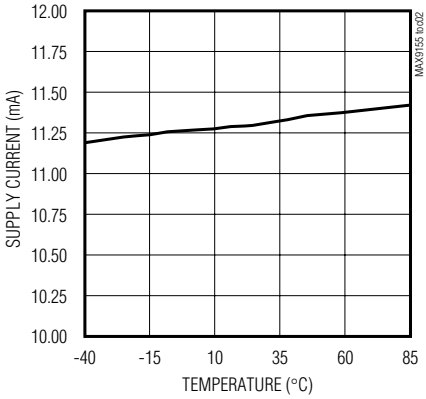
Typical Operating Characteristics

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 10pF, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted. Signal generator output: frequency = 100MHz, 50% duty cycle, R_O = 50Ω, t_R = 1.5ns, and t_F = 1.5ns (0% to 100%), unless otherwise noted.)

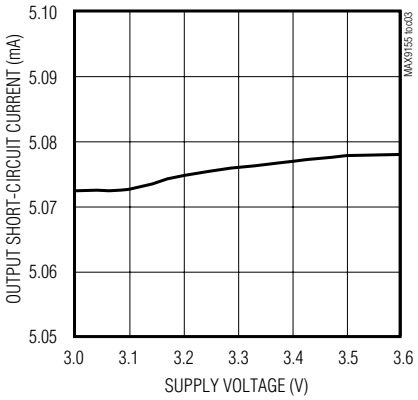
SUPPLY CURRENT vs. INPUT FREQUENCY



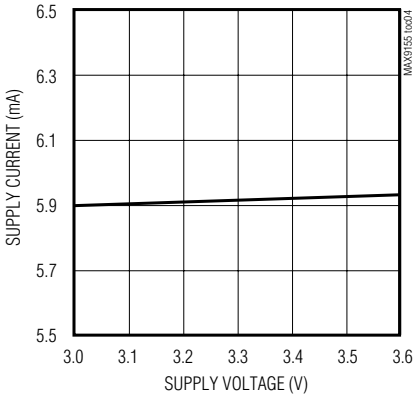
SWITCHING SUPPLY CURRENT vs. TEMPERATURE



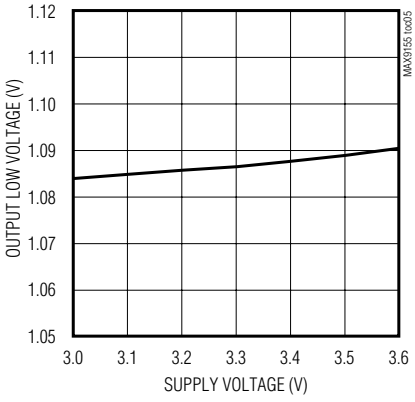
OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



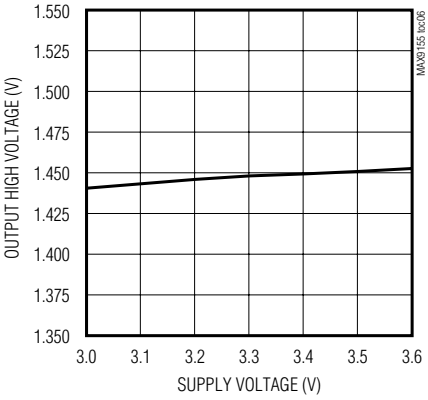
FAIL-SAFE SUPPLY CURRENT vs. SUPPLY VOLTAGE



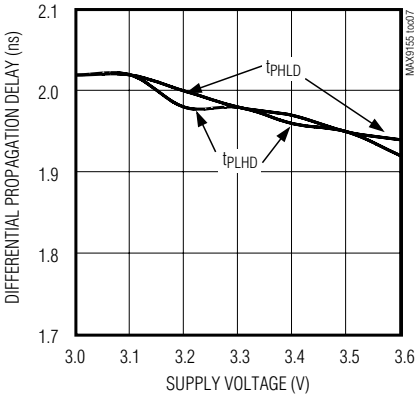
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



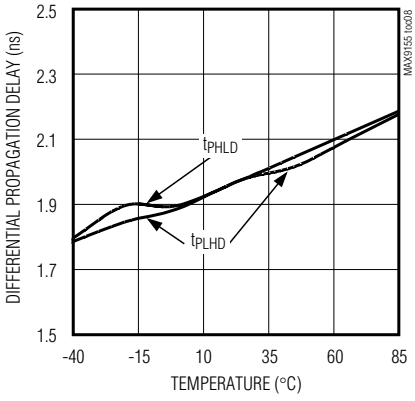
OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



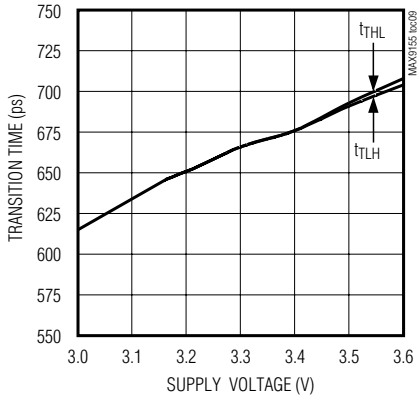
DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



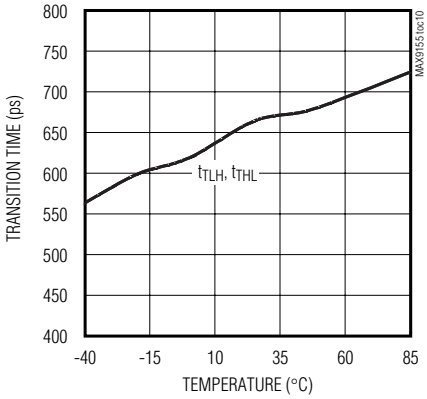
TRANSITION TIME vs. SUPPLY VOLTAGE



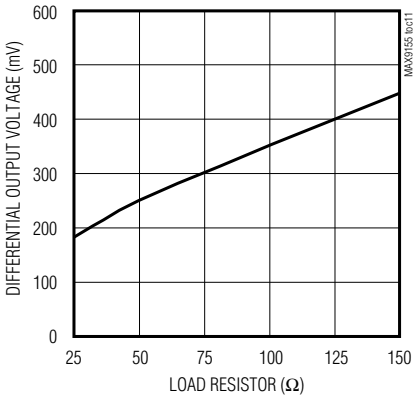
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_L = 100Ω ±1%, C_L = 10pF, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted. Signal generator output: frequency = 100MHz, 50% duty cycle, R_O = 50Ω, t_R = 1.5ns, and t_F = 1.5ns (0% to 100%), unless otherwise noted.)

TRANSITION TIME vs. TEMPERATURE



DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTOR



Pin Description

PIN	NAME	FUNCTION
1	OUT-	Inverting LVDS Output
2	GND	Ground
3	IN-	Inverting LVDS Input
4	IN+	Noninverting LVDS Input
5	V_{CC}	Power Supply. Bypass V_{CC} to GND with 0.01µF ceramic capacitor.
6	OUT+	Noninverting LVDS Output

Table 1. Function Table for LVDS Fail-Safe Input (Figure 2)

INPUT, V_{ID}	OUTPUT, V_{OD}
≥ 50mV	High
≤ -50mV	Low
50mV > V_{ID} > -50mV	Indeterminate
Undriven open, short, or terminated	High

Note: *V_{ID} = (IN+ - IN-), V_{OD} = (OUT+ - OUT-)*
High = 450mV ≥ V_{OD} ≥ 250mV
Low = -250mV ≥ V_{OD} ≥ -450mV

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium, as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9155 is a 200Mbps LVDS repeater intended for high-speed, point-to-point, low-power applications. The MAX9155 accepts an LVDS input and reproduces an LVDS signal at the output. This device is capable of detecting differential signals as low as 50mV and as high as 1.2V within a 0 to 2.4V input voltage range. The LVDS standard specifies an input voltage range of 0 to 2.4V referenced to ground.

Fail-Safe

Fail-safe is a feature that puts the output in a known logic state (differential high) under certain fault conditions. The MAX9155 outputs are differential high when the inputs are undriven and open, terminated, or shorted (Table 1).

Low-Jitter, Low-Noise LVDS Repeater in an SC70 Package

Applications Information

Supply Bypassing

Bypass V_{CC} with a high-frequency surface-mount ceramic 0.01µF capacitor as close to the device as possible.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9155. Use controlled-impedance differential traces. Ensure that noise couples as common mode by running the traces within a differential pair close together.

Maintain the distance within a differential pair to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

The LVDS standards define signal levels for interconnect with a differential characteristic impedance and termination of 100Ω. Interconnects with a characteristic impedance and termination of 90Ω to 132Ω impedance are allowed, but produce different signal levels (see *Termination*).

Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon or coaxial cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

For point-to-point links, the termination resistor should be located at the LVDS receiver input and match the differential characteristic impedance of the transmission line.

For a multidrop bus driven at one end, terminate at the other end of the bus with a resistor that matches the loaded differential characteristic impedance of the bus. For a multidrop bus driven from a point other than the end, terminate each end of the bus with a resistor that matches the loaded differential characteristic impedance of the bus. When terminating at both ends, or for a large number of drops, a bus LVDS (BLVDS) driver is needed to drive the bus to LVDS signal levels. The MAX9155 is not intended to drive double-terminated multidrop buses to LVDS levels.

The differential output voltage level depends upon the differential characteristic impedance of the interconnect and the value of the termination resistance. The MAX9155 is guaranteed to produce LVDS output levels into 100Ω. With the typical 3.6mA output current, the MAX9155 produces an output voltage of 360mV when driving a 100Ω transmission line terminated with a 100Ω termination resistor (3.6mA x 100Ω = 360mV). For typical output levels with different loads, see the Differential Output Voltage vs. Load Resistor typical operating curve.

Chip Information

TRANSISTOR COUNT: 401

PROCESS: CMOS

Test Circuit and Timing Diagrams

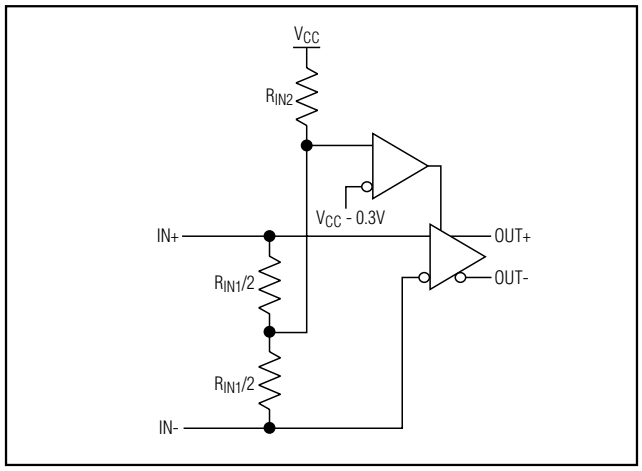


Figure 1. LVDS Fail-Safe Input

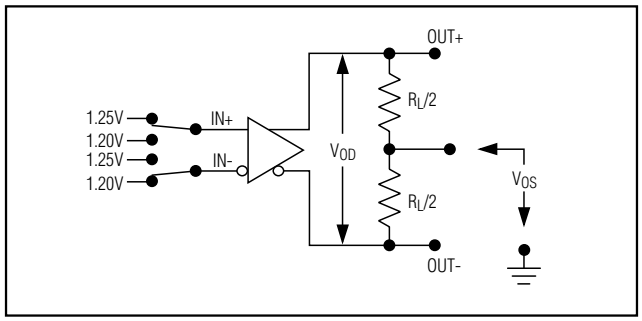


Figure 2. DC Load Test Circuit

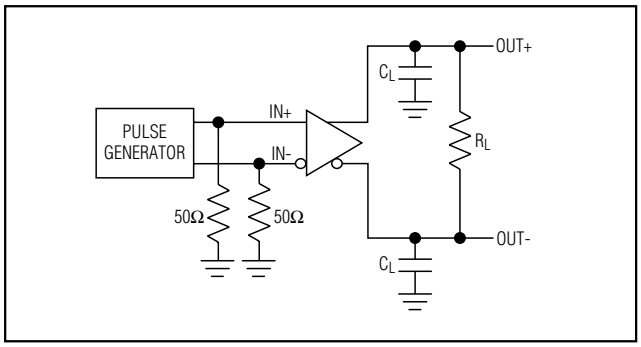


Figure 3. Transition Time and Propagation Delay Test Circuit

Low-Jitter, Low-Noise LVDS Repeater in an SC70 Package

Test Circuit and Timing Diagrams (continued)

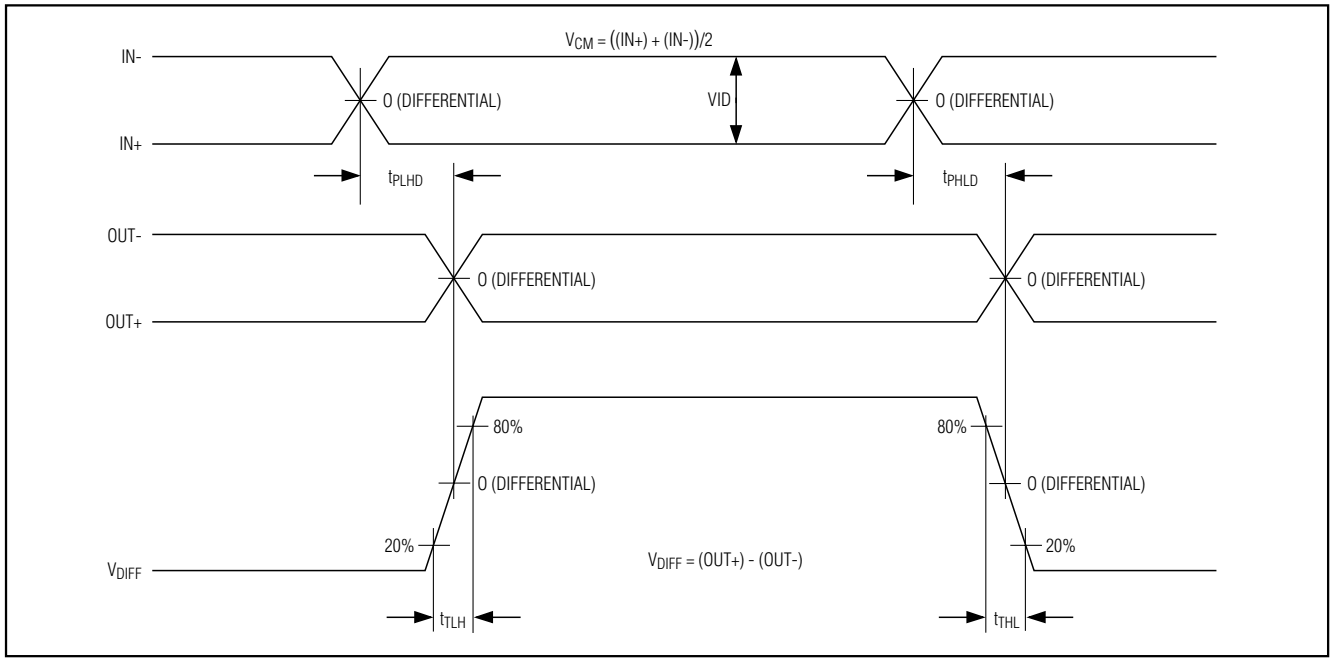


Figure 4. Transition Time and Propagation Delay Timing Diagram

Typical Operating Circuit