19-2384; Rev 0; 4/02

Differential PECL/ECL/LVPECL/LVECL Receiver/Driver

General Description

The MAX9321B low-skew differential receiver/driver is designed for clock and data distribution. The differential input can be adapted to accept a single-ended input by connecting the on-chip V_{BB} supply to an input as a reference voltage.

The MAX9321B features ultra-low propagation delay (172ps) and part-to-part skew (20ps) with 24mA maximum supply current, making this device ideal for clock buffering or repeating. For interfacing to differential PECL and LVPECL signals, these devices operate over a +3.0V to +5.5V supply range, allowing high-performance clock and data distribution in systems with a nominal 3.3V or 5.0V supply. For differential ECL and LVECL operation, this device operates from a -3.0V to -5.5V supply.

The MAX9321B is offered in industry-standard 8-pin SO and TSSOP packages.

Features

- **Improved Second Source of the MC10EP16D**
- **+3.0V to +5.5V Differential PECL/LVPECL Operation**
- **-3.0V to -5.5V Differential ECL/LVECL Operation**
- **Low 17mA Supply Current**
- **20ps Part-to-Part Skew**
- **172ps Propagation Delay**
- **Minimum 300mV Output at 3GHz**
- **Output Low for Open Input**
- **ESD Protection >2kV (Human Body Model)**
- **On-Chip Reference for Single-Ended Input**

Applications

Precision Clock Buffer

Low-Jitter Data Repeater

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9321BESA	-40°C to +85°C	8 SO
MAX9321BEUA*	-40°C to +85°C	8 TSSOP

**Future product—contact factory for availability.*

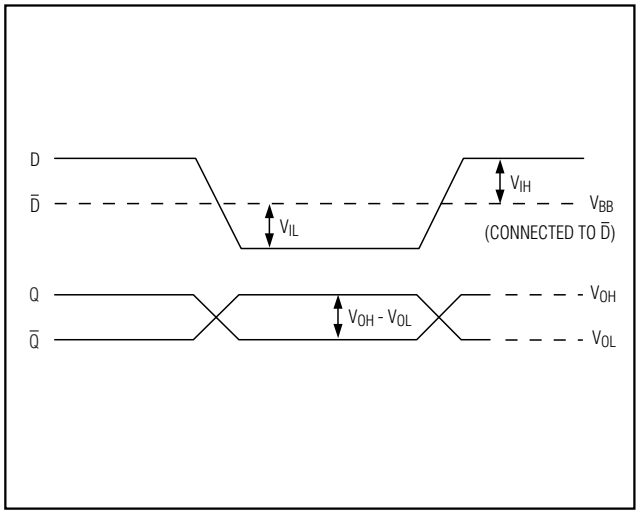
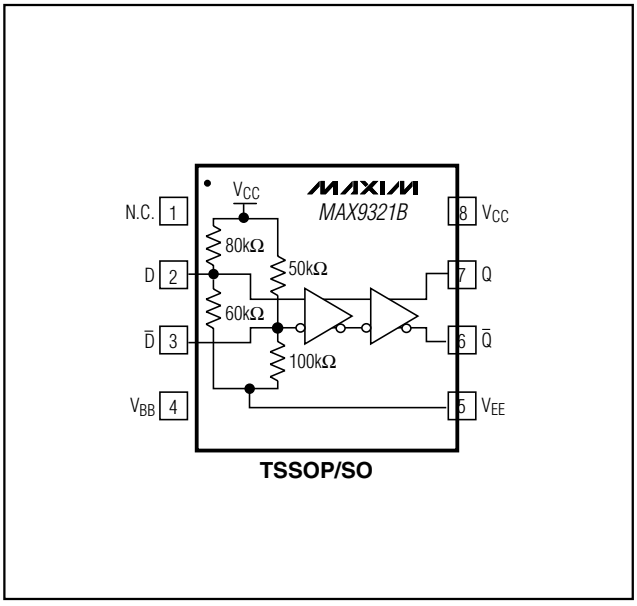


Figure 1. Switching with Single-Ended Inputs

Pin Configuration



Differential PECL/ECL/LVPECL/LVECL Receiver/Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} 6.0V
D or $\overline{D}$ ..... V_{EE} - 0.3V to V_{CC} + 0.3V
D or $\overline{D}$ with the Other Input Floating .... V_{CC} - 5.0V to V_{CC} + 0.3V
D to $\overline{D}$ ..... ±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
V_{BB} Sink/Source Current ..... ±0.6mA
Continuous Power Dissipation (T_A +70°C)
8-Pin TSSOP (derate 4.5mW/°C above +70°C) 362mW
8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin TSSOP ..... +221°C/W
8-Pin SO ..... +170°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow
8-Pin TSSOP ..... +155°C/W
8-Pin SO ..... +99°C/W
Junction-to-Case Thermal Resistance
8-Pin TSSOP ..... +39°C/W
8-Pin SO ..... +40°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model (D, $\overline{D}$, Q_, $\overline{Q}$_) ..... >2kV
Soldering Temperature (10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = 5.0V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (D, $\overline{D}$)												
Single-Ended Input High Voltage	V_{IH}	V_{BB} connected to $\overline{D}$ (V_{IL} for V_{BB} connected to D), Figure 1	V_{CC} - 1.21		V_{CC}	V_{CC} - 1.145		V_{CC}	V_{CC} - 1.085		V_{CC}	V
Single-Ended Input Low Voltage	V_{IL}	V_{BB} connected to $\overline{D}$ (V_{IH} for V_{BB} connected to D), Figure 1 (Note 4)	V_{EE}		V_{CC} - 1.61	V_{EE}		V_{CC} - 1.545	V_{EE}		V_{CC} - 1.485	V
High Voltage of Differential Input	V_{IHD}		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Low Voltage of Differential Input	V_{ILD}		V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V_{EE}		V_{CC} - 0.1	V
Differential Input Voltage	V_{IHD} - V_{ILD}		0.1		3.0	0.1		3.0	0.1		3.0	V
Input High Current	I_{IH}				150			150			150	µA
D Input Low Current	I_{ILD}	V_{CC} - V_{EE} ≤ 3.8V	-100		+100	-100		+100	-100		+100	µA
		V_{CC} - V_{EE} ≥ 3.8V	-140		+140	-140		+140	-140		+140	
$\overline{D}$ Input Low Current	$I_{\overline{ILD}}$	V_{CC} - V_{EE} ≤ 3.8V	-150		+150	-150		+150	-150		+150	µA
		V_{CC} - V_{EE} ≥ 3.8V	-175		+175	-175		+175	-175		+175	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = 5.0V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL OUTPUT (Q, $\overline{Q}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 1	V_{CC} - 1.135		V_{CC} - 0.885	V_{CC} - 1.07		V_{CC} - 0.82	V_{CC} - 1.01		V_{CC} - 0.76	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1	V_{CC} - 1.935		V_{CC} - 1.68	V_{CC} - 1.87		V_{CC} - 1.62	V_{CC} - 1.81		V_{CC} - 1.56	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1	550	820		550	820		550	820		mV
REFERENCE (V_{BB})												
Reference Voltage Output	V_{BB}	I_{BB} = ±0.5mA (Note 5)	V_{CC} - 1.51		V_{CC} - 1.31	V_{CC} - 1.445		V_{CC} - 1.245	V_{CC} - 1.385		V_{CC} - 1.185	V
POWER SUPPLY												
Supply Current	I_{EE}	(Note 6)		16	24		17	24		18	24	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency ≤ 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to 3.0V. Typical values are at V_{CC} - V_{EE} = 5V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 7)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2	145	184	235	145	172	245	130	167	230	ps
Part-to-Part Skew	t_{SKPP}	(Note 8)		25	90		20	100		20	100	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.5GHz, clock pattern (Note 9)		1.7	2.8		1.7	2.8		1.7	2.8	ps (RMS)
		f_{IN} = 3.0GHz, clock pattern (Note 9)		0.6	1.5		0.6	1.5		0.6	1.5	

Differential PECL/ECL/LVPECL/LVECL Receiver/Driver

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency ≤ 1.5GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to 3.0V. Typical values are at V_{CC} - V_{EE} = 5V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 7)

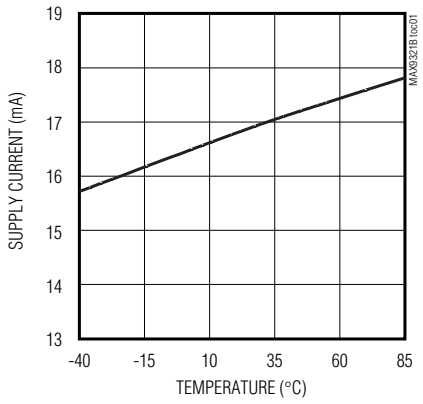
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Added Deterministic Jitter	t_{DJ}	3.0Gpbs 2^{23} - 1 PRBS pattern (Note 9)		57	80		57	80		57	80	ps (P-P)
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV, clock pattern, Figure 2	3.0			3.0			3.0			GHz
		V_{OH} - V_{OL} ≥ 550mV, clock pattern, Figure 2	2.0			2.0			2.0			
Output Rise/ Fall Time (20% to 80%)	t_R, t_F	Figure 2	65	112	135	65	118	135	65	121	135	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C. Guaranteed by design and characterization over the full operating temperature range.
Note 4: Maximum differential input voltage limit of ±3V also applies to single-ended use.
Note 5: Use V_{BB} as a reference for inputs on the same device only.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 9: Device jitter added to the input signal.

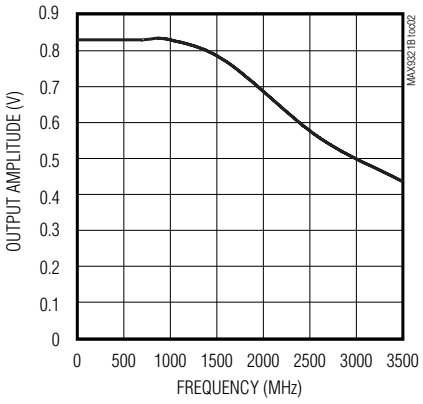
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = 0V, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 1.5GHz, outputs loaded with 50Ω to V_{CC} - 2V, T_A = +25°C, unless otherwise noted.)

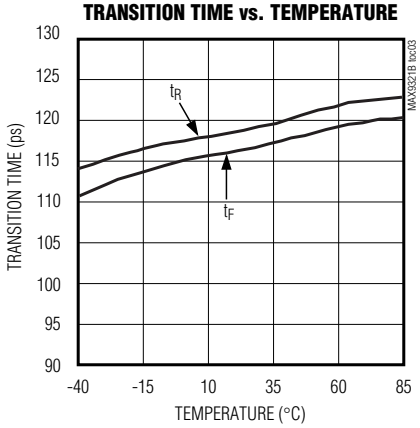
SUPPLY CURRENT, I_{EE} vs. TEMPERATURE



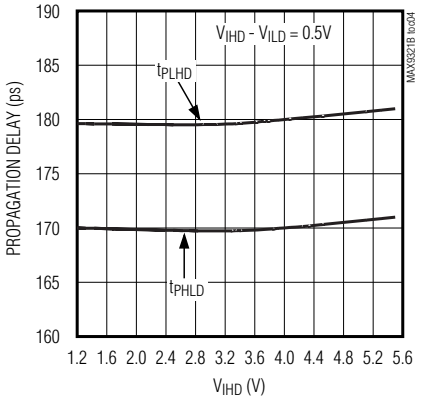
OUTPUT AMPLITUDE, V_{OH} - V_{OL} vs. FREQUENCY



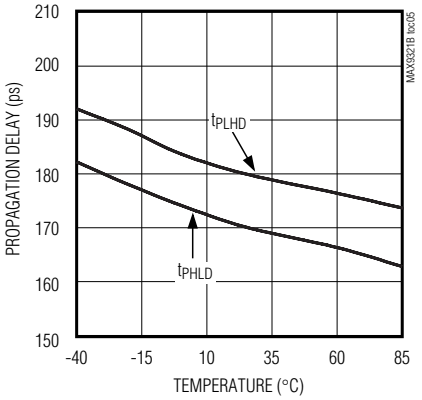
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT, V_{IHD}



PROPAGATION DELAY vs. TEMPERATURE



Differential PECL/ECL/LVPECL/LVECL Receiver/Driver

Pin Description

PIN	NAME	FUNCTION
1	N.C.	No Connection
2	D	Noninverting Differential Input. 80kΩ pullup to V_{CC}, 60kΩ pulldown to V_{EE}.
3	$\overline{D}$	Inverting Differential Input. 50kΩ pullup to V_{CC} and 100kΩ pulldown to V_{EE}.
4	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise leave open.
5	V_{EE}	Negative Supply Voltage
6	$\overline{Q}$	Inverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
7	Q	Noninverting Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
8	V_{CC}	Positive Supply Voltage. Bypass from V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Detailed Description

The MAX9321B low-skew differential receiver/driver is designed for clock and data distribution. For interfacing to differential PECL/LVPECL signals, this device operates over a +3.0V to +5.5V supply range, allowing high-performance clock and data distribution in systems with a nominal 3.3V or 5V supply. For differential ECL/LVECL operation, this device operates from a -3.0V to -5.5V supply.

Inputs

The differential input can be configured to accept a single-ended input. This is accomplished by connecting the on-chip reference voltage, V_{BB}, to an input as a reference. For example, the differential input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{D}$ and connecting the single-ended input to D. An inverting input is obtained by connecting V_{BB} to D and connecting the single-ended input to $\overline{D}$.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, it can be left open. The V_{BB} reference can source or sink 0.5mA. Use V_{BB} only for an input on the same device as the V_{BB} reference.

The maximum magnitude of the differential input from D to $\overline{D}$ is 3.0V. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential input has bias resistors that drive the output to a differential low when the inputs are open. The inverting input is biased with a 50kΩ pullup to V_{CC} and a 100kΩ pulldown to V_{EE}. The noninverting input is biased with an 80kΩ pullup to V_{CC} and a 60kΩ pulldown to V_{EE}.

Specifications for the high and low voltage of the differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously (V_{ILD} cannot be higher than V_{IHD}).

Outputs

Output levels are referenced to V_{CC} and are considered PECL/LVPECL or ECL/LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to GND, the output is PECL/LVPECL. The output is ECL/LVECL when V_{CC} is connected to GND and V_{EE} is connected to a negative supply.

A single-ended input of at least V_{BB} ±100mV or a differential input of at least ±100mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF value capacitor closest to the device. Use multiple parallel ground vias for low inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9321B. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and