19-2846; Rev 1; 7/03

MAXIM

Anything-to-LVPECL/LVDS Translators with Pin-Selectable Divide-by-Four

General Description

The MAX9377/MAX9378 are fully differential, high-speed, low-jitter anything-to-LVPECL and anything-to-LVDS translators, respectively, with a selectable divide-by-four function. Low propagation delay and high speed make them ideal for various high-speed network routing and backplane applications at speeds up to 2GHz in nondivide mode.

The MAX9377/MAX9378 accept any differential input signal within the supply rails and with minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. The MAX9377 outputs are LVPECL and have sufficient current to drive 50Ω transmission lines. The MAX9378 outputs are LVDS and conform to the ANSI EIA/TIA-644 LVDS standard.

The MAX9377/MAX9378 are available in 8-pin µMAX packages and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

Features

- **Guaranteed 2GHz Switching Frequency**
- **Accept LVDS/LVPECL/Anything Inputs**
- **Pin-Selectable Divide-by-Four Function**
- **421ps (typ) Propagation Delays (MAX9377)**
- **30ps (max) Pulse Skew**
- **$2ps_{RMS}$ (max) Random Jitter**
- **Minimum 100mV Differential Input to Guarantee AC Specifications**
- **Temperature-Compensated LVPECL Output**
- **+3.0V to +3.6V Power-Supply Operating Range**
- **ESD Protection: >2kV Human Body Model (HBM)**

Applications

Backplane Logic Standard Translation

LAN

WAN

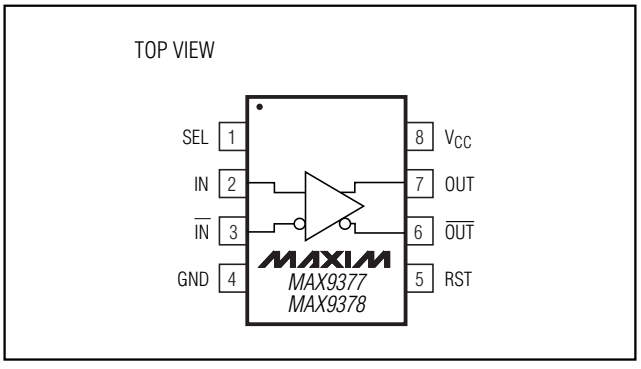
DSLAM

DLC

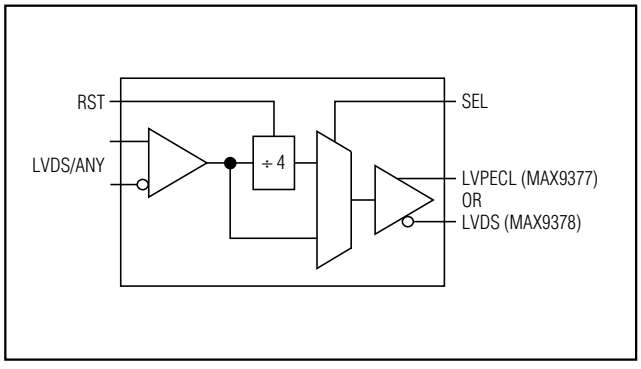
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9377EUA	-40°C to +85°C	8 µMAX
MAX9378EUA	-40°C to +85°C	8 µMAX

Pin Configuration



Functional Diagram



Anything-to-LVPECL/LVDS Translators with Pin-Selectable Divide-by-Four

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
Inputs (IN, $\overline{IN}$, RST, SEL) .....-0.3V to (V_{CC} + 0.3V)
IN to $\overline{IN}$ .....±3.0V
Short-Circuit Duration (MAX9378 OUT, $\overline{OUT}$) .....Continuous
Continuous Output Current 50mA
Surge Output Current 100mA
Continuous Power Dissipation (T_A = +70°C)
8-µMAX (derate 5.9mW/°C above +70°C) 470.6mW
θ_{JA} in Still Air .....+170°C/W
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (IN, $\overline{IN}$, OUT, $\overline{OUT}$) .....≥2kV
Soldering Temperature (10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LVCMOS/LVTTL INPUTS (RST, SEL)												
Input High Voltage	V_{IH}		2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}		GND		0.8	GND		0.8	GND		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{CC} or 2V	0		150	0		150	0		150	µA
Input Low Current	I_{IL}	V_{IL} = 0 or 0.8V	-20		+20	-20		+20	-20		+20	µA
DIFFERENTIAL INPUTS (IN, $\overline{IN}$)												
Differential Input Threshold	V_{THD}		-100	±6	+100	-100	±6	+100	-100	±6	+100	mV
Input Current	I_{IN}, $I_{\overline{IN}}$	V_{IN}, $V_{\overline{IN}}$ = V_{CC} or 0V	-20		+20	-20		+20	-20		+20	µA
Input Common-Mode Voltage	V_{CM}	Figure 1	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	V
LVPECL OUTPUTS (OUT, $\overline{OUT}$) (MAX9377)												
Single-Ended Output High Voltage	V_{OH}	Figure 3	V_{CC} - 1.085	V_{CC} - 1.033	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.992	V_{CC}- 0.880	V_{CC} - 1.025	V_{CC} - 0.978	V_{CC} - 0.880	V
Single-Ended Output Low Voltage	V_{OL}	Figure 3	V_{CC} - 1.830	V_{CC} - 1.755	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.717	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.699	V_{CC} - 1.620	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 3	595	725		595	725		595	725		mV
LVDS OUTPUTS (OUT, $\overline{OUT}$) (MAX9378)												
Differential Output Voltage	V_{OD}	Figure 2	250	370	450	250	363	450	250	348	450	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Change in Magnitude of V_{OD} Between Complementary Output States	$\|\Delta V_{OD}\|$	Figure 2		1.0	20		1.0	20		1.0	20	mV
Offset Common-Mode Voltage	$\|V_{OS}\|$	Figure 2	1.125		1.375	1.125	1.250	1.375	1.125		1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	$\|\Delta V_{OS}\|$	Figure 2		0.1	20		0.1	20		0.1	20	mV
Output Short-Circuit Current, Either Output Shorted to GND	$\|I_{OS}\|$	V_{ID} = ±100mV, one output GND, other output open or shorted to GND		19.0	24		19.0	24		19.0	24	mA
Output Short-Circuit Current, Outputs Shorted Together	$\|I_{OSAB}\|$	V_{ID} = ±100mV, V_{OUT} = $V_{\overline{OUT}}$		4.0	12		4.0	12		4.0	12	mA
POWER SUPPLY												
Supply Current	I_{CC}	MAX9377, all pins open except V_{CC}, GND		13	22		15	22		17	22	mA
		MAX9378, R_L = 100, quiescent, inputs are open		18.0	30		20	30		22	30	

Anything-to-LVPECL/LVDS Translators with Pin-Selectable Divide-by-Four

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input frequency ≤ 1.34GHz, differential input transition time = 125ps (20% to 80%), input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V) MAX9377, LVDS outputs terminated with R_L = 100Ω ±1% (MAX9378), T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reset-to-Differential Output Low Delay	t_{DR}	Figure 4		0.8	1.0	ns
Reset-to-Input Clock Setup Time	t_{SET}	Figure 4	0.5			ns
Clock-to-Divider Output Propagation Delay	t_{PCO}	Figure 4 (Note 5)		0.6	1.0	ns
SEL to Switched Output Delay	t_{SEL}	Figure 5		0.3	0.6	ns
MAX9377						
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 250mV	2.0	2.5		GHz
Propagation Delay Low to High	t_{PLH}	Figure 3, SEL = 0	250	421	600	ps
Propagation Delay High to Low	t_{PHL}	Figure 3, SEL = 0	250	421	600	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	(Note 6)		6	30	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	Figure 3		116	220	ps
Output High-to-Low Transition Time (20% to 80%)	t_F	Figure 3		116	220	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.34GHz (Note 7), SEL = 0		0.7	2	$ps_{(RMS)}$
MAX9378						
Switching Frequency	f_{MAX}	V_{OD} ≥ 250mV	2.0	2.5		GHz
Propagation Delay Low to High	t_{PLH}	Figure 3, SEL = 0	250	363	600	ps
Propagation Delay High to Low	t_{PHL}	Figure 3, SEL = 0	250	367	600	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figure 3 (Note 6)		3	30	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	Figure 2		93	220	ps
Output High-to-Low Transition Time (20% to 80%)	t_F	Figure 2		93	220	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.34GHz (Note 7), SEL = 0		0.8	2	$ps_{(RMS)}$

Note 1: Measurements are made with the device in thermal equilibrium. All voltages are referenced to ground except V_{THD}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design and characterization over the full operating temperature range.

Note 4: Guaranteed by design and characterization, not production tested. Limits are set at ±6 sigma.

Note 5: t_{PCO} is the delay associated with the frequency-divider function. The total delay when divide-by-four is selected is t_{PCO} + t_{PLH}.

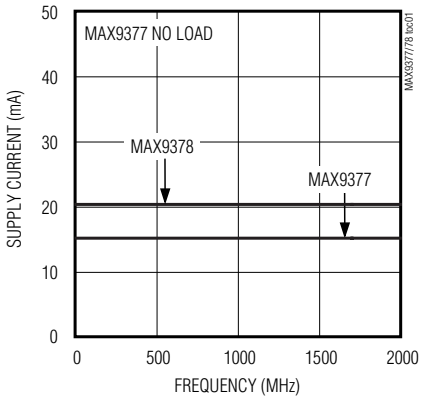
Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output under same conditions; $t_{SKEW} = |t_{PHL} - t_{PLH}|$.

Note 7: Device jitter added to the input signal.

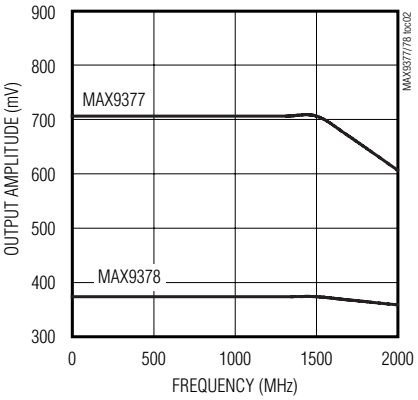
Typical Operating Characteristics

(V_{CC} = +3.3V, differential input voltage $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input frequency = 500MHz, outputs terminated with 50Ω ±1% to V_{CC} - 2.0V (MAX9377), outputs terminated with 100Ω ±1% (MAX9378), T_A = +25°C, unless otherwise noted.)

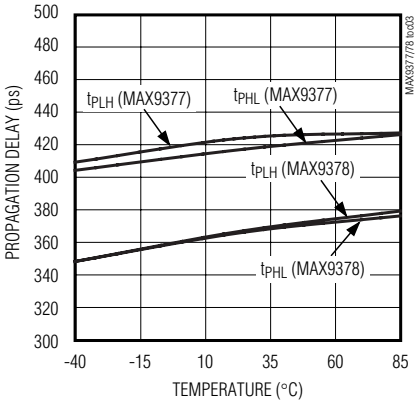
SUPPLY CURRENT vs. FREQUENCY



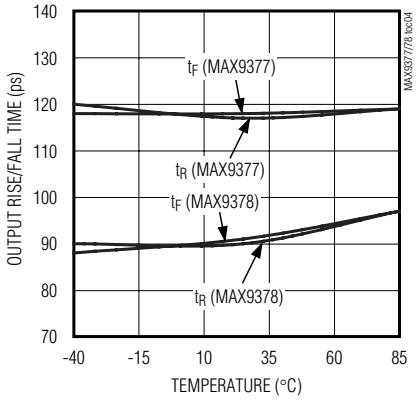
OUTPUT AMPLITUDE vs. FREQUENCY



PROPAGATION DELAY vs. TEMPERATURE



OUTPUT RISE/FALL TIME vs. TEMPERATURE



Anything-to-LVPECL/LVDS Translators with Pin-Selectable Divide-by-Four

Pin Description

PIN	NAME	FUNCTION	
1	SEL	Frequency Divider Select Input. High = divide by four, low = no division. Internal 75kΩ pulldown to GND.	
2	IN	Differential LVDS/Any Noninverting Input	
3	$\overline{IN}$	Differential LVDS/Any Inverting Input	
4	GND	Ground	
5	RST	Frequency Divider Reset Input. Active high, asynchronous, reset. Internal 75kΩ pulldown to GND.	
6	$\overline{OUT}$	MAX9377	Differential LVPECL Inverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.
		MAX9378	Inverting LVDS Output. Terminate to OUT with 100Ω ±1%.
7	OUT	MAX9377	Differential LVPECL Noninverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.
		MAX9378	Noninverting LVDS Output. Terminate to $\overline{OUT}$ with 100Ω ±1%.
8	V_{CC}	Positive Supply. Bypass from V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device	

Detailed Description

The MAX9377/MAX9378 are fully differential, high-speed, low-jitter anything-to-LVPECL and anything-to-LVDS translators, respectively, with a selectable divide-by-four function. Low propagation delay and high speed make them ideal for various high-speed network routing and backplane applications at speeds up to 2GHz in nondivide mode.

The MAX9377/MAX9378 accept any differential input signals within the supply rails and with a minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. The MAX9377 outputs are LVPECL and have sufficient current to drive 50Ω transmission lines. The MAX9378 outputs are LVDS and conform to the ANSI EIA/TIA-644 LVDS standard.

Inputs

Inputs have a wide common-mode range of 0.05V to (V_{CC} - 0.05V), which accommodates any differential signals within the supply rails, and requires a minimum of 100mV to switch the outputs. This allows the MAX9377/MAX9378 inputs to support virtually any differential signaling standard.

RST and SEL Inputs

The frequency-divide functions are controlled by two LVCMOS/LVTTL inputs, RST and SEL. SEL selects either the divide-by-four function or a no-division function as shown in Table 1. RST, an asynchronous active-high input, resets the divide-by-four within the device and places the circuits into a known state. Setting RST high when powering up the device with SEL high prevents the unknown states with the divider from being propagated to the outputs. If the device is powered up with SEL high but without asserting RST, the outputs are only guaranteed to be 1/4th the input frequency after 2.5 cycles have been applied to the input.

Table 1. SEL AND RST Truth Table

RST	SEL	OUTPUT
X	L or open	No frequency division.
H	H	Outputs are placed in differential low.
L	H	Divide-by-four function.

LVPECL Outputs (MAX9377)

The MAX9377 LVPECL outputs are emitter followers that require external resistive paths to a voltage source (V_T = V_{CC} - 2.0V typ) more negative than worst-case V_{OL} for proper static and dynamic operation. When properly terminated, the outputs generate steady-state voltage levels, V_{OL} or V_{OH} with fast transition edges between state levels. Output current always flows into the termination during proper operation.

LVDS Outputs (MAX9378)

The MAX9378 LVDS outputs require a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor. With a 3.5mA typical output current, the MAX9378 produces an output voltage of 350mV when driving a 100Ω load.

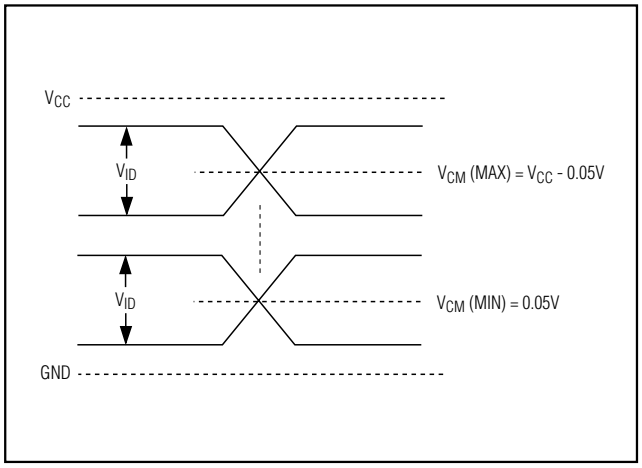


Figure 1. Differential Input Definition

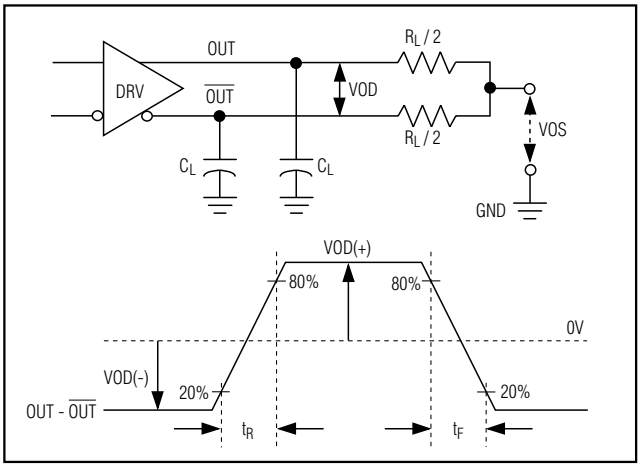


Figure 2. LVDS Output Load and Transition Times

Applications Information

LVPECL Output Termination (MAX9377)

Terminate the MAX9377 LVPECL outputs with 50Ω to (V_{CC} - 2V) or use equivalent Thevenin terminations. Terminate OUT and $\overline{OUT}$ with identical termination on each for low output distortion. When a single-ended signal is taken from the differential output, terminate both OUT and $\overline{OUT}$. Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

LVDS Output Termination (MAX9378)

The MAX9378 LVDS outputs are current-steering devices; no output voltage is generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels are dependent upon the value of the termination resistor. The MAX9378 is optimized for point-to-point communication with the 100Ω termination resistor at the receiver inputs. Termination resistance values may range between 90Ω and132Ω, depending on the characteristic impedance of the transmission medium.

Supply Bypassing

Bypass V_{CC} to ground with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals.

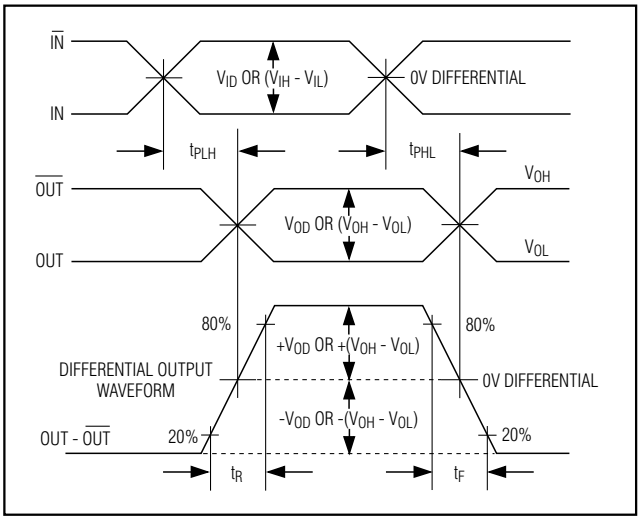


Figure 3. Differential Input-to-Output Propagation Delay Timing Diagram

Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Anything-to-LVPECL/LVDS Translators with Pin-Selectable Divide-by-Four

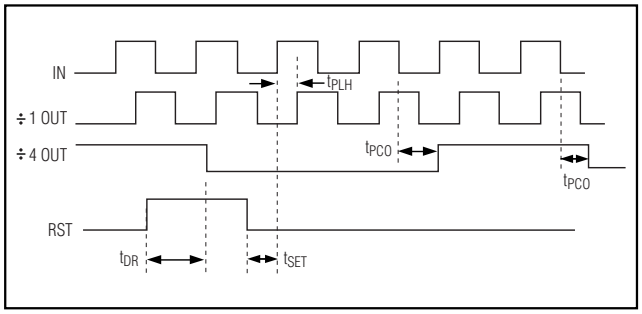


Figure 4. Frequency Divider and Reset Timing Diagram

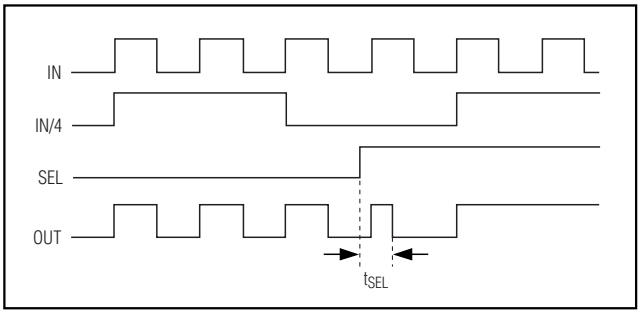


Figure 5. Frequency Select Delay Timing Diagram

Chip Information

MAX9377 TRANSISTOR COUNT: 614

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PROCESS: Bipolar