Click here for production status of specific part numbers.

MAXM22510/MAXM22511 — 2.5kV$_{RMS}$ Complete Isolated RS-485/RS-422 Module Transceiver + Power

General Description

The MAXM22510 and MAXM22511 isolated RS-485/RS-422, full-duplex, transceiver modules provide 2500V$_{RMS}$ (60s) of galvanic isolation between the cable-side (RS-485/RS-422 driver/receiver side) and the UART-side of the device. An integrated DC-DC powers the cable-side of the module. No external components are required.

Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. These devices allow for robust communication up to 500kbps (MAXM22510) and 25Mbps (MAXM22511).

The MAXM22510/MAXM22511 operate from a single 3.3V supply on the UART-side. An integrated DC-DC converter generates the 3.3V operating voltage for the cable-side of the module.

The devices include one drive channel and one receive channel. The receiver is 1/4-unit load, allowing up to 128 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable-side or UART-side power supplies are below functional levels.

The driver outputs and receiver inputs are protected from ±35kV electrostatic discharge (ESD) to GNDB on the cable-side, as specified by the Human Body Model (HBM).

The MAXM22510/MAXM22511 are available in an LGA 44-pin package and operate over the -40°C to +105°C temperature range.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Space Saving Solution
  - Fully Integrated Module for Compact Design
- High-Performance Transceiver Enables Flexible Designs
  - Integrated DC-DC for Cable-Side Power
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 500kbps Maximum Data Rate for the MAXM22510
  - 25Mbps Maximum Data Rate for the MAXM22511
  - Allows Up to 128 Devices on the Bus
- Integrated Protection Ensures for Robust Communication
  - ±35kV ESD (HBM) on Driver Outputs/Receiver Inputs
  - 2.5kV$_{RMS}$ Withstand Isolation Voltage for 60 Seconds (V$_{ISO}$)
  - 630V$_{PEAK}$ Maximum Repetitive Peak-Isolation Voltage (V$_{IORM}$)
  - 445V$_{RMS}$ Maximum Working-Isolation Voltage (V$_{IOWM}$)
  - Withstands ±10kV Surge per IEC 61000-4-5
  - Thermal Shutdown

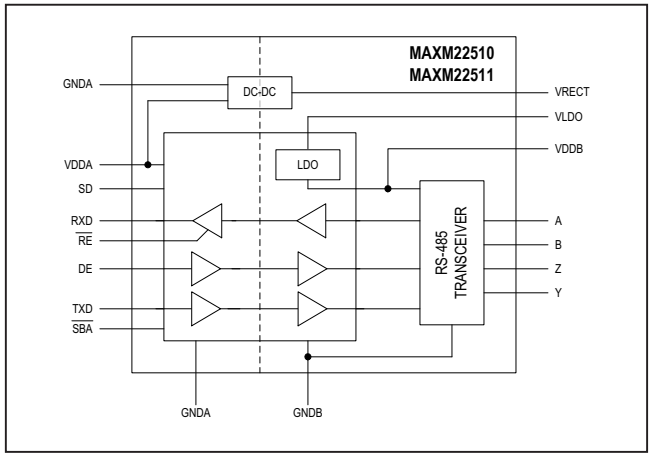
Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A

Applications

- Industrial Automation
- Programmable Logic Controllers
- HVAC
- Power Meters
- Building Automation

Functional Diagram



Absolute Maximum Ratings

V_{DDA} to GNDA .....-0.3V to +4V
V_{DDB} to GNDB.....-0.3V to +6V
V_{RECT}, V_{LDO} to GNDB.....-0.3V to +8V
SD, TXD, DE, $\overline{RE}$ to GNDA .....-0.3V to +6V
$\overline{SBA}$, RXD to GNDA .....-0.3V to (V_{DDA} + 0.3V)
A, B, Y, Z to GNDB.....-8V to +13V
Short-Circuit Duration (RXD, $\overline{SBA}$ to GNDA, A, B, Y, Z ,V_{DDB} to GNDB) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
44-pin LGA (derate 28.6mW/°C above +70°C).....2286mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+125°C
Storage Temperature Range..... -65°C to +125°C
Soldering Temperature (reflow).....+245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 44 LGA	
Package Code	L44119M+1
Outline Number	**21-100226**
Land Pattern Number	**90-100107**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC}) (top)	39.2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} – V_{GNDA} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{DDA}		3.0		3.6	V
Supply Current	I_{DDA}	V_{DDA} = 3.3V, DE = high, $\overline{RE}$ = TXD = low, SD = low, RXD unconnected, no load		25	44	mA
Shutdown Supply Current	I_{SD}	V_{DDA} = 3.3V, SD = high		0.01	10	µA
Undervoltage Lockout Threshold	V_{UVLOA}	V_{DDA} rising	2.55	2.7	2.85	V
	V_{UVLOB}	V_{DDB} rising	2.55	2.7	2.85	
Undervoltage Lockout Threshold Hysteresis	$V_{UVHYSTA}$			200		mV
	$V_{UVHYSTB}$			200		
Unregulated DC-DC Output Voltage	V_{RECT}	V_{DDA} = 3.3V, DE = high, $\overline{RE}$ = TXD = low, SD = low, no load		6		V

DC Electrical Characteristics (continued)

(V_{DDA} – V_{GNDA} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO						
LDO Output Voltage	V_{DDB}		3.0	3.3	3.6	V
LDO Current Limit				300		mA
Load Regulation		V_{LDO} = 3.3V, I_{LOAD} = -20mA to -40mA		0.19	1.7	mV/mA
Line Regulation		V_{LDO} = 3.3V to 7.5V, I_{LOAD} = -20mA		0.12		mV/V
Dropout Voltage		V_{LDO} = 3.18V, I_{DDB} = -120mA		100	180	mV
Load Capacitance		Nominal value (Note 3)	1		10	µF
LOGIC INTERFACE (TXD, RXD, DE, $\overline{RE}$, SD, $\overline{SBA}$)						
Input High Voltage	V_{IH}	$\overline{RE}$, TXD, DE, SD to GNDA	0.7 x V_{DDA}			V
Input Low Voltage	V_{IL}	$\overline{RE}$, TXD, DE, SD to GNDA			0.8	V
Input Hysteresis	V_{HYS}	$\overline{RE}$, TXD, DE, SD to GNDA		220		mV
Input Capacitance	C_{IN}	$\overline{RE}$, TXD, DE, SD, f = 1MHz		2		pF
Input Pullup Current	I_{PU}	TXD, SD	-10	-4.5	-1.5	µA
Input Pulldown Current	I_{PD}	DE, $\overline{RE}$	1.5	4.5	10	µA
$\overline{SBA}$ Pullup Resistance	R_{SBA}		3	5	8	kΩ
Output Voltage High	V_{OH}	RXD to GNDA, I_{OUT} = -4mA	V_{DDA} -0.4			V
Output Voltage Low	V_{OL}	RXD to GNDA, I_{OUT} = 4mA			0.40	V
		$\overline{SBA}$ to GNDA, I_{OUT} = 4mA			0.45	
Short-Circuit Output Pullup Current	I_{SH_PU}	0V ≤ V_{RXD} ≤ V_{DDA}, (V_A - V_B) > -10mV, $\overline{RE}$ = low	-42			mA
Short-Circuit Output Pulldown Current	I_{SH_PD}	0V ≤ V_{RXD} ≤ V_{DDA}, (V_A - V_B) < -200mV, $\overline{RE}$ = low			42	mA
		0V ≤ $V_{\overline{SBA}}$ ≤ V_{DDA}, $\overline{SBA}$ is asserted			60	
Three-State Output Current	I_{OZ}	0V ≤ V_{RXD} ≤ V_{DDA}, $\overline{RE}$ = high	-1		+1	µA
DRIVER						
Differential Driver Output	$\lvert V_{OD} \rvert$	R_L = 54Ω, TXD = high or low, Figure 1a	1.5			V
		R_L = 100Ω, TXD = high or low, Figure 1a	2.0			
		-7V ≤ V_{CM} ≤ +12V, Figure 1b	1.5		5	
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	R_L = 100Ω or 54Ω, Figure 1a (Note 4)			0.2	V

DC Electrical Characteristics (continued)

(V_{DDA} – V_{GNDA} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Common-Mode Output Voltage	V_{OC}	R_L = 100Ω or 54Ω, Figure 1a		V_{DDB}/ 2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1a (Note 4)			0.2	V
Driver Short-Circuit Output Current	I_{OSD}	GNDB ≤ V_{OUT} ≤ +12V, output low (Note 5)	+30		+250	mA
		-7V ≤ V_{OUT} ≤ V_{DDB}, output high (Note 5)	-250		-30	
Single-Ended Driver Output Voltage High	V_{OH}	Y and Z outputs, $I_{Y,Z}$ = -20mA	2.2			V
Single-Ended Driver Output Voltage Low	V_{OL}	Y and Z outputs, $I_{Y,Z}$ = +20mA			0.8	V
Differential Driver Output Capacitance	C_{OD}	DE = $\overline{RE}$ = high, f = 4MHz		12		pF
RECEIVER						
Input Current (A and B)	I_A, I_B	DE = low, V_{DDB} = GNDB or 3.6V, V_{IN} = +12V			+250	μA
		DE = low, V_{DDB} = GNDB or 3.6V, V_{IN} = -7V	-200			
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +12V	-200	-120	-10	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		20		mV
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V, DE = low	48			kΩ
Differential Input Capacitance	$C_{A,B}$	Measured between A and B, DE = $\overline{RE}$ = low, f = 6MHz		12		pF
PROTECTION						
Thermal Shutdown Threshold	T_{SHDN}	Temperature Rising		+160		°C
Thermal Shutdown Hysteresis	T_{HYST}			15		°C
ESD Protection (A, B, Y, Z Pins to GNDB)		Human Body Model		±35		kV
		IEC 61000-4-2 Air Gap Discharge		±18		
		IEC 61000-4-2 Contact Discharge		±8		
ESD Protection (A, B, Y, Z Pins to GNDA)		Human Body Model		±6		kV
		330pF capacitor from GNDB to GNDA		±20		
ESD Protection (All Other Pins)		Human Body Model		±4		kV

Switching Electrical Characteristics (MAXM22510)

(V_{DDA} – V_{GNDA} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common Mode Transient Immunity	CMTI	(Note 6)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF Figure 2 and Figure 3			1040	ns
Differential Driver Output Skew $\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			144	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			900	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 4			2540	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			2540	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			140	ns
Driver Disable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			140	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			240	ns
Receiver Output Skew $\|t_{RPLH} - t_{RPHL}\|$	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			34	ns
Maximum Data Rate	DR_{MAX}		500			kbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time From Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time From High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
POWER						
V_{DDB} Startup Delay After Shutdown		No load on V_{DDB}, SD falling		165		µs
Time to Shutdown		SD rising		80		ns

Switching Electrical Characteristics (MAXM22511)

(V_{DDA} – V_{GNDA} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} – V_{GNDA} = 3.3V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common Mode Transient Immunity	CMTI	(Note 6)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			65	ns
Differential Driver Output Skew $\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			7	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 2 and Figure 3			10	ns
Maximum Data Rate	DR_{MAX}		25			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, Figure 4			80	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, Figure 5			80	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, Figure 5			80	ns
Driver Disable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, Figure 4			80	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			65	ns
Receiver Output Skew $\|t_{RPLH} - t_{RPHL}\|$	t_{RSKEW}	C_L = 15pF, Figure 6 and Figure 7 (Note 7)			7	ns
Maximum Data Rate	DR_{MAX}		25			Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time From Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time From High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, S2 closed, Figure 8			20	ns
POWER						
V_{DDB} Startup Delay After Shutdown		No load on V_{DDB}, SD falling		165		µs
Time to Shutdown		SD rising		80		ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 3: Not production tested. Guaranteed by design and characterization.

Note 4: ΔV_{OD} and ΔV_{OC} are the changes in $|V_{OD}|$ and V_{OC}, respectively, when the TXD input changes state.

Note 5: The short circuit output current applies to the peak current just prior to current limiting.

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC) (Note 3)	1182	V_P
Maximum Repetitive Peak Withstand Voltage	V_{IORM}	(Note 8)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	(Note 8)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}		3600	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	t = 60s, f = 60Hz (Notes 8,9)	2500	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	IEC 61000-4-5, 1.2/50µs	10	kV
Insulation Resistance	R_S	T_A = +150°C, V_{IO} = 500V	$>10^9$	Ω
Insulation Resistance	R_{IO}	T_A = +25°C, V_{IO} = 500V	$>10^{12}$	Ω
Barrier Capacitance Input to Output	CIO		6	pF
Creepage Distance	CPG		8	mm
Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparitive Tracking Resistance Index	CTI	Material Group II (IEC 60112)	550	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB. V_{CM} = 1kV.

Note 7: Capacitive load includes test probe and fixture capacitance.

Note 8: V_{IORM}, V_{IOWM}, and V_{ISO} are defined by the IEC 60747-5-5 standard.

Note 9: As required by UL1577, each IC is proof tested for the 2500 V_{RMS} rating by applying the equivalent positive and negative peak voltage, multiplied by an acceleration factor of 1.2 (±4243V) for 1 second.

Safety Regulatory Approvals

UL
The MAXM22510/MAXM22511 are certified under UL1577. For more details, refer to File E351759.
Rated up to 2500V_{RMS} for single protection.
cUL (Equivalent to CSA notice 5A)
The MAXM22510/MAXM22511 are certified up to 2500V_{RMS} for single protection. For more details, refer to File E351759.

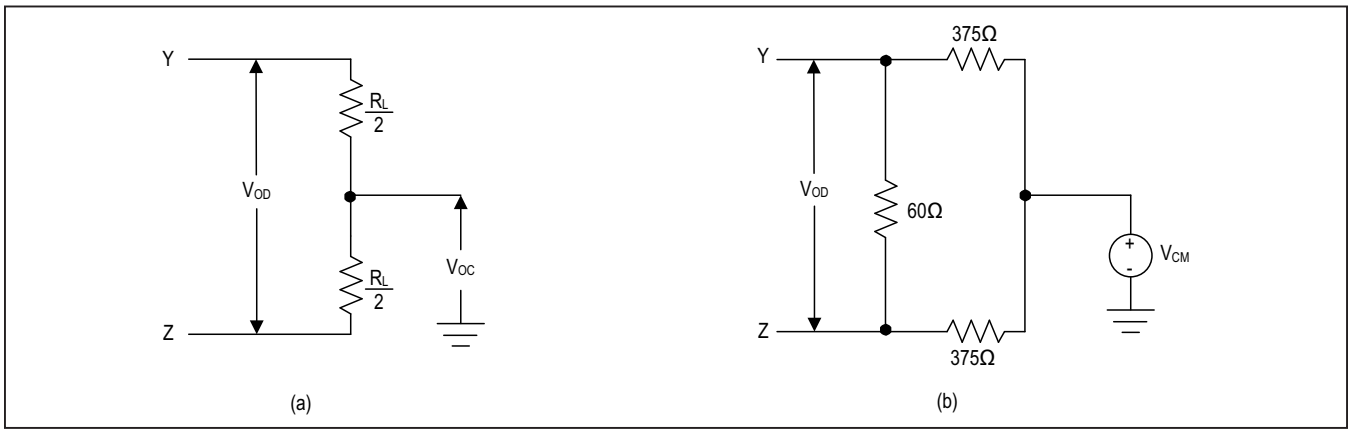


Figure 1. Driver DC Test Load

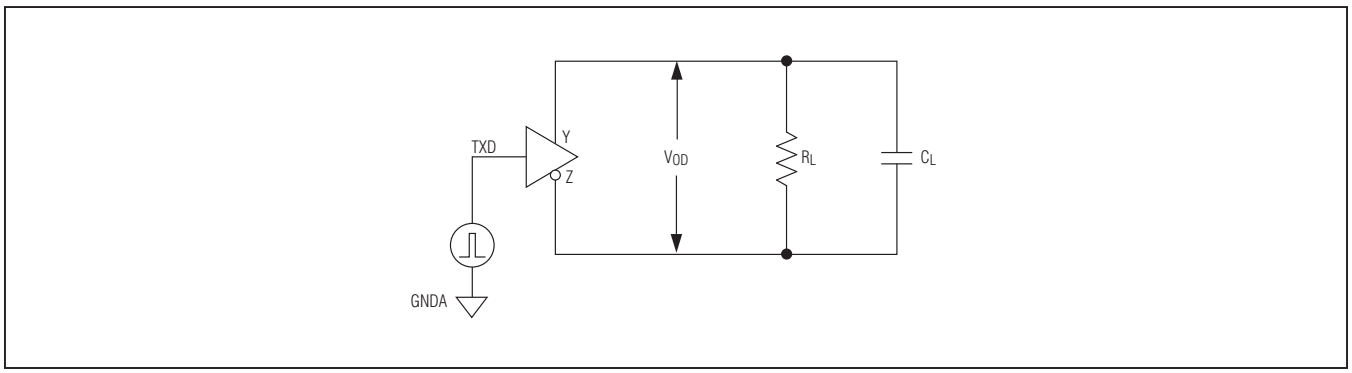


Figure 2. Driver Timing Test Circuit

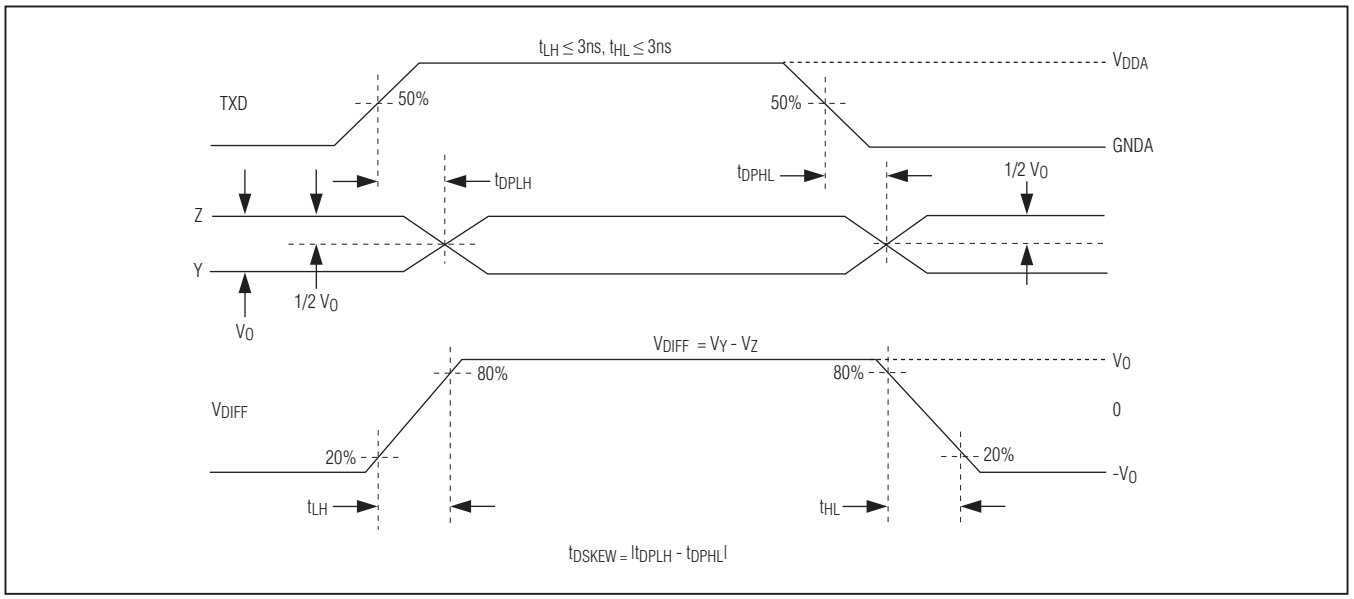


Figure 3. Driver Propagation Delays

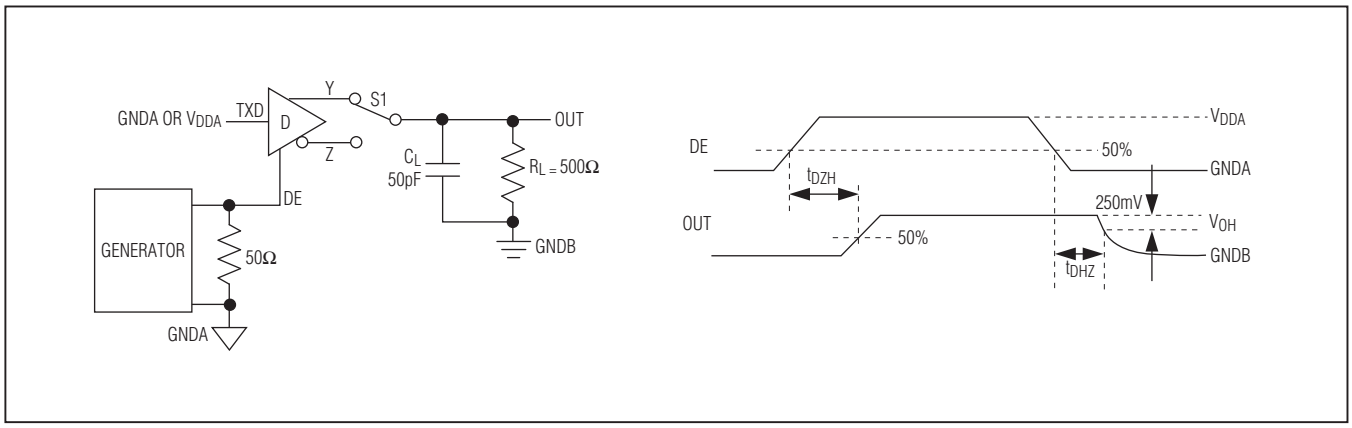


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH})

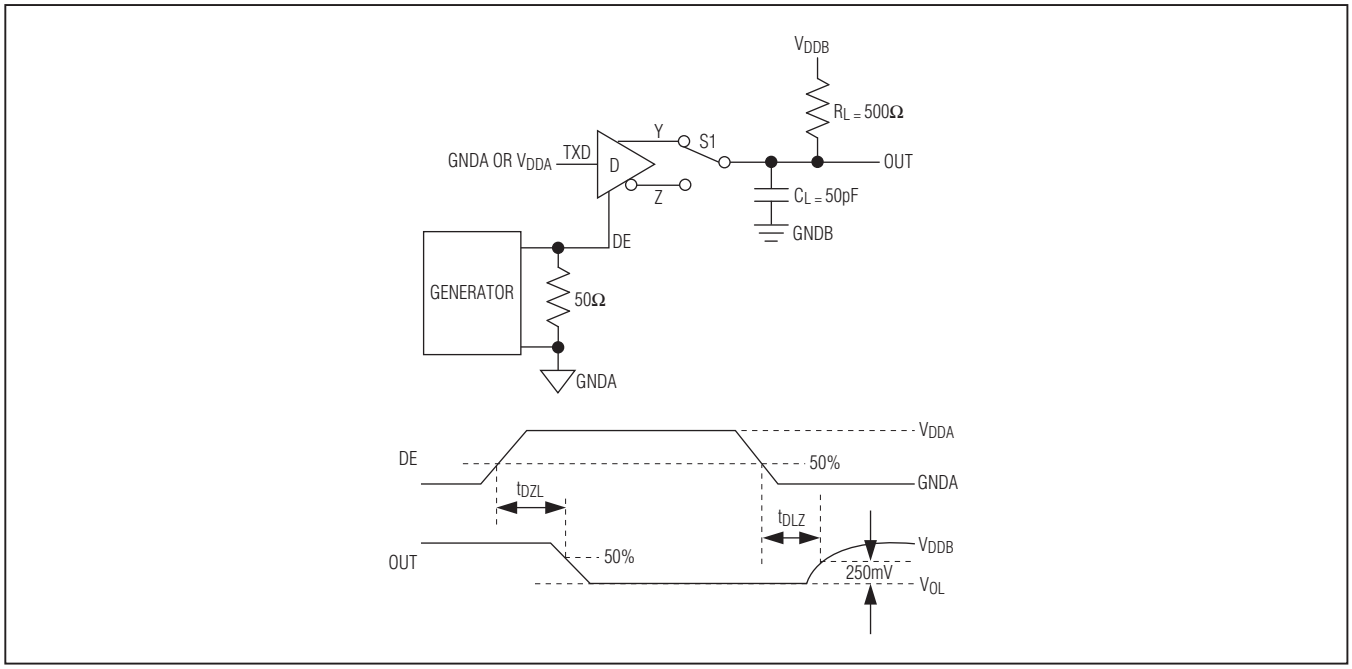


Figure 5. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

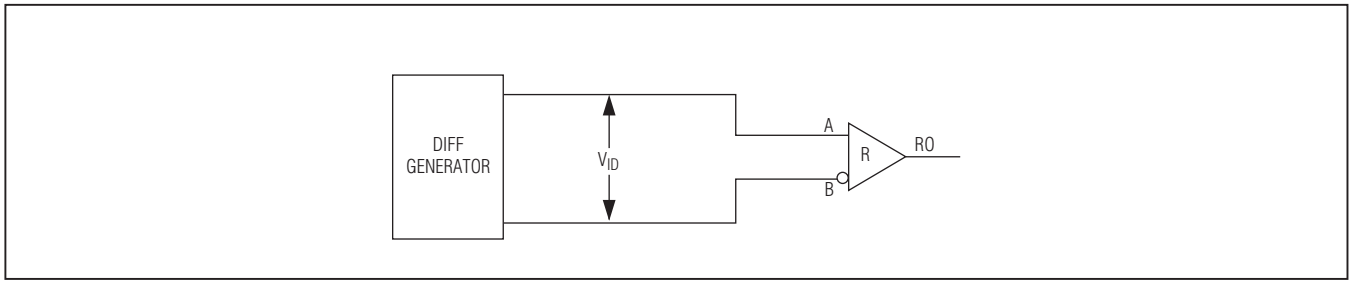


Figure 6. Receiver Propagation Delay Test Circuit

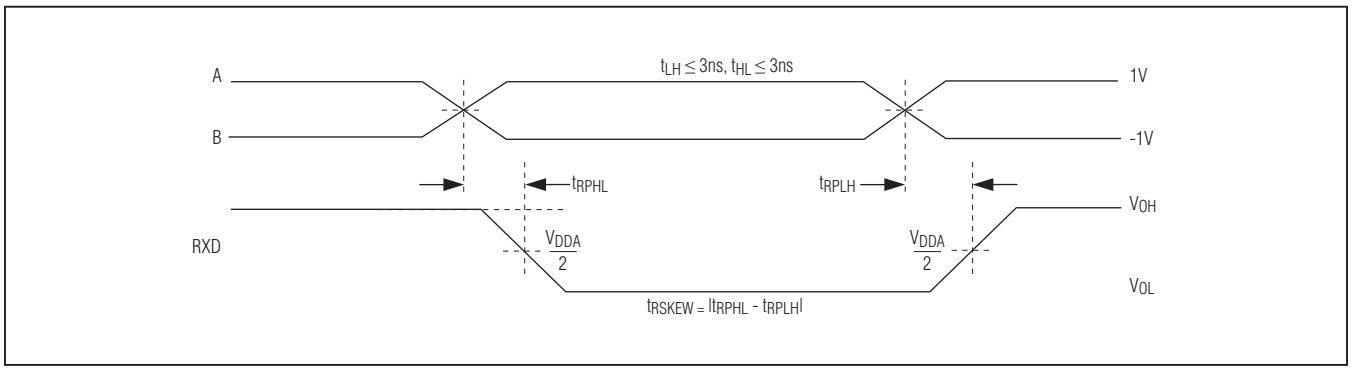


Figure 7. Receiver Propagation Delays

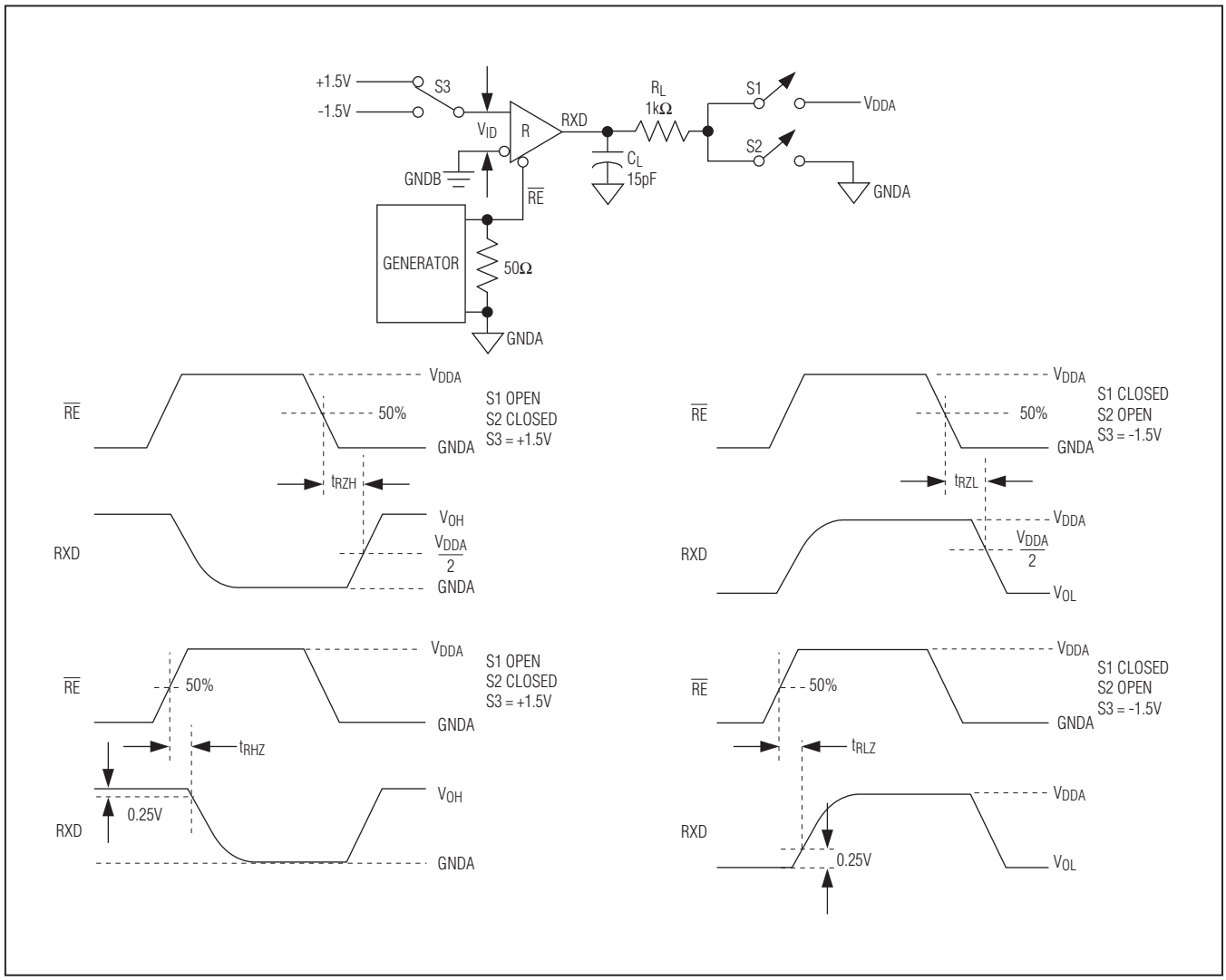
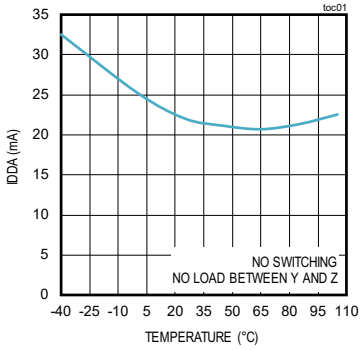


Figure 8. Receiver Enable and Disable Times

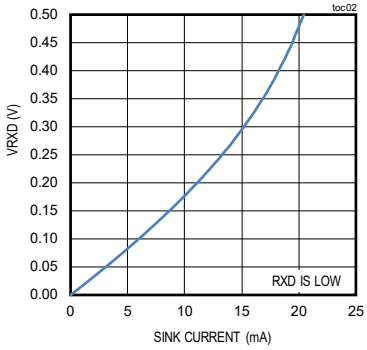
Typical Operating Characteristics

($V_{DDA} - V_{GNDA}$ = 3.3V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C, unless otherwise noted.)

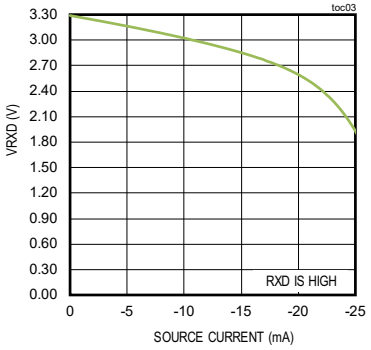
VDDA SUPPLY CURRENT vs. TEMPERATURE



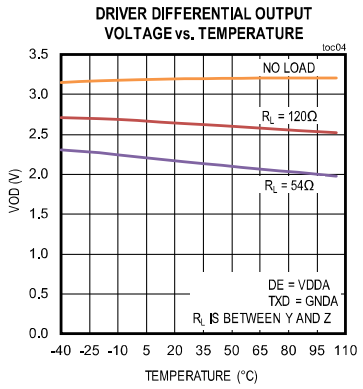
RXD OUTPUT VOLTAGE vs. SINK CURRENT



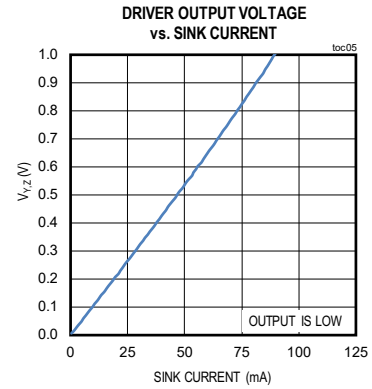
RXD OUTPUT VOLTAGE vs. SOURCE CURRENT



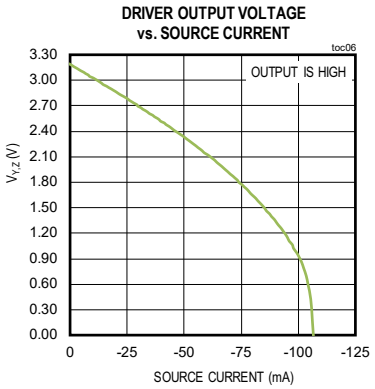
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



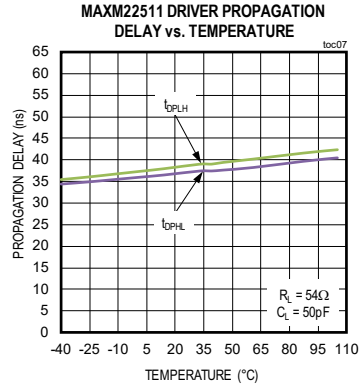
DRIVER OUTPUT VOLTAGE vs. SINK CURRENT



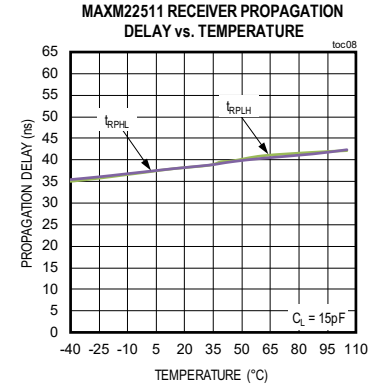
DRIVER OUTPUT VOLTAGE vs. SOURCE CURRENT



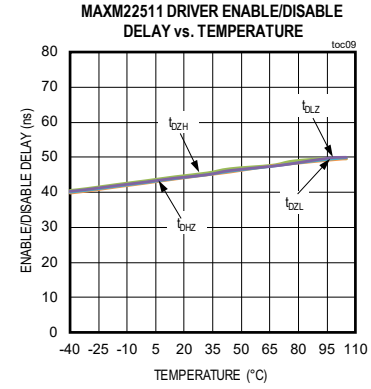
MAXM22511 DRIVER PROPAGATION DELAY vs. TEMPERATURE



MAXM22511 RECEIVER PROPAGATION DELAY vs. TEMPERATURE

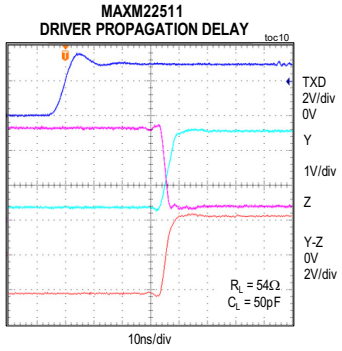


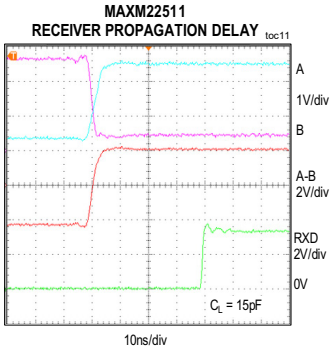
MAXM22511 DRIVER ENABLE/DISABLE DELAY vs. TEMPERATURE

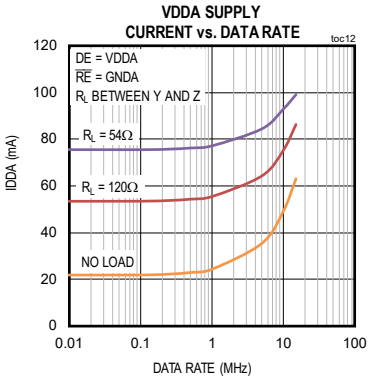


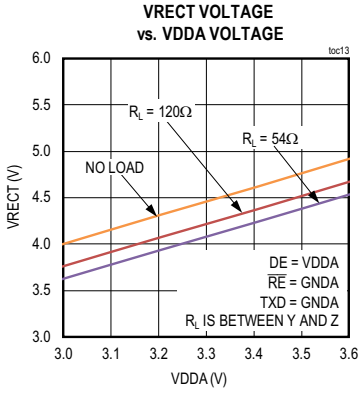
Typical Operating Characteristics (continued)

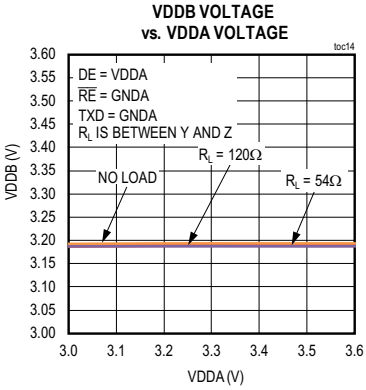
($V_{DDA} - V_{GNDA}$ = 3.3V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C, unless otherwise noted.)

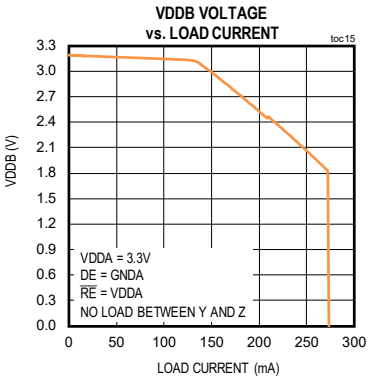


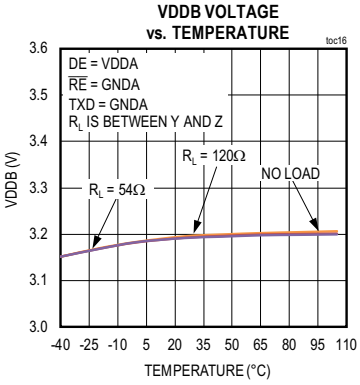






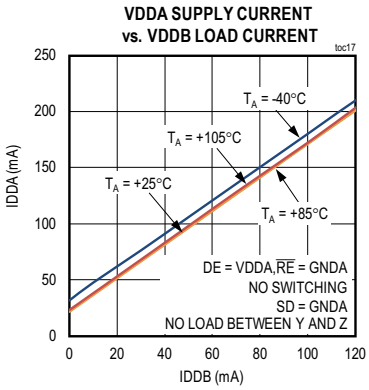


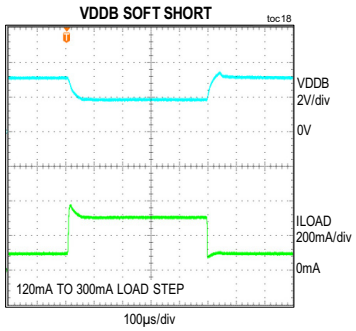


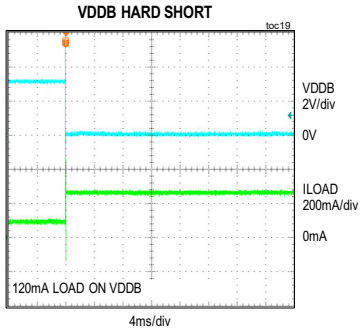


Typical Operating Characteristics (continued)

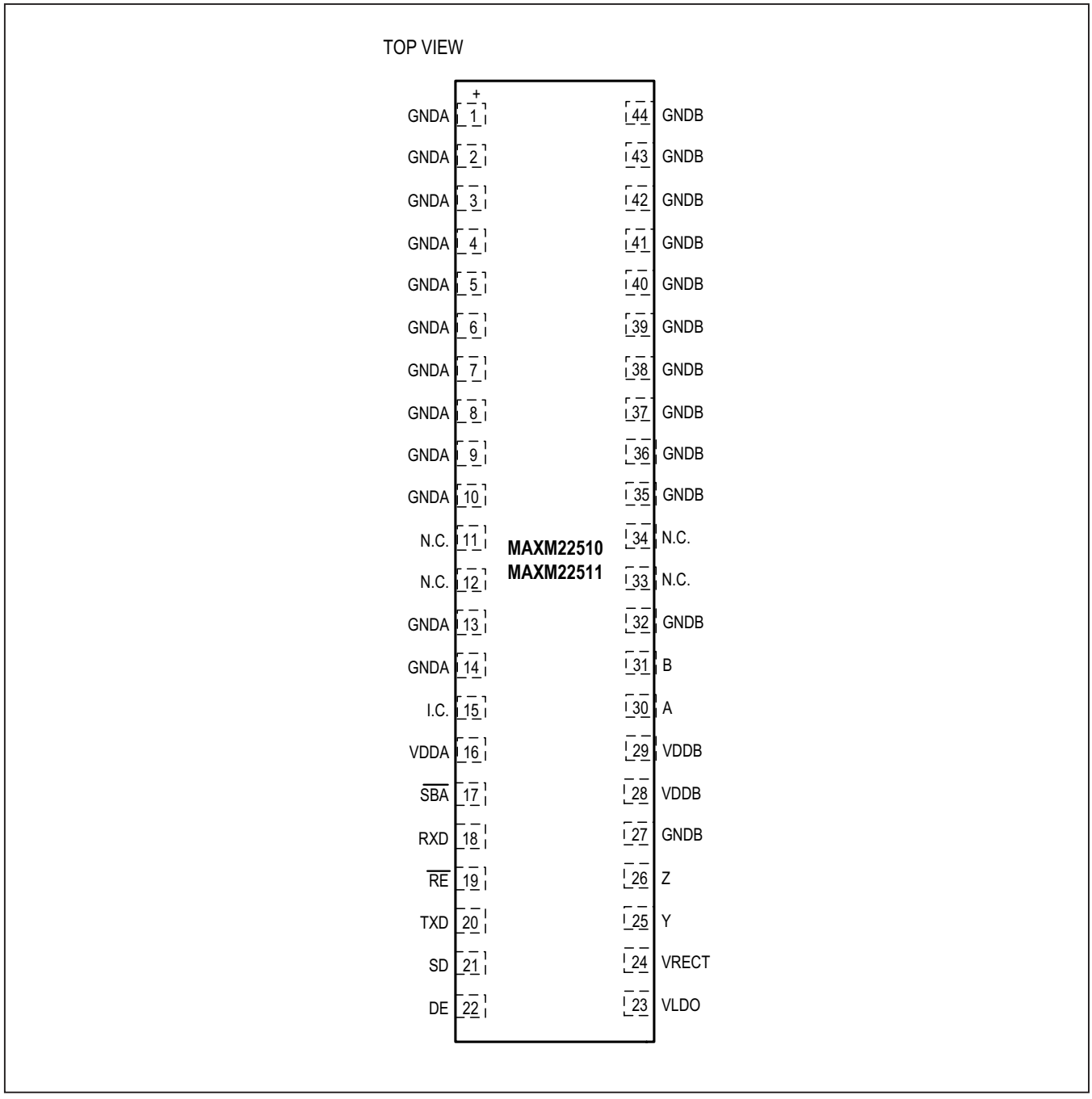
($V_{DDA} - V_{GNDA}$ = 3.3V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C, unless otherwise noted.)







Pin Configuration



Pin Description

PIN	NAME	REFERENCE	FUNCTION
1-10, 13, 14	GNDA	—	UART-side/Side A Ground. GNDA is the ground reference for digital signals and the UART-side/side A power supply.
11, 12, 33, 34	N.C.	—	Not Connected. Not internally connected.
15	I.C.	GNDA	Internally Connected. Leave I.C. unconnected.
16	V_{DDA}	GNDA	UART-side/Side A Power Input. Apply a 3.3V supply voltage to V_{DDA}.
17	$\overline{SBA}$	GNDA	Cable-side/Side B Active Indicator Open-Drain Output. $\overline{SBA}$ asserts low when the cable-side/side B is powered and working. $\overline{SBA}$ has an internal 5kΩ pullup resistor to V_{DDA}. $\overline{SBA}$ is high impedance when the device is in shutdown (SD is high).
18	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when (V_A – V_B) > -10mV and is low when (V_A – V_B) < -200mV. RXD is high when V_{DDB} is less than V_{UVLOB}. RXD is high-impedance when $\overline{RE}$ is high or when SD is high.
19	$\overline{RE}$	GNDA	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high-impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5µA pulldown to GNDA.
20	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (Y) low and the inverting output (Z) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5µA pull-up to V_{DDA}.
21	SD	GNDA	Shutdown Input. Drive SD low for normal operation. Drive SD high to force the part into shutdown mode. When SD is high, the logic inputs/outputs are in a reset state and the cable-side/side B of the device is unpowered. Do not leave SD disconnected.
22	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs Y and Z on the cable-side/side B of the device. Drive DE low to disable Y and Z. Y and Z are high impedance when DE is low. DE has an internal 4.5µA pull-down to GNDA.
23	V_{LDO}	GNDB	Cable-side/Side B LDO Input. Connect V_{LDO} to V_{RECT} to power the cable-side of the device.
24	V_{RECT}	GNDB	Cable-side/Side B DC-DC Unregulated Output. Connect V_{RECT} to V_{LDO} to power the cable-side of the device.
25	Y	GNDB	Noninverting Driver Output
26	Z	GNDB	Inverting Driver Output
27, 32, 35-44	GNDB	—	Cable-Side/Side B Ground. GNDB is the ground reference for the internal LDO and the RS-485/RS-422 bus signals.
28, 29	V_{DDB}	GNDB	Cable-Side/Side B LDO Power Output. V_{DDB} is the output of the internal LDO.
30	A	GNDB	Noninverting Receiver Input
31	B	GNDB	Inverting Receiver Input

Function Tables

TRANSMITTING						
INPUTS					OUTPUTS	
V_{DDA}	V_{DDB}	SD	DE*	TXD	Y	Z
≥ V_{UVLOA}	≥ V_{UVLOB}	0	1	1	1	0
				0	0	1
			0	X	High-Z	High-Z
	< V_{UVLOB}		X	X	High-Z	High-Z
< V_{UVLOA}	X	0	X	X	High-Z	High-Z
X	X	1	X	X	High-Z	High-Z

**Note: Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pulldown to GNDA.*

X = Don't care

RECEIVING (DE = 0)					
INPUTS					OUTPUTS
V_{DDA}	V_{DDB}	SD	$\overline{RE}$*	(V_A- V_B)	RXD
≥ V_{UVLOA}	≥ V_{UVLOB}	0	0	> -10mV	1
				< -200mV	0
				Open/Short	1
			1	X	High-Z
	< V_{UVLOB}	0	0	X	1
< V_{UVLOA}	< V_{UVLOB}	0	0	X	1**
X	X	1	X	X	High-Z

**Note: Drive $\overline{RE}$ high to disable the receiver output. Drive $\overline{RE}$ low to enable to receiver output. $\overline{RE}$ has an internal pulldown to GNDA.*

***Note: RXD goes high impedance when V_{DDA} falls below 1.6V (typ).*

X = Don't care

$\overline{SBA}$			
V_{DDA}	V_{DDB}	SD	$\overline{SBA}$
< V_{UVLOA}	< V_{UVLOB}	0	High
≥ V_{UVLOA}	< V_{UVLOB}	0	High
	≥ V_{UVLOB}	0	Low
X	X	1	High-Z

X = Don't care

Detailed Description

The MAXM22510/MAXM22511 isolated RS-485/RS-422 full-duplex transceiver modules provide 2500V$_{RMS}$ (60s) of galvanic isolation between the RS-485/RS-422 cable-side of the transceiver and the UART-side. These integrated modules require no external components and no external isolated power supply for the cable-side.

These transceivers allow up to 500kbps (MAXM22510) or 25Mbps (MAXM22511) communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

Data Isolation

Data isolation is achieved using high-voltage capacitors that allow data transmission between the UART-side and the RS-485/RS-422 cable-side of the transceiver.

Integrated DC-DC for Isolated Power

Power isolation is achieved with an integrated DC-DC and LDO. A single 3.3V supply on the UART-side of the device is used to generate a regulated 3.3V supply for the cable-side.

The internal transformer used to transfer isolated power in the MAXM22510/MAXM22511 is based on a ferrite core to help reduce unwanted EMI emissions.

No power is transferred from the UART-side to the cable-side when the shutdown pin (SD) is high.

True Fail-Safe

The devices guarantee a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between -10mV and -200mV. If the differential receiver input voltage (V_A – V_B) is greater than or equal to -10mV, RXD is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold of the devices, this results in a logic-high at RXD.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Thermal Shutdown

The devices are protected from overtemperature damage by integrated thermal-shutdown circuitry. When the junction temperature (T_J) exceeds +160°C (typ), the driver outputs and RXD are high-impedance, and V_{DDB} falls to 0V. The device resumes normal operation when T_J falls below +145°C (typ).

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load. A standard driver can drive up to 32 unit-loads. The MAXM22510/MAXM22511 transceivers have a 1/4-unit load receiver, which allows up to 128 transceivers, connected in parallel, on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

Typical Application

The MAXM22510/MAXM22511 full-duplex transceivers are designed for bidirectional data communications on multi-point bus transmission lines. Figure 9 and Figure 10 show

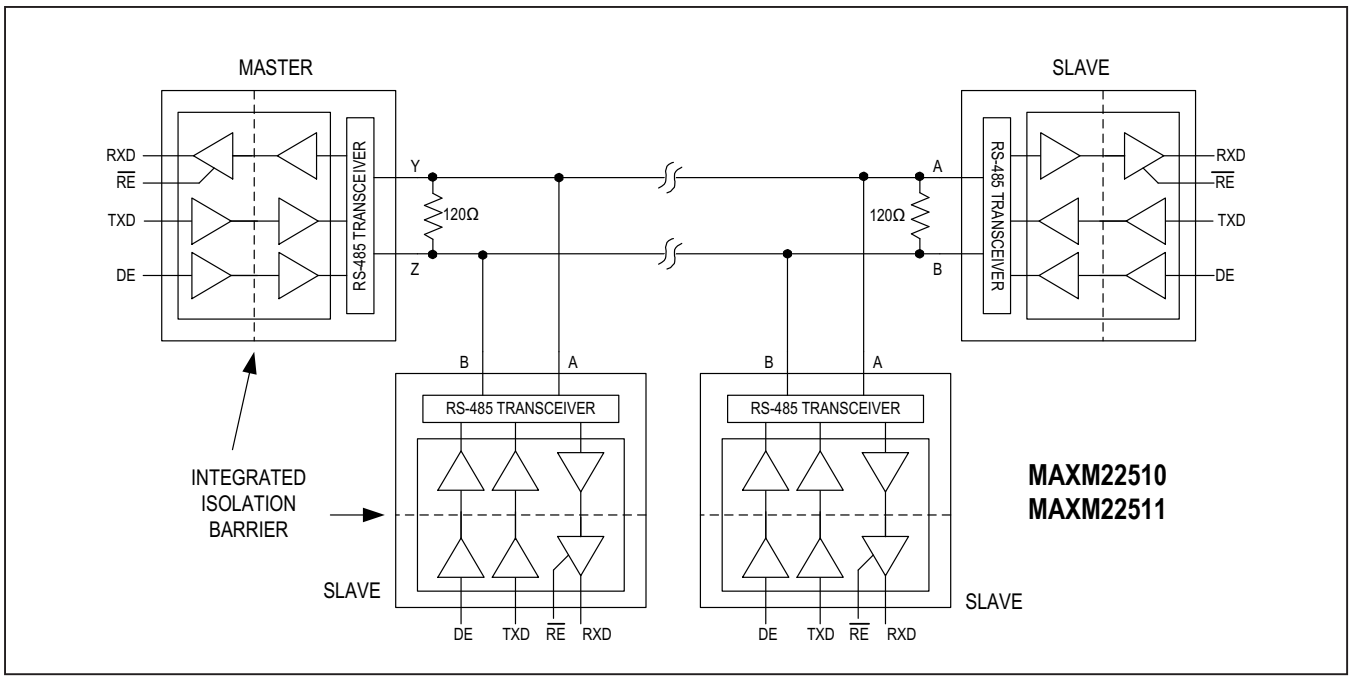


Figure 9. Typical Isolated Full-Duplex RS-485/RS-422 Application

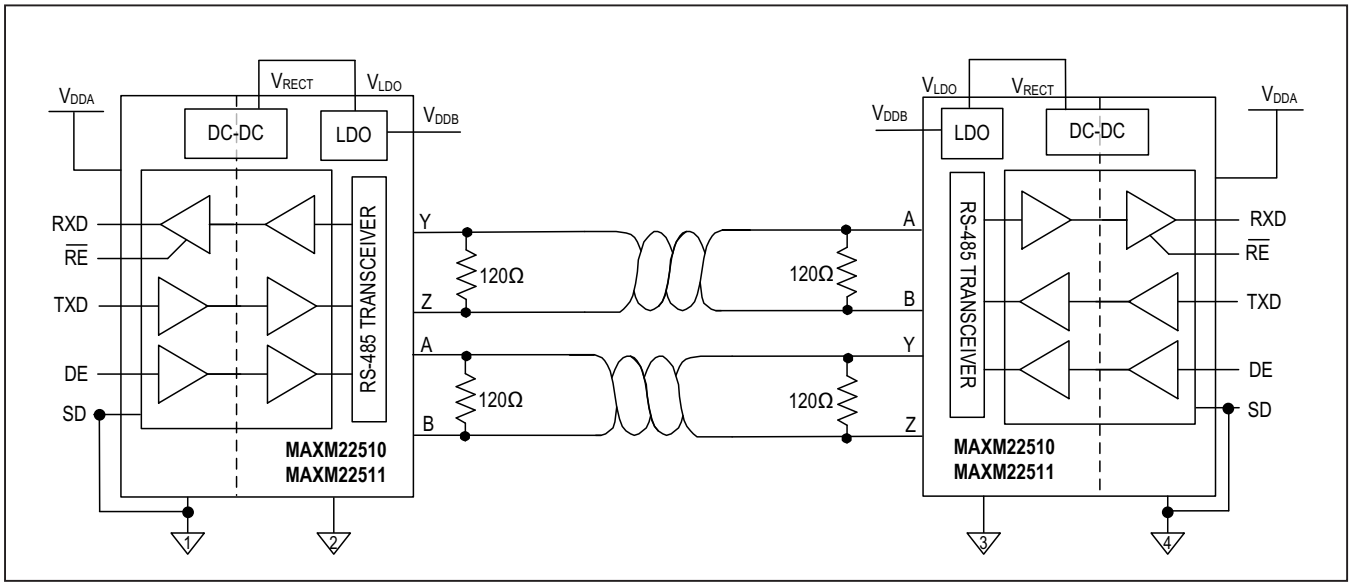


Figure 10. Typical Isolated Point-to-Point Application

typical network application circuits. To minimize reflections, the bus should be terminated at both ends in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.

Layout Considerations

It is recommended to design an isolation, or "keep-out," channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable-side and UART-side will defeat the isolation.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable-side of the devices, it is good practice to have the bus connectors and termination resistor as close as possible to the I/O pins.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the devices have extra protection against static electricity to the cable-side ground reference. The ESD structures withstand high-ESD events during normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

Optionally, place a 330pF Y capacitor between GNDA and GNDB for improved cable-side to UART-side ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAXM22510/MAXM22511 are characterized for protection to the cable-side ground (GNDB) to the following limits:

- ±35kV HBM
- ±18kV using the Air-Gap Discharge method specified in IEC 61000-4-2
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 11 shows the HBM test model, while Figure 12 shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The devices help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

Figure 13 shows the IEC 61000-4-2 model and Figure 14 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

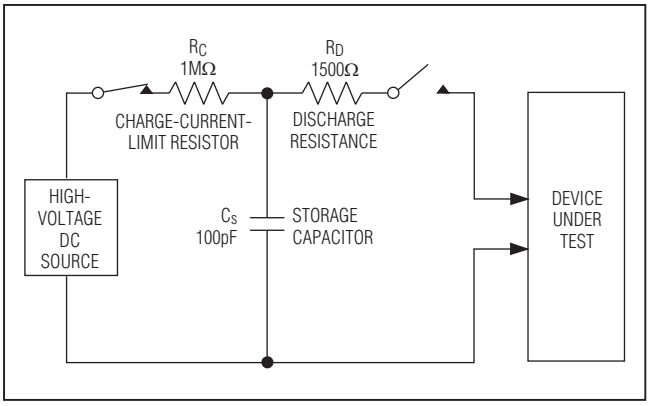


Figure 11. Human Body ESD Test Model

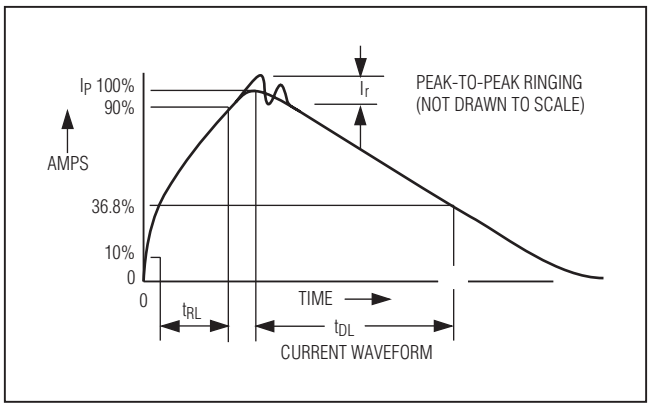


Figure 12. Human Body Current Waveform

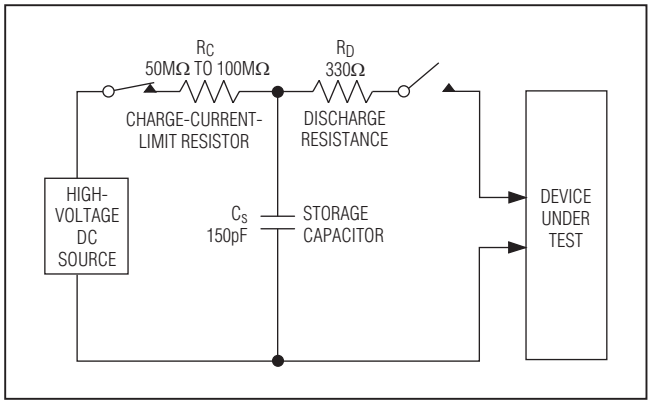


Figure 13. IEC 61000-4-2 ESD Test Model

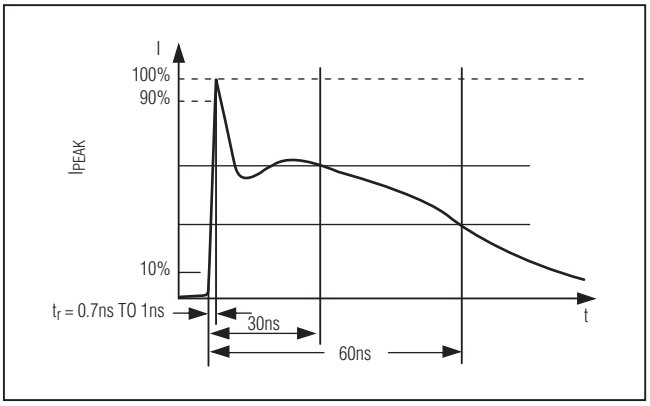
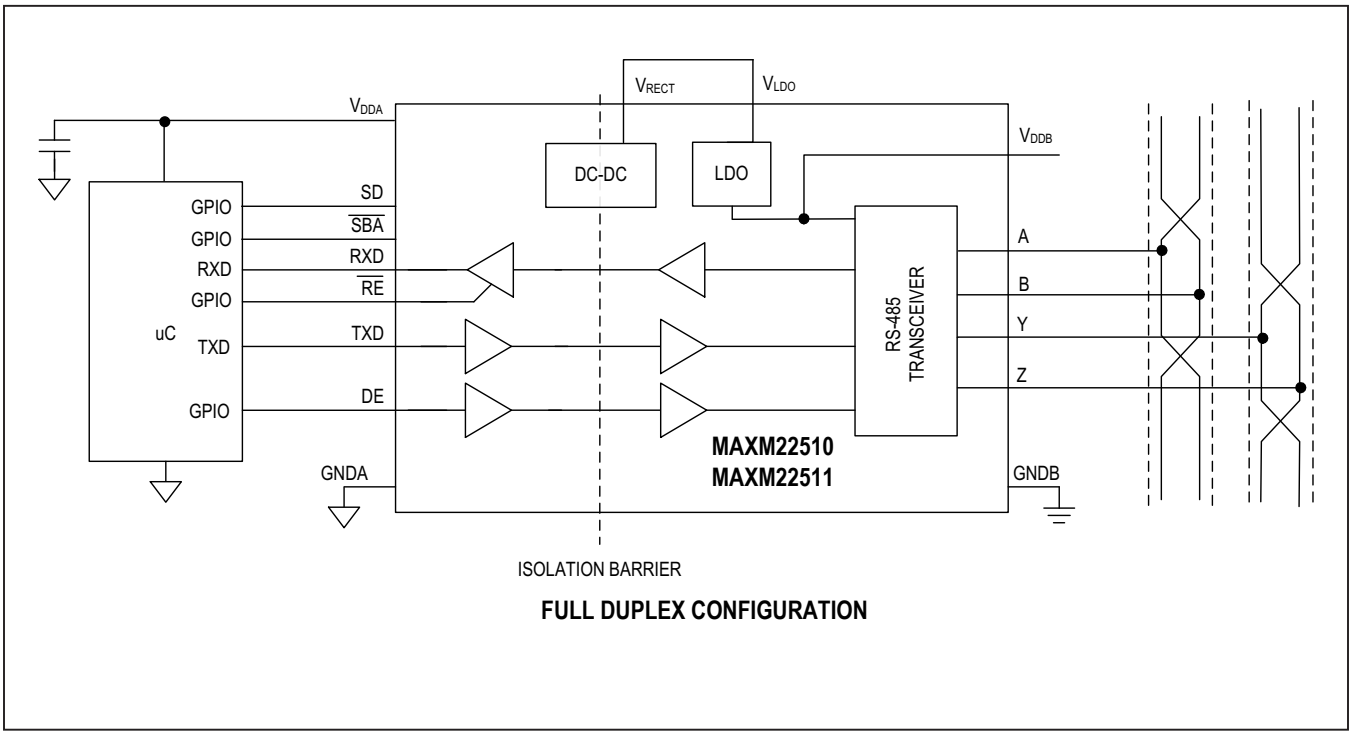
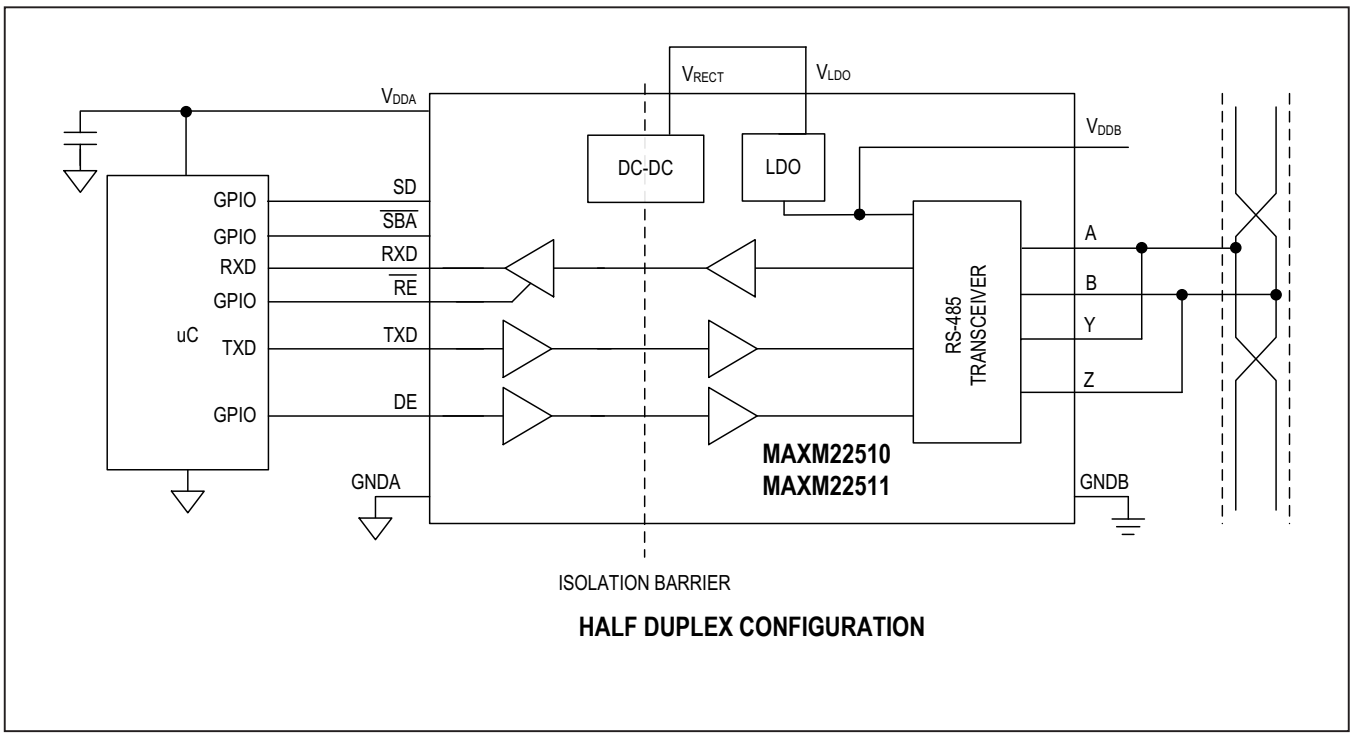


Figure 14. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits



FULL DUPLEX CONFIGURATION



HALF DUPLEX CONFIGURATION

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXM22510GLH+	-40°C to +105°C	44 LGA
MAXM22510GLH+T	-40°C to +105°C	44 LGA
MAXM22511GLH+	-40°C to +105°C	44 LGA
MAXM22511GLH+T	-40°C to +105°C	44 LGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS