General Description

The DS28E17 is a 1-Wire slave to I²C master bridge device that interfaces directly to I²C slaves at standard (100kHz max) or fast (400kHz max). Data transfers serially by means of the 1-Wire® protocol, which requires only a single data lead and a ground return. Every DS28E17 is guaranteed to have a unique 64-bit ROM registration number that serves as a node address in the 1-Wire network. Multiple DS28E17 devices can coexist with other devices in the 1-Wire network and be accessed individually without affecting other devices. The DS28E17 allows using complex I²C devices such as display controllers, ADCs, DACs, I²C sensors, etc. in a 1-Wire environment. Each self-timed DS28E17 provides 1-Wire access for a single I²C interface.

Applications

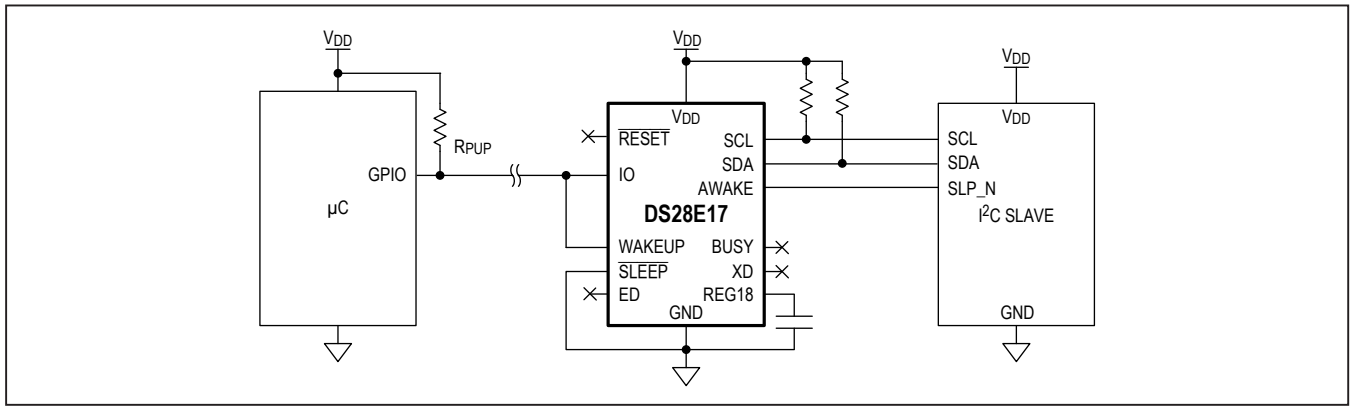
- Accessory Identification and Control
- I²C Sensors
- Display Controllers
- ADCs/DACs

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Converts 1-Wire Communication Protocol to I²C Master I/O
  - Operates I²C Slave Peripherals over the Single-Contact, 1-Wire Interface
- Extend I²C Communication Distance with 1-Wire Protocol
  - 100 Meters (typ) in Standard Speed for a Properly Configured Network
- Flexible 1-Wire Slave and I²C Master Operational Modes
  - Supports 15kbps and 77kbps 1-Wire Protocol with Packetized I²C Data Payloads
  - Factory-Programmed, Unique 64-Bit 1-Wire ROM ID Provides Unalterable Serial Number to End Equipment
  - Standard 100kHz and 400kHz Communication Rates for I²C
  - I²C Clock Stretching Automatically Supported
- Low Power Consumption
  - 0.3µA (typ) in Sleep Mode
  - 2.6mA (typ) when Operational
  - Separate Pins for Sleep and Wakeup Flexibility
  - Remote Power Controlled by an Awake Pin
  - Sleep Mode Enabled by Sleep Pin or a 1-Wire Device Command
- Easy to Integrate
  - 3.3V(nom) Supply, Small 4mm x 4mm x 0.75mm TQFN Package, -40°C to +85°C Operation
  - Evaluation HW and SW Available

Typical Operating Circuit



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Absolute Maximum Ratings

Voltage Range on V_{DD} with Respect to GND.....-0.3V to +3.6V
Voltage Range on Any Lead with
Respect to GND .....-0.3V to V_{DD} + 0.5V
Continuous Output Current for Any Single I/O Pin 32mA
Continuous Output Current for All I/O Pins Combined 32mA

Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Lead Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{PUP}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 3)	2.45		3.6	V
1.8V Internal Regulator	V_{REG18}		1.62	1.72	1.98	V
Supply Current	I_{DD}			2.6	4.5	mA
Sleep Mode Current	I_{SLP}	T_A = 25°C		0.3	3	µA
		T_A = 0 to +75°C		1	12	
		T_A = -40 to +85°C		2	16	
Sleep Mode Resume	t_{SLPON}			2		µs
IO PIN: GENERAL						
1-Wire Pullup Resistance	R_{PUP}	(Note 3, 4)	300		2200	Ω
Input Capacitance	C_{IO}	(Notes 4)			15	pF
Input Hysteresis	V_{IHYS}	(Notes 5)		300		mV
Input Leakage Current	I_L		-100		+100	nA
Input Low Voltage	V_{IL}	(Notes 3, 6, 7)			0.3 x V_{DD}	V
Input Low Voltage	V_{IH}	(Notes 3, 8)	0.7 x V_{DD}			V
Output Low Voltage	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA		0.4	0.5	V
		V_{DD} = 2.45V, I_{OL} = 8mA		0.4	0.5	V
Recovery Time (Notes 3, 9)	t_{REC}	Standard speed, R_{PUP} = 2200Ω	5			µs
		Overdrive speed, R_{PUP} = 2200Ω	8			
Time Slot Duration (Notes 3, 10)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	13			

Electrical Characteristics (continued)

(T_A = -40°C to +85°C, V_{DD} = V_{PUP}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire RESET, PRESENSE-DETECT CYCLE						
Reset Low Time (Note 3)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 3, 11)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 3, 12)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	5		16	
Write-One Low Time (Notes 3, 12)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	0.7		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 3, 13)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	0.7		2 - δ	
Read Sample Time (Notes 3, 13)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
ROM						
Data Retention	t_{DR}	T_A = 25°C	100			Years
ED, BUSY, XD, AWAKE OUTPUT PINS						
Output Low Voltage	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA		0.4	0.5	V
		V_{DD} = 2.45V, I_{OL} = 8mA		0.4	0.5	V
Output High Voltage	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5V			V
WAKEUP, $\overline{\text{SLEEP}}$, $\overline{\text{RESET}}$ INPUT PINS						
Input Low Voltage	V_{IL1}	(Notes 3, 6)			0.3 x V_{DD}	V
Input Low Voltage	V_{IH1}	(Notes 3, 8)	0.7 x V_{DD}			V
Input Capacitance	C_{IO1}	(Notes 4)			15	pF
Input Leakage Current	I_{L1}	Not including $\overline{\text{RESET}}$	-100		+100	nA
Input Pullup Resistance	R_{PU}	$\overline{\text{RESET}}$ only, V_{DD} = 3.0V, V_{OL} = 0.4V	16	28	39	kΩ
Wakeup	t_{WAK}			300		µs

Electrical Characteristics (continued)

(T_A = -40°C to +85°C, V_{DD} = V_{PUP}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C GENERAL (i.e., SCL, SDA PINS)						
Input Low Voltage	V_{IL_I2C}	Supply voltages that mismatch I²C bus levels must relate input levels to the R_P pullup voltage	-0.5		0.3 x V_{DD}	V
Input High Voltage	V_{IH_I2C}	Supply voltages that mismatch I²C bus levels must relate input levels to the R_P pullup voltage	0.7 x V_{DD}		V_{DD} + 0.5	V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DD} > 2V, 3mA sink current	0		0.4	V
Pulse Width of Spike Filtering That Must Be Supressed by Input Filter	t_{SP_I2C}	Applies to fast mode only	0		50	ns
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DD} to 0.9 x V_{DD}	-10		+10	µA
I/O Capacitance	C_{IO_I2C}				10	pF
I²C BUS CONTROLLER TIMING (FIGURE 7)						
I²C Bus Operating Frequency	f_{I2C}	Standard mode	0		100	kHz
		Fast mode			400	
Hold Time After (Repeated) START	$t_{HD:STA}$	Standard mode	4.0			µs
		Fast mode	0.6			
Clock Low Period	t_{LOW_I2C}	Standard mode	4.7			µs
		Fast mode	1.3			
Clock High Period	t_{HIGH_I2C}	Standard mode	4.0			µs
		Fast mode	0.6			
Setup Time for Repeated START	$t_{SU:STA}$	Standard mode	4.7			µs
		Fast mode	0.6			
Hold Time for Data	$t_{HD:DAT}$	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
Setup Time for Data	$t_{SU:DAT}$	Standard mode	250			ns
		Fast mode	100			
SDA/SCL Fall Time	t_{F_I2C}	Standard mode			300	ns
		Fast mode	20 + 0.1C_B		300	

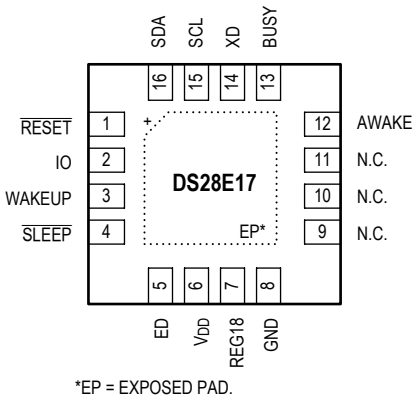
Electrical Characteristics (continued)

(T_A = -40°C to +85°C, V_{DD} = V_{PUP}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA/SCL Rise Time	t_{R_I2C}	Standard mode			1000	ns
		Fast mode	20 + 0.1C_B		300	
Setup Time for STOP	$t_{SU:STO}$	Standard mode	4.0			µs
		Fast mode	0.6			
Bus Free Time Between STOP and START	t_{BUF}	Standard mode	4.7			µs
		Fast mode	1.3			
Capacitive Load for Each Bus Line	C_B				400	pF
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}		0.1 x V_{DD}			V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}		0.2 x V_{DD}			V

Note 2: Limits are 100% production tested at T_A = +25°C and T_A = +70°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.
Note 3: System requirement.
Note 4: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. The pullup resistance power should be applied at the same time or after V_{DD} to minimize back charging.
Note 5: Guaranteed by design and/or characterization only. Not production tested.
Note 6: Voltage below which, during a falling edge on IO, a logic-zero is detected.
Note 7: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.
Note 8: Voltage above which, during a rising edge on IO, a logic-one is detected.
Note 9: Applies to a single device attached to a 1-Wire line.
Note 10: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.
Note 11: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E17 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up.
Note 12: ε in Figure 5 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{IH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F$ - ε and $t_{W0LMAX} + t_F$ - ε, respectively.
Note 13: δ in Figure 6 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

Pin Configurations



*EP = EXPOSED PAD.

Pin Description

PIN	NAME	TYPE	FUNCTION
1	$\overline{\text{RESET}}$	Input	Active-Low Reset. This bidirectional pin recognizes external active-low reset inputs and employs an internal pullup resistor to allow for a combination of wired-OR external reset sources. An RC is not required for power-up, as this function is provided internally. This pin also acts as an output when the source of the reset is internal to the device (e.g., power-up, power-fail, etc.). In this case, the pin is low while the DS28E17 is in a reset state, and returns high as the device exits this state.
2	IO	Open drain	1-Wire Bus Interface. This is an open-drain pin that requires an external pullup resistor (R_{PUP}).
3	WAKEUP	Input	Wakeup. This pin, on a single rising edge, wakes up the device from sleep mode. The pin only looks for a rising edge during sleep mode.
4	$\overline{\text{SLEEP}}$	Input	Sleep. This pin, on a single falling edge, sets the sleep mode.
5	ED	Output	Error Detected. This push-pull pin drives low when an error is detected. Errors include invalid command, bad CRC16, and when an I²C command is not acknowledged (i.e., NACK'd). The pin is reset on a 1-Wire reset command.
6	V_{DD}	Power	Digital Supply Voltage. This power pin requires power from 2.45V to 3.6V.
7	REG18	—	Regulator Capacitor. This pin is nominally 1.72V and requires a 1uF cap. Only minimal loads of less than 200uA should use this pin.
8	GND	—	Digital Ground
9, 10, 11	N.C.	—	No Connection
12	AWAKE	Output	Awake. This push-pull pin drives high when DS28E17 is awake and drives low when asleep. Can be used to awaken or put to sleep other devices (e.g. processor, sensor, etc) on the peripheral based on the state of DS28E17 (i.e. Sleep mode or awake).
13	BUSY	Output	Busy. This push-pull pin drives low after receiving the packet's CRC16 and remains low until the entire I²C transaction has completed. All 1-Wire communication is ignored when this signal is low.
14	XD	Output	Expecting Data. This push-pull pin drives low after receiving a Device command and remains low until the entire transmitted 1-Wire packet is received. This pin returns high after the CRC16. **Note: Pin does not toggle for Device commands that are not 1-Wire packets.**

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
15	SCL	Output	I²C Serial-Clock. Must be connected to the I²C bus supply voltage through a pullup resistor.
16	SDA	IO	I²C Serial-DataInput/Output. Must be connected to the I²C bus supply voltage through a pullup resistor.
—	EP	—	Exposed Pad. Solder or thermally connect the Exposed Pad to GND or an electrically unconnected pad to achieve specified thermal characteristics.

Detailed Description

The DS28E17 combines a 1-Wire front end, an I²C bus controller, and functionality to bridge these two interfaces for data communication in a single chip. Data is transferred serially through the 1-Wire protocol, which requires only a single data lead and a ground return for signaling. The DS28E17 has a transparent buffer to write and read to the I²C bus controller. I²C data is written and read back by sending 1-Wire packets. As well, a ROM ID accessible from 1-Wire command protocol guarantees unique identification and is also used to address the device in a multidrop 1-Wire network environment, where multiple devices reside on a common 1-Wire bus and operate independently of each other.

Overview

Figure 1 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the seven ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, Resume, Overdrive-Skip ROM, or Overdrive-Match ROM. Upon completion of an Overdrive-Skip ROM or Overdrive-Match ROM command byte executed at standard speed, the device enters overdrive mode where all subsequent communication occurs at a higher speed. **All data is read and written least significant bit first.**

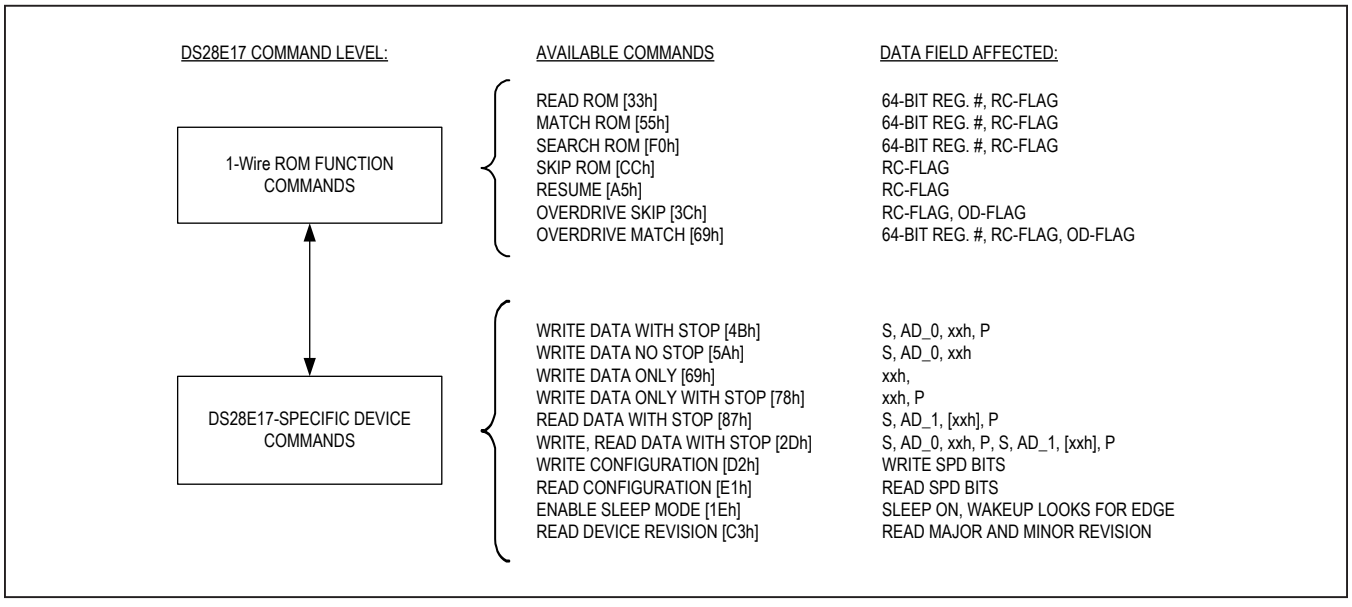


Figure 1. Hierarchical Structure for 1-Wire Protocol

64-Bit ROM ID

Each DS28E17 contains a unique ROM ID that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a cyclic redundancy check (CRC) of the first 56 bits. See Figure 2 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire CRC is available in Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products*.

The shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the last bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of the CRC returns the shift register to all 0s.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances the DS28E17 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots, which are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port (i.e., IO pin) of the DS28E17 is open drain or an input to read data.

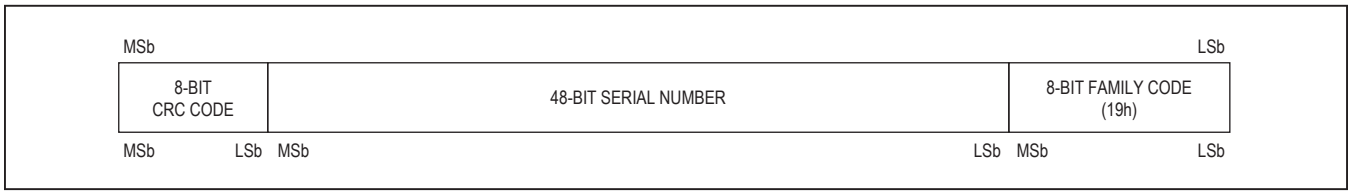


Figure 2. 64-Bit ROM ID

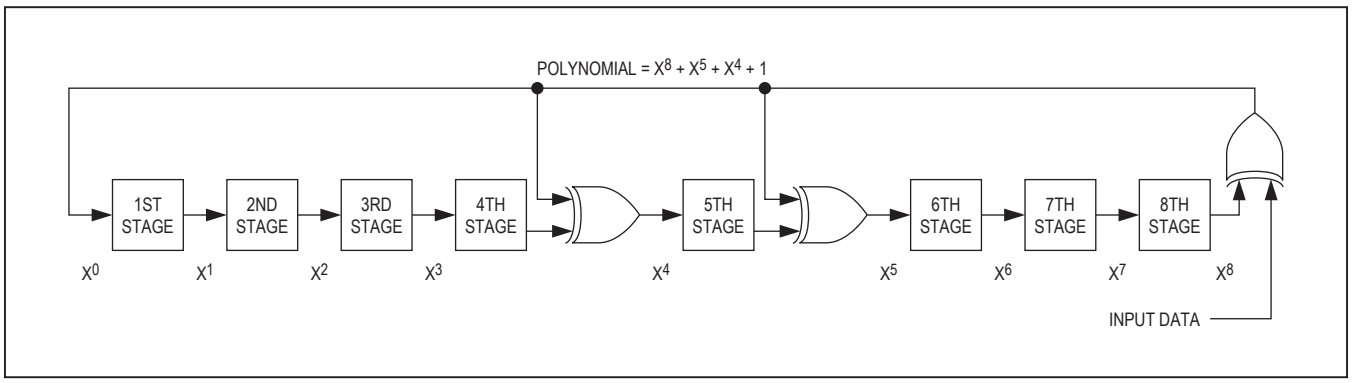


Figure 3. 1-Wire CRC Generator

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A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E17 supports both a standard and overdrive communication speed of 15kbps (max) and 77kbps (max), respectively. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E17 requires a pullup resistor of 2.2kΩ (max) at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low, one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E17 through the 1-Wire port is as follows:

- Initialization
- ROM function command
- Device command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E17 is on the bus and is ready to operate.

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E17 supports. All ROM function commands are 8 bits long. A list of these commands follows. See the flowchart in Figure 4a and Figure 4b.

Read ROM [33h]

The Read ROM command allows the bus master to read the DS28E17's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E17 on a multidrop bus. Only the DS28E17 that exactly matches the 64-bit ROM sequence responds to the subsequent Device command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit in the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to Application Note 187: *1-Wire Search Algorithm* for a detailed discussion, including an example.

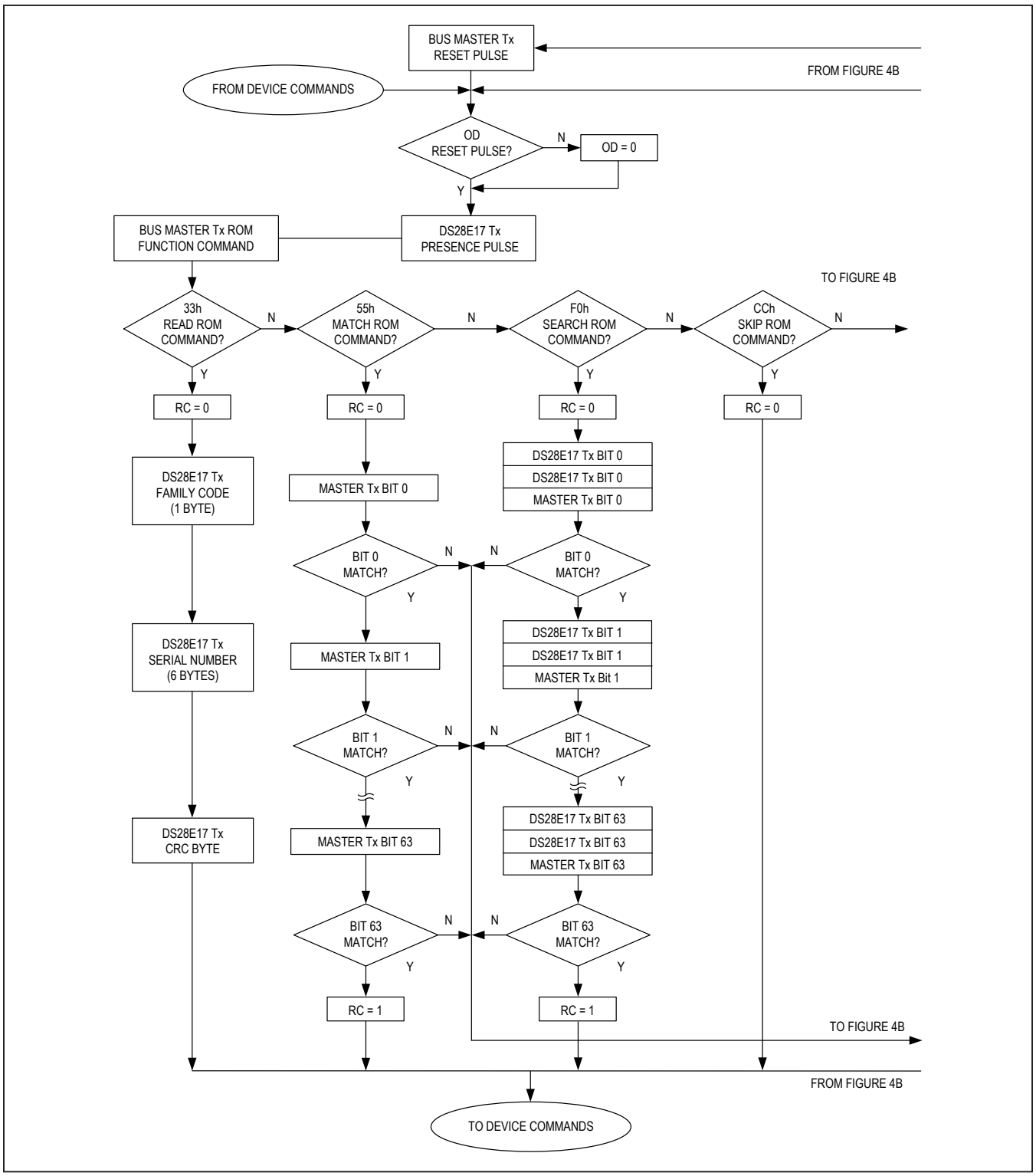

Figure 4a. ROM Functions Flow Chart

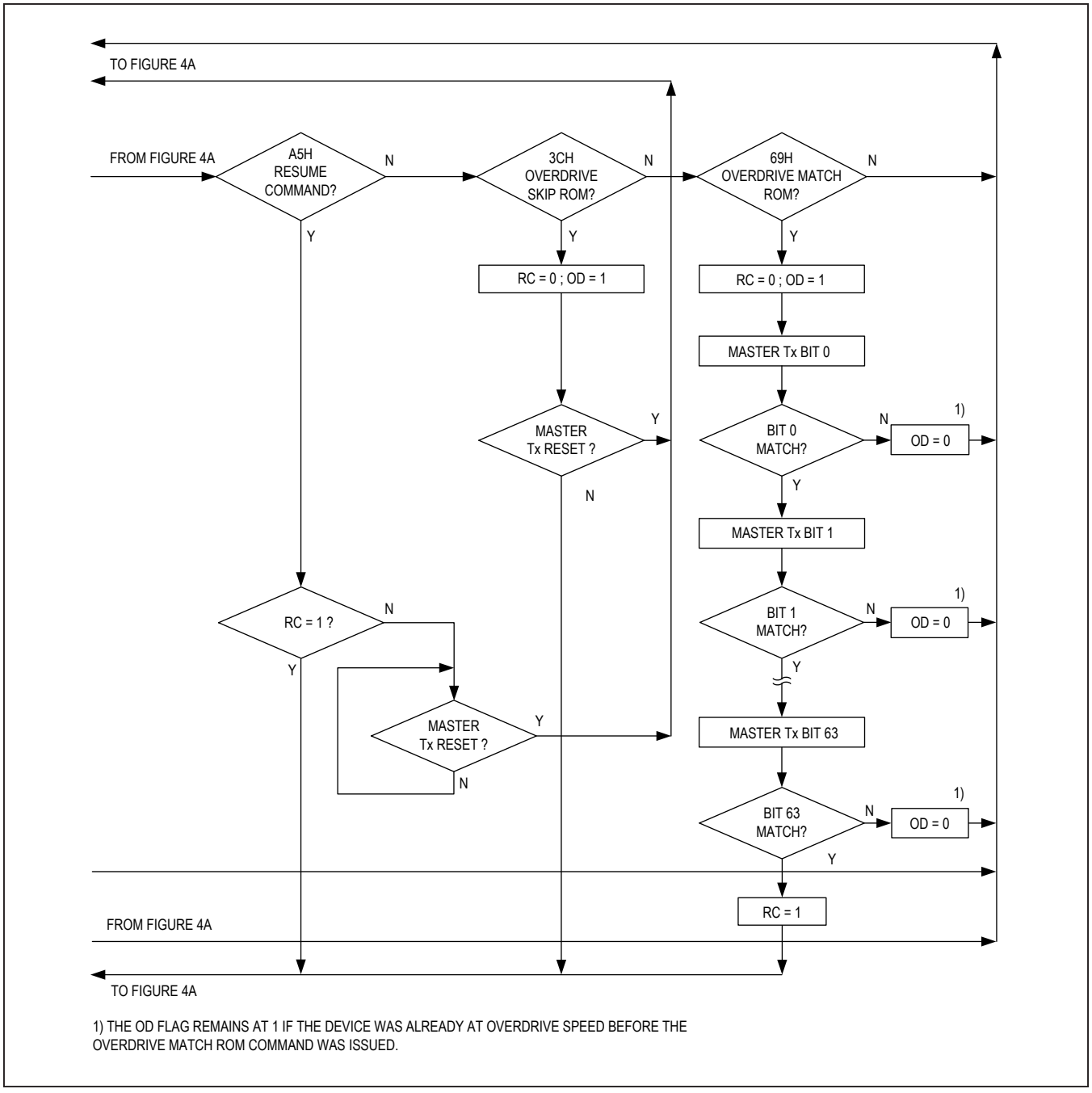

Figure 4b. ROM Functions Flow Chart (continued)

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the Device commands without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the Device commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus master to access the Device commands without providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E17 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28E17 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E17 that exactly matches the 64-bit ROM sequence responds to the subsequent Device command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

1-Wire Signaling

The DS28E17 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all falling edges. The DS28E17 can communicate at two different speeds: standard speed and overdrive speed. If not explicitly set into the overdrive mode, the DS28E17 communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from above V_{IHMIN} to below V_{ILMAX}. To get

from active to idle, the voltage needs to rise from below V_{ILMAX} to above V_{IHMIN}. The time it takes for the voltage to make this rise is seen in Figure 5 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E17 when determining a logical level, not triggering any events. For more information on the capacitance of a 1-Wire network, refer to Application 6208: *Extending I²C Communication Distance with the DS28E17.*

Figure 5 shows the initialization sequence required to begin any communication with the DS28E17. A reset pulse followed by a presence pulse indicates that the DS28E17 is ready to receive data, given the correct ROM and Device command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS28E17 is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode. If the device is in overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined.

After the bus master has released the line it goes into receive mode. Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. When the threshold V_{IH} is crossed, the DS28E17 waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of $t_{PDH-MAX}$, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS28E17 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at overdrive speed to accommodate other 1-Wire devices.

Read/Write Time Slots

Data communication with the DS28E17 takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. Figure 6 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below V_{IL}, the DS28E17 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the VIL threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{ILMAX} until the write-zero low time tW0LMIN is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{IH} threshold has been crossed, the DS28E17 needs a recovery time t_{REC} before it is ready for the next time slot.

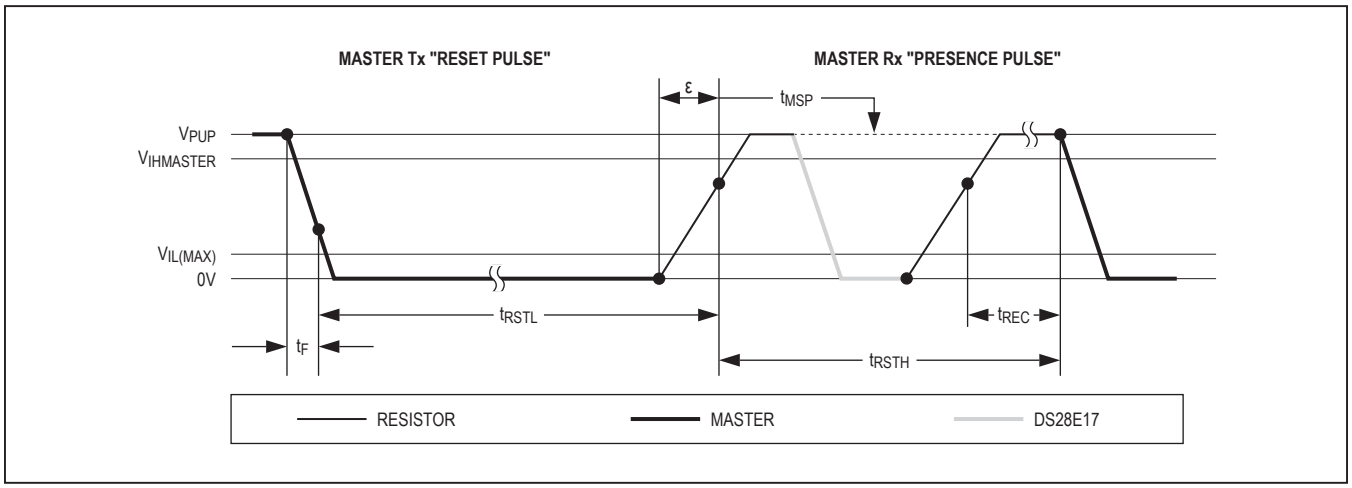

Figure 5. Initialization Procedure: Reset and Presence Pulse

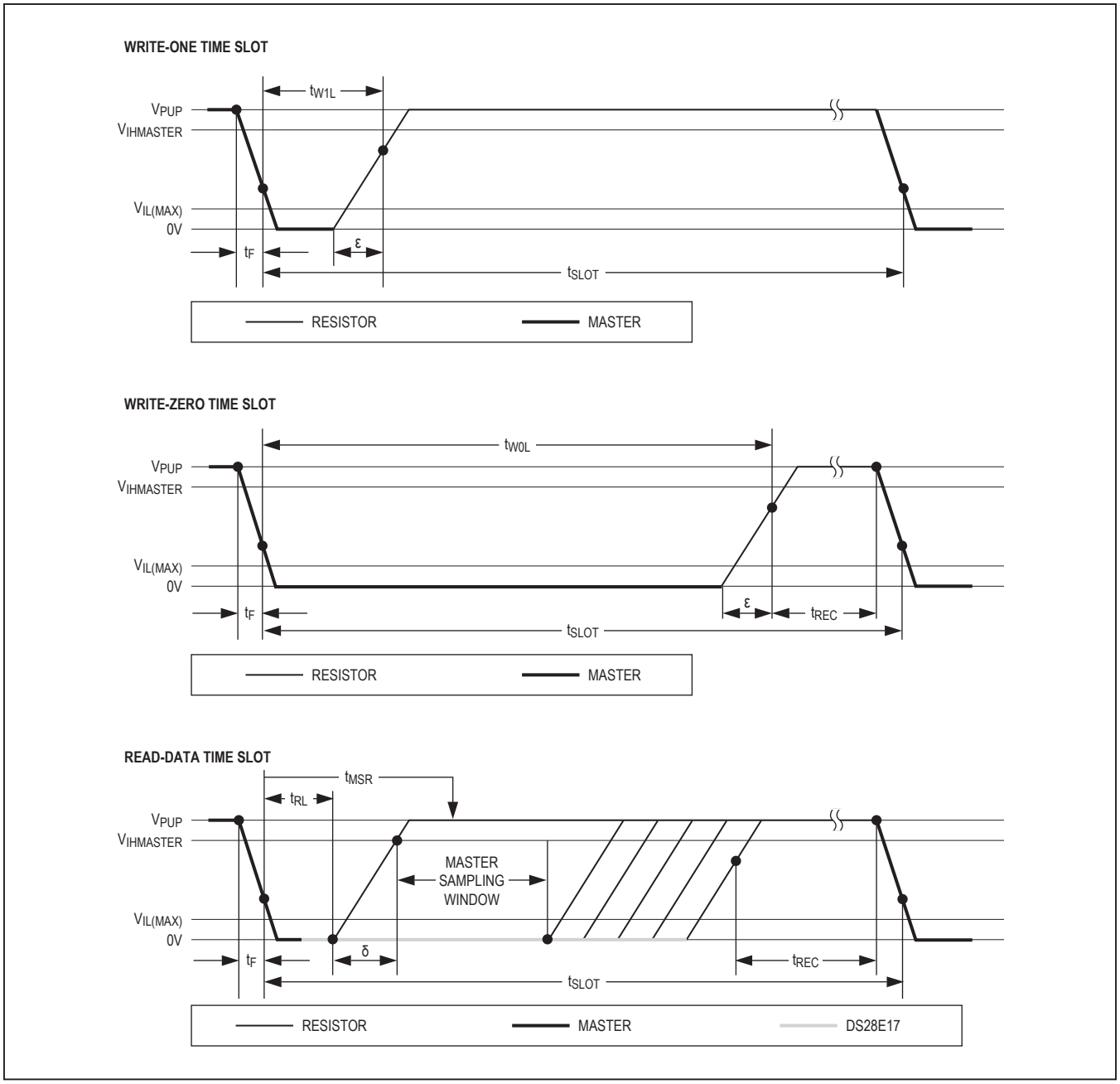

Figure 6. Read/Write Timing Diagrams

Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{ILMAX} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E17 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E17 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E17 on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the master must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E17 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E17 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

I²C Bus Signaling

The I²C bus is a 2-wire, bidirectional bus using two bus lines—the serial data line (SDA) and the serial clock line (SCL)—and a ground line. Both the SDA and SDL lines must be driven as open-collector/drain outputs. External resistors are required to pull the lines to a logic-high state.

The device supports only the master protocols. In the master mode, the device has ownership of the I²C bus, drives the clock, and generates the START and STOP signals per Figure 7. This allows it to send data to a slave or receive data from a slave as required.

Clock stretching is automatically accepted when SCL is held low by an I²C slave. In other words, the DS28E17 that is communicating with the I²C slave does not finish the transmission of the current bit, but waits until the SCL signal actually goes logic-high.

Device Commands

This section describes the 8-bit long Device commands. The Device commands are as follows:

- Write data with stop (4Bh)
- Write data no stop (5Ah)
- Write data only (69h)
- Write data only with stop (78h)
- Read data with stop (87h)
- Write, read data with stop (2Dh)
- Write configuration (D2h)
- Read configuration (E1h)
- Enable sleep mode (1Eh)
- Read device revision (C3h)

Device commands 1 through 6 exercise the I²C interface for writing, reading and write/reading I²C data from/to the 1-Wire. Send these 1-Wire Device commands and formed 1-Wire packet, after first sending a 1-Wire ROM function command that addresses the device. Follow the Device command by several write data bytes (e.g., I²C Slave

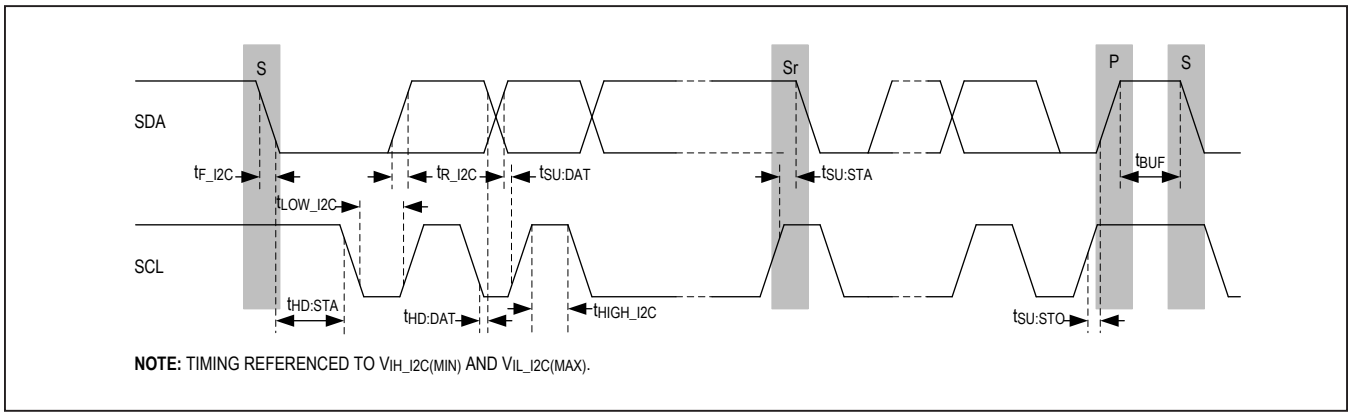

Figure 7. I²C Bus Controller Timing Diagram

Address, Write Length, Write Data, CRC16, etc.) that form the write portion of the packet. Upon completion of the Device command and write data bytes, it is important for the host to wait a predetermined delay or poll the BUSY pin or continuously perform 1-Wire bit reads until the signaling of all done by receiving a single 0b timeslot from the device. When using a delay or monitoring the BUSY pin, a single-bit read timeslot is still required before reading data bytes. The provided time allows the device to complete execution of Device command. Lastly, the host performs reading of the data bytes (e.g., Status, Write Status, Read Data, etc.). The reading of the data bytes completes the formed packet (i.e., transaction/data) and the device returns to the initialization sequence waiting for a 1-Wire reset and presence pulse per Figure 4a.

Device specific settings are readable and configurable through Device commands 7 through 10. The Write Configuration and Read Configuration commands set the I²C speed. In addition to the sleep pin, the Enable Sleep Mode command puts the device into sleep mode. While in this mode, the device monitors the wakeup input pin for a rising edge. Lastly, the Read Device Revision command provides reading of the revision of the device.

Device Commands to Exercise the I²C Interface

Follow the legend in Table 1 for 1-Wire and in Table 2 for I²C as to understand the signaling occurring.

In general, the device commands that exercise the I²C interface follow this format from the 1-Wire vantage point per Table 4.

Table 1. 1-Wire Color Legend

1-Wire COLOR CODES
Host Writes
Host Reads
Host delay or BUSY pin polling or single 0b timeslot polling

Table 2. I²C Character Legend

LEGEND	I²C EQUIVALENT
S	Start
Sr	Repeated start
AD, 0	Write address
AD, 1	Read address
$xxh_{[\#]}$	Write data
$[xxh]_{[\#]}$	Read data
P	Stop
ACK	Acknowledged
NACK	Not acknowledged
(idle)	Bus not busy

#: Number of bytes.

Table 3. I²C Data Direction Codes

I²C COLOR CODES
Master to slave
Slave to master

Table 4. General 1-Wire Sequence for the I²C Interface

INITIALIZATION		ADDRESSING	FORMED 1-Wire PACKET		
1-Wire Reset	Presence Pulse	ROM Function Command	Device Command, Data, etc.	Delay	Read Bytes

Write Data with Stop

Device Command	4Bh
Typical Usage	This is used to address and write 1–255 bytes to an I²C slave in one transaction.
I²C Features	Start, Address, Write Data, Stop
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e., during the delay). If polling is used, the host issues single-bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status or Write Status bytes.

Formed 1-Wire Packet

Command 4Bh	I²C Slave Address[1]	Write Length[2]	Write Data[3]	CRC16[4]	Delay or Busy Poll[5]	Status[6]	Write Status[7]

[1] Defines the 7-bit I²C address to be written. The least significant bit must be zero, indicating an I²C write.

[2] Defines number of data bytes to be written ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[3] Send the user defined write data ranging from 1–255 bytes.

[4] CRC16 of command, I²C slave address, write length, and write data.

[5] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status and Write Status bytes.

[6] and [7] are optional to read, but recommend as to know if success of the I²C transaction occurred or not.

Expected Output on I²C

S	AD, 0	ACK	xxh[1]	ACK	…	xxh[255]	ACK	P

Write Data No Stop

Device Command	5Ah
Typical Usage	Addresses and writes 1–255 bytes to an I²C slave without completing the transaction with a stop. This command allows writing large amounts of data at one time when used in conjunction with the Write Data Only or Write Data Only with Stop Device commands.
I²C Features	Start, Address, Write Data
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e. during the delay). If polling is used, the host issues single-bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status or Write Status bytes.

Formed 1-Wire Packet

Command 5Ah	I²C Slave Address[1]	Write Length[2]	Write Data[3]	CRC16[4]	Delay or Busy Poll[5]	Status[6]	Write Status[7]

[1] Defines the 7-bit I²C address to be written. The least significant bit automatically clears indicating an I²C write.

[2] Defines number of data bytes to be written ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[3] Send the user defined write data ranging from 1–255 bytes.

[4] CRC16 of command, I²C slave address, write length, and write data.

[5] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status and Write Status bytes.

[6] and [7] are optional to read, but recommend as to know if success of the I²C transaction occurred or not.

Expected Output on I²C

S	AD, 0	ACK	xxh[1]	ACK	…	xxh[255]	ACK

Expected Output on I²C with Repeated Start

S	AD, 0	ACK	xxh[1]	ACK	…	xxh[255]	ACK

…Continues by repeating the command…

Sr	AD, 0	ACK	xxh[1]	ACK	…	xxh[255]	ACK

Write Data Only

Device Command	69h
Typical Usage	Used when a start and I²C address have previously been issued with a Write Data No Stop Device command. This command writes 1–255 bytes to an I²C slave without completing the transaction with a stop and enables writing large amounts of data at one time when used with the Write Data Only or a last Write Data Only with Stop Device commands.
I²C Features	Write Data
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e., during the delay). If polling is used, the host issues single bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status or Write Status bytes.

Formed 1-Wire Packet

Command 69h	Write Length[1]	Write Data[2]	CRC16[3]	Delay or Busy Poll[4]	Status[5]	Write Status[6]

[1] Defines number of data bytes to be written ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[2] Send the user defined write data ranging from 1–255 bytes.

[3] CRC16 of command, write length, and write data.

[4] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status and Write Status bytes.

[5] and [6] are optional to read, but recommend as to know if success of the I²C transaction occurred or not.

Expected Output on I²C

xxh[1]	ACK	…	xxh[255]	ACK

Write Data Only with Stop

Device Command	78h
Typical Usage	Used when a start and I²C address have previously been issued with a Write Data No Stop Device command. This command writes 1–255 bytes to an I²C slave completing the transaction with a stop.
I²C Features	Write Data, Stop
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e., during the delay). If polling is used, the host issues single-bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status or Write Status bytes.

Formed 1-Wire Packet

Command 78h	Write Length[1]	Write Data[2]	CRC16[3]	Delay or Busy Poll[4]	Status[5]	Write Status[6]

[1] Defines number of data bytes to be written ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[2] Send the user defined write data ranging from 1–255 bytes.

[3] CRC16 of command, write length, and write data.

[4] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status and Write Status bytes.

[5] and [6] are optional to read, but recommend as to know if success of the I²C transaction occurred or not.

Expected Output on I²C

xxh[1]	ACK	…	xxh[255]	ACK	P

Read Data with Stop

Device Command	87h
Typical Usage	This is used to address and read 1–255 bytes from an I²C slave in one transaction.
I²C Features	Start, Address, Read Data, Stop
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e., during the delay). If polling is used, the host issues single-bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status and Read Data.

Formed 1-Wire Packet

Command 87h	I²C Slave Address[1]	# of Bytes to Read[2]	CRC16[3]	Delay or Busy Poll[4]	Status[5]	Read Data[6]

[1] Defines the 7-bit I²C address to be written. The least significant bit must be set, indicating an I²C read.

[2] Defines number of data bytes to be read ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[3] CRC16 of command, I²C slave address, and number of bytes read.

[4] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status and Write Status bytes.

[5] Read the Status to verify if success of the I²C transaction occurred or not.

[6] Receive the expected number of I²C read bytes set in the # of Bytes to Read field.

Expected Output on I²C

S	AD, 1	ACK	[xxh][1]	ACK	…	[xxh][255]	NACK	P

Write, Read Data with Stop

Device Command	2Dh
Typical Usage	This is used to first address and write 1–255 bytes to an I²C slave. Secondly, it addresses and reads 1–255 bytes from an I²C slave and issues a stop.
I2C Features	Start, Address, Write Data, repeat Start, Address, Read Data, Stop
Restriction	No 1-Wire commands or 1-Wire data is accepted during execution of the I²C communication (i.e., during the delay). If polling is used, the host issues single-bit read timeslots and receives a 0b when I²C communication completes. When using a delay or monitoring the BUSY pin a single-bit read timeslot is still required before reading the Status or Write Status bytes.

Formed 1-Wire Packet

Command 2Dh	I²C Slave Address[1]	Write Length[2]	Write Data[3]	# of Bytes to Read[4]	CRC16[5]	Delay or Busy Poll[6]	Status[7]	Write Status[8]	Read Data[9]

[1] Defines the 7-bit I²C address to be written. The least significant bit automatically clears indicating an I²C write during the I²C write sequence and automatically is set for the I²C read sequence.

[2] Defines number of data bytes to be written ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[3] Send the user defined write data ranging from 1–255 bytes.

[4] Defines number of data bytes to be read ranging from 01h to FFh. A value of zero asserts the error detected pin (ED), and the device returns waiting for a valid 1-Wire reset.

[5] CRC16 of command, I²C slave address, write length, write data and # of bytes to read. For the CRC16 calculation, the least significant bit of the I²C slave address is expected to be zero.

[6] Host waits a predetermined delay or polls the busy pin or continuously performs 1-Wire bit reads until receiving a 0b timeslot. The 0b timeslot must read out regardless of the method used before reading the Status, Write Status, and Read Data bytes.

[7] and [8] read to know if success of the I²C transaction occurred or not.

[9] Receive the expected number of I²C read bytes set in the # of Bytes to Read field.

Expected Output on I²C

S	AD, 0	ACK	xxh[1]	ACK	...	xxh[255]	ACK	Sr

... Continues with the I²C read …

AD, 1	ACK	[xxh][1]	ACK	...	[xxh][255]	NACK	P

Status Register Description for I2C Interface

Status Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	Start	0	Address	CRC16

Any of the Device commands that interact with the I2C bus return a Status byte that describes success or not of the I2C transaction. As well, the ED pin asserts when any of the bits in the Status byte are set. The ED pin clears when a valid 1-Wire reset is received.

Here are the meanings of the bits:

CRC16 (Bit 0)

Indicates the received 1-Wire packet data does not match the corresponding CRC16. When set, the device responds with an invalid Write Status byte of FFh since no I2C communication was initiated.

0 = Valid CRC16

1 = Invalid CRC16.

Address (Bit 1)

If this bit is set, only the I2C address was sent, but no write data was transmitted do to the byte not being acknowledged by the I2C slave device. The device responds with an invalid Write Status byte of FFh.

0 = I2C slave device acknowledged the I2C address

1 = I2C slave device does not acknowledge the I2C address

Start (Bit 3)

0 = Start

1 = Invalid start

Write Status Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0

Write Byte (Byte 7:0)

Indicates which write byte did not acknowledge. A value of 00h indicates all bytes were acknowledged by the slave. A non-zero value indicates the byte number that did not acknowledge.

Device Commands for Specific Settings

These 1-Wire commands configure the I2C speed of the device. The 1-Wire sequence follows the color codes in Table 1.

Write Configuration Command

Device Command	D2h
Typical Usage	This is used to write the settings of the I²C speed bits per the formatting of the Configuration register. After selecting the device by a ROM function command, send this Device command followed by the desired byte setting for the Configuration register.
Features	Writing to the SPD bits.
Restriction	Write only command.

Configuration Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	SPD	SPD

SPD (Bits 1:0)

00b = I²C speed set to 100kHz

01b = I²C speed set to 400kHz (power-on default)

10b = I²C speed set to 900kHz

11b = Not used

1-Wire Sequence

1-Wire Reset	Presence Pulse	ROM Function Command	Command D2h	Write Byte

Read Configuration

Device Command	E1h
Typical Usage	This is used to read the settings of the I²C speed bits from the Configuration register. After addressing the device by a ROM function command, this Device command, followed by a read data byte returns the setting of the Configuration register.
Features	Reading the SPD bits
Restriction	Read only command

1-Wire Sequence

1-Wire Reset	Presence Pulse	ROM Function Command	Command E1h	Read Byte

Enable Sleep Mode

Device Command	1Eh
Typical Usage	In addition to the SLEEP_N pin, the Enable Sleep Mode command puts the device into a low current mode. All 1-Wire communication is ignored until woken up. Immediately after the command, the device monitors the WAKEUP input pin and exits sleep mode on a rising edge.
Features	Reduces current (i.e., < 16µA)
Restriction	This is a write only command. Therefore, the only way to return to normal operation is by a rising edge on the WAKEUP pin.

1-Wire Sequence

1-Wire Reset	Presence Pulse	ROM Function Command	Command 1Eh

Read Device Revision

Device Command	C3h
Typical Usage	The command reads the device revision. Send this 1-Wire Device command and read data byte, after first sending a 1-Wire ROM function command that addresses the device. The read data byte contains the major revision in the upper nibble of the bytes and the minor revision in the lower nibble of the byte.
Features	Reads the device revision
Restriction	Only reads the revision of code in the die but does not provide any information about the package revision.

1-Wire Sequence

1-Wire Reset	Presence Pulse	ROM Function Command	Command C3h	Read Byte

CRC-16 Generation

The DS28E17 uses two types of CRCs.

One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM ID. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM ID and compare it to the value stored within the DS28E17 to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (noninverted) form as shown previously in Figure 3.

The other CRC is a 16-bit type, generated according to the standardized CRC-16 polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC in DS28E17 is used for fast verification of a data transfer when receiving a formed 1-Wire packet. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC generator inside the DS28E17 device (Figure 8) calculates a new 16- bit CRC, and compares it to the received CRC from the host. The DS28E17 compares the CRC value read from the host to the one it calculates from the 1-Wire formed packet and decides whether to continue with an I²C operation or to set the CRC16-bit error flag. When the CRC16 flag is set, the ED pin goes high since an error was detected. For more information on generating CRC values, refer to Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products*.

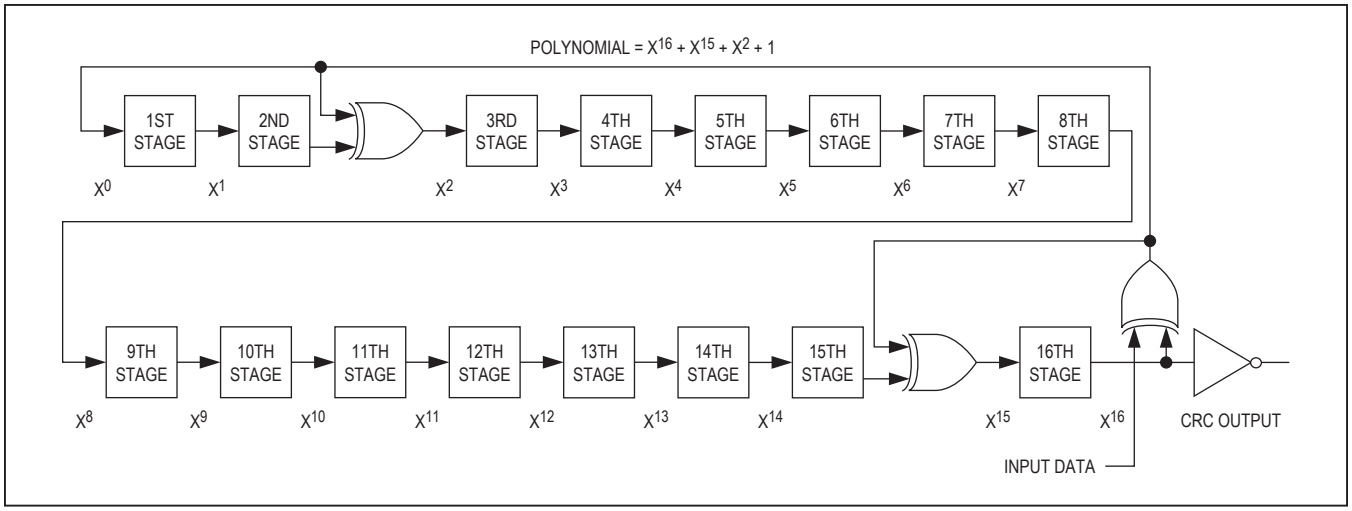

Figure 8. CRC-16 Hardware Description and Polynomial

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E17Q+T	-40°C to 85°C	16 TQFN-EP* (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1644+4	21-0139	90-0070