

3.3 V/5 V ECL Coaxial Cable Driver

MC10EP89

Description

The MC10EP89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in digital video broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver produces swings 70% larger than a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 V (5 V) and 1.4 V (3.3 V) swing allow for termination at both ends of the cable, while maintaining a 800 mV (5 V) and 700 mV (3.3 V) swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard $V_{CC}-2.0$ V. All of the DC parameters are tested with a $50\ \Omega$ to $V_{CC}-3.0$ V load. The driver accepts a standard differential ECL input and can run off of the digital video broadcast standard -5.0 V supply.

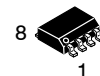
Features

- 310 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- 1.6 V (5 V) and 1.4 V (3.3 V) V_{OUTpp} Swing
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



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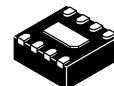
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SOIC-8
D SUFFIX
CASE 751

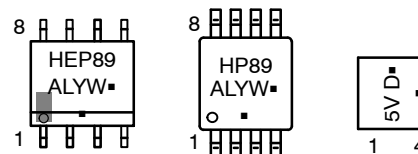


TSSOP-8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- D = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|----------------------|-----------------------|
| MC10EP89DG | SOIC-8 (Pb-Free) | 98 Units / Tube |
| MC10EP89DTG | TSSOP-8 (Pb-Free) | 100 Units / Tube |
| MC10EP89DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |
| MC10EP89MNR4G | DFN8 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC10EP89

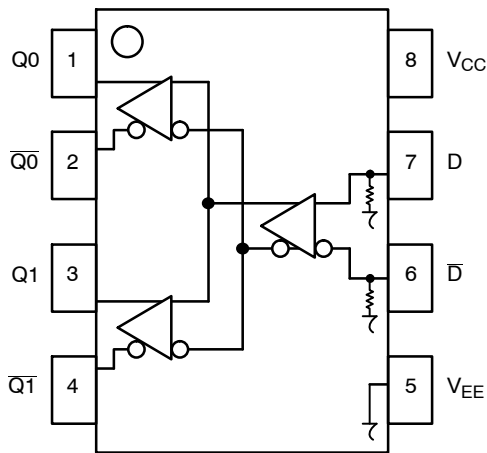


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|---------------------------------|------------------|
| D*, \bar{D}^* | ECL Data Inputs |
| Q0, Q1, $\bar{Q}0$, $\bar{Q}1$ | ECL Data Outputs |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |

* Pins will default LOW when left open.

Table 2. ATTRIBUTES

| Characteristics | Value |
|---|-------------------------------|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | N/A |
| ESD Protection Human Body Model Machine Model Charged Device Model | > 4 kV > 200 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| SOIC-8 TSSOP-8 DFN8 | Level 1 Level 3 Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL-94 V-0 @ 0.125 in |
| Transistor Count | 152 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note [AND8003/D](#).

MC10EP89

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|-----------------------|-------------------|-------------|------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 6 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -6 | V |
| V_I | PECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6 | V |
| | NECL Mode Input Voltage | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6 | V |
| I_{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | 8 SOIC | 190 | °C/W |
| | | 500 lfpm | 8 SOIC | 130 | °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 8 SOIC | 41 to 44 | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | 8 TSSOP | 185 | °C/W |
| | | 500 lfpm | 8 TSSOP | 140 | °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 8 TSSOP | 41 to 44 | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | DFN8 | 129 | °C/W |
| | | 500 lfpm | DFN8 | 84 | °C/W |
| T_{sol} | Wave Solder (Pb-Free) | <2 to 3 sec @ 260°C | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MC10EP89

Table 4. DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 24 | 30 | 36 | 26 | 34 | 40 | 30 | 36 | 42 | mA |
| V_{OH} | Output HIGH Voltage (Note 3) | 2130 | 2255 | 2405 | 2180 | 2336 | 2455 | 2200 | 2400 | 2475 | mV |
| V_{OL} | Output LOW Voltage (Note 3) | 500 | 784 | 1100 | 480 | 786 | 1100 | 440 | 882 | 1060 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2070 | | 2410 | 2170 | | 2490 | 2240 | | 2580 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1350 | | 1800 | 1350 | | 1820 | 1350 | | 1855 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.
- All loading with $50\ \Omega$ to $V_{CC} - 3.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 27 | 34 | 41 | 30 | 37 | 44 | 33 | 40 | 47 | mA |
| V_{OH} | Output HIGH Voltage (Note 6) | 3830 | 3955 | 4105 | 3880 | 4037 | 4155 | 3900 | 4102 | 4175 | mV |
| V_{OL} | Output LOW Voltage (Note 6) | 1900 | 2205 | 2500 | 1850 | 2265 | 2450 | 1850 | 2177 | 2450 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3770 | | 4110 | 3870 | | 4190 | 3940 | | 4280 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3050 | | 3500 | 3050 | | 3520 | 3050 | | 3555 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.5 V to -0.5 V.
- All loading with $50\ \Omega$ to $V_{CC} - 3.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10EP89

Table 6. DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.3\text{ V}$ (Note 8)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 24 | 30 | 36 | 26 | 34 | 40 | 30 | 36 | 42 | mA |
| V_{OH} | Output HIGH Voltage (Note 9) | -1170 | -1145 | -895 | -1120 | -964 | -845 | -1100 | -900 | -825 | mV |
| V_{OL} | Output LOW Voltage (Note 9) | -2800 | -2516 | -2200 | -2820 | -2514 | -2220 | -2860 | -2478 | -2240 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1230 | | -890 | -1130 | | -810 | -1060 | | -720 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1950 | | -1500 | -1950 | | -1480 | -1950 | | -1445 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | -1.3 | | 0.0 | -1.3 | | 0.0 | -1.3 | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

8. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -0.3 V.

9. All loading with $50\ \Omega$ to $V_{CC} - 3.0\text{ V}$.

10. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -5.2$ (Note 11)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 27 | 34 | 41 | 30 | 37 | 44 | 33 | 40 | 47 | mA |
| V_{OH} | Output HIGH Voltage (Note 12) | -1170 | -1045 | -895 | -1120 | -964 | -845 | -1100 | -900 | -825 | mV |
| V_{OL} | Output LOW Voltage (Note 12) | -3100 | -2795 | -2500 | -3150 | -2835 | -2550 | -3150 | -2824 | -2550 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1230 | | -890 | -1130 | | -810 | -1060 | | -720 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1950 | | -1500 | -1950 | | -1480 | -1950 | | -1445 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | -3.2 | | 0.0 | -3.2 | | 0.0 | -3.2 | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.7 V to -0.3 V.

12. All loading with $50\ \Omega$ to $V_{CC} - 3.0\text{ V}$.

13. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC10EP89

Table 8. AC CHARACTERISTICS $V_{CC} = 0V$; $V_{EE} = -3.0V$ to $-5.5V$ or $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|--|-------|-----|-----------|------|-----|-----------|------|-----|-----------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle (See Figure 2 $F_{max}/JITTER$) | | > 2 | | | > 2 | | | > 2 | | GHz |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential | 220 | 280 | 340 | 250 | 310 | 370 | 270 | 330 | 390 | ps |
| t_{SKEW} | Within Device Skew Q, \bar{Q} Device to Device Skew (Note 15) | | 5.0 | 20 120 | | 5.0 | 20 120 | | 5.0 | 20 120 | ps |
| t_{JITTER} | Cycle-to-Cycle Jitter (See Figure 2 $F_{max}/JITTER$) | | 0.5 | < 1 | | 0.5 | < 1 | | 0.5 | < 1 | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Times Q, \bar{Q} (20% – 80%) | 175 | 250 | 325 | 200 | 275 | 350 | 225 | 295 | 375 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-3.0V$.
 15. Skew is measured between outputs under identical transitions.

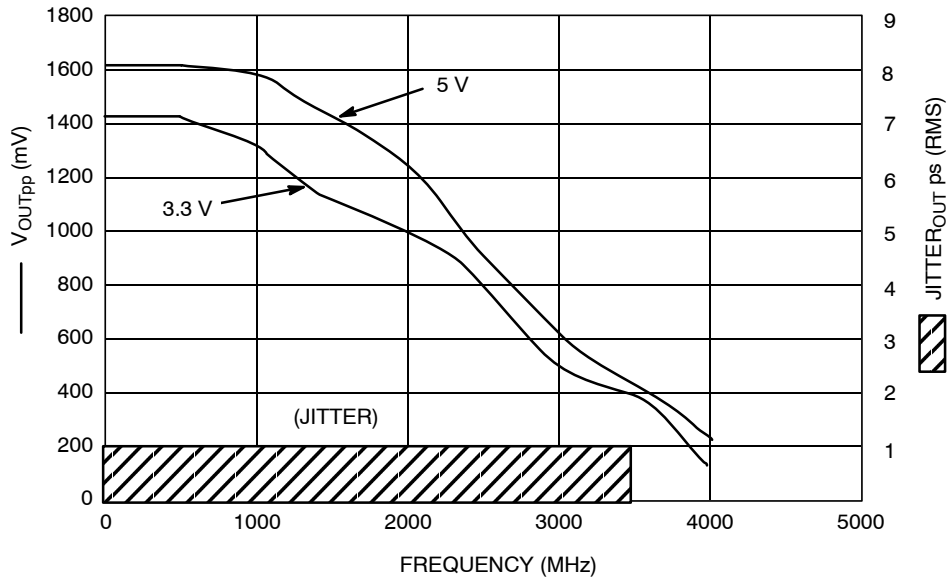


Figure 2. $F_{max}/Jitter$

MC10EP89

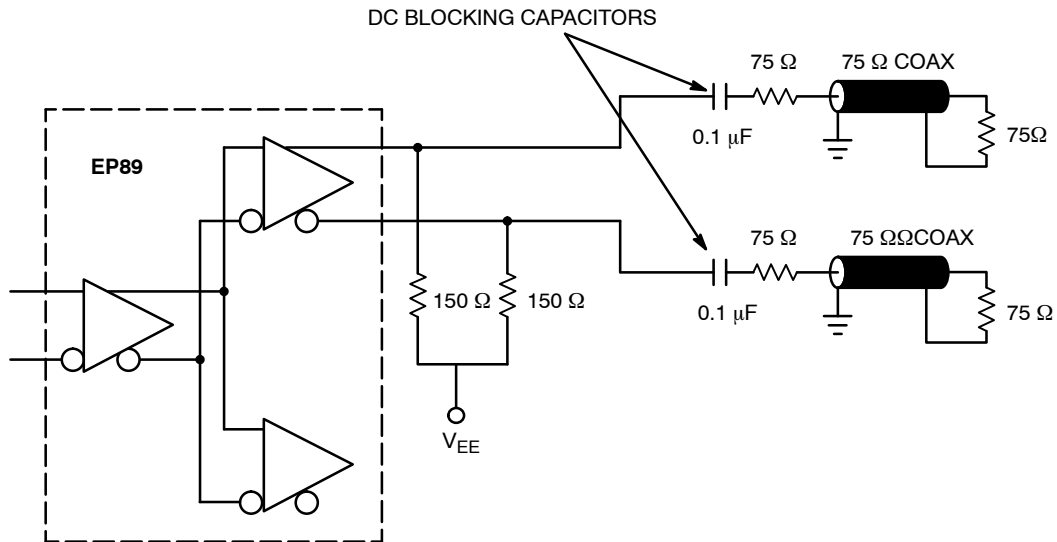


Figure 3. Cable Driver Termination Configuration

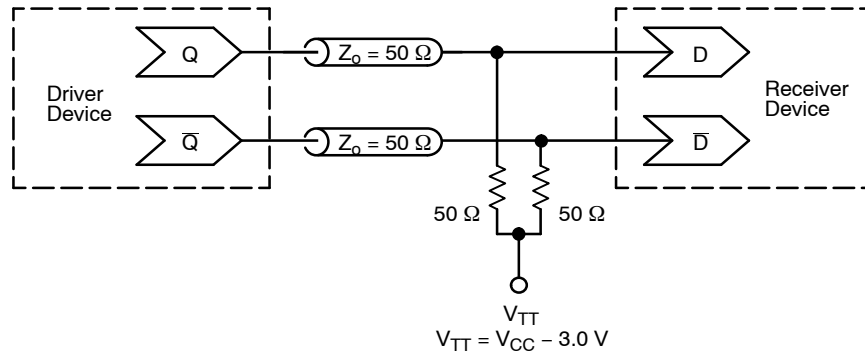


Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1642/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

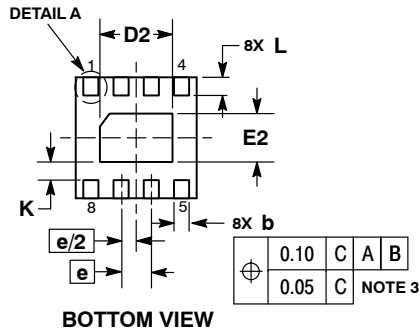
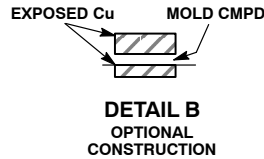
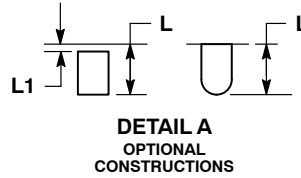
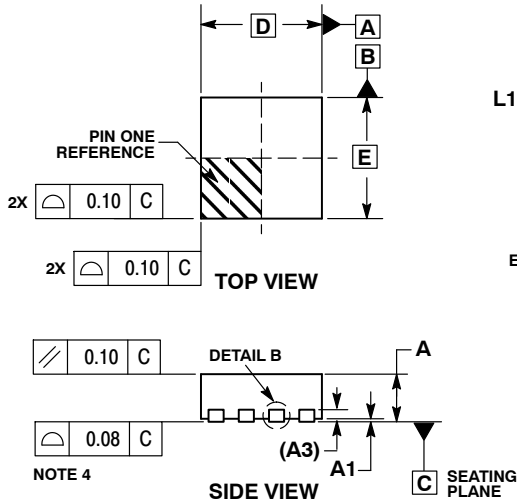
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CASE 506AA-01
ISSUE E

DATE 22 JAN 2010

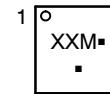


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.00 | BSC |
| D2 | 1.10 | 1.30 |
| E | 2.00 | BSC |
| E2 | 0.70 | 0.90 |
| e | 0.50 | BSC |
| K | 0.30 | REF |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |

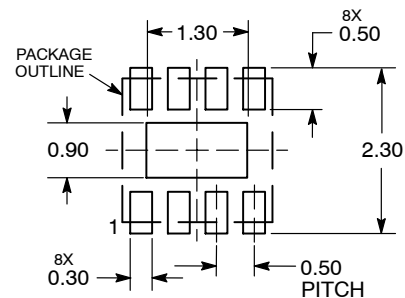
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

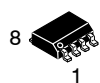
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | DFN8, 2.0X2.0, 0.5MM PITCH | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

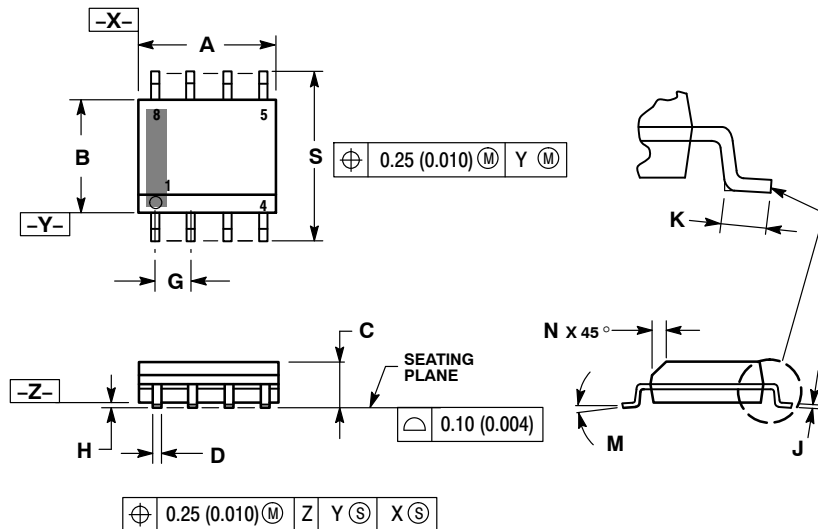
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ISSUE AK

DATE 16 FEB 2011

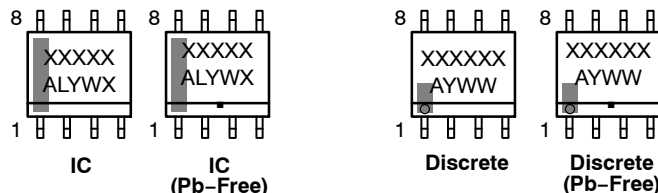
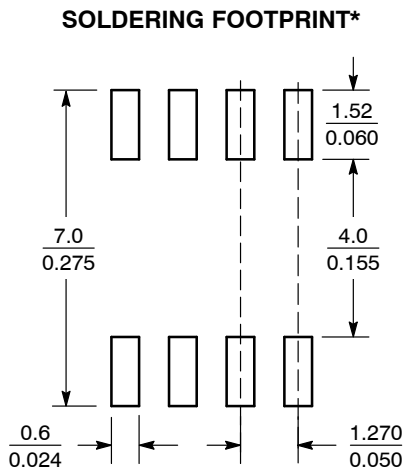


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

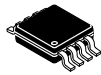
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

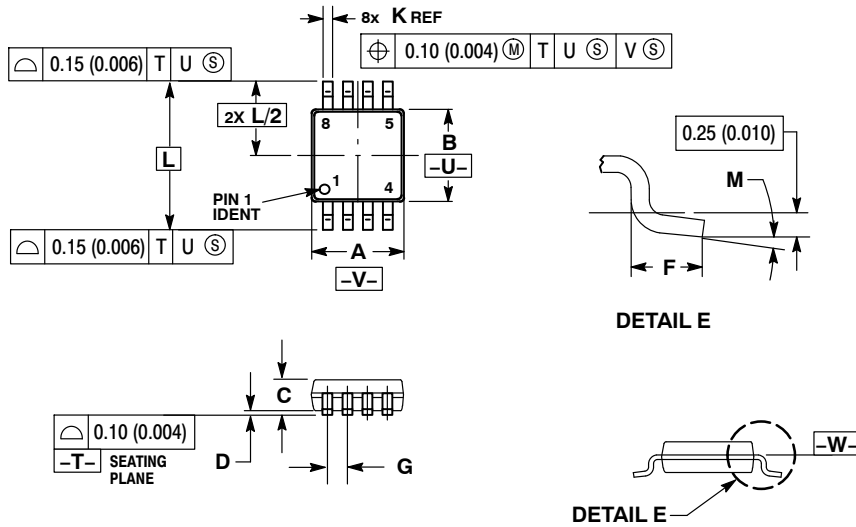
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SCALE 2:1

TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

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