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Hex Schmitt Trigger

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to "square up" slowly changing waveforms.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysteresis, Use MC14106B which is Pin–for–Pin Replacement for CD40106B and MM74Cl4
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	٧
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

"D/DT" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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MARKING DIAGRAMS

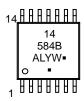


SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G





SOEIAJ-14 F SUFFIX CASE 965



A = Assembly Location

WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or = Pb-Free Package

(Note: Microdot may be in either location)

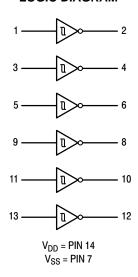
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

PIN ASSIGNMENT

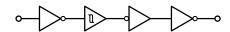
14 🛮 V_{DD} 13 IN 6 OUT 1 IN 2 🛚 3 12 OUT 6 OUT 2 4 11 IN 5 IN 3 🛮 5 10 OUT 5 OUT 3 [6 9 IN 4 8 OUT 4 V_{SS} [7

LOGIC DIAGRAM



EQIVALENT CIRCUIT SCHEMATIC

(1/6 OF CIRCUIT SHOWN)



ORDERING INFORMATION

Device	Package	Shipping [†]	
MC14584BDG		55 Units / Rail	
NLV14584BDG*	SOIC-14	55 Units / Rail	
MC14584BDR2G	(Pb-Free)	2500 / Tape & Reel	
NLV14584BDR2G*		2500 / Tape & Reel	
MC14584BDTR2G	TSSOP-14	2500 / Tape & Reel	
NLV14584BDTR2G*	(Pb-Free)	2500 / Tape & Reel	
MC14584BFG	SOEIAJ-14	50 Units / Rail	
MC14584BFELG	(Pb-Free)	2000 / Tape & Reel	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			V _{DD}	- 5	5°C		25°C		125	5°C	
Characterist	ic	Symbol	Vdc	Min	Max	Min	Typ ⁽²⁾	Max	Min	Max	Unit
Output Voltage V _{in} = V _{DD}	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = 0	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	Іон	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - -	- 1.7 - 0.36 - 0.9 - 2.4	- - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	l _{OL}	5.0 10 15	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	- - -	mAdc
Input Current		I _{in}	15	_	±0.1	_	±0.00001	±0.1	_	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	-	-	-	_	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	- - -	0.25 0.5 1.0	- - -	0.0005 0.0010 0.0015	0.25 0.5 1.0	- - -	7.5 15 30	μAdc
Total Supply Current (3) (4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)		lτ	5.0 10 15			$I_T = (3$	I.8 μΑ/kHz) f 3.6 μΑ/kHz) f 5.4 μΑ/kHz) f	+ I _{DD}			μAdc
Hysteresis Voltage		V _H ⁽⁵⁾	5.0 10 15	0.27 0.36 0.77	1.0 1.3 1.7	0.25 0.3 0.6	0.6 0.7 1.1	1.0 1.2 1.5	0.21 0.25 0.50	1.0 1.2 1.4	Vdc
Threshold Voltage Positive–Going		V _{T+}	5.0 10 15	1.9 3.4 5.2	3.5 7.0 10.6	1.8 3.3 5.2	2.7 5.3 8.0	3.4 6.9 10.5	1.7 3.2 5.2	3.4 6.9 10.5	Vdc
Negative-Going		V _{T-}	5.0 10 15	1.6 3.0 4.5	3.3 6.7 9.7	1.6 3.0 4.6	2.1 4.6 6.9	3.2 6.7 9.8	1.5 3.0 4.7	3.2 6.7 9.9	Vdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

5. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+max} - V_{T-min}$).

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ ⁽⁶⁾	Max	Unit
Output Rise Time	t _{TLH}	5.0	_	100	200	ns
		10	_	50	100	
		15	_	40	80	
Output Fall Time	t _{THL}	5.0	_	100	200	ns
		10	_	50	100	
		15	_	40	80	
Propagation Delay Time	t _{PLH} , t _{PHL}	5.0	_	125	250	ns
		10	_	50	100	
		15	_	40	80	

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

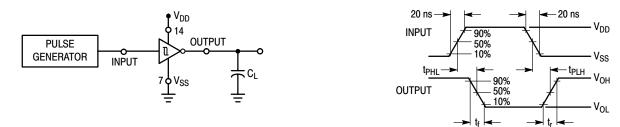
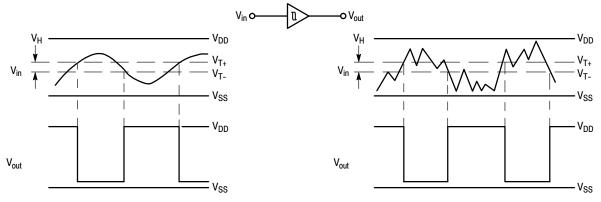


Figure 1. Switching Time Test Circuit and Waveforms



(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

Figure 2. Typical Schmitt Trigger Applications

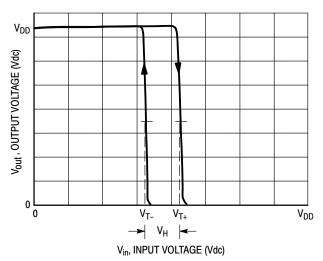
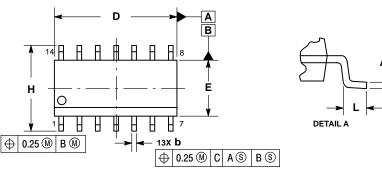
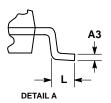


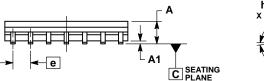
Figure 3. Typical Transfer Characteristics

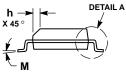
PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K









NOTES:

- IOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

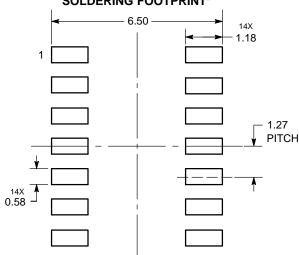
 3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAYMAIM MATERIAL CONDITION.
- MAXIMUM MATERIAL CONDITION.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.35	1.75	0.054	0.068	
A1	0.10	0.25	0.004	0.010	
A3	0.19	0.25	0.008	0.010	
b	0.35	0.49	0.014	0.019	
D	8.55	8.75	0.337	0.344	
Ε	3.80	4.00	0.150	0.157	
е	1.27	1.27 BSC		BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.019	
L	0.40	1.25	0.016	0.049	
М	0 °	7°	0 °	7°	

SOLDERING FOOTPRINT*

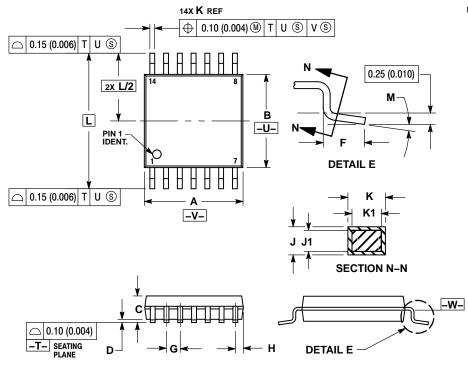


DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G ISSUE B



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH OR GATE BURRS SHALL NOT
 EXCEED 0.15 (0.006) PER SIDE.

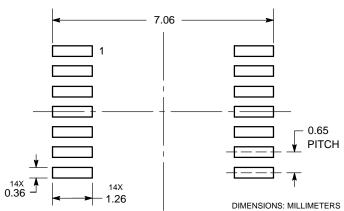
 4. DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
 NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08
 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.
- CO. TERMINAL NUMBERS ARE SHOWN
 REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE
 DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
C		1.20	-	0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
Κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
М	0 °	8 °	0°	8 °	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.