

# PF1510

## Power management integrated circuit (PMIC) for low power application processors

Rev. 4 — 5 March 2021

Product data sheet

## 1 General description

The PF1510 is a power management integrated circuit (PMIC) designed specifically for use with i.MX processors on low-power portable, smart wearable and Internet-of-Things (IoT) applications. It is also capable of providing full power solution to i.MX 7ULP, i.MX 6SL, 6UL, 6ULL and 6SX processors.

With three high efficiency buck converters, three linear regulators, DDR reference and RTC supply, the PF1510 can provide power for a complete system, including application processors, memory, and system peripherals.

### 1.1 Features and benefits

This section summarizes the PF1510 features:

- Input voltage VIN from 5V bus, USB, or AC adapter (4.1 V to 6.0 V)
  - Linear front-end input LDO (1500 mA input limit)
  - Up to 6.5 V input operating range
  - VIN can withstand transient and DC inputs from 0 V up to +22 V
- Buck converters:
  - SW1, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW2, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW3, 1.0 A; 1.8 V to 3.3 V in 100 mV steps
  - Internal digital soft start
  - Quiescent current 1.0  $\mu$ A in ULP mode with light load
  - Peak efficiency > 90 %
  - Dynamic voltage scaling on SW1 and SW2
  - Modes: forced PWM quasi-fixed frequency mode, adaptive variable-frequency mode
  - Programmable output voltage, current limit and soft start
- LDO regulators
  - LDO1, 0.75 to 1.5 V/1.8 to 3.3 V, 300 mA with load switch mode
  - LDO2, 1.8 to 3.3 V, 400 mA
  - LDO3, 0.75 to 1.5 V/1.8 to 3.3 V, 300 mA with load switch mode
  - Quiescent current < 1.5  $\mu$ A in Low-power mode
  - Programmable output voltage
  - Soft start and ramp
  - Current limit protection
  - USB\_PHY low dropout linear regulator
  - LDO2P7 always on regulator output
- LDO/switch supply
  - RTC supply VSNVS 3.0 V, 2.0 mA
  - Coin cell charger



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- DDR memory reference voltage, VREFDDR, 0.5 to 0.9 V, 10 mA
- OTP (One time programmable) memory for device configuration
  - User programmable start-up sequence, timing, soft-start and power-down sequence
  - Programmable regulator output voltages
- I<sup>2</sup>C interface
- User programmable Standby, Sleep/Low-power, and Off (REGS\_DISABLE) modes
- Ambient temperature range -40 °C to 105 °C

## 1.2 Applications

- Low-power IoT applications
- Wireless game controllers
- Embedded monitoring systems
- Home automation
- POS
- E-Reader
- Smart mobile/wearable devices

## 2 Application diagram

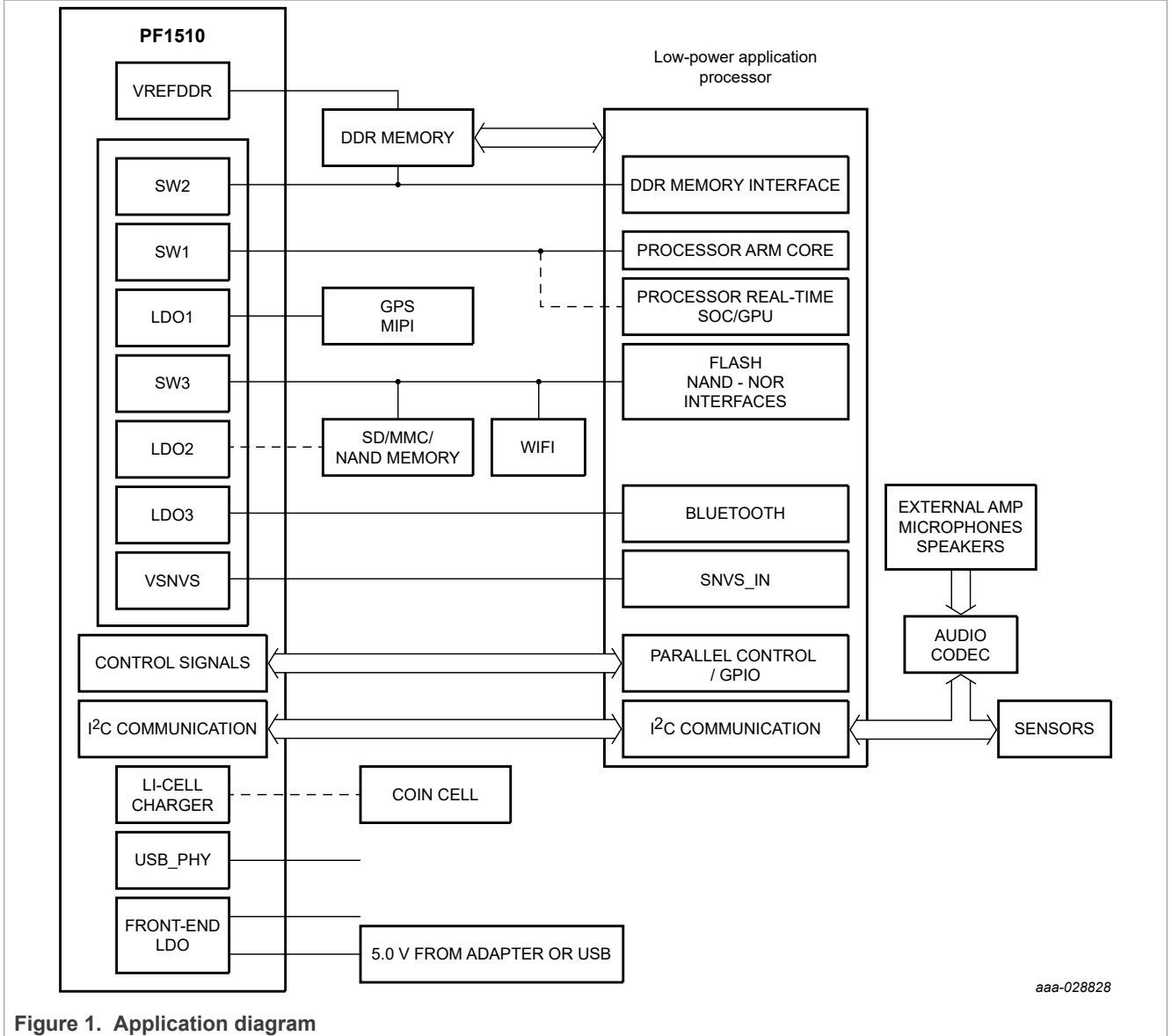
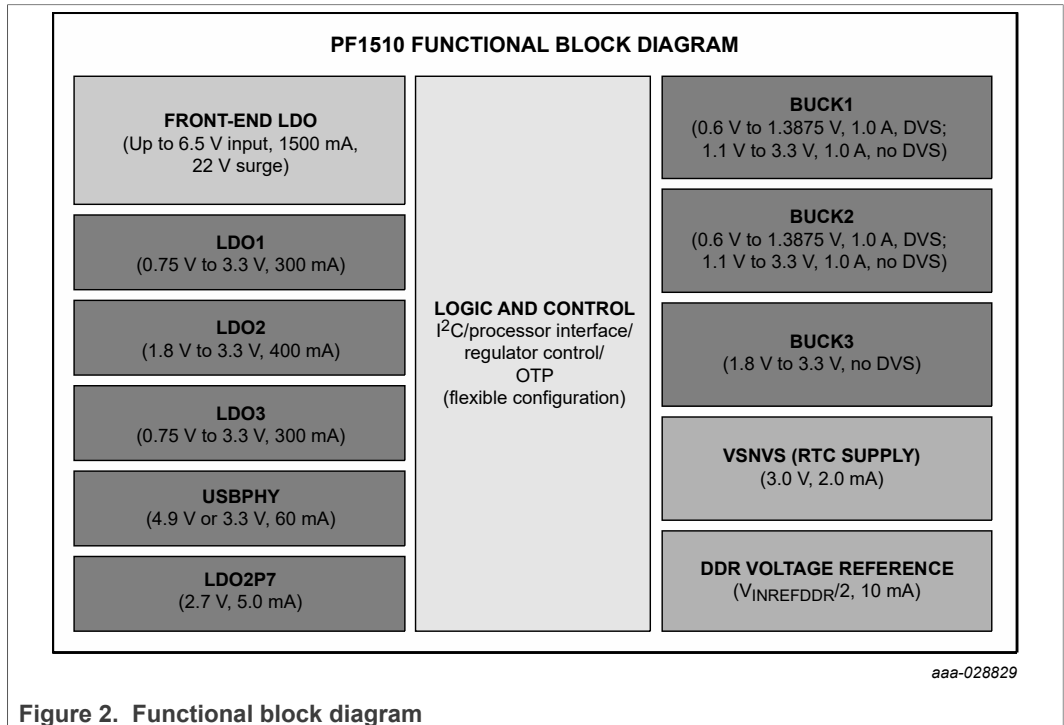


Figure 1. Application diagram

## 2.1 Functional block diagram



2.2 Internal block diagram

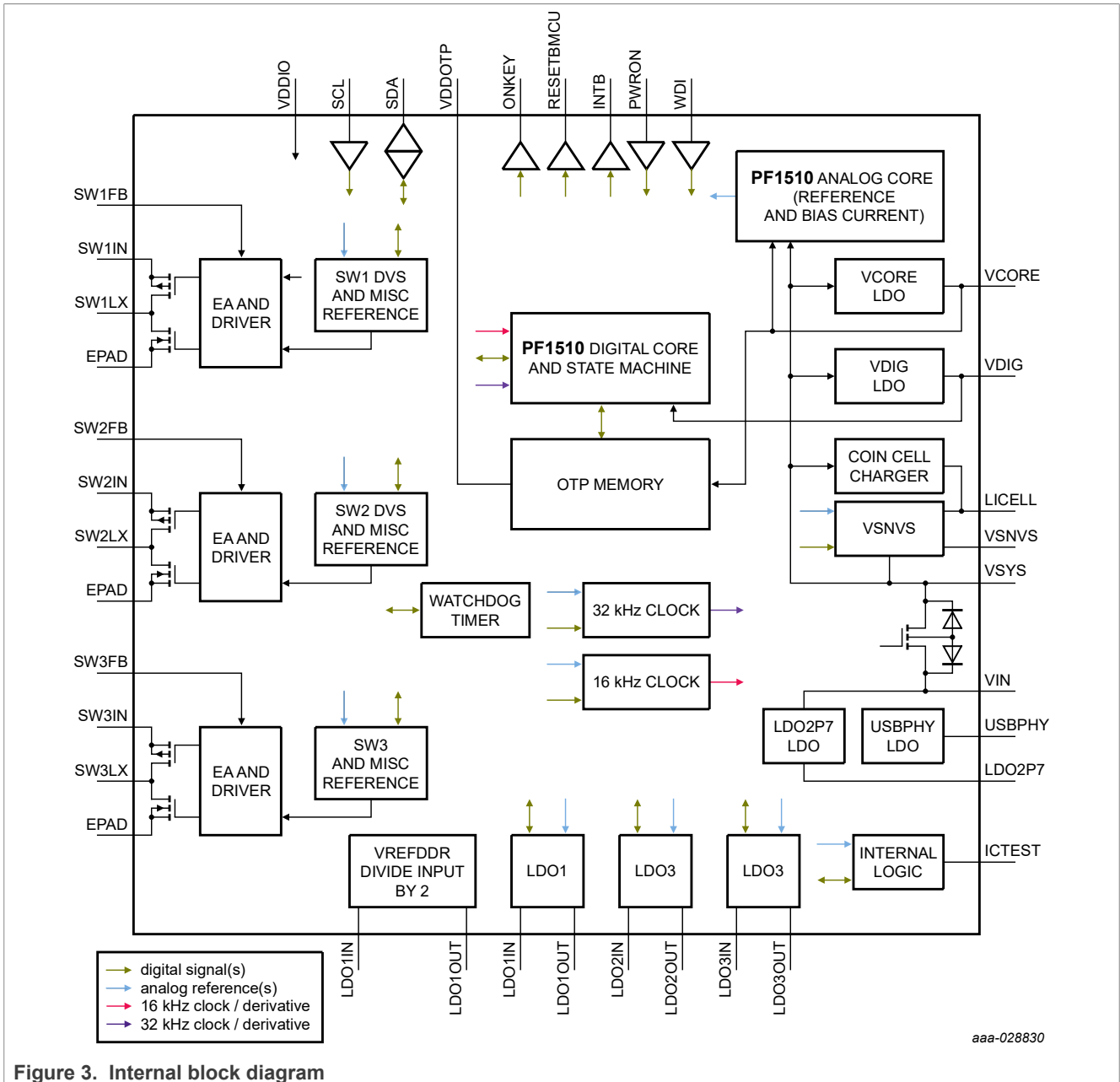


Figure 3. Internal block diagram

3 Orderable parts

The PF1510 is available only with preprogrammed configurations. These preprogrammed devices are identified using the program codes from [Table 1](#), which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in [Table 53](#).

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Table 1. Orderable part variations

| Part number <sup>[1]</sup> | Temperature (T <sub>A</sub> )                         | Package   | Programming options                      |
|----------------------------|---|---|--|
| MC32PF1510A0EP             | -40 °C to 85 °C (for use in consumer applications)    | 98ASA00913D, 40-pin QFN<br>5.0 mm x 5.0 mm with exposed pad | 0 - not programmed                       |
| MC32PF1510A1EP             |   |   | 1 (Default)                              |
| MC32PF1510A2EP             |   |   | 2 (i.MX 7ULP with LPDDR3) <sup>[2]</sup> |
| MC32PF1510A3EP             |   |   | 3 (i.MX 6UL with DDR3L)                  |
| MC32PF1510A4EP             |   |   | 4 (i.MX 7ULP with LPDDR3)                |
| MC32PF1510A5EP             |   |   | 5 (i.MX 6UL with DDR3)                   |
| MC32PF1510A6EP             |   |   | 6 (i.MX 6ULL with DDR3L)                 |
| MC32PF1510A7EP             |   |   | 7 (i.MX 6UL with LPDDR2)                 |
| MC34PF1510A0EP             | -40 °C to 105 °C (for use in industrial applications) |   | 0 - not programmed                       |
| MC34PF1510A1EP             |   |   | 1 (Default)                              |
| MC34PF1510A2EP             |   |   | 2 (i.MX 7ULP with LPDDR3) <sup>[2]</sup> |
| MC34PF1510A3EP             |   |   | 3 (i.MX 6UL with DDR3L)                  |
| MC34PF1510A4EP             |   |   | 4 (i.MX 7ULP with LPDDR3)                |
| MC34PF1510A5EP             |   |   | 5 (i.MX 6UL with DDR3)                   |
| MC34PF1510A6EP             |   | 6 (i.MX 6ULL with DDR3L)                                    |  |
| MC34PF1510A7EP             |   | 7 (i.MX 6UL with LPDDR2)                                    |  |

[1] For tape and reel, add an R2 suffix to the part number.

[2] For internal validation only

## 4 Pinning information

### 4.1 Pinning

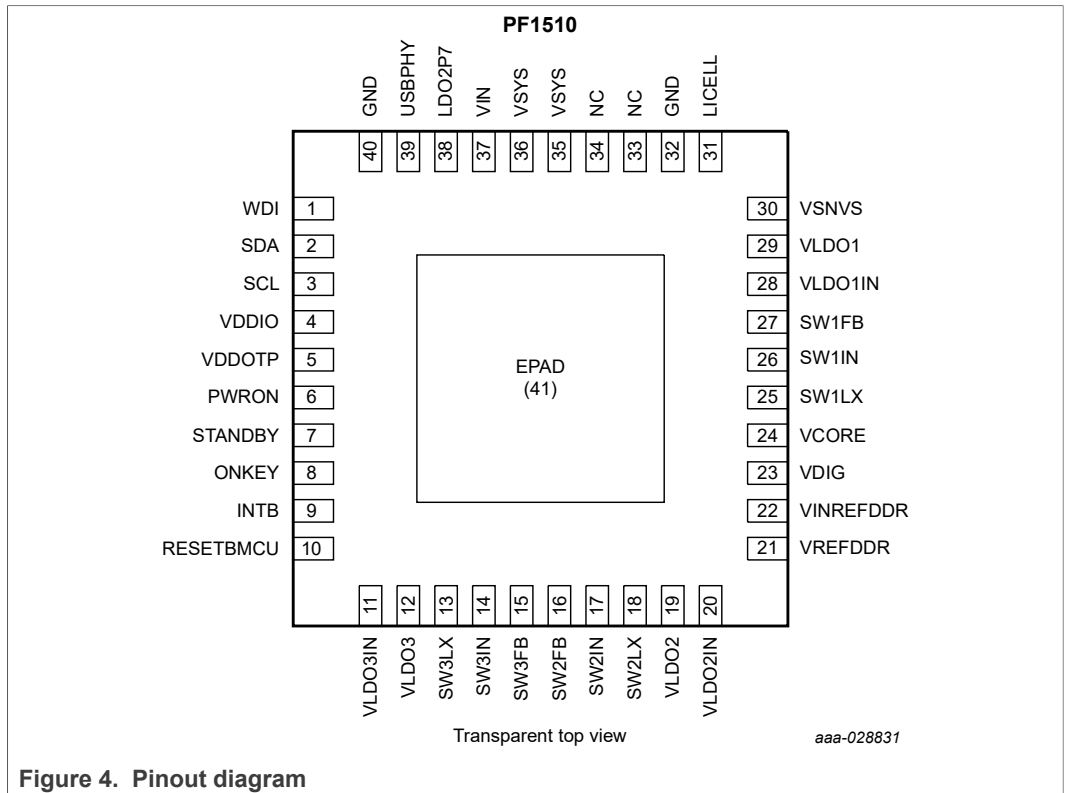


Figure 4. Pinout diagram

## 4.2 Pin definitions

Table 2. Pin description

| Pin number | Block     | Pin name                                 | Recommended connection   | Recommended connection when not used                        |
|------------|-----------|--|--|---|
| 1          | WDI       | Watchdog input from processor            | Connect to WDI signal from processor. Pull up via 8 kΩ - 100 kΩ to VDDIO                 | Connect via 100 kΩ to regulator with output voltage < 3.6 V |
| 2          | SDA       | I <sup>2</sup> C data line               | Pull-up to VDDIO   | Leave floating  |
| 3          | SCL       | I <sup>2</sup> C clock line              | Pull-up to VDDIO   | Leave floating  |
| 4          | VDDIO     | Supply for I <sup>2</sup> C bus          | Connect to 1.7 to 3.6 V supply. Bypass with 0.1 μF capacitor to ground                   | Leave floating  |
| 5          | VDDOTP    | Supply to program OTP fuses              | Connect to ground for the fuse loading   | N/A   |
| 6          | PWRON     | Power On/Off from processor              | Connect to PMIC_ON_REQ from processor. Pull up via 8 kΩ - 100 kΩ to VSNVS if required    | N/A   |
| 7          | STANDBY   | Standby input signal from processor      | Connect to PMIC_STBY_REQ signal from processor   | Connect to ground   |
| 8          | ONKEY     | ONKEY push button input                  | Connect to push button and pull up via 8kΩ - 100 kΩ to VIN                               | Connect via 100 kΩ to VSYS                                  |
| 9          | INTB      | Open drain interrupt signal to processor | Pull-up via 68 kΩ - 100 kΩ to VSNVS or other rail at voltage less than or equal to VDDIO | Leave floating  |
| 10         | RESETBMCU | Open drain reset output to processor     | Pull-up via 68 kΩ - 100 kΩ to VSNVS or other rail at voltage less than or equal to VDDIO | Leave floating  |
| 11         | VLDO3IN   | LDO3 regulator input                     | Connect to VSYS and bypass with 1.0 mF capacitor to ground                               | Connect to regulator with output voltage < 4.5 V            |
| 12         | VLDO3     | LDO3 regulator output                    | Bypass with 4.7 μF capacitor to ground   | Leave floating  |
| 13         | SW3LX     | SW3 switching node                       | Connect to SW3 inductor  | Leave floating  |
| 14         | SW3IN     | Input to SW3 regulator                   | Connect to VSYS and bypass with 0.1 μF + 4.7 μF capacitors to ground                     | Connect to VSYS   |
| 15         | SW3FB     | Output voltage feedback for SW3          | Connect to SW3 output voltage rail near load   | Leave floating  |
| 16         | SW2FB     | Output voltage feedback for SW2          | Connect to SW2 output voltage rail near load   | Leave floating  |
| 17         | SW2IN     | Input to SW2 regulator                   | Connect to VSYS and bypass with 0.1 μF + 4.7 μF capacitors to ground                     | Connect to VSYS   |
| 18         | SW2LX     | SW2 switching node                       | Connect to SW2 inductor  | Leave floating  |
| 19         | VLDO2     | LDO2 regulator output                    | Bypass with 10 μF capacitor to ground  | Leave floating  |
| 20         | VLDO2IN   | LDO2 regulator input                     | Connect to VSYS and bypass with 1.0 mF capacitor to ground                               | Connect to regulator with output voltage < 4.5 V            |
| 21         | VREFDDR   | VREFDDR regulator output                 | Bypass with 1.0 μF capacitor to ground   | Leave floating  |
| 22         | VINREFDDR | VREFDDR regulator input                  | Ensure there is at least 1.0 μF net capacitance from VINREFDDR to ground                 | Leave floating  |
| 23         | VDIG      | Digital core supply                      | Bypass with 1.0 μF capacitor to ground   | N/A   |
| 24         | VCORE     | Analog core supply                       | Bypass with 1.0 μF capacitor to ground   | N/A   |
| 25         | SW1LX     | SW1 switching node                       | Connect to SW1 inductor  | Leave floating  |
| 26         | SW1IN     | Input to SW1 regulator                   | Connect to VSYS and bypass with 0.1 μF + 4.7 μF capacitors to ground                     | Connect to VSYS   |
| 27         | SW1FB     | Output voltage feedback for SW1          | Connect to SW1 output voltage rail near load   | Leave floating  |
| 28         | VLDO1IN   | LDO1 regulators input                    | Connect to VSYS and bypass with 1.0 μF capacitor to ground                               | Connect to regulator with output voltage < 4.5 V            |
| 29         | VLDO1     | LDO1 regulator output                    | Bypass with 4.7 μF capacitor to ground   | Leave floating  |



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Table 2. Pin description...continued

| Pin number | Block  | Pin name   | Recommended connection   | Recommended connection when not used                  |
|------------|--------|--|--|---|
| 30         | VSNVS  | VSNVS regulator/switch output  | Bypass with 0.47 $\mu$ F capacitor to ground   | Bypass with 0.47 $\mu$ F capacitor to ground          |
| 31         | LICELL | Coin cell supply input/output  | Bypass with 0.1 $\mu$ F capacitor. Connect to optional coin cell.  | Bypass with 0.1 $\mu$ F capacitor to ground           |
| 32         | GND    | Ground   | Connect to ground  | Connect to ground                                     |
| 33         | NC     | Not connected  | Not connected  | Leave floating  |
| 34         | NC     |  |  |   |
| 35         | VSYS   | Main input voltage to PMIC   | Bypass with 2x 22 $\mu$ F/10 V capacitors or a 47 $\mu$ F/10 V capacitor to ground   | N/A   |
| 36         | VSYS   |  |  |   |
| 37         | VIN    | Main IC supply   | Connect to a valid 5.0 V input, bypass with a 2.2 $\mu$ F/25 V capacitor to ground   | Leave floating  |
| 38         | LDO2P7 | LDO2P7 regulator output  | Bypass with 2.2 $\mu$ F capacitor to ground mandatory  | Bypass with 2.2 $\mu$ F capacitor to ground mandatory |
| 39         | USBPHY | USBPHY regulator output  | Bypass with 1.0 $\mu$ F capacitor to ground  | Leave floating  |
| 40         | GND    | Ground   | Connect to ground  | Connect to ground                                     |
| —          | EP     | Expose pad. Functions as ground return for buck and boost regulators | Ground. Connect this pad to the inner and external ground planes through multiple vias to allow effective thermal dissipation. | N/A   |

## 5 General product characteristics

### 5.1 Thermal characteristics

Table 3. Thermal ratings

| Symbol  | Description (Rating)  | Min           | Max                | Unit           |
|---|---|---------------|--------------------|----------------|
| <b>THERMAL RATINGS</b>  |   |               |                    |                |
| $T_A$   | Ambient operating temperature range (industrial)<br>Ambient operating temperature range (consumer)  | -40<br>-40    | 105<br>85          | $^{\circ}$ C   |
| $T_J$   | Operating junction temperature range  | [1] -40       | 125                | $^{\circ}$ C   |
| $T_{ST}$  | Storage temperature range   | -65           | 150                | $^{\circ}$ C   |
| $T_{PPRT}$  | Peak package reflow temperature   | [2] [3] —     | —                  | $^{\circ}$ C   |
| <b>QFN40 THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS</b> |   |               |                    |                |
| $R_{\theta JA}$   | Junction to ambient thermal resistance, natural convection<br>Four layer board (2s2p)<br>Six layer board (2s4p)<br>Eight layer board (2s6p) | [4] [5] [6] — | 27<br>20.6<br>17.8 | $^{\circ}$ C/W |
| $R_{\theta JMA}$  | Junction to ambient (@200ft/min)<br>Four layer board (2s2p)   | [4] [6] —     | 21.4               | $^{\circ}$ C/W |
| $R_{\theta JB}$   | Junction to board   | [7] —         | 8.8                | $^{\circ}$ C/W |
| $R_{\theta JCBOTTOM}$   | Junction to case bottom   | [8] —         | 1.4                | $^{\circ}$ C/W |
| $\Psi_{JT}$   | Junction to package top – Natural convection  | [9] —         | 0.6                | $^{\circ}$ C/W |

[1] Do not operate beyond 125  $^{\circ}$ C for extended periods of time. Operation above 150  $^{\circ}$ C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.

[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

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- [3] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to <http://www.nxp.com>, search by part number [ remove prefixes/suffixes and enter the core ID to view all orderable parts (for MC33xxxD enter 33xxx), and review parametrics.
- [4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- [5] The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
- [6] Per JEDEC JESD51-6 with the board horizontal.
- [7] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- [8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- [9] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 5.2 Absolute maximum ratings

Table 4. Maximum ratings

| Symbol        | Description (Rating)   | Min  | Max | Unit |
|---------------|--|------|-----|------|
| <b>I/Os</b>   |  |      |     |      |
| VIN           | Main IC supply   | -0.3 | 24  | V    |
| VDDIO         | I/O supply voltage. Connect to voltage rail between 1.7 V and 3.3 V. | -0.3 | 3.6 | V    |
| SCL           | SCL when used in I <sup>2</sup> C mode. SCLK when used in SPI mode.  | -0.3 | 3.6 | V    |
| SDA           | SDA when used in I <sup>2</sup> C mode. MISO when used in SPI mode.  | -0.3 | 3.6 | V    |
| RESETBMCU     | RESETBMCU open drain output  | -0.3 | 3.6 | V    |
| PWRON         | PWRON input  | -0.3 | 3.6 | V    |
| STANDBY       | STANDBY input  | -0.3 | 3.6 | V    |
| ONKEY         | ONKEY push button input  | -0.3 | 4.8 | V    |
| INTB          | INTB open-drain output   | -0.3 | 3.6 | V    |
| WDI           | Watchdog input from processor  | -0.3 | 3.6 | V    |
| <b>VDDOTP</b> |  |      |     |      |
| VDDOTP        | Connect to ground in the application                                 | -0.3 | 10  | V    |
| <b>BUCK 1</b> |  |      |     |      |
| SW1IN         | Buck 1 input supply  | -0.3 | 4.8 | V    |
| SW1LX         | Buck 1 switching node  | -0.3 | 4.8 | V    |
| SW1FB         | Buck 1 feedback input  | -0.3 | 3.6 | V    |
| <b>BUCK 2</b> |  |      |     |      |
| SW2IN         | Buck 2 input supply  | -0.3 | 4.8 | V    |
| SW2LX         | Buck 2 switching node  | -0.3 | 4.8 | V    |
| SW2FB         | Buck 2 output voltage feedback                                       | -0.3 | 3.6 | V    |
| <b>BUCK 3</b> |  |      |     |      |
| SW3IN         | Buck 3 input supply  | -0.3 | 4.8 | V    |
| SW3LX         | Buck 3 switching node  | -0.3 | 4.8 | V    |
| SW3FB         | Buck 3 output voltage feedback                                       | -0.3 | 3.6 | V    |
| <b>LDO1</b>   |  |      |     |      |
| VLDO1IN       | LDO1 input supply  | -0.3 | 4.8 | V    |
| VLDO1         | LDO1 output  | -0.3 | 3.6 | V    |

Table 4. Maximum ratings...continued

| Symbol                     | Description (Rating)                        | Min  | Max  | Unit  |   |
|----------------------------|---|------|------|-------|---|
| <b>LDO2</b>                |   |      |      |       |   |
| VLDO2IN                    | LDO2 input supply                           | -0.3 | 4.8  | V     |   |
| VLDO2                      | LDO2 output                                 | -0.3 | 3.6  | V     |   |
| <b>LDO3</b>                |   |      |      |       |   |
| VLDO3IN                    | LDO3 input supply                           | -0.3 | 4.8  | V     |   |
| VLDO3                      | LDO3 output                                 | -0.3 | 3.6  | V     |   |
| <b>VSNVS</b>               |   |      |      |       |   |
| VSNVS                      | VSNVS regulator output                      | -0.3 | 3.6  | V     |   |
| LICELL                     | Coin cell input                             | -0.3 | 3.6  | V     |   |
| <b>FRONT-END LDO</b>       |   |      |      |       |   |
| LDO2P7                     | LDO2P7 regulator output                     | -0.3 | 3.6  | V     |   |
| USBPHY                     | USBPHY regulator output                     | -0.3 | 5.5  | V     |   |
| <b>INPUT/OUTPUT SUPPLY</b> |   |      |      |       |   |
| VINREFDDR                  | VREFDDR input supply                        | -0.3 | 3.6  | V     |   |
| VREFDDR                    | VREFDDR output                              | -0.3 | 3.6  | V     |   |
| <b>IC CORE</b>             |   |      |      |       |   |
| VSYS                       | Main input voltage to PMIC                  | -0.3 | 4.8  | V     |   |
| VDIG                       | VDIG regulator output (used within PF1510)  | -0.3 | 1.65 |       |   |
| VCORE                      | VCORE regulator output (used within PF1510) | -0.3 | 1.65 | V     |   |
| <b>ELECTRICAL RATINGS</b>  |   |      |      |       |   |
| V <sub>ESD</sub>           | ESD ratings                                 |      |      |       |   |
|                            | Human body model                            | [1]  | —    | ±2000 | V |
|                            | Charge device model (corner pins)           |      | —    | ±750  |   |
|                            | Charge device model (all other pins)        |      | —    | ±500  |   |

[1] Testing is performed in accordance with the human body model (HBM) ( $C_{ZAP} = 100$  pF,  $R_{ZAP} = 1500$   $\Omega$ ), and the charge device model (CDM), Robotic ( $C_{ZAP} = 4.0$  pF).

### 5.3 Electrical characteristics

#### 5.3.1 Electrical characteristics – Front-end LDO

All parameters are specified at  $T_A = -40$  to  $105$  °C,  $V_{IN} = 5.0$  V,  $V_{SYS} = 3.7$  V, typical external component values, unless otherwise noted. Typical values are characterized at  $V_{IN} = 5.0$  V,  $V_{SYS} = 3.7$  V and  $25$  °C, unless otherwise noted.

Table 5. Front-end LDO

| Symbol                     | Parameter  | Measurement condition           | Min        | Typ | Max        | Unit |
|----------------------------|--|---------------------------------|------------|-----|------------|------|
| <b>FRONT-END LDO INPUT</b> |  |                                 |            |     |            |      |
| $V_{IN}$                   | $V_{IN}$ voltage range                                   | Operating voltage               | $V_{UVLO}$ | —   | $V_{OVLO}$ | V    |
| $V_{IN\_WITHSTAND}$        | $V_{IN}$ maximum withstand voltage rating                |                                 | —          | —   | 22         | V    |
| $V_{IN\_OVLO}$             | $V_{IN}$ overvoltage threshold                           | Rising                          | 6.0        | 6.5 | 7.0        | V    |
| $V_{OVLO\_HYS}$            | $V_{IN}$ overvoltage threshold hysteresis                | Falling                         | 50         | 150 | 250        | mV   |
| $t_{D-OVLO}$               | $V_{IN}$ overvoltage delay                               |                                 | 5.0        | 10  | 15         | μs   |
| $V_{UVLO}$                 | $V_{IN}$ to GND minimum turn on threshold accuracy       | $V_{IN}$ rising                 | 3.8        | 4.0 | 4.2        | V    |
| $V_{UVLO-HYS}$             | $V_{IN}$ UVLO hysteresis                                 |                                 | 400        | 500 | 600        | mV   |
| $V_{IN2SYS\_50}$           | $V_{IN}$ to $V_{SYS}$ minimum turn on threshold accuracy | $V_{IN}$ rising, 50 mV setting  | 20         | 50  | 80         | mV   |
| $V_{IN2SYS\_175}$          | $V_{IN}$ to $V_{SYS}$ minimum turn on threshold accuracy | $V_{IN}$ rising, 175 mV setting | 100        | 175 | 250        | mV   |

Table 6. Input currents

| Symbol                   | Parameter                                | Measurement condition | Min  | Typ   | Max | Unit |
|--------------------------|--|-----------------------|------|-------|-----|------|
| <b>VIN CURRENT LIMIT</b> |  |                       |      |       |     |      |
| $ILIM_{10}$              | $V_{IN}$ current limit (10 mA settings)  | 10 mA                 | 6.0  | 8.5   | 11  | mA   |
| $ILIM_{15}$              | $V_{IN}$ current limit (15 mA settings)  | 15 mA                 | 10.5 | 12.75 | 16  | mA   |
| $ILIM_{20}$              | $V_{IN}$ current limit (20 mA settings)  | 20 mA                 | 14   | 17    | 21  | mA   |
| $ILIM_{25}$              | $V_{IN}$ current limit (25 mA settings)  | 25 mA                 | 17.5 | 21.25 | 26  | mA   |
| $ILIM_{30}$              | $V_{IN}$ current limit (30 mA setting)   | 30 mA                 | 21   | 25.5  | 30  | mA   |
| $ILIM_{35}$              | $V_{IN}$ current limit (35 mA settings)  | 35 mA                 | 24.5 | 29.75 | 35  | mA   |
| $ILIM_{40}$              | $V_{IN}$ current limit (40 mA settings)  | 40 mA                 | 28   | 34    | 40  | mA   |
| $ILIM_{45}$              | $V_{IN}$ current limit (45 mA settings)  | 45 mA                 | 31.5 | 38.25 | 45  | mA   |
| $ILIM_{50}$              | $V_{IN}$ current limit (50 mA settings)  | 50 mA                 | 35   | 42.5  | 50  | mA   |
| $ILIM_{100}$             | $V_{IN}$ current limit (100 mA settings) | 100 mA                | 85   | 95    | 105 | mA   |
| $ILIM_{150}$             | $V_{IN}$ current limit (150 mA settings) | 150 mA                | 125  | 137.5 | 160 | mA   |
| $ILIM_{200}$             | $V_{IN}$ current limit (200 mA settings) | 200 mA                | 170  | 190   | 210 | mA   |
| $ILIM_{300}$             | $V_{IN}$ current limit (300 mA setting)  | 300 mA                | 260  | 285   | 320 | mA   |
| $ILIM_{400}$             | $V_{IN}$ current limit (400 mA settings) | 400 mA                | 345  | 380   | 425 | mA   |

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Table 6. Input currents...continued

| Symbol               | Parameter                            | Measurement condition | Min  | Typ  | Max  | Unit |
|----------------------|--------------------------------------|-----------------------|------|------|------|------|
| ILIM <sub>500</sub>  | VIN current limit (500 mA settings)  | 500 mA                | 430  | 475  | 530  | mA   |
| ILIM <sub>600</sub>  | VIN current limit (600 mA settings)  | 600 mA                | 520  | 570  | 640  | mA   |
| ILIM <sub>700</sub>  | VIN current limit (700 mA settings)  | 700 mA                | 610  | 665  | 750  | mA   |
| ILIM <sub>800</sub>  | VIN current limit (800 mA settings)  | 800 mA                | 690  | 760  | 850  | mA   |
| ILIM <sub>900</sub>  | VIN current limit (900 mA settings)  | 900 mA                | 780  | 855  | 950  | mA   |
| ILIM <sub>1000</sub> | VIN current limit (1000 mA settings) | 1000 mA               | 855  | 950  | 1100 | mA   |
| ILIM <sub>1500</sub> | VIN current limit (1500 mA settings) | 1500 mA               | 1260 | 1400 | 1700 | mA   |
| R <sub>INSD</sub>    | Input self discharge resistance      |                       | 18   | 30   | 42   | kΩ   |

Table 7. Switch impedances and leakage currents

| Symbol               | Parameter              | Measurement Condition | Min | Typ | Max | Unit |
|----------------------|------------------------|-----------------------|-----|-----|-----|------|
| R <sub>VIN2SYS</sub> | VIN to VSYS resistance |                       | 100 | 250 | 550 | mΩ   |
| I <sub>sys</sub>     | VSYS leakage current   | VSYS = 0 V            | 0   | 0.2 | 10  | μA   |

Table 8. Watchdog timer

| Symbol             | Parameter               | Measurement condition | Min | Typ | Max | Unit |
|--------------------|-------------------------|-----------------------|-----|-----|-----|------|
| t <sub>WD</sub>    | Watchdog timer period   |                       | —   | 80  | —   | s    |
| t <sub>WDACC</sub> | Watchdog timer accuracy |                       | -20 | 0   | 20  | %    |

Table 9. Internal 2.7 V Regulator (LDO2P7)

| Symbol                | Parameter       | Measurement condition | Min | Typ | Max | Unit |
|-----------------------|-----------------|-----------------------|-----|-----|-----|------|
| V <sub>GDRV</sub>     | Output voltage  |                       | 2.6 | 2.7 | 2.8 | V    |
| I <sub>GDRV</sub>     | Output current  |                       | 5.0 | —   | —   | mA   |
| V <sub>DO(GDRV)</sub> | Dropout voltage |                       | 0   | —   | 800 | mV   |

Table 10. USBPHY LDO

| Symbol                  | Parameter                             | Measurement condition   | Min  | Typ  | Max  | Unit |
|-------------------------|---------------------------------------|---|------|------|------|------|
| V <sub>USB_PHY</sub>    | Output voltage                        | I <sub>OUT</sub> = 10 mA; 3.3 V and 4.9 V settings. VIN = 5.5 V | -5.0 | —    | 5.0  | %    |
| I <sub>USB_PHY</sub>    | Maximum output current                |   | 60   | —    | —    | mA   |
| USB <sub>RDIS</sub>     | Internal discharge resistance         |   | 500  | 1000 | 1500 | Ω    |
| USB <sub>CAPSTA</sub>   | Output capacitor for stable operation | 0 μA < I <sub>OUT</sub> < 60 mA, MAX ESR = 10 mΩ                | 0.7  | 1.0  | 2.2  | μF   |
| I <sub>QUSB</sub>       | Quiescent supply current              |   | —    | 35   | —    | μA   |
| USBPHY <sub>LDREG</sub> | DC load regulation                    | VIN = 5.5 V, 30 μA < I <sub>OUT</sub> < 60 mA                   | 0    | 5.0  | 13   | mV   |

Table 10. USBPHY LDO...continued

| Symbol                  | Parameter            | Measurement condition                              | Min | Typ | Max | Unit |
|-------------------------|----------------------|--|-----|-----|-----|------|
| USBPHY <sub>DO</sub>    | Dropout voltage      | V <sub>IN</sub> = 5.0 V, I <sub>OUT</sub> = 60 mA  | —   | 200 | 350 | mV   |
| USBPHY <sub>LIM</sub>   | Output current limit |  | 65  | 150 | 200 | mA   |
| PSRR <sub>USB_PHY</sub> | PSRR                 | V <sub>IN</sub> = 5.5 V, C <sub>OUT</sub> = 1.0 μF | 55  | 60  | 75  | dB   |

5.3.2 Electrical characteristics – SW1 and SW2

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = V<sub>SWxIN</sub> = 2.5 to 4.5 V, V<sub>SWx</sub> = 1.2 V, I<sub>SWx</sub> = 200 mA, typical external component values, f<sub>SWx</sub> = 2.0 MHz, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = V<sub>SWxIN</sub> = 3.6 V, V<sub>SWx</sub> = 1.1 V, I<sub>SWx</sub> = 100 mA, and 25 °C, unless otherwise noted.

Table 11. SW1 and SW2 electrical characteristics

| Symbol             | Parameter   | Min  | Typ | Max | Unit |
|--------------------|---|------|-----|-----|------|
| V <sub>SWxIN</sub> | Operating input voltage   | 2.5  | —   | 4.5 | V    |
| I <sub>SWx</sub>   | Rated output current  | 1000 | —   | —   | mA   |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS enabled mode (OTP_SWx_DVS_SEL = 0)<br>Normal power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 1.0 A<br>0.6 V ≤ V <sub>SWx</sub> ≤ 1.0 V    | -15  | —   | 15  | mV   |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS enabled mode (OTP_SWx_DVS_SEL = 0)<br>Normal power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 1.0 A<br>1.0 V < V <sub>SWx</sub> ≤ 1.3875 V | -2.0 | —   | 2.0 | %    |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS enabled mode (OTP_SWx_DVS_SEL = 0)<br>Low-power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 0.1 A<br>0.6 V ≤ V <sub>SWx</sub> ≤ 1.0 V       | -30  | —   | 30  | mV   |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS enabled mode (OTP_SWx_DVS_SEL = 0)<br>Low-power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 0.1 A<br>1.0 V < V <sub>SWx</sub> ≤ 1.3875 V    | -3.0 | —   | 3.0 | %    |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS disabled mode (OTP_SWx_DVS_SEL = 1)<br>Normal power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 1.0 A<br>1.1 V ≤ V <sub>SWx</sub> ≤ 1.5 V   | -45  | —   | 45  | mV   |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS disabled mode (OTP_SWx_DVS_SEL = 1)<br>Normal power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 1.0 A<br>1.8 V ≤ V <sub>SWx</sub> ≤ 3.3 V   | -3.0 | —   | 3.0 | %    |
| V <sub>SWx</sub>   | Output voltage accuracy<br>DVS disabled mode (OTP_SWx_DVS_SEL = 1)<br>Low-power mode, 2.5 V < V <sub>SWxIN</sub> < 4.5 V, 0 < I <sub>SWx</sub> < 0.1 A<br>1.1 V < V <sub>SWx</sub> ≤ 1.5 V      | -55  | —   | 55  | mV   |

## Power management integrated circuit (PMIC) for low power application processors

Table 11. SW1 and SW2 electrical characteristics...continued

| Symbol           | Parameter   | Min                      | Typ                      | Max                      | Unit          |
|------------------|---|--------------------------|--------------------------|--------------------------|---------------|
| $V_{SWx}$        | Output voltage accuracy<br>DVS disabled mode (OTP_SWx_DVS_SEL = 1)<br>Low-power mode, $2.5\text{ V} < V_{SWxIN} < 4.5\text{ V}$ , $0 < I_{SWx} < 0.1\text{ A}$<br>$1.8\text{ V} \leq V_{SWx} \leq 3.3\text{ V}$ | -4.0                     | —                        | 4.0                      | %             |
| $\Delta V_{SWx}$ | Output ripple   | —                        | 5.0                      | —                        | mV            |
| SWxEFF           | Efficiency<br>$V_{SWxIN} = 3.6\text{ V}$ , $L_{SWx} = 1.0\text{ }\mu\text{H}$ , DCR = 50 mΩ<br>LP/ ULP mode, 1.2 V, 1.0 mA  | —                        | 88                       | —                        | %             |
| SWxEFF           | Efficiency<br>$V_{SWxIN} = 3.6\text{ V}$ , $L_{SWx} = 1.0\text{ }\mu\text{H}$ , DCR = 50 mΩ<br>Normal power mode, 1.2 V, 50 mA  | —                        | 90                       | —                        | %             |
| SWxEFF           | Efficiency<br>$V_{SWxIN} = 3.6\text{ V}$ , $L_{SWx} = 1.0\text{ }\mu\text{H}$ , DCR = 50 mΩ<br>Normal power mode, 1.2 V, 150 mA   | —                        | 92                       | —                        | %             |
| SWxEFF           | Efficiency<br>$V_{SWxIN} = 3.6\text{ V}$ , $L_{SWx} = 1.0\text{ }\mu\text{H}$ , DCR = 50 mΩ<br>Normal power mode, 1.2 V, 400 mA   | —                        | 89                       | —                        | %             |
| SWxEFF           | Efficiency<br>$V_{SWxIN} = 3.6\text{ V}$ , $L_{SWx} = 1.0\text{ }\mu\text{H}$ , DCR = 50 mΩ<br>Normal power mode, 1.2 V, 1000 mA  | —                        | 83                       | —                        | %             |
| $I_{SWxLIMH}$    | Current limiter peak (high-side MOSFET) current detection<br>SWxLIM[1:0] = 00<br>SWxLIM[1:0] = 01<br>SWxLIM[1:0] = 10<br>SWxLIM[1:0] = 11   | 0.7<br>0.8<br>1.0<br>1.4 | 1.0<br>1.2<br>1.5<br>2.0 | 1.3<br>1.6<br>2.0<br>2.6 | A             |
| $I_{SWxLIML}$    | Current limiter low-side MOSFET current detection (sinking current)   | 0.7                      | 1.0                      | 1.3                      | A             |
| $I_{SWxQ}$       | Quiescent current (at 25 °C)<br>Low-power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)  | —                        | 1.0                      | —                        | $\mu\text{A}$ |
| $I_{SWxQ}$       | Quiescent current (at 25 °C)<br>Low-power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)   | —                        | 6.0                      | —                        | $\mu\text{A}$ |
| $I_{SWxQ}$       | Quiescent current (at 25 °C)<br>Normal power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)   | —                        | 5.5                      | —                        | $\mu\text{A}$ |
| $I_{SWxQ}$       | Quiescent current (at 25 °C)<br>Normal power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)  | —                        | 10                       | —                        | $\mu\text{A}$ |
| $V_{SWxOSH}$     | Startup overshoot (Normal mode)<br>$I_{SWx} = 0\text{ mA}$<br>DVS speed = 12.5 mV/4 $\mu\text{s}$ , $V_{SYS} = V_{SWxIN} = 3.6\text{ V}$ , $V_{SWx} = 1.35\text{ V}$  | —                        | —                        | 25                       | mV            |
| $t_{ONSWx}$      | Turn on time<br>10 % to 90 % of end value<br>DVS speed = 12.5 mV/4 $\mu\text{s}$ , $V_{SYS} = V_{SWxIN} = 3.6\text{ V}$ , $V_{SWx} = 1.35\text{ V}$   | —                        | —                        | 500                      | $\mu\text{s}$ |

## Power management integrated circuit (PMIC) for low power application processors

Table 11. SW1 and SW2 electrical characteristics...continued

| Symbol               | Parameter  | Min | Typ | Max | Unit |
|----------------------|--|-----|-----|-----|------|
| V <sub>SWxLOTR</sub> | Transient load regulation (Normal power mode)                  |     |     |     | mV   |
|                      | Transient load = 50 mA to 250 mA, di/dt = 200 mA/μs            |     |     |     |      |
|                      | Overshoot  | —   | 25  | —   |      |
|                      | Undershoot   | —   | 25  | —   |      |
| R <sub>ONSWxP</sub>  | SWx P-MOSFET R <sub>DS(on)</sub> at V <sub>SWxIN</sub> = 3.6 V | —   | 200 | —   | mΩ   |
| R <sub>ONSWxN</sub>  | SWx N-MOSFET R <sub>DS(on)</sub> at V <sub>SWxIN</sub> = 3.6 V | —   | 150 | —   | mΩ   |
| R <sub>SWxDIS</sub>  | Turn off discharge resistance                                  | —   | 500 | —   | Ω    |

## 5.3.3 Electrical characteristics – SW3

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = V<sub>SW3IN</sub> = 2.5 to 4.5 V, V<sub>SW3</sub> = 1.8 V, I<sub>SW3</sub> = 200 mA, typical external component values, f<sub>SW3</sub> = 2.0 MHz, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = V<sub>SW3IN</sub> = 3.6 V, V<sub>SW3</sub> = 1.8 V, I<sub>SW3</sub> = 200 mA, and 25 °C, unless otherwise noted.

Table 12. SW3 electrical characteristics

| Symbol               | Parameter   | Min                      | Typ                      | Max                      | Unit |
|----------------------|---|--------------------------|--------------------------|--------------------------|------|
| V <sub>SW3IN</sub>   | Operating input voltage   | 2.5                      | —                        | 4.5                      | V    |
| V <sub>SW3</sub>     | Output voltage accuracy (all voltage settings)<br>Normal power mode, 2.5 V < V <sub>SW3IN</sub> < 4.5 V, 0 < I <sub>SW3</sub> < 1.0 A     | -2.0                     | —                        | 2.0                      | %    |
| V <sub>SW3</sub>     | Output voltage accuracy (all voltage settings)<br>Low-power mode, 2.5 V < V <sub>SW3IN</sub> < 4.5 V, 0 < I <sub>SW3</sub> < 0.1 A        | -3.0                     | —                        | 3.0                      | %    |
| ΔV <sub>SW3</sub>    | Output ripple   | —                        | 5.0                      | —                        | mV   |
| SW3EFF               | Efficiency<br>V <sub>SW3IN</sub> = 3.6 V, L <sub>SW3</sub> = 1.0 μH, DCR = 50 mΩ<br>LP/ ULP Mode, 1.8 V, 1.0 mA                           | —                        | 88                       | —                        | %    |
| SW3EFF               | Efficiency<br>V <sub>SW3IN</sub> = 3.6 V, L <sub>SWx</sub> = 1.0 μH, DCR = 50 mΩ<br>Normal power mode, 1.8 V, 50 mA                       | —                        | 90                       | —                        | %    |
| SW3EFF               | Efficiency<br>V <sub>SW3IN</sub> = 3.6 V, L <sub>SWx</sub> = 1.0 mH, DCR = 50 mΩ<br>Normal power mode, 1.8 V, 100 mA                      | —                        | 91                       | —                        | %    |
| SW3EFF               | Efficiency<br>V <sub>SW3IN</sub> = 3.6 V, L <sub>SWx</sub> = 1.0 μH, DCR = 50 mΩ<br>Normal power mode, 1.8 V, 400 mA                      | —                        | 92                       | —                        | %    |
| SW3EFF               | Efficiency<br>V <sub>SW3IN</sub> = 3.6 V, L <sub>SWx</sub> = 1.0 μH, DCR = 50 mΩ<br>Normal power mode, 1.8 V, 1000 mA                     | —                        | 83                       | —                        | %    |
| I <sub>SW3LIMH</sub> | Current limiter peak (high-side MOSFET) current detection<br>SW3LIM[1:0] = 00<br>SW3LIM[1:0] = 01<br>SW3LIM[1:0] = 10<br>SW3LIM[1:0] = 11 | 0.7<br>0.8<br>1.0<br>1.4 | 1.0<br>1.2<br>1.5<br>2.0 | 1.3<br>1.6<br>2.0<br>2.6 | A    |
| I <sub>SW3LIML</sub> | Current limiter low-side MOSFET current detection (sinking current)   | 0.7                      | 1.0                      | 1.3                      | A    |



Table 12. SW3 electrical characteristics...continued

| Symbol               | Parameter  | Min    | Typ      | Max    | Unit |
|----------------------|--|--------|----------|--------|------|
| I <sub>SW3Q</sub>    | Quiescent current (at 25 °C)<br>Low-power mode   | —      | 1.0      | —      | µA   |
| V <sub>SW3OSH</sub>  | Start-up overshoot (Normal mode)<br>I <sub>SW3</sub> = 0 mA<br>V <sub>SYS</sub> = V <sub>SW3IN</sub> = 3.6 V, V <sub>SW3</sub> = 1.8 V | —      | —        | 50     | mV   |
| t <sub>ONSW3</sub>   | Turn on time<br>10 % to 90 % of end value<br>V <sub>SYS</sub> = V <sub>SW3IN</sub> = 3.6 V, V <sub>SW3</sub> = 1.8 V                   | —      | —        | 500    | µs   |
| V <sub>SW3LOTR</sub> | Transient load regulation (Normal power mode)<br>Transient load = 50 mA to 250 mA, di/dt = 200 mA/µs<br>Overshoot<br>Undershoot        | —<br>— | 50<br>50 | —<br>— | mV   |
| R <sub>ONSW3N</sub>  | SW3 N-MOSFET R <sub>DS(on)</sub> at V <sub>SW3IN</sub> = 3.6 V   | —      | 150      | —      | mΩ   |
| R <sub>ONSW3P</sub>  | SW3 P-MOSFET R <sub>DS(on)</sub> at V <sub>SW3IN</sub> = 3.6 V   | —      | 200      | —      | mΩ   |
| R <sub>SW3DIS</sub>  | Turn off discharge resistance  | —      | 300      | —      | Ω    |

### 5.3.4 Electrical characteristics – LDO1

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = 2.5 to 4.5 V, V<sub>LDO1IN</sub> = 3.6 V, VLDO1[4:0] = 11111, I<sub>LDO1</sub> = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = 3.6 V, V<sub>LDO1IN</sub> = 3.6 V, VLDO1[4:0] = 11111, I<sub>LDO1</sub> = 10 mA, and 25 °C, unless otherwise noted.

Table 13. LDO1 electrical characteristics

| Symbol                  | Parameter   | Min                  | Typ                          | Max               | Unit |
|-------------------------|---|----------------------|------------------------------|-------------------|------|
| V <sub>LDO1IN</sub>     | Operating input voltage<br>V <sub>LDO1</sub> + 250 mV ≤ V <sub>SYS</sub> ≤ 4.5 V  | 1.0                  | —                            | 4.5               | V    |
| V <sub>LDO1NOM</sub>    | Nominal output voltage  | —                    | See <a href="#">Table 33</a> | —                 | V    |
| I <sub>LDO1MAX</sub>    | Rated output load current, Normal mode  | 300                  | —                            | —                 | mA   |
| I <sub>LDO1MAXLPM</sub> | Rated output load current, Low-power mode   | 10                   | —                            | —                 | mA   |
| V <sub>LDO1TOL</sub>    | Output voltage tolerance, Normal mode<br>V <sub>LDO1INMIN</sub> < V <sub>LDO1IN</sub> < 4.5 V, 0 mA < I <sub>LDO1</sub> ≤ 300 mA<br>0.8 V ≤ V <sub>LDO1</sub> < 1.8 V<br>1.8 V ≤ V <sub>LDO1</sub> ≤ 3.3 V<br>V <sub>LDO1INMIN</sub> < V <sub>LDO1IN</sub> < 4.5 V, 0 mA < I <sub>LDO1</sub> < 10 mA (Low-power mode) | -2.5<br>-2.5<br>-4.0 | —<br>—<br>—                  | 2.5<br>2.5<br>4.0 | %    |
| I <sub>LDO1LIM</sub>    | Current limit<br>I <sub>LDO1</sub> when V <sub>LDO1</sub> is forced to V <sub>LDO1NOM</sub> /2  | 320                  | —                            | 1000              | mA   |
| I <sub>LDO1OCP</sub>    | LDO1FAULTI threshold (also used to disable LDO1 when REGSCPEN = 1)  | 320                  | —                            | 1000              | mA   |
| I <sub>LDO1Q</sub>      | Quiescent current (at 25 °C)<br>No load, change in I <sub>VSYS</sub> and I <sub>VLDO1IN</sub><br>When LDO1 enabled in Normal mode<br>When LDO1 enabled in Low-power mode  | —<br>—               | 17<br>2.5                    | —<br>—            | µA   |

Table 13. LDO1 electrical characteristics...continued

| Symbol                         | Parameter  | Min    | Typ      | Max    | Unit |
|--------------------------------|--|--------|----------|--------|------|
| R <sub>DSON_QFN_LDO1</sub>     | Dropout on resistance  | —      | —        | 350    | mΩ   |
| PSRR <sub>LDO1</sub>           | PSRR<br>I <sub>LDO1</sub> = 150 mA, 20 Hz to 20 kHz<br>V <sub>LDO1</sub> = 3.30 V, V <sub>LDO1IN</sub> = 3.8 V, V <sub>SYS</sub> = 4.2 V                 | —      | 56       | —      | dB   |
| TR <sub>V<sub>LDO1</sub></sub> | Turn on time<br>10 % to 90 % of end value<br>V <sub>LDO1INMIN</sub> < V <sub>LDO1IN</sub> ≤ 4.5 V, I <sub>LDO1</sub> = 0.0 mA                            | —      | 200      | 500    | μs   |
| R <sub>LDO1DIS</sub>           | Turn off discharge resistance  | —      | 250      | —      | Ω    |
| LDO1OUT <sub>OSHT</sub>        | Start-up overshoot (% of final value)<br>V <sub>LDO1INMIN</sub> < V <sub>LDO1IN</sub> ≤ 4.5 V, I <sub>LDO1</sub> = 0.0 mA                                | —      | 1.0      | 2.0    | %    |
| V <sub>LDO1LOTR</sub>          | Transient load response<br>V <sub>LDO1INMIN</sub> < V <sub>LDO1IN</sub> ≤ 4.5 V, I <sub>LDO1</sub> = 10 mA to 200 mA in 10 μs<br>Overshoot<br>Undershoot | —<br>— | 50<br>50 | —<br>— | mV   |

### 5.3.5 Electrical characteristics – LDO2

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = 3.6 V, V<sub>LDOIN2</sub> = 3.6 V, VLDO2[3:0] = 1111, I<sub>LDO2</sub> = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = 3.6 V, V<sub>LDOIN2</sub> = 3.6 V, VLDO2[3:0] = 1111, I<sub>LDO2</sub> = 10 mA, and 25 °C, unless otherwise noted.

Table 14. LDO2 electrical characteristics

| Symbol                     | Parameter   | Min                                 | Typ                          | Max        | Unit |
|----------------------------|---|-------------------------------------|------------------------------|------------|------|
| V <sub>LDO2IN</sub>        | Operating input voltage<br>1.8 V ≤ V <sub>LDO2NOM</sub> ≤ 2.5 V<br>2.6 V ≤ V <sub>LDO2NOM</sub> ≤ 3.3 V   | 2.8<br>V <sub>LDO2NOM</sub> + 0.250 | —<br>—                       | 4.5<br>4.5 | V    |
| V <sub>LDO2NOM</sub>       | Nominal output voltage  | —                                   | See <a href="#">Table 35</a> | —          | V    |
| I <sub>LDO2MAX</sub>       | Rated output load current, Normal mode  | 400                                 | —                            | —          | mA   |
| I <sub>LDO2MAXLPM</sub>    | Rated output load current, Low-power mode   | 10                                  | —                            | —          | mA   |
| V <sub>LDO2TOL</sub>       | Output voltage tolerance<br>V <sub>LDO2INMIN</sub> < V <sub>LDO2IN</sub> < 4.5 V<br>10.0 mA ≤ I <sub>LDO2</sub> < 400 mA<br>0.0 mA < I <sub>LDO2</sub> < 10 mA (Low-power mode)                                       | -2.0<br>-4.0                        | —<br>—                       | 2.0<br>4.0 | %    |
| I <sub>LDO2LIM</sub>       | Current limit<br>I <sub>LDO2</sub> when V <sub>LDO2</sub> is forced to V <sub>LDO2NOM</sub> /2  | 450                                 | 750                          | 1050       | mA   |
| I <sub>LDO2OCP</sub>       | LDO2FAULTI threshold (also used to disable LDO2 when REGSCPEN = 1)  | 450                                 | —                            | 1050       | mA   |
| I <sub>LDO2Q</sub>         | Quiescent Current (25 °C)<br>No load, change in I <sub>V<sub>SYS</sub></sub> and I <sub>V<sub>LDO2IN</sub></sub><br>When V <sub>LDO2</sub> enabled in Normal mode<br>When V <sub>LDO2</sub> enabled in Low-power mode | —<br>—                              | 15<br>1.5                    | —<br>—     | μA   |
| R <sub>DSON_QFN_LDO2</sub> | Dropout on resistance   | —                                   | —                            | 300        | mΩ   |

Table 14. LDO2 electrical characteristics...continued

| Symbol                           | Parameter  | Min    | Typ      | Max    | Unit |
|----------------------------------|--|--------|----------|--------|------|
| PSRR <sub>V<sub>LDO2</sub></sub> | PSRR<br>I <sub>LDO2</sub> = 200 mA, 20 Hz to 20 kHz<br>V <sub>LDO2</sub> = 3.30 V, V <sub>LDO2IN</sub> = 3.9 V, V <sub>SYST</sub> = 4.2 V                | —      | 60       | —      | dB   |
| t <sub>ONLDO2</sub>              | Turn on time<br>10 % to 90 % of end value<br>V <sub>LDO2INMIN</sub> < V <sub>LDO2IN</sub> ≤ 4.5 V, I <sub>LDO2</sub> = 0.0 mA                            | —      | 200      | 500    | μs   |
| R <sub>LDO2DIS</sub>             | Turn off discharge resistance  | —      | 250      | —      | Ω    |
| LDO2OUT <sub>OSHT</sub>          | Start-up overshoot (% of final value)<br>V <sub>LDO2INMIN</sub> < V <sub>LDO2IN</sub> ≤ 4.5 V, I <sub>LDO2</sub> = 0.0 mA                                | —      | 1.0      | 2.0    | %    |
| V <sub>LDO2LOTR</sub>            | Transient load response<br>V <sub>LDO2INMIN</sub> < V <sub>LDO2IN</sub> ≤ 4.5 V, I <sub>LDO2</sub> = 10 mA to 100 mA in 10 μs<br>Overshoot<br>Undershoot | —<br>— | 50<br>50 | —<br>— | mV   |

5.3.6 Electrical characteristics – LDO3

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYST</sub> = 2.5 to 4.5 V, V<sub>LDO3IN</sub> = 3.6 V, V<sub>LDO3[4:0]</sub> = 11111, I<sub>LDO3</sub> = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>SYST</sub> = 3.6 V, V<sub>LDO3IN</sub> = 3.6 V, V<sub>LDO3[4:0]</sub> = 11111, I<sub>LDO3</sub> = 10 mA, and 25 °C, unless otherwise noted.

Table 15. LDO3 electrical characteristics

| Symbol                     | Parameter   | Min                       | Typ                          | Max                    | Unit |
|----------------------------|---|---------------------------|------------------------------|------------------------|------|
| V <sub>LDO3IN</sub>        | Operating input voltage<br>V <sub>LDO3</sub> + 250 mV ≤ V <sub>SYST</sub> ≤ 4.5 V   | 1.0                       | —                            | 4.5                    | V    |
| V <sub>LDO3NOM</sub>       | Nominal output voltage  | —                         | See <a href="#">Table 33</a> | —                      | V    |
| I <sub>LDO3MAX</sub>       | Rated output load current, Normal mode  | 300                       | —                            | —                      | mA   |
| I <sub>LDO3MAXLPM</sub>    | Rated output load current, Low-power mode   | 10                        | —                            | —                      | mA   |
| V <sub>LDO3TOL</sub>       | Output voltage tolerance, Normal mode<br>V <sub>LDO3INMIN</sub> < V <sub>LDO3IN</sub> < 4.5 V, 0 mA < I <sub>LDO3</sub> < 300 mA<br>0.8 V ≤ V <sub>LDO3</sub> < 1.8 V<br>1.8 V ≤ V <sub>LDO3</sub> ≤ 3.3 V<br>V <sub>LDO3INMIN</sub> < V <sub>LDO3IN</sub> < 4.5 V, 0 mA < I <sub>LDO3</sub> < 10 mA (Low-power mode) | —<br>-2.5<br>-2.5<br>-4.0 | —<br>—<br>—<br>—             | —<br>2.5<br>2.5<br>4.0 | %    |
| I <sub>LDO3LIM</sub>       | Current limit<br>I <sub>LDO3</sub> when V <sub>LDO3</sub> is forced to V <sub>LDO3NOM</sub> /2  | 320                       | —                            | 1000                   | mA   |
| I <sub>LDO3OCP</sub>       | LDO3FAULTI threshold (also used to disable LDO3 when REGSCPEN = 1)  | 320                       | —                            | 1000                   | mA   |
| I <sub>LDO3Q</sub>         | Quiescent current (at 25 °C)<br>No load, change in I <sub>VSYST</sub> and I <sub>VLDO3IN</sub><br>When LDO3 enabled in Normal mode<br>When LDO3 enabled in Low-power mode   | —<br>—                    | 17<br>2.5                    | —<br>—                 | μA   |
| R <sub>DSON_QFN_LDO3</sub> | Dropout on resistance   | —                         | —                            | 350                    | mΩ   |

Table 15. LDO3 electrical characteristics...continued

| Symbol                         | Parameter  | Min    | Typ      | Max    | Unit |
|--------------------------------|--|--------|----------|--------|------|
| PSRR <sub>LDO3</sub>           | PSRR<br>I <sub>LDO3</sub> = 150 mA, 20 Hz to 20 kHz<br>V <sub>LDO3</sub> = 3.30 V, V <sub>LDO3IN</sub> = 3.8 V, V <sub>SYS</sub> = 4.2 V                 | —      | 56       | —      | dB   |
| TR <sub>V<sub>LDO3</sub></sub> | Turn on time<br>10 % to 90 % of end value<br>V <sub>LDO3INMIN</sub> < V <sub>LDO3IN</sub> < 4.5 V, I <sub>LDO3</sub> = 0.0 mA                            | —      | 200      | 500    | µs   |
| R <sub>LDO3DIS</sub>           | Turn off discharge resistance  | —      | 250      | —      | Ω    |
| LDO3OUT <sub>OSHT</sub>        | Start-up overshoot (% of final value)<br>V <sub>LDO3INMIN</sub> < V <sub>LDO3IN</sub> ≤ 4.5 V, I <sub>LDO3</sub> = 0.0 mA                                | —      | 1.0      | 2.0    | %    |
| V <sub>LDO3LOTR</sub>          | Transient load response<br>V <sub>LDO3INMIN</sub> < V <sub>LDO3IN</sub> ≤ 4.5 V, I <sub>LDO3</sub> = 10 mA to 100 mA in 10 µs<br>Overshoot<br>Undershoot | —<br>— | 50<br>50 | —<br>— | mV   |

### 5.3.7 Electrical characteristics – VREFDDR

T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = 2.5 to 4.5 V, I<sub>REFDDR</sub> = 0.0 mA, V<sub>INREFDDR</sub> = 1.35 V and typical external component values, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = 3.6 V, I<sub>REFDDR</sub> = 0.0 mA, V<sub>INREFDDR</sub> = 1.35 V, and 25 °C, unless otherwise noted.

Table 16. VREFDDR electrical characteristics

| Symbol                           | Parameter   | Min   | Typ                      | Max   | Unit |
|----------------------------------|---|-------|--------------------------|-------|------|
| V <sub>INREFDDR</sub>            | Operating input voltage range   | 0.9   | —                        | 1.8   | V    |
| V <sub>REFDDR</sub>              | Output voltage, 0.9 V < V <sub>INREFDDR</sub> < 1.8 V, 0 mA < I <sub>REFDDR</sub> < 10 mA   | —     | V <sub>INREFDDR</sub> /2 | —     | V    |
| V <sub>REFDDRTOL</sub>           | Output voltage tolerance, as a percentage of V <sub>INREFDDR</sub> , 1.2 V < V <sub>INREFDDR</sub> < 1.65 V, 0 mA < I <sub>REFDDR</sub> < 10 mA | 49.25 | 50                       | 50.75 | %    |
| I <sub>REFDDRQ</sub>             | Quiescent current (at 25 °C)  | —     | 1.1                      | —     | µA   |
| I <sub>REFDDR<sub>LM</sub></sub> | Current limit, I <sub>REFDDR</sub> when V <sub>REFDDR</sub> is forced to V <sub>INREFDDR</sub> /4   | 10.5  | 24                       | 38    | mA   |
| t <sub>ONREFDDR</sub>            | Turn on time, 10 % to 90 % of end value, V <sub>INREFDDR</sub> = 1.2 V to 1.65 V, I <sub>REFDDR</sub> = 0.0 mA                                  | —     | —                        | 100   | µs   |

### 5.3.8 Electrical characteristics – VSNVS

All parameters are specified at T<sub>A</sub> = -40 to 105 °C, V<sub>SYS</sub> = 3.6 V, V<sub>SNVS</sub> = 3.0 V, I<sub>SNVS</sub> = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at V<sub>SYS</sub> = 3.6 V, V<sub>SNVS</sub> = 3.0 V, I<sub>SNVS</sub> = 5.0 µA, and 25 °C, unless otherwise noted.

Table 17. VSNVS electrical characteristics

| Symbol              | Parameter  | Min         | Typ    | Max        | Unit |
|---------------------|--|-------------|--------|------------|------|
| V <sub>SNVSIN</sub> | Operating input voltage<br>Valid coin cell range<br>Valid V <sub>SYS</sub> | 1.8<br>2.45 | —<br>— | 3.3<br>4.5 | V    |

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Table 17. VSNVS electrical characteristics...continued

| Symbol                | Parameter  | Min                                    | Typ           | Max            | Unit |
|-----------------------|--|--|---------------|----------------|------|
| I <sub>SNVS</sub>     | Operating load current<br>V <sub>SNVSINMIN</sub> < V <sub>SNVSIN</sub> < V <sub>SNVSINMAX</sub>  | 2000                                   | —             | —              | μA   |
| V <sub>TL1</sub>      | VSYS threshold (VSYS powered to coin cell powered)   | —                                      | UVDET failing | —              | V    |
| V <sub>TH1</sub>      | VSYS threshold (coin cell powered to VSYS powered)   | —                                      | UVDET rising  | —              | V    |
| V <sub>SNVS</sub>     | Output voltage (when running from VSYS)<br>0 μA < I <sub>SNVS</sub> < 2000 μA<br>Output voltage (when running from LICELL)<br>0 μA < I <sub>SNVS</sub> < 2000 μA<br>2.84 V < V <sub>COIN</sub> < 3.3 V | -7.0 %<br><br>V <sub>COIN</sub> - 0.20 | 3.0<br><br>—  | 7.0 %<br><br>— | V    |
| V <sub>SNVSDROP</sub> | Dropout voltage<br>VSYS = 2.9 V<br>I <sub>SNVS</sub> = 2000 μA   | —                                      | —             | 220            | mV   |
| I <sub>SNVSLIM</sub>  | Current limit<br>VSYS > V <sub>TH1</sub>   | 5200                                   | —             | 24000          | μA   |
| V <sub>SNVSTON</sub>  | Turn on time (load capacitor, 0.47 μF)<br>10 % to 90 % of final value V <sub>SNVS</sub><br>V <sub>COIN</sub> = 0.0 V, I <sub>SNVS</sub> = 0 μA   | —                                      | —             | 3.0            | ms   |
| V <sub>SNVSOSH</sub>  | Start-up overshoot<br>I <sub>SNVS</sub> = 5.0 μA<br>dVSYS/dt = 50 mV/μs  | —                                      | 40            | 70             | mV   |
| R <sub>DSONSNVS</sub> | Internal switch R <sub>DS(on)</sub><br>V <sub>COIN</sub> = 2.6 V   | —                                      | —             | 100            | Ω    |

## 5.3.9 Electrical characteristics – IC level bias currents

All parameters are specified at 25 °C, VSYS = 3.6 V, VIN = 0 V, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V<sub>SNVS</sub> = 3.0 V, and 25 °C, unless otherwise noted.

Table 18. IC level electrical characteristics

| Mode      | PF1510 conditions  | System conditions                                  | Typ  | Max | Unit |
|-----------|--|--|------|-----|------|
| Coin cell | VSNVS from LICELL<br>All other blocks off<br>VSYS = 0.0 V  | No load on VSNVS                                   | 1.5  | 4.0 | μA   |
| CORE_OFF  | VSNVS from VSYS<br>Wake-up from ONKEY active<br>All other blocks off<br>VSYS > UVDET   | No load on VSNVS,<br>PMIC able to wake-up          | 1.5  | 4.0 | μA   |
| Sleep     | VSNVS from VSYS<br>Wake-up from PWRON active<br>Trimmed reference active<br>DDR I/O rail in Low-power mode<br>VREFDDR disabled | No load on VSNVS.<br>DDR memories in self refresh. | 12.5 | 25  | μA   |

Table 18. IC level electrical characteristics...continued

| Mode            | PF1510 conditions   | System conditions   | Typ | Max | Unit |
|-----------------|---|---|-----|-----|------|
| Standby/Suspend | VSNVS from either VSYS or LICELL<br>SW1 in ultra Low-power mode<br>SW2 in ultra Low-power mode<br>SW3 in ultra Low-power mode<br>Trimmed reference active<br>VLDO1 is disabled<br>VLDO2 enabled in Low-power mode<br>VLDO3 enabled in Low-power mode<br>VREFDDR enabled | No load on VSNVS.<br>Processor enabled in Low-power mode. | 23  | 46  | μA   |
| REGS_DISABLE    | VSNVS from VSYS<br>Wake-up from ONKEY active<br>Other blocks are off<br>VSYS > UVDET  | No load on VSNVS,<br>PMIC able to wake-up                 | 14  | 20  | μA   |

## 6 Detailed description

The PF1510 PMIC features three high efficiency low quiescent current buck regulators, three LDO regulators, a DDR voltage reference to supply voltages for the application processor and peripheral devices.

The buck regulators provide the supply to processor cores and to other low voltage circuits such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores for power optimization.

The three LDO regulators are general purpose to power various processor rails, system connectivity devices and/or peripherals. Depending on the system power configuration, the general purpose LDO regulators can be directly supplied from the main system supply VSYS or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN.

A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operation.

The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS (Secure Non-Volatile Storage)/RTC (Real Time Clock) circuitry on the processor. VSNVS is powered from VSYS or from a coin cell.

The PF1510 uses an integrated linear front-end LDO that provides 4.5 V at VSYS from the 5.0 V VIN.

Table 19. Voltage regulators

| Supply    | Output voltage (V)          | Programming step size (mV) | Load current (mA) |
|-----------|-----------------------------|----------------------------|-------------------|
| SW1 / SW2 | 0.60 to 1.3875 / 1.1 to 3.3 | 12.5/variable              | 1000              |
| SW3       | 1.80 to 3.30                | 100                        | 1000              |
| LDO1      | 0.75 to 1.50                | 50                         | 300               |
|           | 1.80 to 3.30                | 100                        |                   |
| LDO2      | 1.80 to 3.30                | 100                        | 400               |

Table 19. Voltage regulators...continued

| Supply  | Output voltage (V)           | Programming step size (mV) | Load current (mA) |
|---------|------------------------------|----------------------------|-------------------|
| LDO3    | 0.75 to 1.50<br>1.80 to 3.30 | 50<br>100                  | 300               |
| USBPHY  | 3.3 or 4.9                   | —                          | 60                |
| VSNVS   | 3.0                          | N/A                        | 2                 |
| VREFDDR | 0.5*VINREFDDR                | N/A                        | 10                |

## 6.1 Buck regulators

The PF1510 features three high efficiency buck regulators with internal compensation. Each buck regulator is capable of meeting optimum power efficiency operation using reduced power variable-frequency pulse skip switching scheme at light loads as well as operating in forced PWM quasi-fixed frequency switching mode at higher loads. The switching regulator controller combines the advantages of hysteretic and voltage mode control which provides outstanding load regulation and transient response, low output ripple voltage and seamless transition between pulse-skip mode and Active Quasi-fixed frequency switching mode. The control circuitry includes an AC loop which senses the output voltage (at SWx<sub>FB</sub> pin) and directly feeds it to a fast comparator stage. This comparator sets the switching frequency, which is almost constant for steady state operating conditions. It also provides immediate response to dynamic load changes.

In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The transition into and out of low power pulse-skip switching mode takes place automatically according to the load current to maintain optimum power efficiency. Additionally, further power savings through cutting the buck circuitry quiescent current can be achieved by activating a Low-power mode upon entering either STANDBY or SLEEP PMIC power mode or as commanded via I<sup>2</sup>C control bits. In SW1 and SW2. An OTP option enables or disables DVS in the regulators. When DVS is disabled and the low-power bit is set, the regulator enters an Ultra Low Power (ULP) mode cuts the operating quiescent current even in order to reach extremely low standby power levels needed for ultra low power processors such as that from Kinetis K and L series.

As indicated above, the buck controller supports PWM (Pulse Width Modulation) mode for medium and high load conditions and low-power variable-frequency pulse skip mode at light loads. During high current mode, it operates in continuous conduction and the switching frequency is up to 2.0 MHz with a controlled on-time variation depending on the input voltage and output voltage. If the load current decreases, the converter seamlessly enters the pulse-skip mode to cut the operating quiescent current and maintain high efficiency down to very light loads. In pulse-skip mode the switching frequency varies linearly with the load current. Since the controller supports both power modes within one single building block, the transition from normal power mode to lower power pulse-skip mode and vice versa is seamless without dramatic effects on the output voltage.

In the adopted pulse-skip scheme, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a non-switching (pause) period where most of the internal circuits are shutdown to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the pause period depends on the load current and the inductor peak current.

## 6.2 SW1 and SW2 detailed description

SW1 and SW2 are identical buck regulators designed to carry a nominal load current of 1.0 A. Detailed characteristics and features of SW1 and SW2 are described in this section. Being identical, reference is made only to SWx though the same specifications apply to SW1 and SW2.

### 6.2.1 SWx dynamic voltage scaling description

SWx integrates an optional DVS circuit that is enabled via OTP. To reduce overall power consumption, when DVS is enabled SWx output voltage can be varied depending on the mode or activity level of the processor.

- **Normal operation:**

The output voltage is selected by I<sup>2</sup>C bits SWx\_VOLT[5:0]. A voltage transition initiated by I<sup>2</sup>C is governed by the SWx\_DVSSPEED I<sup>2</sup>C bit as shown in [Table 20](#).

- **Standby mode:**

The output voltage can be selected by I<sup>2</sup>C bits SWx\_STBY\_VOLT[5:0]. Voltage transitions initiated by a Standby event are governed by the SWx\_DVSSPEED I<sup>2</sup>C bit as shown in [Table 20](#). This applies only when DVS is enabled.

- **Sleep mode:**

The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I<sup>2</sup>C bits SWx\_SLP\_VOLT[5:0]. Voltage transitions initiated by a turn off event are governed by the SWx\_DVSSPEED I<sup>2</sup>C bit for SWx as shown in [Table 20](#). This applies only when DVS is enabled.

As shown in [Figure 5](#), during a falling DVS transition, dv/dt of the output voltage depends on the load current. Setting the SWx\_FPWM\_IN\_DVS bit forces the regulator in the FPWM mode during the falling transition allowing it to accurately track the DVS reference removing the load dependency. The SWx\_FPWM\_IN\_DVS bit is active only when OTP\_SWx\_DVS\_SEL = 0.

Table 20. SWx DVS setting selection

| SWx_DVS speed | Function                 |
|---------------|--------------------------|
| 0             | 12.5 mV step each 2.0 μs |
| 1             | 12.5 mV step each 4.0 μs |

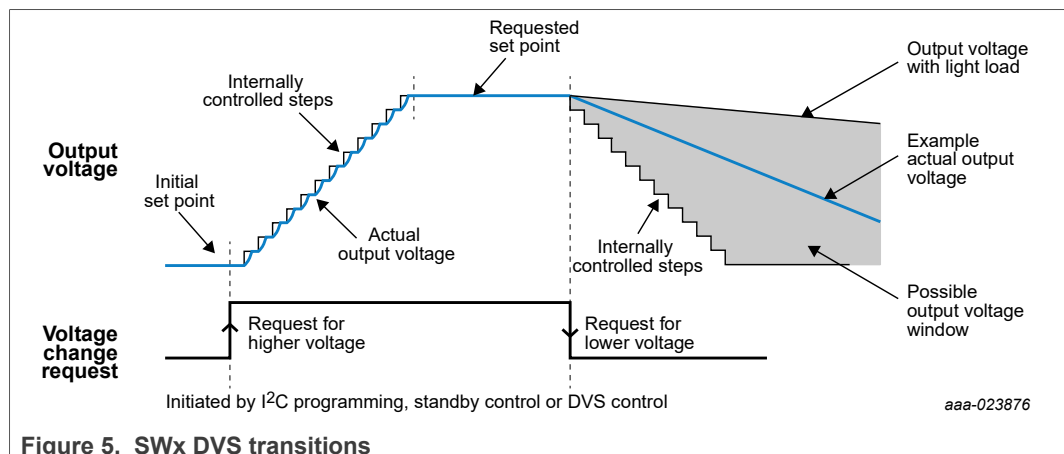


Figure 5. SWx DVS transitions



### 6.2.2 SWx DVS and non-DVS operation

SWx has two distinct modes of operation selectable via OTP:

- DVS enabled: a DVS reference is activated and output accuracy of the regulator is tight at the cost of slightly higher quiescent current. See [Section 5.3 "Electrical characteristics"](#) for details. In [Figure 6](#), **DVS FB** and **DVS REF** are enabled via OTP for this mode of operation.
- DVS disabled: the regulator operates as a traditional buck converter with a fixed reference and soft-start. The quiescent current in this mode is lower at the cost of output accuracy and transient response. See [Section 5.3 "Electrical characteristics"](#) for details. In [Figure 6](#), **VREF FB** and **VREF** are enabled via OTP for this mode of operation.

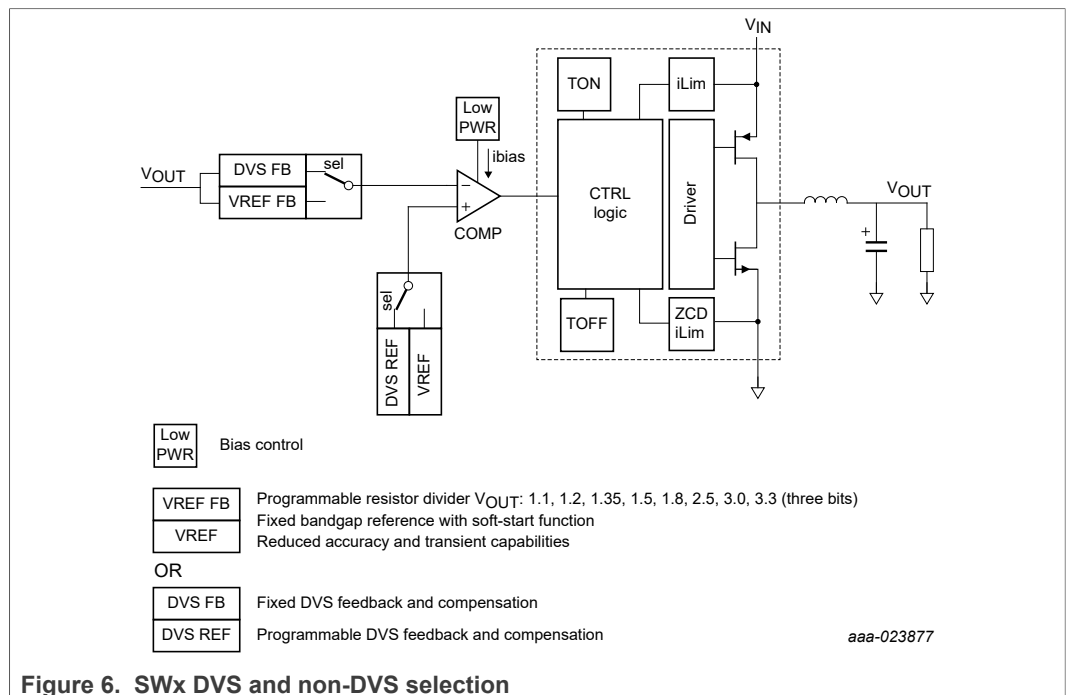


Figure 6. SWx DVS and non-DVS selection

### 6.2.3 Regulator control

To improve system efficiency, the buck regulators can operate in different switching/bias modes. The changing between DCM (Discontinuous Conduction Mode)/CCM (Continuous Conduction Mode) takes place automatically based on detecting the load current level. It can be enforced by one of the following means: I<sup>2</sup>C programming, exiting/entering the Standby mode, exiting/entering Sleep/Low-power mode.

Available modes for buck regulators are presented in [Table 21](#). These switching modes are available with OTP\_SWx\_DVS\_SEL = 0 and OTP\_SWx\_DVS\_SEL = 1. [Table 22](#) shows the bit settings for operating the buck converter in these modes based on the PMIC operating state.

Table 21. Buck regulator operating modes

| Mode | Description  |
|------|--|
| OFF  | The regulator is switched off and the output voltage is discharged using an internal resistor. |

Table 21. Buck regulator operating modes...continued

| Mode      | Description   |
|-----------|---|
| Adaptive  | This is the default mode of operation of the buck regulator. In this mode, the regulator operates in a quasi-fixed frequency switching mode at moderate and high loads, with pulse skip (variable switching frequency) scheme at light load for optimized efficiency.   |
| F-PWM     | In this mode, the regulator is always in PWM mode operation regardless of load conditions.  |
| Low-power | To further extend power savings when the load current is minimal, this mode cuts the quiescent current of the buck converter by reducing the bias to the comparator. The regulator is operated in low power modes (Standby and/or Sleep) with the proper I <sup>2</sup> C setting. See <a href="#">Table 22</a> . |

The following table shows actions to control different bits for SW1 and SW2.

Table 22. Buck mode control

| PMIC state        | SWx_EN | SWx_STBY | SWx_OMODE | SWx_LPWR | SWx_FPWM | SWx operating mode                              |
|-------------------|--------|----------|-----------|----------|----------|---|
| Run/Standby/Sleep | 0      | X        | X         | X        | X        | SW disabled                                     |
| Run               | 1      | X        | X         | 0        | 0        | SW enabled. Operates in DCM at light loads      |
| Run               | 1      | X        | X         | 0        | 1        | SW enabled. Forced PWM mode                     |
| Run               | 1      | X        | X         | 1        | 0        | SW Enabled. Does not operate in Low-power mode. |
| Run               | 1      | X        | X         | 1        | 1        | SW enabled. Forced PWM mode                     |
| Standby           | 1      | 0        | X         | X        | X        | SW disabled                                     |
| Standby           | 1      | 1        | X         | 0        | 0        | SW enabled. Operates in DCM at light loads.     |
| Standby           | 1      | 1        | X         | 0        | 1        | SW enabled. Forced PWM mode.                    |
| Standby           | 1      | 1        | X         | 1        | 0        | SW enabled. Operates in Low-power mode.         |
| Standby           | 1      | 1        | X         | 1        | 1        | SW enabled. Forced PWM mode                     |
| Sleep             | 1      | X        | 0         | X        | X        | SW disabled                                     |
| Sleep             | 1      | X        | 1         | 0        | 0        | SW enabled. Operates in DCM at light loads.     |
| Sleep             | 1      | X        | 1         | 0        | 1        | SW enabled. Forced PWM mode.                    |
| Sleep             | 1      | X        | 1         | 1        | 0        | SW enabled. Operates in Low-power mode.         |
| Sleep             | 1      | X        | 1         | 1        | 1        | SW enabled. Forced PWM mode                     |

### 6.2.4 Current limit protection

SWx features high and low-side FET current limit. When current through the FETs goes above their respective thresholds, the FET is turned off to prevent further increase in current.

The protection is enabled in a cycle-by-cycle mode. Hitting either current limit sets the corresponding interrupt sense bits. If the faults persist for longer than the 8.0 ms debounce time, the interrupt status bit is set.

### 6.2.5 Output voltage setting in SWx

Output voltage of SWx is programmable via OTP. During startup (REGS\_DISABLE mode to RUN mode), contents of the OTP\_SWx\_VOLT[5:0] are mapped into the SWx\_VOLT[5:0], SWx\_STBY\_VOLT[5:0] and SWx\_SLP\_VOLT[5:0] register which set the regulator output voltage during Run, Standby and Sleep modes respectively.

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In the DVS enabled mode (OTP\_SWx\_DVS\_SEL = 0), values of SWx\_VOLT[5:0], SWx\_STBY[VOLT[5:0] and SWx\_SLP\_VOLT[5:0] can be changed via I<sup>2</sup>C after the PMIC starts up (RESETBMCU is released).

In the DVS disabled mode (OTP\_SWx\_DVS\_SEL = 1), value of SWx\_VOLT[5:0], SWx\_STBY[VOLT[5:0] and SWx\_SLP\_VOLT[5:0] are read-only and must not be written to.

Table 23. SW1 and SW2 output voltage setting

| Set point | SWx_VOLT[5:0]<br>SWx_STBY_VOLT[5:0]<br>SWx_SLP_VOLT[5:0] | Output voltage<br>with DVS enabled<br>OTP_SWx_DVS_SEL = 0 | Output voltage<br>with DVS disabled<br>OTP_SWx_DVS_SEL = 1 |
|-----------|--|---|--|
| 0         | 000000   | 0.6000  | 1.10   |
| 1         | 000001   | 0.6125  | 1.20   |
| 2         | 000010   | 0.6250  | 1.35   |
| 3         | 000011   | 0.6375  | 1.50   |
| 4         | 000100   | 0.6500  | 1.80   |
| 5         | 000101   | 0.6625  | 2.50   |
| 6         | 000110   | 0.6750  | 3.00   |
| 7         | 000111   | 0.6875  | 3.30   |
| 8         | 001000   | 0.7000  | 3.30   |
| 9         | 001001   | 0.7125  | 3.30   |
| 10        | 001010   | 0.7250  | 3.30   |
| 11        | 001011   | 0.7375  | 3.30   |
| 12        | 001100   | 0.7500  | 3.30   |
| 13        | 001101   | 0.7625  | 3.30   |
| 14        | 001110   | 0.7750  | 3.30   |
| 15        | 001111   | 0.7875  | 3.30   |
| 16        | 010000   | 0.8000  | 3.3  |
| 17        | 010001   | 0.8125  | 3.30   |
| 18        | 010010   | 0.8250  | 3.30   |
| 19        | 010011   | 0.8375  | 3.30   |
| 20        | 010100   | 0.8500  | 3.30   |
| 21        | 010101   | 0.8625  | 3.30   |
| 22        | 010110   | 0.8750  | 3.30   |
| 23        | 010111   | 0.8875  | 3.30   |
| 24        | 011000   | 0.9000  | 3.30   |
| 25        | 011001   | 0.9125  | 3.30   |
| 26        | 011010   | 0.9250  | 3.30   |
| 27        | 011011   | 0.9375  | 3.30   |
| 28        | 011100   | 0.9500  | 3.30   |

Table 23. SW1 and SW2 output voltage setting...continued

| Set point | SW <sub>x</sub> _VOLT[5:0]<br>SW <sub>x</sub> _STBY_VOLT[5:0]<br>SW <sub>x</sub> _SLP_VOLT[5:0] | Output voltage<br>with DVS enabled<br>OTP_SW <sub>x</sub> _DVS_SEL = 0 | Output voltage<br>with DVS disabled<br>OTP_SW <sub>x</sub> _DVS_SEL = 1 |
|-----------|---|--|---|
| 29        | 011101  | 0.9625   | 3.30  |
| 30        | 011110  | 0.9750   | 3.30  |
| 31        | 011111  | 0.9875   | 3.30  |
| 32        | 100000  | 1.0000   | 3.30  |
| 33        | 100001  | 1.0125   | 3.30  |
| 34        | 100010  | 1.0250   | 3.30  |
| 35        | 100011  | 1.0375   | 3.30  |
| 36        | 100100  | 1.0500   | 3.30  |
| 37        | 100101  | 1.0625   | 3.30  |
| 38        | 100110  | 1.0750   | 3.30  |
| 39        | 100111  | 1.0875   | 3.30  |
| 40        | 101000  | 1.1000   | 3.30  |
| 41        | 101001  | 1.1125   | 3.30  |
| 42        | 101010  | 1.125  | 3.30  |
| 43        | 101011  | 1.1375   | 3.30  |
| 44        | 101100  | 1.1500   | 3.30  |
| 45        | 101101  | 1.1625   | 3.30  |
| 46        | 101110  | 1.1750   | 3.30  |
| 47        | 101111  | 1.1875   | 3.30  |
| 48        | 110000  | 1.2000   | 3.30  |
| 49        | 110001  | 1.2125   | 3.30  |
| 50        | 110010  | 1.2250   | 3.30  |
| 51        | 110011  | 1.2375   | 3.30  |
| 52        | 110100  | 1.2500   | 3.30  |
| 53        | 110101  | 1.2625   | 3.30  |
| 54        | 110110  | 1.2750   | 3.30  |
| 55        | 110111  | 1.2875   | 3.30  |
| 56        | 111000  | 1.3000   | 3.30  |
| 57        | 111001  | 1.3125   | 3.3   |
| 58        | 111010  | 1.3250   | 3.30  |
| 59        | 111011  | 1.3375   | 3.30  |
| 60        | 111100  | 1.3500   | 3.30  |
| 61        | 111101  | 1.3625   | 3.30  |
| 62        | 111110  | 1.3750   | 3.30  |
| 63        | 111111  | 1.3875   | 3.30  |

6.2.6 SWx external components

Table 24 shows the combination of inductor and capacitor values that work with the SWx regulator.

The design is optimized for a 1.0 μH inductor.

Table 24. Acceptable inductance and capacitance values

|                          |           |
|--------------------------|-----------|
| Inductance / capacitance | 2 x 10 μF |
| 1.0 μH                   |           |

Table 25 and Table 26 show example inductor and capacitor part numbers respectively.

Table 25. Example inductor part numbers

| Part number | Size (mm) | 1.0 μH        |
|-------------|-----------|---------------|
| DFE201610E  | 2.0 x 1.6 | 57 mΩ, 3.6 A  |
| DFE201610P  | 2.0 x 1.6 | 70 mΩ, 3.1 A  |
| DFE201210U  | 2.0 x 1.2 | 95 mΩ, 3.1 A  |
| DFE160810S  | 1.6 x 0.8 | 120 mΩ, 2.0 A |
| DFE201208S  | 2.0 x 1.2 | 86 mΩ, 2.4 A  |
| DFE160808S  | 1.6 x 0.8 | 144 mΩ, 1.9 A |

Table 26. Example capacitor part numbers

| Murata part number | Description                     |
|--------------------|---------------------------------|
| GRM188R60J106ME47D | 6.3 V, 10 μF, 0402, X5R         |
| GRM188D70J106MA73  | 6.3 V, 10 μF, 0402, X7R         |
| GRM188R61A106KE69  | 10 μF 10 V 10 % X5R 0603 .95 mm |
| GRM219R61A106KE44  | 10 μF 10 V 10 % X5R 0805 .95 mm |

6.3 SW3 detailed description

SW3 is a buck regulator designed to carry a nominal load current of 1.0 A. The output voltage is programmable from 1.8 V to 3.3 V in 100 mV steps. Dynamic voltage scaling is not supported in this regulator.

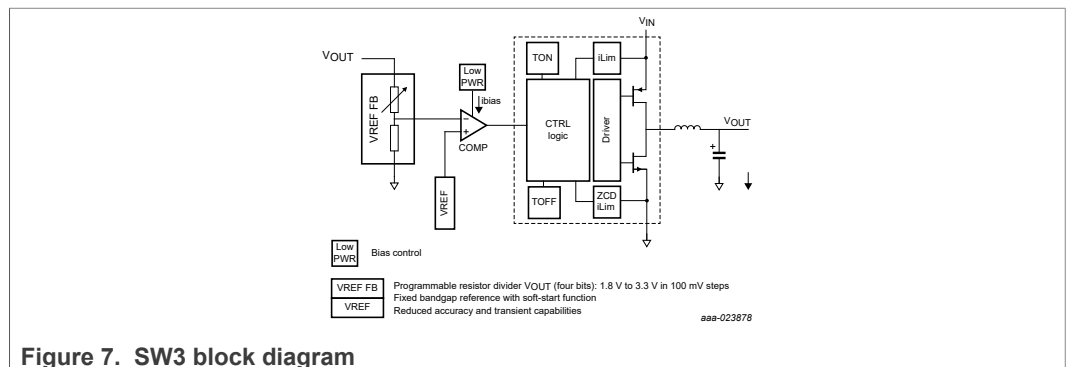


Figure 7. SW3 block diagram

### 6.3.1 Regulator control

To improve system efficiency the buck regulator can operate in different switching/ bias modes. The changing between DCM/CCM takes place automatically based on detecting the load current level. It can be enforced by one of the following means: I<sup>2</sup>C programming, exiting/entering the Standby mode, exiting/entering Sleep/ Low-power mode.

Available modes for buck regulators are presented in [Table 27](#).

[Table 28](#) shows the bit settings for operating the buck converter in these modes based on the PMIC operating state.

**Table 27. SW3 buck regulator operating modes**

| Mode      | Description   |
|-----------|---|
| OFF       | The regulator is switched off and the output voltage is discharged using an internal resistor.  |
| Adaptive  | This is the default mode of operation of the buck regulator. In this mode, the regulator operates in a quasi-fixed frequency switching mode at moderate and high loads, with pulse skip (variable switching frequency) scheme at light load for optimized efficiency.   |
| F-PWM     | In this mode, the regulator is always in PWM mode operation regardless of load conditions.  |
| Low-power | To further extend power savings when the load current is minimal, this mode cuts the quiescent current of the buck converter by reducing the bias to the comparator. The regulator is operated in low power modes (Standby and/or Sleep) with the proper I <sup>2</sup> C setting. See <a href="#">Table 28</a> . |

**Table 28. SW3 buck mode control**

| PMIC state                | SW3_EN | SW3_STBY | SW3_OMODE | SW3_LPWR | SW3_FPWM | SW3 operating mode                               |
|---------------------------|--------|----------|-----------|----------|----------|--|
| Run/<br>Standby/<br>Sleep | 0      | X        | X         | X        | X        | SW disabled                                      |
| Run                       | 1      | X        | X         | 0        | 0        | SW enabled<br>Operates in DCM at light loads     |
| Run                       | 1      | X        | X         | 0        | 1        | SW enabled<br>Forced PWM mode                    |
| Run                       | 1      | X        | X         | 1        | 0        | SW enabled<br>Does not operate in Low-power mode |
| Run                       | 1      | X        | X         | 1        | 1        | SW enabled<br>Forced PWM mode                    |
| Standby                   | 1      | 0        | X         | X        | X        | SW disabled                                      |
| Standby                   | 1      | 1        | X         | 0        | 0        | SW enabled<br>Operates in DCM at light loads     |
| Standby                   | 1      | 1        | X         | 0        | 1        | SW enabled<br>Forced PWM mode                    |

Table 28. SW3 buck mode control...continued

| PMIC state | SW3_EN | SW3_STBY | SW3_OMODE | SW3_LPWR | SW3_FPWM | SW3 operating mode                           |
|------------|--------|----------|-----------|----------|----------|--|
| Standby    | 1      | 1        | X         | 1        | 0        | SW enabled<br>operates in Low-power mode     |
| Standby    | 1      | 1        | X         | 1        | 1        | SW enabled<br>Forced PWM mode                |
| Sleep      | 1      | X        | 0         | X        | X        | SW disabled                                  |
| Sleep      | 1      | X        | 1         | 0        | 0        | SW enabled<br>Operates in DCM at light loads |
| Sleep      | 1      | X        | 1         | 0        | 1        | SW enabled<br>Forced PWM mode                |
| Sleep      | 1      | X        | 1         | 1        | 0        | SW enabled<br>Operates in Low-power mode     |
| Sleep      | 1      | X        | 1         | 1        | 1        | SW enabled<br>Forced PWM mode                |

### 6.3.2 Current limit protection

SW3 features high and low-side FET current limit. When current through the FETs goes above their respective thresholds, the FET is turned off to prevent further increase in current.

The protection is enabled in a cycle-by-cycle mode. Hitting either current limit sets the corresponding interrupt sense bits. If the faults persist for longer than the 8.0 ms debounce time, the interrupt status bit is set.

### 6.3.3 Output voltage setting in SW3

Output voltage of SW3 is programmable via OTP. During start up (REGS\_DISABLE mode to RUN mode), contents of the OTP\_SW3\_VOLT[5:0] are mapped into the SW3\_VOLT[5:0], SW3\_STBY\_VOLT[5:0] and SW3\_SLP\_VOLT[5:0] register which set the regulator output voltage during Run, Standby and Sleep modes respectively.

Values of SW3\_VOLT[5:0], SW3\_STBY\_VOLT[5:0] and SW3\_SLP\_VOLT[5:0] are read-only and cannot be written to.

Table 29. SW3 output voltage setting

| Set point | SW3_VOLT[3:0]<br>SW3_STBY_VOLT[3:0]<br>SW3_SLP_VOLT[3:0] | Output voltage (V) |
|-----------|--|--------------------|
| 0         | 0000   | 1.80               |
| 1         | 0001   | 1.90               |
| 2         | 0010   | 2.00               |
| 3         | 0011   | 2.10               |
| 4         | 0100   | 2.20               |
| 5         | 0101   | 2.30               |

Table 29. SW3 output voltage setting...continued

| Set point | SW3_VOLT[3:0]<br>SW3_STBY_VOLT[3:0]<br>SW3_SLP_VOLT[3:0] | Output voltage (V) |
|-----------|--|--------------------|
| 6         | 0110   | 2.40               |
| 7         | 0111   | 2.50               |
| 8         | 1000   | 2.60               |
| 9         | 1001   | 2.70               |
| 10        | 1010   | 2.80               |
| 11        | 1011   | 2.90               |
| 12        | 1100   | 3.00               |
| 13        | 1101   | 3.10               |
| 14        | 1110   | 3.20               |
| 15        | 1111   | 3.30               |

### 6.3.4 SW3 external components

[Table 30](#) shows the combination of inductor and capacitor values that work with the SW3 regulator.

Table 30. Acceptable inductance and capacitance values

|                          |                |
|--------------------------|----------------|
| Inductance / capacitance | 2 x 10 $\mu$ F |
| 1.0 $\mu$ H              |                |

[Table 31](#) and [Table 32](#) show example inductor and capacitor part numbers respectively.

Table 31. Example inductor part numbers

| Part number | Size (mm) | 1.0 $\mu$ H            |
|-------------|-----------|------------------------|
| DFE201610E  | 2.0 x 1.6 | 57 m $\Omega$ , 3.6 A  |
| DFE201610P  | 2.0 x 1.6 | 70 m $\Omega$ , 3.1 A  |
| DFE201210U  | 2.0 x 1.2 | 95 m $\Omega$ , 3.1 A  |
| DFE160810S  | 1.6 x 0.8 | 120 m $\Omega$ , 2.0 A |
| DFE201208S  | 2.0 x 1.2 | 86 m $\Omega$ , 2.4 A  |
| DFE160808S  | 1.6 x 0.8 | 144 m $\Omega$ , 1.9 A |

Table 32. Example capacitor part numbers

| Murata part number | Description                          |
|--------------------|--------------------------------------|
| GRM188R60J106ME47D | 6.3 V, 10 $\mu$ F, 0402, X5R         |
| GRM188D70J106MA73  | 6.3 V, 10 $\mu$ F, 0402, X7R         |
| GRM188R61A106KE69  | 10 $\mu$ F 10 V 10 % X5R 0603 .95 mm |
| GRM219R61A106KE44  | 10 $\mu$ F 10 V 10 % X5R 0805 .95 mm |



## 7 Low dropout linear regulators, VREFDDR and VSNVS

### 7.1 General description

This section describes the LDO regulators provided by the PF1510. All regulators use the main bandgap as reference.

When a regulator is disabled, the output is discharged by an internal pull-down.

VLDO1 and VLDO3 can be used as load switches by setting the corresponding load switch enable bit OTP\_VLDOx\_LS.

All general purpose LDOs have short-circuit protection capability. The Short-circuit Protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected and REGSCPEN bit is set, the LDO is disabled by resetting its VLDOxEN bit, while at the same time, an interrupt VLDOxFAULTI is generated to flag the fault to the system processor. The VLDOxFAULTI interrupt is maskable through the VLDOxFAULTM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, the regulators are not automatically disabled upon a short-circuit detection. However, the current limiter continues to limit the output current of the regulator. By default, the REGSCPEN is not set; therefore, at start up none of the regulators are disabled if an overloaded condition occurs. A fault interrupt, VLDOxFAULTI is generated in an overload condition regardless of the state of the REGSCPEN bit. Each LDO features a Low-power mode where the quiescent current consumed is significantly lower than in regulator operation. In the Low-power mode, load current of each regulator is limited to 10 mA.

### 7.2 LDO1 and LDO3 detailed description

LDO1 and LDO3 are identical 300 mA low dropout (LDO) regulators that provide output voltage with high accuracy and are programmable through I<sup>2</sup>C interface bits. Being identical, reference is made to these LDOs as LDOy.

To support this wide input range, LDOy circuit incorporates a PMOS pass FET as well as an NMOS pass FET. The LDO uses the main bandgap as its reference.

The regulator incorporates a soft-start circuit that ramps the internal reference in order to provide smooth output waveform with minimal overshooting during power up. When the regulator is disabled, the output is discharged by an internal pull-down resistor. Additionally, the LDO can be used as a load switch by setting the corresponding Load Switch enable bit OTP\_LDOy\_LS.

Moreover, LDOy includes current limit protection with the option to turn off the LDO when an overcurrent is detected.

#### 7.2.1 Features summary

- Input range LDO from 1.0 V to 4.5 V
- Programmable output voltage between 0.75 V to 1.5 V (uses NMOS) or 1.8 V and 3.3 V (uses PMOS) with 2 % accuracy
- Soft-start ramp control during power up and discharge mechanism during power down
- Low quiescent current (~ 2.5  $\mu$ A) at Low-power mode
- Current limit protection

- Configurable into load switch via OTP bit

7.2.2 LDOy block diagram

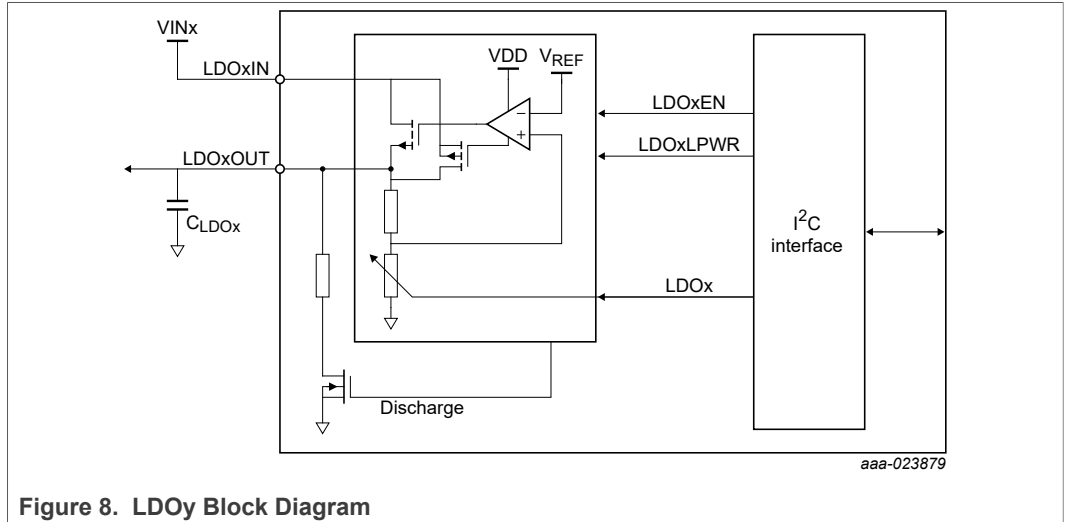


Figure 8. LDOy Block Diagram

7.2.3 LDOy external components

Use a 4.7  $\mu\text{F}$  X5R/X7R capacitor from output to ground with a voltage rating at least 2 times the nominal output voltage.

7.2.4 LDOy output voltage setting

LDOy output voltage is programmed by setting the LDOy[4:0] bits as shown in [Table 33](#).

Table 33. LDOy output voltage setting

| Set point | LDOy[4:0] | LDOy output (V) |
|-----------|-----------|-----------------|
| 0         | 00000     | 0.7500          |
| 1         | 00001     | 0.8000          |
| 2         | 00010     | 0.8500          |
| 3         | 00011     | 0.9000          |
| 4         | 00100     | 0.9500          |
| 5         | 00101     | 1.0000          |
| 6         | 00110     | 1.0500          |
| 7         | 00111     | 1.1000          |
| 8         | 01000     | 1.1500          |
| 9         | 01001     | 1.2000          |
| 10        | 01010     | 1.2500          |
| 11        | 01011     | 1.3000          |
| 12        | 01100     | 1.3500          |
| 13        | 01101     | 1.4000          |
| 14        | 01110     | 1.4500          |

Table 33. LDOy output voltage setting...continued

| Set point | LDOy[4:0] | LDOy output (V) |
|-----------|-----------|-----------------|
| 15        | 01111     | 1.5000          |
| 16        | 10000     | 1.8000          |
| 17        | 10001     | 1.9000          |
| 18        | 10010     | 2.0000          |
| 19        | 10011     | 2.1000          |
| 20        | 10100     | 2.2000          |
| 21        | 10101     | 2.3000          |
| 22        | 10110     | 2.4000          |
| 23        | 10111     | 2.5000          |
| 24        | 11000     | 2.6000          |
| 25        | 11001     | 2.7000          |
| 26        | 11010     | 2.8000          |
| 27        | 11011     | 2.9000          |
| 28        | 11100     | 3.0000          |
| 29        | 11101     | 3.1000          |
| 30        | 11110     | 3.2000          |
| 31        | 11111     | 3.3000          |

### 7.2.5 LDOy low power mode operation

LDOy can operate in a Low-power mode with reduced quiescent current. The Low-power mode can be activated in Standby and Sleep modes by setting the LDOy\_LPWR bit as shown in [Table 34](#). Maximum load current is limited to 10 mA when operating in the Low-power mode.

Table 34. LDOy control bits

| PMIC state        | LDOy_EN | LDOy_STBY | LDOy_OMODE | LDOy_LPWR | LDOy operating mode           |
|-------------------|---------|-----------|------------|-----------|-------------------------------|
| Run/Standby/Sleep | 0       | X         | X          | X         | LDO disabled                  |
| Run               | 1       | X         | X          | X         | LDO enabled                   |
| Standby           | 1       | 0         | X          | X         | LDO disabled                  |
| Standby           | 1       | 1         | X          | 0         | LDO enabled                   |
| Standby           | 1       | 1         | X          | 1         | LDO enabled in Low-power mode |
| Sleep             | 1       | X         | 0          | X         | LDO disabled                  |
| Sleep             | 1       | X         | 1          | 0         | LDO enabled                   |
| Sleep             | 1       | X         | 1          | 1         | LDO enabled in Low-power mode |

### 7.2.6 LDOy current limit protection

LDOy has built in current limit protection. When the load current exceeds the current limit threshold, the regulator goes from a voltage regulation mode to a current regulation mode that limits the available output current.

By setting the REGSCPEN bit, LDOy can be automatically disabled in the event of an over current situation. In the event of an over current, the LDO will be disabled by resetting its LDOy\_EN bit, while at the same time an interrupt LDOy\_FAULTI is generated to flag the fault to the system processor. The LDOy\_FAULTI interrupt is maskable through the LDOy\_FAULTM mask bit.

If REGSCPEN is not set, the regulator will not be automatically disabled, but will instead enter the current limit mode. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators will be disabled if an overloaded condition occurs. A fault interrupt, LDOy\_FAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

Current limit is not active when LDOy is operated in the load switch mode.

### 7.2.7 LDOy load switch mode

The LDOy path can be turned into a switch by setting the OTP\_LDOy\_LS bit. Setting this bit fully turns on the LDO pass FET. This could be useful if power domain partitioning or additional isolation is needed on the system application. Soft-start is engaged during start up of the load switch to reduce inrush currents.

## 7.3 LDO2 detailed description

LDO2 is a 400 mA low dropout (LDO) regulator that provides output voltage with high accuracy and programmable through I<sup>2</sup>C/ interface bits. To support this wide input range the LDO circuit incorporates a PMOS pass FET. The LDO uses the main bandgap as its reference.

The regulator incorporates a soft-start circuit that ramps the internal reference in order to provide smooth output waveform with minimal overshooting during power up. When the regulator is disabled, the output is discharged by an internal pull-down resistor. The pull-down is also activated when RESETBMCU is low.

Moreover, LDO2 includes current limit protection with option to turn off the LDO when an overcurrent is detected.

### 7.3.1 LDO2 features summary

- Input range LDO from 2.8 V to 4.5 V
- Programmable output voltage between 1.8 V and 3.3 V with 2 % accuracy
- Soft-start ramp control during power up and discharge mechanism during power down
- Low quiescent current (~ 1.5  $\mu$ A) at Low-power mode
- Current limit protection

7.3.2 LDO2 block diagram

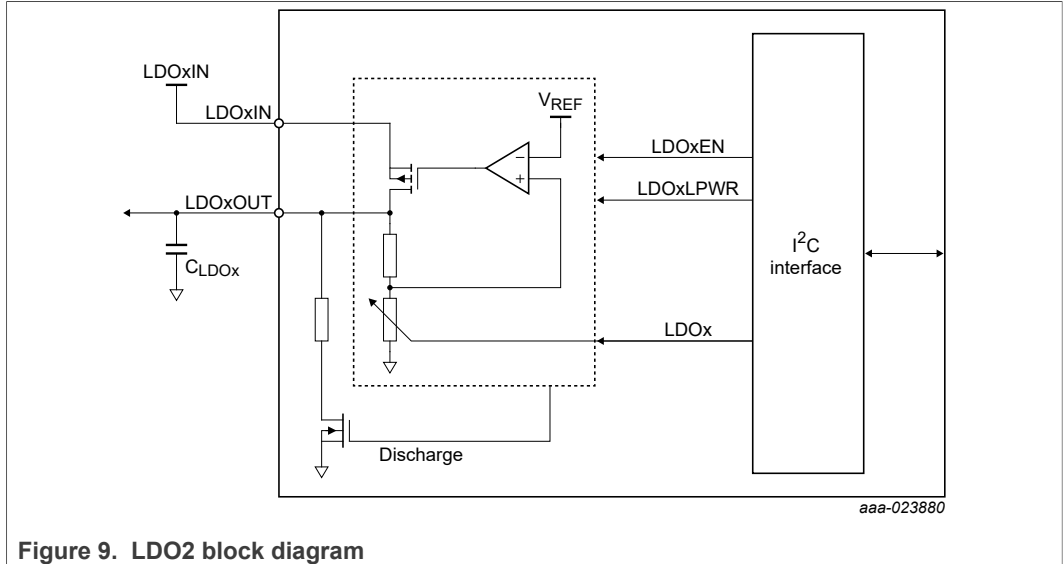


Figure 9. LDO2 block diagram

7.3.3 LDO2 external components

Use a 10  $\mu\text{F}$  X5R/X7R capacitor from output to ground with a voltage rating at least 2 times the nominal output voltage.

7.3.4 LDO2 output voltage setting

LDO2 output voltage is programmed by setting the VLDO2[3:0] bits as shown in [Table 35](#).

Table 35. LDO2 output voltage setting

| Set point | VLDO2[3:0] | VLDO2 output (V) |
|-----------|------------|------------------|
| 0         | 0000       | 1.80             |
| 1         | 0001       | 1.90             |
| 2         | 0010       | 2.00             |
| 3         | 0011       | 2.10             |
| 4         | 0100       | 2.20             |
| 5         | 0101       | 2.30             |
| 6         | 0110       | 2.40             |
| 7         | 0111       | 2.50             |
| 8         | 1000       | 2.60             |
| 9         | 1001       | 2.70             |
| 10        | 1010       | 2.80             |
| 11        | 1011       | 2.90             |
| 12        | 1100       | 3.00             |
| 13        | 1101       | 3.10             |
| 14        | 1110       | 3.20             |

Table 35. LDO2 output voltage setting...continued

| Set point | VLDO2[3:0] | VLDO2 output (V) |
|-----------|------------|------------------|
| 15        | 1111       | 3.30             |

### 7.3.5 LDO2 Low-power mode operation

LDO2 can operate in a Low-power mode with reduced quiescent current. The low power mode can be activated in Standby and Sleep modes by setting the LDO2LPWR bit as shown in [Table 36](#). Maximum load current is limited to 10 mA when operating in the Low-power mode.

Table 36. LDO2 control bits

| PMIC state | LDO2EN | LDO2STBY | LDO2OMODE | LDO2LPWR | LDO2 operating mode           |
|------------|--------|----------|-----------|----------|-------------------------------|
| Run        | 0      | X        | X         | X        | LDO disabled                  |
| Run        | 1      | X        | X         | X        | LDO enabled                   |
| Standby    | 1      | 0        | X         | X        | LDO disabled                  |
| Standby    | 1      | 1        | X         | 0        | LDO enabled                   |
| Standby    | 1      | 1        | X         | 1        | LDO enabled in Low-power mode |
| Sleep      | 1      | X        | 0         | X        | LDO disabled                  |
| Sleep      | 1      | X        | 1         | 0        | LDO enabled                   |
| Sleep      | 1      | X        | 1         | 1        | LDO enabled in Low-power mode |

### 7.3.6 LDO2 current limit protection

LDO2 has built in current limit protection. When the load current exceeds the current limit threshold, the regulator goes from a voltage regulation mode to a current regulation mode limiting the available output current.

By setting the REGSCPEN bit, LDO2 can be automatically disabled in the event of an over current situation. In the event of an over current, the LDO is disabled by resetting its VLDO2EN bit, while at the same time an interrupt VLDO2FAULTI is generated to flag the fault to the system processor. The VLDO2FAULTI interrupt is maskable through the VLDO2FAULTM mask bit.

If REGSCPEN is not set, the regulator will not be automatically disabled, but instead enter the current limit mode. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators will be disabled if an overloaded condition occurs. A fault interrupt, VLDO2FAULTI is generated in an overload condition regardless of the state of the REGSCPEN bit.

## 7.4 VREFDDR reference

VREFDDR is an internal NMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories.

A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

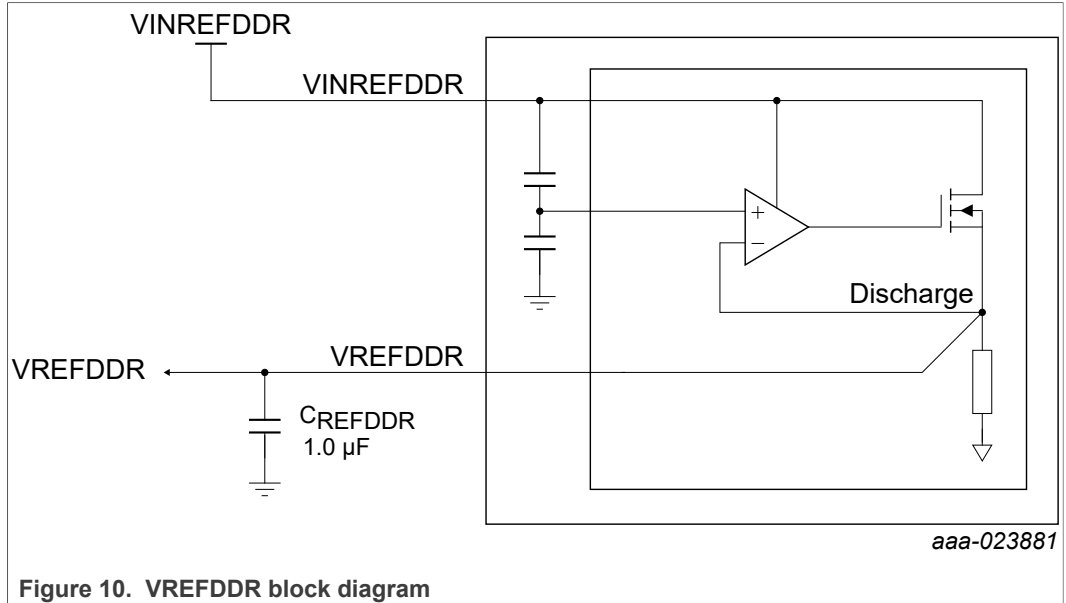


Figure 10. VREFDDR block diagram

### 7.5 VSNVS LDO/Switch

VSNVS powers the low-power SNVS/RTC domain on the processor. It derives its power from either VSYS or a coin cell. When powered by both, VSYS powers VSNVS if VSYS > VTH threshold and LICELL powers VSNVS when VSYS < VTL. When powered by VSYS, VSNVS is an LDO capable of supplying 2.0 mA at 3.0 V. When powered by coin cell, VSNVS output tracks the coin cell voltage by means of a switch. In this case, the VSNVS voltage is simply the coin cell voltage minus the voltage drop across the switch.

Upon subsequent removal of VSYS, with the coin cell attached, VSNVS will change configuration from an LDO to a switch.

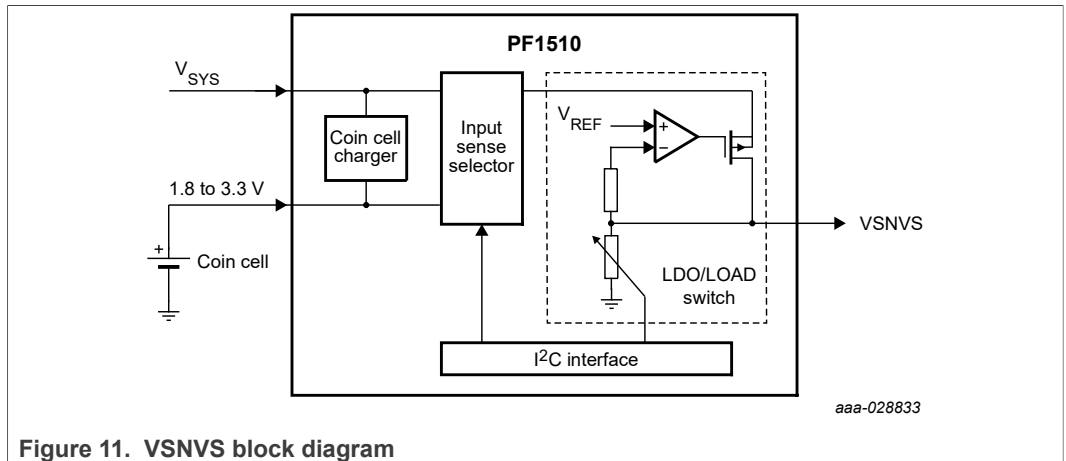


Figure 11. VSNVS block diagram

## 8 Front-end LDO description

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The VIN operates from 4.0 V to 6.5 V with up to 22 V overvoltage protection.

The VIN current limit works by monitoring the current being drawn from the VIN and comparing it to the programmed current limit. The current limit should be set based on the current-handling capability of the input adaptor. Generally, this limit is chosen to optimally fulfill the system-power requirements. See [Table 40](#).

The PMIC is powered from the VSYS node in the PF1510.

The VSYS voltage can be regulated to either 3.5 V, 3.7 V or 4.3 V. See [Table 38](#).



8.1 Operating modes and behavioral description

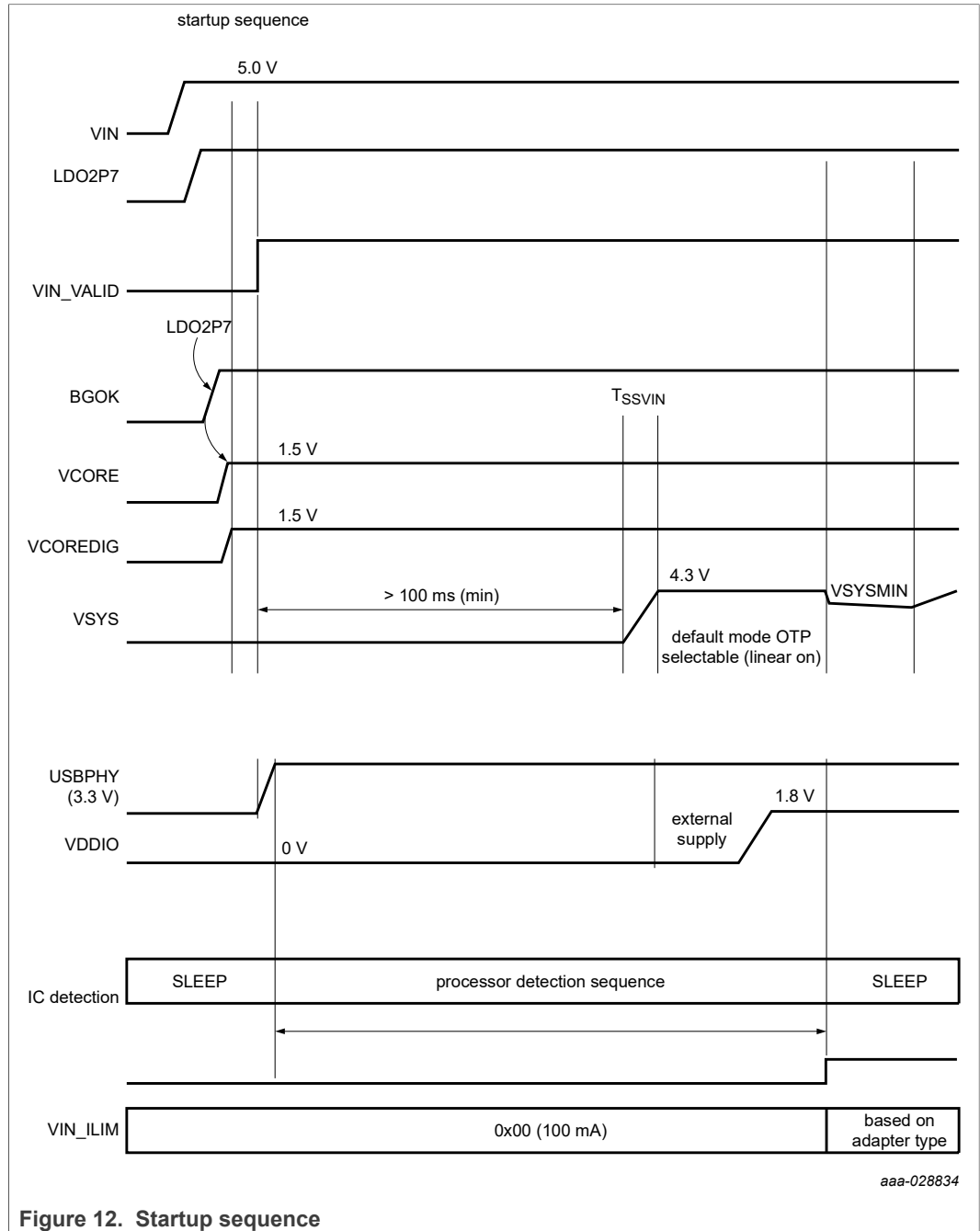


Table 37. Front-end regulator register

| FRONT-END REGULATOR REGISTER |           |    |          |    |    |    |    |    |
|------------------------------|-----------|----|----------|----|----|----|----|----|
| ADDR:                        | 0x8F      |    |          |    |    |    |    |    |
|                              | D7        | D6 | D5       | D4 | D3 | D2 | D1 | D0 |
| BITS:                        | VSYSTEMIN |    | Reserved |    |    |    |    |    |
| POR:                         | 0         | 0  | 1        | 0  | 1  | 0  | 1  | 1  |

Table 37. Front-end regulator register...continued

| FRONT-END REGULATOR REGISTER |  |  |  |  |  |  |  |  |
|------------------------------|--|--|--|--|--|--|--|--|
| ACCESS:                      |  |  |  |  |  |  |  |  |

The VSYS<sub>MIN</sub> value is programmable via OTP as per the table below.

Table 38. VSYS<sub>MIN</sub> setting

| VSYS <sub>MIN</sub> [1:0] setting | VSYS <sub>MIN</sub> setting (V) |
|-----------------------------------|---------------------------------|
| 00                                | 3.5                             |
| 01                                | 3.7                             |
| 10                                | 4.3                             |
| 11                                | Reserved                        |

The VSYS<sub>MIN</sub> setting is the "normal" regulation point for VSYS. This parameter sets the point where the VSYS loop starts taking control and regulates the output. 4.3 V is the recommended setting to ensure that there is enough headroom before reaching UVDET (PMIC undervoltage detection, 2.9 V typ.).

Typically, the VSYS output range can go as low as 300 mV below the VSYS<sub>MIN</sub> setting. Therefore, the recommended setting for the VSYS output should be between 4.0 V to 4.3 V.

Table 39. VIN current limit register

| VIN CURRENT LIMIT REGISTER |          |     |     |     |     |          |    |    |
|----------------------------|----------|-----|-----|-----|-----|----------|----|----|
| ADDR:                      | 0x94     |     |     |     |     |          |    |    |
|                            | D7       | D6  | D5  | D4  | D3  | D2       | D1 | D0 |
| BITS:                      | VIN_ILIM |     |     |     |     | RESERVED |    |    |
| POR:                       | 0        | 1   | 1   | 0   | 1   | 0        | 0  | 0  |
| ACCESS:                    | R/W      | R/W | R/W | R/W | R/W | —        |    |    |

The table below shows valid VIN limit settings.

Table 40. VIN limit settings

| VIN_ILIM[4:0] setting | VIN current limit (mA) |
|-----------------------|------------------------|
| 00000                 | 10                     |
| 00001                 | 15                     |
| 00010                 | 20                     |
| 00011                 | 25                     |
| 00100                 | 30                     |
| 00101                 | 35                     |
| 00110                 | 40                     |
| 00111                 | 45                     |
| 01000                 | 50                     |
| 01001                 | 100                    |
| 01010                 | 150                    |

Table 40. VIN limit settings...continued

| VIN_ILIM[4:0] setting | VIN current limit (mA) |
|-----------------------|------------------------|
| 01011                 | 200                    |
| 01100                 | 300                    |
| 01101                 | 400                    |
| 01110                 | 500                    |
| 01111                 | 600                    |
| 10000                 | 700                    |
| 10001                 | 800                    |
| 10010                 | 900                    |
| 10011                 | 1000                   |
| 10100                 | 1500                   |
| 10101 to 11101        | Reserved               |
| 11110                 | Reserved               |
| 11111                 | Reserved               |

## 9 Control and interface signals

The PF1510 PMIC is fully programmable via the I<sup>2</sup>C interface. Additional communication is provided by direct logic interfacing including interrupt and reset pins as well as pins for power buttons.

### 9.1 PWRON

PWRON is an input signal to the IC that acts as an enable signal for the voltage regulators in the PF1510.

The PWRON pin can be configured as either a level sensitive input (OTP\_PWRON\_CFG = 0), or as an edge sensitive input (OTP\_PWRON\_CFG = 1).

As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into Sleep mode.

As an edge sensitive input, such as when connected to a mechanical switch, a falling edge will turn on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters Sleep mode.

Table 41. PWRON pin OTP configuration options

| OTP_PWRON_CFG | Mode   |
|---------------|--|
| 0             | PWRON pin HIGH = ON<br>PWRON pin LOW = OFF or Sleep mode                                   |
| 1             | PWRON pin pulled LOW momentarily = ON<br>PWRON pin LOW for 4.0 seconds = OFF or Sleep mode |

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Table 42. PWRON pin logic level

| Pin name | Parameter       | Load condition | Min | Max | Unit |
|----------|-----------------|----------------|-----|-----|------|
| PWRON    | V <sub>IL</sub> | —              | 0.0 | 0.4 | V    |
|          | V <sub>IH</sub> | —              | 1.4 | 3.6 | V    |

When OTP\_PWRON\_CFG = 1, PWRON pin pulled low momentarily takes the system from REGS\_DISABLE/SLEEP to RUN mode. There is no effect if PWRON is pulled low momentarily while in RUN or STANDBY modes. Only an interrupt is generated.

PWRON pin low for 4.0 seconds with PWRONRSTEN bit = 1: Enters REGS\_DISABLE or Sleep mode.

See [Section 10 "PF1510 state machine"](#) for detailed description.

In this configuration, the PWRON input can be a mechanical switch debounced through a programmable de-bouncer, PWRONDBNC[1:0], to avoid a response to a very short key press. The interrupt is generated for both the falling and the rising edge of the PWRON pin. By default, a 31.25 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONDBNC[1:0]. The interrupt is cleared by software, or when cycling through the REGS\_DISABLE mode.

Table 43. PWRONDBNC settings

| Bits           | State | Turn on debounce (ms) | Falling edge INT debounce (ms) | Rising edge INT debounce (ms) |
|----------------|-------|-----------------------|--------------------------------|-------------------------------|
| PWRONDBNC[1:0] | 00    | 31.25                 | 31.25                          | 31.25                         |
|                | 01    | 31.25                 | 31.25                          | 31.25                         |
|                | 10    | 125                   | 125                            | 31.25                         |
|                | 11    | 750                   | 750                            | 31.25                         |

## 9.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when deasserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit.

Table 44. Standby pin polarity control

| STANDBY (pin) | STANDBYINV (I <sup>2</sup> C bit) | STANDBY control     |
|---------------|-----------------------------------|---------------------|
| 0             | 0                                 | Not in Standby mode |
| 0             | 1                                 | In Standby mode     |
| 1             | 0                                 | In Standby mode     |
| 1             | 1                                 | Not in Standby mode |

Table 45. STANDBY pin logic level

| Pin name | Parameter       | Load condition | Min | Max | Unit |
|----------|-----------------|----------------|-----|-----|------|
| STANDBY  | V <sub>IL</sub> | —              | 0   | 0.4 | V    |
|          | V <sub>IH</sub> | —              | 1.4 | 3.6 | V    |

Since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode. When enabled (STANDBYDLY = 01, 10, or 11), STANDBYDLY delays the Standby initiated response for the entire IC, until the STBYDLY counter expires. An allowance should be made for three additional 32 kHz cycles required to synchronize the Standby event.

### 9.3 RESETBMCU

RESETBMCU is an open-drain, active low output configurable via OTP for two modes of operation.

In its default mode, it is deasserted at the end of the start-up sequence. In this mode, the signal can be used to bring the processor out of reset (POR), or as an indicator that all supplies have been enabled; it is only asserted during a turn off event.

When configured for its fault mode, RESETBMCU is deasserted after the startup sequence is completed only if no faults occurred during start up. At any time, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted low.

The PF1510 is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP\_PWRGD\_EN to 1.

The time from the last regulator in the start-up sequence to when RESETBMCU is deasserted is programmable between 2.0 ms and 1024 ms via OTP\_POR\_DLY[2:0] bits.

Table 46. RESETBMCU pin logic level

| Pin name  | Parameter       | Load condition | Min         | Max         | Unit |
|-----------|-----------------|----------------|-------------|-------------|------|
| RESETBMCU | V <sub>OL</sub> | -2.0 mA        | 0           | 0.2 * VDDIO | V    |
|           | V <sub>OH</sub> | Open Drain     | 0.8 * VDDIO | 3.6 V       | V    |

### 9.4 INTB

INTB is an open-drain, active low output. It is asserted when any interrupt occurs, provided that the interrupt is unmasked. INTB is deasserted after the fault interrupt is cleared by software, which requires writing a “1” to the interrupt bit.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the interrupt status register. This gives the processor the option of polling for status from the IC.

The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking. The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Table 47. INTB pin logic level

| Pin name | Parameter       | Load condition | Min | Max         | Unit |
|----------|-----------------|----------------|-----|-------------|------|
| INTB     | V <sub>OL</sub> | -2.0 mA        | 0   | 0.2 * VDDIO | V    |

Table 47. INTB pin logic level...continued

| Pin name | Parameter       | Load condition | Min         | Max   | Unit |
|----------|-----------------|----------------|-------------|-------|------|
|          | V <sub>OH</sub> | Open Drain     | 0.8 * VDDIO | 3.6 V | V    |

## 9.5 WDI

WDI is an input signal to the IC. It is typically connected to the watchdog output of the processor. When the WDI pin is pulled low, the PMIC enters the “REGS\_DISABLE” mode where all the regulators are turned off. The WDI acts as a hard reset input from the processor.

During PMIC startup (REGS\_DISABLE to RUN mode), the WDI pin is masked till RESETBMCU is deasserted.

Table 48. WDI pin logic level

| Pin name | Parameter       | Load condition | Min         | Max         | Unit |
|----------|-----------------|----------------|-------------|-------------|------|
| WDI      | V <sub>IL</sub> | —              | 0           | 0.2 * VDDIO | V    |
|          | V <sub>IH</sub> | —              | 0.8 * VDDIO | 3.6         | V    |

## 9.6 ONKEY

ONKEY is an input pin to the IC and is typically connected to a push-button switch. The ONKEY pin is pulled high when the switch is depressed, and is pulled low when the switch is pressed.

Pressing the switch generates interrupts which the processor uses to initiate PMIC state transitions. Pressing the ONKEY for longer than the delay programmed by OTP\_TGRESET[1:0] (ranges from 4.0 s to 16 s), forces the PMIC into the REGS\_DISABLE state.

Table 49. ONKEY pin logic level

| Pin name | Parameter       | Load condition | Min | Max | Unit |
|----------|-----------------|----------------|-----|-----|------|
| ONKEY    | V <sub>IL</sub> | —              | 0   | 0.4 | V    |
|          | V <sub>IH</sub> | —              | 1.4 | 4.8 | V    |

Table 50. ONKEYDBNC settings

| Bits           | State | Turn On Debounce (ms) | Falling Edge INT Debounce (ms) | Rising Edge INT Debounce (ms) |
|----------------|-------|-----------------------|--------------------------------|-------------------------------|
| ONKEYDBNC[1:0] | 00    | 31.25                 | 31.25                          | 31.25                         |
|                | 01    | 31.25                 | 31.25                          | 31.25                         |
|                | 10    | 125                   | 125                            | 31.25                         |
|                | 11    | 750                   | 750                            | 31.25                         |

The ONKEY input can be a mechanical switch debounced through a programmable debouncer, ONKEYDBNC[1:0], to avoid a response to a very short (unintentional) key press. The interrupt is generated during the rising edge of the ONKEY pin.

The falling edge debounce timing can be extended with ONKEYDBNC[1:0] as defined [Table 50](#). The interrupt is cleared by software, or when cycling through the REGS\_DISABLE mode.

See [Section 12 "Register map"](#) for detailed description of the ONKEY interrupt registers.

## 9.7 Control interface I<sup>2</sup>C block description

The PF1510 contains an I<sup>2</sup>C interface port which allows access by a processor, or any I<sup>2</sup>C master, to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I<sup>2</sup>C master via software.

### 9.7.1 I<sup>2</sup>C device ID

I<sup>2</sup>C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The PF1510 I<sup>2</sup>C device address is 0x08.

### 9.7.2 I<sup>2</sup>C operation

The I<sup>2</sup>C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for general call addressing). Timing diagrams, electrical specifications, and further details can be found in the I<sup>2</sup>C specification, which is available for download at:

[http://www.nxp.com/acrobat\\_download/literature/9398/39340011.pdf](http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf)

I<sup>2</sup>C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

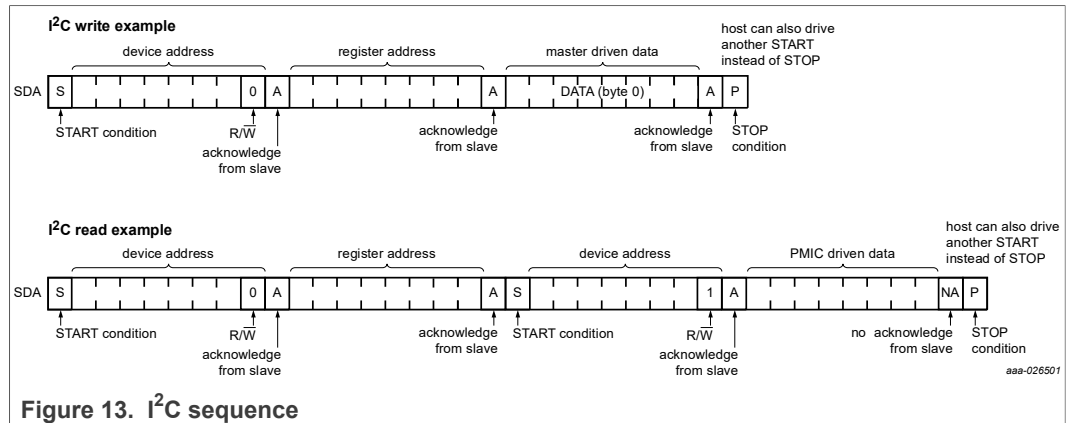


Figure 13. I²C sequence

## 10 PF1510 state machine

The PMIC part of the PF1510 can operate in a number of states as shown in [Figure 14](#).

The states can be split into two categories:

1. “System On” that includes the RUN, STANDBY and SLEEP modes
2. “System Off” that includes the REGS\_DISABLE and CORE\_OFF modes

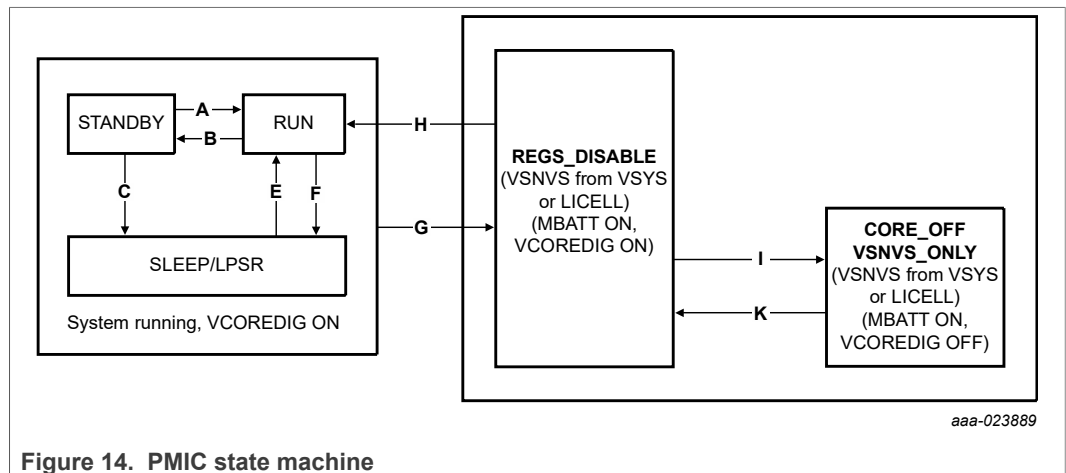


Figure 14. PMIC state machine

In the “System On” modes, some or all of the PMIC regulators are powered and in general the system processor is powered.

In the “System Off” modes, all (or all regulators except VSNVS) are powered off. In general the system processor is powered off during these states. In the REGS\_DISABLE and CORE\_OFF modes, the VSNVS supply remains enabled keeping the system RTC running.

The only way to transition from “System Off” to “System On” and vice versa is through the REGS\_DISABLE mode. From the REGS\_DISABLE mode, the only exit into a “System On” state is into the “Run” mode. Transition from the REGS\_DISABLE mode to the Run mode requires a Turn On event. See [Section 10.3 "Turn on events"](#).

Transition from any of the “System On” modes to the REGS\_DISABLE state is allowed. This transition is referred to as a Turn Off event. See [Section 10.4 "Turn off events"](#).



## 10.1 System ON states

### 10.1.1 Run state

In this state, the PMIC regulators are enabled and the system is powered up. RESETBMCU is de-asserted in this state.

This mode can be entered in several ways:

1. From REGS\_DISABLE through a Turn On Event: During this transition, the PMIC regulators are powered up as per their programmed start-up sequence. After all the regulators are powered, the RESETBMCU pin is de-asserted.
2. From STANDBY by using the STANDBY pin
3. From SLEEP mode by using the PWRON pin: Typically, some of the regulators are turned off in the SLEEP mode compared to the RUN mode. In the SLEEP mode, some of the buck regulator output voltages are set lower than those in the RUN mode. While transitioning from the SLEEP to the RUN mode, regulators that were turned off in the SLEEP mode are turned back on in the RUN mode following the same sequence as the programmed OTP sequence. Output voltage transitions during transition from the SLEEP to the RUN mode also occurs at the same OTP sequence time slot. RESETBMCU is de-asserted through this state transition.

### 10.1.2 STANDBY state

This state is entered by controlling the logic level of the STANDBY pin. It can be entered only from the RUN mode.

The STANDBY pin polarity is programmable through the STANDBYINV I<sup>2</sup>C bit. By default, STANDBYINV = 0 and a logic high on the STANDBY pin moves the state machine from the RUN state to the STANDBY state. When STANDBYINV = 1, a logic low moves the state machine from the RUN state to the STANDBY state.

Regulator output voltage may be changed, or regulator outputs could be disabled while entering the STANDBY state and vice versa.

For details on the power-down sequence, see [Section 10.7 "Regulator power-down sequencer"](#). While exiting STANDBY state into the RUN mode, regulator output voltage changes and regulator enables follow the power-up sequence.

It is possible to exit STANDBY state and enter the SLEEP state. SLEEP state is generally a lower power system state compared to the STANDBY state. Exiting STANDBY into the SLEEP state follows the power-down sequence.

RESETBMCU is de-asserted in the STANDBY state.

### 10.1.3 SLEEP state

This state is entered from either the RUN state or the STANDBY state by controlling the PWRON pin. The exact condition required for this transition depends on the OTP configuration of the PWRON pin. For details see [Section 9.1 "PWRON"](#).

The power-down sequence is followed while entering this state and the power-up sequence is followed while exiting this state into the RUN state.

RESETBMCU is de-asserted in the SLEEP state.

## 10.2 System OFF states

RESETBMCU is asserted (low) in all the System Off states.

### 10.2.1 REGS\_DISABLE

This state can be considered the 'home state' for the state machine. In this state, the state machine waits for appropriate commands to proceed to other states.

REGS\_DISABLE can be entered from one of the "System On" state through a turn off event.

REGS\_DISABLE can be entered from the CORE\_OFF by pressing the ONKEY button for more than 1000 ms or by applying the Vin.

In the REGS\_DISABLE state, the PMIC core circuitry is active. VSNVS is a best-of-supply output of VSYS and LICELL.

### 10.2.2 CORE\_OFF

This state is entered in two ways:

1. From the REGS\_DISABLE mode by pressing and holding the ONKEY button low  $> T_{\text{greset}}$
2. From the REGS\_DISABLE mode if the GOTO\_CORE\_OFF bit is set

This state cannot be entered if Vin is applied.

In this state, the internal core of the PMIC is turned off to reduce quiescent current. VSNVS is the only regulator that is supplied to external loads.

## 10.3 Turn on events

A turn on event takes the PMIC from the REGS\_DISABLE state to the RUN state (transition H in [Figure 14](#)).

The turn on events are:

1. PWRON logic high with PWRON\_CFG = 0
2. PWRON H -> L with PWRON\_CFG = 1

$VSYS > UVDET_{\text{rising}}$  and  $T_J < T_{\text{SHDN\_fall}}$  are preconditions for a turn on event to occur.

The turn on is said to be complete after the RESETBMCU pin is deasserted. The WDI pin is masked till the RESETBMCU pin is deasserted.

## 10.4 Turn off events

A turn off event takes the PMIC state machine from one of the "System On" states (RUN, STANDBY or SLEEP) to the REGS\_DISABLE state. The power-down sequence is followed during all of the turn off events.

The turn off events are:

1. Thermal Shutdown ( $T_J > T_{\text{SHDN\_rise}}$ )
2. PWRON logic low with OTP\_PWRON\_CFG = 0
3. PWRON low  $> 4.0$  s with OTP\_PWRON\_CFG = 1 && PWRONRSTEN = 1

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4. WDI = 0. This occurs when the processor watchdog expires and pulls the WDI pin low to create a hard reset.
5. ONKEY pressed low > T<sub>greset</sub> && ONKEYRST\_EN = 1. This facilitates creating a hard reset when pressing the ONKEY button without processor intervention.

10.5 State diagram and transition conditions

Table 51. State transition table

| Transition | Description  | PWRON_CFG = 0 (Level sensitive)   | PWRON_CFG = 1 (Edge sensitive)  |
|------------|--|---|---|
| A          | Standby to Run   | (STANDBY pin = 0 && STANDBYINV bit = 0)<br>OR<br>(STANDBY pin = 1 && STANDBYINV bit = 1)  | (STANDBY pin = 0 && STANDBYINV bit = 0)<br>OR<br>(STANDBY pin = 1 && STANDBYINV bit = 1)  |
| B          | Run to Standby   | (STANDBY pin = 1 && STANDBYINV bit = 0)<br>OR<br>(STANDBY pin = 0 && STANDBYINV bit = 1)  | (STANDBY pin = 1 && STANDBYINV bit = 0)<br>OR<br>(STANDBY pin = 0 && STANDBYINV bit = 1)  |
| C          | Standby to Sleep   | (PWRON = 0) && (Any SWxOMODE = 1    Any LDOxOMODE = 1)  | (PWRON High to Low and PWRON = 0 > 4s) && (PWRONRSTEN = 1) && (Any SWxOMODE = 1    Any LDOxOMODE = 1)   |
| E          | Sleep to Run   | PWRON = 1   | PWRON High to Low to High <sup>[1]</sup>  |
| F          | Run to Sleep   | (PWRON = 0) && (Any SWxOMODE = 1    Any LDOxOMODE = 1)  | (PWRON High to Low and PWRON = 0 > 4s) && (PWRONRSTEN = 1) && (Any SWxOMODE = 1    Any LDOxOMODE = 1)   |
| G          | Run/Standby/Sleep to REGS_DISABLE  | (Thermal shutdown)<br>OR<br>(PWRON = 0 && All SWxOMODE = 0 && All LDOxOMODE = 0)<br>OR<br>(WDI = 0) <sup>[2]</sup><br>OR<br>(ONKEY High to Low and ONKEY = 0 > T <sub>greset</sub> && ONKEY_RST_EN = 1)<br>OR<br>(VSYS < UVDET_Fall) <sup>[3]</sup> | (Thermal shutdown)<br>OR<br>(PWRON = 0 > 4s && PWRONRSTEN = 1 && All SWxOMODE = 0 && All LDOxOMODE = 0)<br>OR<br>(PWRON High to Low and PWRON = 0 > 4s when in Sleep state)<br>OR<br>(WDI = 0) <sup>[2]</sup><br>OR<br>(ONKEY High to Low and ONKEY = 0 > T <sub>greset</sub> and ONKEY_RST_EN = 1)<br>OR<br>(VSYS < UVDET_Fall) <sup>[3]</sup> |
| H          | REGS_DISABLE to Run<br>(Only if VSYS > UVDET and T <sub>J</sub> < T <sub>SHDN_fall</sub> ) | PWRON = 1   | (PWRON High to Low )<br>OR<br>(If entered REGS_DISABLE via long press on PWRON && RESTARTEN = 1 && PWRON stays Low > 1.0 s)<br>OR<br>(Vin applied) <sup>[4] [5]</sup>   |
| I          | REGS_DISABLE to CORE_OFF<br>(Only if VIN_INVALID = 1)                                      | (GOTO_CORE_OFF = 1 && ONKEY = 1)<br>OR<br>(ONKEY High to Low and ONKEY = 0 > T <sub>greset</sub> && ONKEY_RST_EN = 1) <sup>[6][7]</sup>   | (GOTO_CORE_OFF = 1 && ONKEY = 1)<br>OR<br>(ONKEY High to Low and ONKEY = 0 > T <sub>greset</sub> && ONKEY_RST_EN = 1) <sup>[6][8]</sup>   |
| K          | CORE_OFF to REGS_DISABLE   | (ONKEY High to Low and ONKEY = 0 > 1000 ms)<br>OR<br>(Vin applied)  | (ONKEY High to Low and ONKEY = 0 > 1000 ms)<br>OR<br>(Vin applied)  |

[1] This low period is < 4.0 s. If it is longer than 4.0 s, it transitions to G  
 [2] PWRON pin is pulled low by processor after WDI = 0.  
 [3] Follows regulator power-down sequence for this transition  
 [4] WDI pin is masked till RESETBMCU is deasserted.  
 [5] Debounce on PWRON programmable via PWRONDBNC[1:0]  
 [6] PWRON pin is pulled low by processor after ONKEY = 0 > T<sub>greset</sub>.  
 [7] GOTO\_CORE\_OFF is set by user when system is ON. For other products, a secondary processor is used to set this bit while in REGS\_DISABLE  
 [8] GOTO\_CORE\_OFF must be set by user when system is ON

## 10.6 Regulator power-up sequencer

Start-up sequence of all the switching and linear regulators in the PF1510 is programmable. VSNVS's sequence is not programmable but is always the first regulator to power up when the PF1510 is powered up via a cold start (from no input to valid input). When SYS is first applied to the PF1510, VSNVS comes up first.

The switching and linear regulators power up based on their programmed OTP sequence using the respective OTP\_XX\_SEQ[2:0] when transitioning from REGS\_DISABLE to the RUN state.

RESETBMCU is pulled low from VCOREDIG POR till the end of the power-up sequencer.

RESETBMCU is pulled high 2.0 ms to 1024 ms after the last regulator powers up. This delay is OTP programmable through the OTP\_POR\_DLY[2:0] bits.

When transitioning from STANDBY mode to RUN mode, the power-up sequencer is activated only if any of the regulators turn back on during this transition.

The power-up sequencer ends as soon as the last regulator powers up, rather than waiting for a fixed time.

The power-up sequencer is always activated when transitioning from Sleep to Run modes. The sequencer ends as soon as the last regulator powers up, rather than waiting for a fixed time.

The PWRUP\_I interrupt is set to indicate completion of transition from STANDBY to RUN and SLEEP to RUN.

The PWRUP\_I interrupt is set while transitioning from STANDBY to RUN even if the sequencers were not used. This is used to indicate that the transition is complete.

## 10.7 Regulator power-down sequencer

The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1\_PWRDN\_SEQ[2:0], SW2\_PWRDN\_SEQ[2:0], SW3\_PWRDN\_SEQ[2:0], LDO1\_PWRDN\_SEQ[2:0], LDO2\_PWRDN\_SEQ[2:0], LDO3\_PWRDN\_SEQ[2:0], VREFDDR\_PWRDN\_SEQ[2:0]) that sets its power-down sequence.

The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1\_PWRDN\_SEQ[2:0] = OTP\_SW1\_PWRUP\_SEQ[2:0].

When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX\_PWRDN\_SEQ[2:0] setting. This way, by default power-down is a mirror of the power-up sequence.

In one of the "System On" states, the processor can change the values of the XXX\_PWRDN\_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX\_PWRDN\_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once. During transition from Run to Standby, the power-down sequencer is activated if any of the regulators are turned off during this transition.

If regulators are not turned off during this transition, the power-down sequencer is bypassed and the transition happens at once (any associated DVS transitions still take time).

During transition from Run to Sleep, the power-down sequencer is always activated. However, if all XXX\_PWRDN\_SEQ[2:0] = 0, the transition happens immediately.

The PWRDN\_I interrupt is set during transition from Run to Sleep and Run to Standby even if regulators are not turned off during these transitions.

## 11 Device start up

### 11.1 Startup timing diagram

The startup timing of the regulators is programmable through OTP, [Figure 15](#) shows the startup timing of the regulators as determined by their OTP A4 sequence.

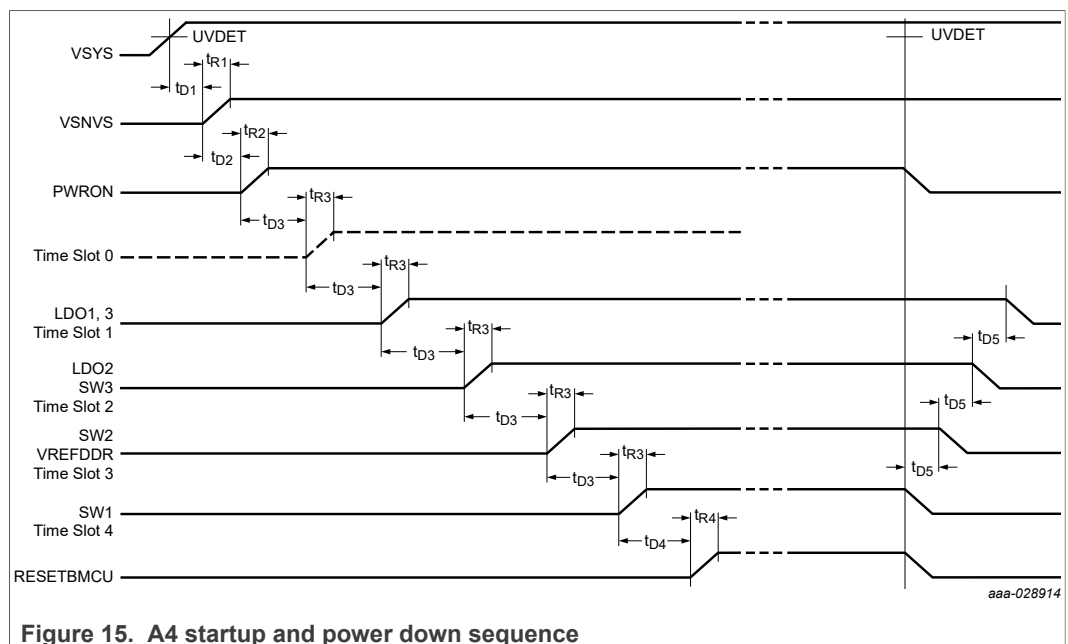


Figure 15. A4 startup and power down sequence

Table 52. A4 startup and power down sequence timing

| Parameter       | Description <sup>[1]</sup>  | Min      | Typ        | Max | Unit |
|-----------------|---|----------|------------|-----|------|
| t <sub>D1</sub> | Turn-on delay of VSNVS  | —        | 0.6        | —   | ms   |
| t <sub>R1</sub> | Rise time of VSNVS  | —        | 0.1        | —   | ms   |
| t <sub>D2</sub> | User determined delay   | —        | —          | —   | ms   |
| t <sub>R2</sub> | Rise time of PWRON  | —        | [2]        | —   | ms   |
| t <sub>D3</sub> | Power up delay between regulators<br>• OTP_SEQ_CLK_SPEED = 0<br>• OTP_SEQ_CLK_SPEED = 1 | —<br>[3] | 0.5<br>2.0 | —   | ms   |
| t <sub>R3</sub> | Rise time of regulators   | —        | 0.2        | —   | ms   |
| t <sub>D4</sub> | Turn-on delay of RESETBCMU  | —        | 2.0        | —   | ms   |
| t <sub>R4</sub> | Rise time of RESETBCMU  | —        | 0.2        | —   | ms   |
| t <sub>D5</sub> | Power down delay between regulators   | —        | 2.0        | —   | ms   |

[1] All regulators avoid drop-out mode at startup

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- [2] Depends on the external signal driving PWRON  
 [3] A4 configuration  
 [4] Rise time is a function of slew rate of regulators and nominal voltage selected.

## 11.2 Device start up configuration

Table 53. PF1510 start up configuration

| Registers                        | Pre-programmed OTP configuration                     |                          |          |              |          |         |          |
|----------------------------------|--|--------------------------|----------|--------------|----------|---------|----------|
|                                  | A1   | A2                       | A3       | A4           | A5       | A6      | A7       |
| Default I <sup>2</sup> C Address | 0x08   | 0x08                     | 0x08     | 0x08         | 0x08     | 0x08    | 0x08     |
| OTP_VSNVS_VOLT[2:0]              | 3.0 V  | 3.0 V                    | 3.0 V    | 3.0 V        | 3.0 V    | 3.0 V   | 3.0 V    |
| OTP_SW1_VOLT[5:0]                | 1.1 V  | 1.0V                     | 1.3875 V | 1.1 V        | 1.3875 V | 1.275 V | 1.3875 V |
| OTP_SW1_PWRUP_SEQ[2:0]           | 1  | 5                        | 3        | 4            | 3        | 3       | 3        |
| OTP_SW2_VOLT[5:0]                | 1.1 V  | 1.2V                     | 1.35 V   | 1.2 V        | 1.5 V    | 1.35 V  | 1.2 V    |
| OTP_SW2_PWRUP_SEQ[2:0]           | 2  | 5                        | 3        | 3            | 3        | 3       | 3        |
| OTP_SW3_VOLT[5:0]                | 1.8 V  | 1.8V                     | 3.3 V    | 1.8 V        | 3.3 V    | 3.3 V   | 1.8 V    |
| OTP_SW3_PWRUP_SEQ[2:0]           | 3  | 1                        | 3        | 2            | 3        | 3       | 3        |
| OTP_LDO1_VOLT[4:0]               | 1.0 V  | 1.8 V                    | 1.8 V    | 3.3 V        | 1.8 V    | 1.8 V   | 3.3 V    |
| OTP_LDO1_PWRUP_SEQ[2:0]          | 4  | 1                        | 3        | 1            | 3        | 3       | 3        |
| OTP_LDO2_VOLT[3:0]               | 2.5 V  | 3.3 V                    | 3.3 V    | 3.3 V        | 3.3 V    | 3.3 V   | 3.3 V    |
| OTP_LDO2_PWRUP_SEQ[2:0]          | 4  | 1                        | 2        | 2            | 2        | 2       | 2        |
| OTP_LDO3_VOLT[4:0]               | 1.0 V  | 1.8 V                    | 3.3 V    | 1.8 V        | 3.3 V    | 3.3 V   | 3.3 V    |
| OTP_LDO3_PWRUP_SEQ[2:0]          | 5  | 1                        | 3        | 1            | 3        | 3       | 3        |
| OTP_VREFDDR_PWRUP_SEQ[2:0]       | 5  | 5                        | 3        | 3            | 3        | 3       | 3        |
| OTP_SW1_DVS_SEL                  | Non-DVS mode   | DVS mode                 |          |              |          |         |          |
| OTP_SW2_DVS_SEL                  | DVS mode   | Non-DVS mode             | DVS mode | Non-DVS mode |          |         |          |
| OTP_LDO1_LS_EN                   | LDO mode   |                          |          |              |          |         |          |
| OTP_LDO3_LS_EN                   | LS mode  | LDO mode                 |          |              |          |         |          |
| OTP_SW1_RDIS_ENB                 | Enabled  |                          |          |              |          |         |          |
| OTP_SW2_RDIS_ENB                 | Enabled  |                          |          |              |          |         |          |
| OTP_SW3_RDIS_ENB                 | Enabled  |                          |          |              |          |         |          |
| OTP_SW1_DVSSPEED                 | 12.5 mV step each 4.0 μs                             |                          |          |              |          |         |          |
| OTP_SW2_DVSSPEED                 | 12.5 mV step each 2.0 μs                             | 12.5 mV step each 4.0 μs |          |              |          |         |          |
| OTP_SWx_EN_AND_STBY_EN           | SW1, SW2, SW3 enabled in RUN and STANDBY             |                          |          |              |          |         |          |
| OTP_LDOx_EN_AND_STBY_EN          | LDO1, LDO2, LDO3, VREFDDR enabled in RUN and STANDBY |                          |          |              |          |         |          |
| OTP_PWRON_CFG                    | Level sensitive                                      |                          |          |              |          |         |          |
| OTP_SEQ_CLK_SPEED                | 0.5 ms time slots                                    | 2 ms time slots          |          |              |          |         |          |

Table 53. PF1510 start up configuration...continued

| Registers           | Pre-programmed OTP configuration          |                                 |    |    |    |                 |                 |
|---------------------|---|---------------------------------|----|----|----|-----------------|-----------------|
|                     | A1  | A2                              | A3 | A4 | A5 | A6              | A7              |
| OTP_TGRESET[1:0]    | 4 secs global reset timer                 |                                 |    |    |    |                 |                 |
| OTP_POR_DLY[2:0]    | 2 ms RESETBMCU power-up delay             |                                 |    |    |    |                 |                 |
| OTP_UVDET[1:0]      | Rising 3.0 V; falling 2.9 V               |                                 |    |    |    |                 |                 |
| OTP_I2C_DEGLITCH_EN | I <sup>2</sup> C deglitch filter disabled |                                 |    |    |    |                 |                 |
| OTP_VSYSMIN[1:0]    | VSYSMIN = 4.3 V                           |                                 |    |    |    | VSYSMIN = 3.7 V | VSYSMIN = 4.3 V |
| OTP_VIN_ILIM[4:0]   | VIN ILIM = 500 mA                         | VIN ILIM = 1500 mA              |    |    |    |                 |                 |
| OTP_USBPHYLDO       | USBPHY LDO disabled                       | USBPHY LDO enabled              |    |    |    |                 |                 |
| OTP_USBPHY          | USBPHY = 3.3 V                            |                                 |    |    |    |                 |                 |
| OTP_ACTDISPHY       | USBPHY active discharge disabled          | USBPHY active discharge enabled |    |    |    |                 |                 |

## 12 Register map

### 12.1 Specific PMIC Registers (Offset is 0x00)

The following pages contain description of the various registers in the PF1510.

Table 54. Register DEVICE\_ID - ADDR 0x00

| Name      | Bit    | R/W | Default | Description   |
|-----------|--------|-----|---------|---|
| DEVICE_ID | 2 to 0 | R   | 100     | Loaded from fuses<br><b>000</b> — Future use<br><b>001</b> — Future use<br><b>010</b> — Future use<br><b>011</b> — Future use<br><b>100</b> — PF1510<br><b>101</b> — Future use<br><b>110</b> — Future use<br><b>111</b> — Future use |
| FAMILY    | 7 to 3 | R   | 01111   | Identifies PMIC<br><b>01111</b> — 0b0_1111 for "15" used to denote the "PF1510"   |

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Table 55. Register OTP\_FLAVOR - ADDR 0x01

| Name   | Bit    | R/W | Default | Description   |
|--------|--------|-----|---------|---|
| UNUSED | 7 to 0 | R   | 0x00    | Blown by ATE to indicate flavor of OTP used<br><b>0x00</b> — OTP not burned<br><b>0x01</b> — A1<br><b>0x02</b> — A2<br><b>0x03</b> — A3<br>continues... |

Table 56. Register SILICON\_REV - ADDR 0x02

| Name            | Bit    | R/W | Default | Description |
|-----------------|--------|-----|---------|-------------|
| METAL_LAYER_REV | 2 to 0 | R   | 000     | Unused      |
| FULL_LAYER_REV  | 5 to 3 | R   | 001     | Unused      |
| FAB_FIN         | 7 to 6 | R   | 00      | Unused      |

Table 57. Register INT\_CATEGORY - ADDR 0x06

| Name      | Bit | R/W | Default | Description   |
|-----------|-----|-----|---------|---|
| VIN_INT   | 0   | R   | 0       | This bit is set high if the VIN_I interrupt bit is set<br><b>0</b> — No interrupt bit is set, cleared, or did not occur<br><b>1</b> — "OR" function of all interrupt status bit   |
| SW1_INT   | 1   | R   | 0       | This bit is set high if any of the Buck 1 interrupt status bits are set<br><b>0</b> — SW1 interrupts cleared or did not occur<br><b>1</b> — Any of the SW1 interrupt status bits are set  |
| SW2_INT   | 2   | R   | 0       | This bit is set high if any of the Buck 2 interrupt status bits are set<br><b>0</b> — SW2 interrupts cleared or did not occur<br><b>1</b> — Any of the SW2 interrupt status bits are set  |
| SW3_INT   | 3   | R   | 0       | This bit is set high if any of the Buck 3 interrupt status bits are set<br><b>0</b> — SW3 interrupts cleared or did not occur<br><b>1</b> — any of the SW3 interrupt status bits are set  |
| LDO_INT   | 4   | R   | 0       | This bit is set high if any of the LDO interrupt status bits are set.<br>This includes LDO1, LDO2 and LDO3.<br><b>0</b> — LDO interrupts cleared or did not occur<br><b>1</b> — Any of the LDO interrupt status bits are set  |
| ONKEY_INT | 5   | R   | 0       | This bit is set high if any of the interrupts associated with ONKEY<br>push button are set.<br><b>0</b> — ONKEY related interrupts cleared or did not occur<br><b>1</b> — Any of the ONKEY interrupt status bits are set  |
| TEMP_INT  | 6   | R   | 0       | This bit is set if any of the interrupts associated with the die<br>temperature monitor are set<br><b>0</b> — PMIC junction temperature related interrupts cleared or did<br>not occur<br><b>1</b> — any of the PMIC junction temperature interrupts status bits<br>are set |



Table 57. Register INT\_CATEGORY - ADDR 0x06...continued

| Name     | Bit | R/W | Default | Description  |
|----------|-----|-----|---------|--|
| MISC_INT | 7   | R   | 0       | This bit is set if interrupts not covered by the above mentioned categories occur<br><b>0</b> — Other interrupts (not covered by categories above) cleared, or did not occur<br><b>1</b> — Status bit of other interrupts (not covered by categories above) is set |

Table 58. Register SW\_INT\_STAT0 - ADDR 0x08

| Name     | Bit    | R/W                 | Default | Description  |
|----------|--------|---------------------|---------|--|
| SW1_LS_I | 0      | RW1C <sup>[1]</sup> | 0       | SW1 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| SW2_LS_I | 1      | RW1C                | 0       | SW2 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| SW3_LS_I | 2      | RW1C                | 0       | SW3 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED   | 7 to 3 | —                   | —       | Unused   |

[1] Read or Write 1 to clear the bit

Table 59. Register SW\_INT\_MASK0 - ADDR 0x09

| Name     | Bit    | R/W | Default | Description   |
|----------|--------|-----|---------|---|
| SW1_LS_M | 0      | RW  | 1       | SW1 low-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| SW2_LS_M | 1      | RW  | 1       | SW2 low-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| SW3_LS_M | 2      | RW  | 1       | SW3 low-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| UNUSED   | 7 to 3 | —   | —       | Unused  |

Table 60. Register SW\_INT\_SENSE0 - ADDR 0x0A

| Name     | Bit    | R/W | Default | Description   |
|----------|--------|-----|---------|---|
| SW1_LS_S | 0      | R   | 0       | SW1 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce).<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| SW2_LS_S | 1      | R   | 0       | SW2 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce).<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| SW3_LS_S | 2      | R   | 0       | SW3 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce).<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| UNUSED   | 7 to 3 | —   | —       | Unused  |

Table 61. Register SW\_INT\_STAT1 - ADDR 0x0B

| Name     | Bit    | R/W                 | Default | Description  |
|----------|--------|---------------------|---------|--|
| SW1_HS_I | 0      | RW1C <sup>[1]</sup> | 0       | SW1 high-side current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| SW2_HS_I | 1      | RW1C                | 0       | SW2 high-side current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| SW3_HS_I | 2      | RW1C                | 0       | SW3 high-side current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED   | 7 to 3 | —                   | —       | Unused   |

[1] Read or Write 1 to clear the bit

Table 62. Register SW\_INT\_MASK1 - ADDR 0x0C

| Name     | Bit | R/W | Default | Description  |
|----------|-----|-----|---------|--|
| SW1_HS_M | 0   | RW  | 1       | SW1 high-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| SW2_HS_M | 1   | RW  | 1       | SW2 high-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |

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Table 62. Register SW\_INT\_MASK1 - ADDR 0x0C...continued

| Name     | Bit    | R/W | Default | Description  |
|----------|--------|-----|---------|--|
| SW3_HS_M | 2      | RW  | 1       | SW3 high-side current limit interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| UNUSED   | 7 to 3 | —   | —       | Unused   |

Table 63. Register SW\_INT\_SENSE1 - ADDR 0x0D

| Name     | Bit    | R/W | Default | Description  |
|----------|--------|-----|---------|--|
| SW1_HS_S | 0      | R   | 0       | SW1 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle.<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| SW2_HS_S | 1      | R   | 0       | SW2 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle.<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| SW3_HS_S | 2      | R   | 0       | SW3 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle.<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| UNUSED   | 7 to 3 | —   | —       | Unused   |

Table 64. Register SW\_INT\_STAT2 - ADDR 0x0E

| Name           | Bit    | R/W                 | Default | Description  |
|----------------|--------|---------------------|---------|--|
| SW1_DVS_DONE_I | 0      | RW1C <sup>[1]</sup> | 0       | Interrupt to indicate SW1 DVS complete. This interrupt should occur every time regulator output voltage is changed (either via I <sup>2</sup> C within a given state, or if there is change in voltage when transitioning states, Run to Standby, for example).<br><b>0</b> — DVS not complete and/or bit cleared<br><b>1</b> — DVS complete |
| SW2_DVS_DONE_I | 1      | RW1C                | 0       | Interrupt to indicate SW2 DVS complete. This interrupt should occur every time regulator output voltage is changed (either via I <sup>2</sup> C within a given state, or if there is change in voltage when transitioning states, Run to Standby, for example).<br><b>0</b> — DVS not complete and/or bit cleared<br><b>1</b> — DVS complete |
| UNUSED         | 7 to 2 | —                   | —       | Unused   |

[1] Read or Write 1 to clear the bit

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Table 65. Register SW\_INT\_MASK2 - ADDR 0x0F

| Name           | Bit    | R/W | Default | Description  |
|----------------|--------|-----|---------|--|
| SW1_DVS_DONE_M | 0      | RW  | 1       | Mask for interrupt that indicates SW1 DVS complete<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| SW2_DVS_DONE_M | 1      | RW  | 1       | Mask for interrupt that indicates SW2 DVS complete<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| UNUSED         | 7 to 2 | —   | —       | Unused   |

Table 66. Register SW\_INT\_SENSE2 - ADDR 0x10

| Name      | Bit    | R/W | Default | Description   |
|-----------|--------|-----|---------|---|
| SW1_DVS_S | 0      | R   | 0       | Indicates DVS in progress for SW1<br><b>0</b> — DVS not in progress<br><b>1</b> — DVS in progress |
| SW2_DVS_S | 1      | R   | 0       | Indicates DVS in progress for SW2<br><b>0</b> — DVS not in progress<br><b>1</b> — DVS in progress |
| UNUSED    | 7 to 2 | —   | —       | Unused  |

Table 67. Register LDO\_INT\_STAT0 - ADDR 0x18

| Name        | Bit    | R/W                 | Default | Description   |
|-------------|--------|---------------------|---------|---|
| LDO1_FAULTI | 0      | RW1C <sup>[1]</sup> | 0       | LDO1 current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| LDO2_FAULTI | 1      | RW1C                | 0       | LDO2 current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| LDO3_FAULTI | 2      | RW1C                | 0       | LDO3 current limit interrupt<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED      | 7 to 3 | —                   | —       | Unused  |

[1] Read or Write 1 to clear the bit

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Table 68. Register LDO\_INT\_MASK0 - ADDR 0x19

| Name        | Bit    | R/W | Default | Description   |
|-------------|--------|-----|---------|---|
| LDO1_FAULTM | 0      | RW  | 1       | LDO1 current limit fault interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| LDO2_FAULTM | 1      | RW  | 1       | LDO2 current limit fault interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.  |
| LDO3_FAULTM | 2      | RW  | 1       | LDO3 current limit fault interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| UNUSED      | 7 to 3 | —   | —       | Unused  |

Table 69. Register LDO\_INT\_SENSE0 - ADDR 0x1A

| Name        | Bit    | R/W | Default | Description   |
|-------------|--------|-----|---------|---|
| LDO1_FAULTS | 0      | R   | 0       | LDO1 fault interrupt sense<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| LDO2_FAULTS | 1      | R   | 0       | LDO2 fault interrupt sense<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| LDO3_FAULTS | 2      | R   | 0       | LDO3 fault interrupt sense<br><b>0</b> — Fault removed<br><b>1</b> — Fault exists |
| UNUSED      | 7 to 3 | —   | —       | Unused  |

Table 70. Register TEMP\_INT\_STAT0 - ADDR 0x20

| Name      | Bit    | R/W                 | Default | Description   |
|-----------|--------|---------------------|---------|---|
| THERM110I | 0      | RW1C <sup>[1]</sup> | 0       | Die temperature crosses 110 °C interrupt. Bidirectional interrupt.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED    | 1      | —                   | —       | Unused  |
| THERM125I | 2      | RW1C                | 0       | Die temperature crosses 125 °C interrupt. Bidirectional interrupt.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED    | 7 to 3 | —                   | —       | Unused  |

[1] Read or Write 1 to clear the bit

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Table 71. Register TEMP\_INT\_MASK0 - ADDR 0x21

| Name      | Bit    | R/W | Default | Description   |
|-----------|--------|-----|---------|---|
| THERM110M | 0      | RW  | 1       | Die temperature crosses 110 °C interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set. |
| UNUSED    | 1      | —   | —       | Unused  |
| THERM125M | 2      | RW  | 1       | Die temperature crosses 125 °C interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| UNUSED    | 7 to 3 | —   | —       | Unused  |

Table 72. Register TEMP\_INT\_SENSE0 - ADDR 0x22

| Name      | Bit    | R/W | Default | Description  |
|-----------|--------|-----|---------|--|
| THERM110S | 0      | R   | 0       | 110 °C interrupt sense<br><b>0</b> — Die temperature below 110 °C<br><b>1</b> — Die temperature above 110 °C |
| UNUSED    | 1      | —   | —       | Unused   |
| THERM125S | 2      | R   | 0       | 125 °C interrupt sense<br><b>0</b> — Die temperature below 125 °C<br><b>1</b> — Die temperature above 125 °C |
| UNUSED    | 7 to 3 | —   | —       | Unused   |

Table 73. Register ONKEY\_INT\_STAT0 - ADDR 0x24

| Name        | Bit | R/W                 | Default | Description   |
|-------------|-----|---------------------|---------|---|
| ONKEY_PUSHI | 0   | RW1C <sup>[1]</sup> | 0       | Interrupt to indicate a push of the ONKEY button. Goes high after debounce.<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared. Interrupt occurs whenever ONKEY button is pushed low for longer than the falling edge debounce setting.<br>Interrupt also occurs whenever ONKEY button is released high for longer than the rising edge debounce setting, provided it went past the falling edge debounce time. In other words, this interrupt occurs whenever a change in status of the ONKEY_PUSHHS sense bit occurs. |
| ONKEY_1SI   | 1   | RW1C                | 0       | Interrupt after ONKEY pressed for > 1 s<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared  |
| ONKEY_2SI   | 2   | RW1C                | 0       | Interrupt after ONKEY pressed for > 2 s<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared  |

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Table 73. Register ONKEY\_INT\_STAT0 - ADDR 0x24...continued

| Name      | Bit    | R/W  | Default | Description  |
|-----------|--------|------|---------|--|
| ONKEY_3SI | 3      | RW1C | 0       | Interrupt after ONKEY pressed for > 3 s<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| ONKEY_4SI | 4      | RW1C | 0       | Interrupt after ONKEY pressed for > 4 s<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| ONKEY_8SI | 5      | RW1C | 0       | Interrupt after ONKEY pressed for > 8 s<br><b>0</b> — Interrupt cleared or did not occur<br><b>1</b> — Interrupt occurred and/or not cleared |
| UNUSED    | 7 to 6 | —    | —       | Unused   |

[1] Read or Write 1 to clear the bit

Table 74. Register ONKEY\_INT\_MASK0 - ADDR 0x25

| Name        | Bit | R/W | Default | Description   |
|-------------|-----|-----|---------|---|
| ONKEY_PUSHM | 0   | RW  | 1       | Interrupt mask for ONKEY_PUSH_I<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| ONKEY_1SM   | 1   | RW  | 1       | Interrupt mask for ONKEY_1SI<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.    |
| ONKEY_2SM   | 2   | RW  | 1       | Interrupt mask for ONKEY_2SI<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.    |
| ONKEY_3SM   | 3   | RW  | 1       | Interrupt mask for ONKEY_3SI<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.    |
| ONKEY_4SM   | 4   | RW  | 1       | Interrupt mask for ONKEY_4SI<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.    |
| ONKEY_8SM   | 5   | RW  | 1       | Interrupt mask for ONKEY_8SI<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.    |

Table 74. Register ONKEY\_INT\_MASK0 - ADDR 0x25...continued

| Name   | Bit    | R/W | Default | Description |
|--------|--------|-----|---------|-------------|
| UNUSED | 7 to 6 | —   | —       | Unused      |

Table 75. Register ONKEY\_INT\_SENSE0 - ADDR 0x26

| Name        | Bit    | R/W | Default | Description   |
|-------------|--------|-----|---------|---|
| ONKEY_PUSHS | 0      | R   | 0       | Push interrupt sense<br><b>0</b> — ONKEY not pushed low. This bit follows debounced version of the ONKEY button being released.<br><b>1</b> — ONKEY pushed low. This follows the ONKEY button after the debounce circuit (debounce is programmable).  |
| ONKEY_1SS   | 1      | R   | 0       | 1 s interrupt sense or cleared after ONKEY button is released<br><b>0</b> — ONKEY not pushed low for >1 s or cleared after ONKEY button is released.<br><b>1</b> — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push button is released. |
| ONKEY_2SS   | 2      | R   | 0       | 2 s interrupt sense or cleared after ONKEY button is released<br><b>0</b> — ONKEY not pushed low for >1 s or cleared after ONKEY button is released.<br><b>1</b> — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push button is released. |
| ONKEY_3SS   | 3      | R   | 0       | 3 s interrupt sense or cleared after ONKEY button is released<br><b>0</b> — ONKEY not pushed low for >1 s or cleared after ONKEY button is released<br><b>1</b> — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push button is released.  |
| ONKEY_4SS   | 4      | R   | 0       | 4 s interrupt sense or cleared after ONKEY button is released<br><b>0</b> — ONKEY not pushed low for >1 s or cleared after ONKEY button is released.<br><b>1</b> — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push button is released. |
| ONKEY_8SS   | 5      | R   | 0       | 8 s interrupt sense or cleared after ONKEY button is released<br><b>0</b> — ONKEY not pushed low for >1 s or cleared after ONKEY button is released.<br><b>1</b> — ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push button is released. |
| UNUSED      | 7 to 6 | —   | —       | Unused  |



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Table 76. Register MISC\_INT\_STAT0 - ADDR 0x28

| Name           | Bit    | R/W                 | Default | Description   |
|----------------|--------|---------------------|---------|---|
| PWRUP_I        | 0      | RW1C <sup>[1]</sup> | 0       | Interrupt to indicate completion of transition from STANDBY to RUN and from SLEEP to RUN<br><b>0</b> — Interrupt cleared or has not occurred<br><b>1</b> — Interrupt has occurred |
| PWRDN_I        | 1      | RW1C                | 0       | Interrupt to indicate completion of transition from RUN to STANDBY and from RUN to SLEEP<br><b>0</b> — Interrupt cleared or has not occurred<br><b>1</b> — Interrupt has occurred |
| PWRON_I        | 2      | RW1C                | 0       | Power on button event interrupt<br><b>0</b> — Interrupt cleared or has not occurred<br><b>1</b> — Interrupt has occurred  |
| LOW_SYS_WARN_I | 3      | RW1C                | 0       | LOW_SYS_WARN threshold crossed interrupt<br><b>0</b> — Interrupt cleared or has not occurred<br><b>1</b> — Interrupt has occurred   |
| SYS_OVLO_I     | 4      | RW1C                | 0       | SYS_OVLO threshold crossed interrupt<br><b>0</b> — Interrupt cleared or has not occurred<br><b>1</b> — Interrupt has occurred   |
| UNUSED         | 7 to 5 | —                   | —       | Unused  |

[1] Read or Write 1 to clear the bit

Table 77. Register MISC\_INT\_MASK0- ADDR 0x29

| Name           | Bit | R/W               | Default | Description   |
|----------------|-----|-------------------|---------|---|
| PWRUP_M        | 0   | RW <sup>[1]</sup> | 1       | Mask for interrupt to indicate completion on transition from STANDBY to RUN and from SLEEP to RUN<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| PWRDN_M        | 1   | RW                | 1       | Mask for interrupt to indicate completion on transition from RUN to STANDBY and from RUN to SLEEP<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| PWRON_M        | 2   | RW                | 1       | Power on button event interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.  |
| LOW_SYS_WARN_M | 3   | RW                | 1       | LOW_SYS_WARN threshold crossed interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.   |

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Table 77. Register MISC\_INT\_MASK0- ADDR 0x29...continued

| Name       | Bit    | R/W | Default | Description   |
|------------|--------|-----|---------|---|
| SYS_OVLO_M | 4      | RW  | 1       | SYS_OVLO threshold crossed interrupt mask<br><b>0</b> — Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set.<br><b>1</b> — Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set. |
| UNUSED     | 7 to 5 | —   | —       | Unused  |

[1] Asynchronous Set, Read and Write

Table 78. Register MISC\_INT\_SENSE0 - ADDR 0x2A

| Name           | Bit    | R/W | Default | Description  |
|----------------|--------|-----|---------|--|
| PWRUP_S        | 0      | R   | 0       | Sense for interrupt to indicate completion on transition from STANDBY to RUN and from SLEEP to RUN<br><b>0</b> — Transition not in progress<br><b>1</b> — Transition in progress |
| PWRDN_S        | 1      | R   | 0       | Interrupt to indicate completion on transition from RUN to STANDBY and from RUN to SLEEP<br><b>0</b> — Transition not in progress<br><b>1</b> — Transition in progress           |
| PWRON_S        | 2      | R   | 0       | Power on button event interrupt sense<br><b>0</b> — PWRON low<br><b>1</b> — PWRON high   |
| LOW_SYS_WARN_S | 3      | R   | 0       | LOW_SYS_WARN threshold crossed interrupt sense<br><b>0</b> — SYS > LOW_SYS_WARN<br><b>1</b> — SYS < LOW_SYS_WARN   |
| SYS_OVLO_S     | 4      | R   | 0       | SYS_OVLO threshold crossed interrupt sense<br><b>0</b> — SYS < SYS_OVLO<br><b>1</b> — SYS > SYS_OVLO   |
| UNUSED         | 7 to 5 | —   | —       | Unused   |

Table 79. Register COINCELL\_CONTROL - ADDR 0x30

| Name     | Bit    | R/W | Default | Description   |
|----------|--------|-----|---------|---|
| VCOIN    | 3 to 0 | RW  | 0000    | Coin cell charger charging voltage<br><b>0000</b> — 1.8 V<br><b>0111</b> — 3.3 V (goes up in 100 mV step per LSB) |
| COINCHEN | 4      | RW  | 0       | Coin cell charger enable<br><b>0</b> — Charger disabled<br><b>1</b> — Charger enabled                             |
| UNUSED   | 7 to 5 | —   | —       | Unused  |

Table 80. Register SW1\_VOLT - ADDR 0x32

| Name     | Bit    | R/W                 | Default | Description   |
|----------|--------|---------------------|---------|---|
| SW1_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW1 voltage setting register (Run mode)<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings<br><b>Reset condition</b> — POR |
| UNUSED   | 7 to 5 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 81. Register SW1\_STBY\_VOLT - ADDR 0x33

| Name          | Bit    | R/W                 | Default | Description   |
|---------------|--------|---------------------|---------|---|
| SW1_STBY_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW1 output voltage setting register (Standby mode). The default value here should be identical to SW1_VOLT[5:0] register.<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings |
| UNUSED        | 7 to 6 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 82. Register SW1\_SLP\_VOLT - ADDR 0x34

| Name         | Bit    | R/W                 | Default | Description   |
|--------------|--------|---------------------|---------|---|
| SW1_SLP_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW1 output voltage setting register (Sleep mode). The default value here should be identical to SW1_VOLT[5:0] register.<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings |
| UNUSED       | 7 to 6 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 83. Register SW1\_CTRL - ADDR 0x35

| Name        | Bit | R/W                 | Default | Description  |
|-------------|-----|---------------------|---------|--|
| SW1_EN      | 0   | RW1S <sup>[1]</sup> | 0       | Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Run mode<br><b>1</b> — Regulator enabled in Run mode   |
| SW1_STBY_EN | 1   | RW1S                | 0       | Enables buck regulator in Standby mode. User can turn regulator off by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP).<br><b>0</b> — Regulator disabled in Standby mode<br><b>1</b> — Regulator enabled in Standby mode |
| SW1_OMODE   | 2   | RW <sup>[2]</sup>   | 0       | Enables buck regulator in Sleep mode. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Sleep mode<br><b>1</b> — Regulator enabled in Sleep mode   |

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Table 83. Register SW1\_CTRL - ADDR 0x35...continued

| Name            | Bit | R/W  | Default | Description   |
|-----------------|-----|------|---------|---|
| SW1_LPWR        | 3   | RW   | 0       | Enables the buck to enter Low-power mode during Standby and Sleep<br><b>0</b> — Regulator not in Low-power mode<br><b>1</b> — Regulator in Low-power mode during Standby or Sleep modes   |
| SW1_DVSSPEED    | 4   | RW1S | 0       | Controls slew rate of DVS transitions. Loaded from OTP and changeable by user after boot up. Not used when OTP_SW1_DVS_SEL = 1.<br><b>0</b> — DVS rate at 12.5 mV/2 $\mu$ s<br><b>1</b> — DVS rate at 12.5 mV/4 $\mu$ s   |
| SW1_FPWM_IN_DVS | 5   | RW   | 0       | Enables CCM operation during DVS down<br><b>0</b> — does not force FPWM during DVS<br><b>1</b> — forces regulator to track the DVS reference while it is falling rather than relying on the load current to pull the voltage low  |
| SW1_FPWM        | 6   | RW   | 0       | Forces buck to go into CCM mode<br><b>0</b> — Not in FPWM mode<br><b>1</b> — Forced in PWM mode irrespective of load current  |
| SW1_RDIS_ENB    | 7   | RW1S | 0       | Controls discharge resistor on output when regulator disabled<br><b>0</b> — Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge.<br><b>1</b> — Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor. |

[1] Load from OTP fuse, Read and Write

[2] Asynchronous Set, Read and Write

Table 84. Register SW1\_SLP\_VOLT - ADDR 0x36

| Name          | Bit    | R/W                 | Default | Description   |
|---------------|--------|---------------------|---------|---|
| SW1_ILIM      | 1 to 0 | RW1S <sup>[1]</sup> | 00      | Sets current limit of SW1 regulator<br><b>00</b> — Typical current limit of 1.0 A<br><b>01</b> — Typical current limit of 1.2 A<br><b>10</b> — Typical current limit of 1.5 A<br><b>11</b> — Typical current limit of 2.0 A |
| UNUSED        | 3 to 2 | —                   | —       | Unused  |
| SW1_TMODE_SEL | 4      | RW                  | 0       | <b>0</b> — TON control<br><b>1</b> — TOFF control   |
| UNUSED        | 7 to 5 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 85. Register SW2\_VOLT - ADDR 0x38

| Name     | Bit    | R/W                 | Default | Description   |
|----------|--------|---------------------|---------|---|
| SW2_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW2 voltage setting register (Run mode)<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings |
| UNUSED   | 7 to 6 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 86. Register SW2\_STBY\_VOLT - ADDR 0x39

| Name          | Bit    | R/W                 | Default | Description   |
|---------------|--------|---------------------|---------|---|
| SW2_STBY_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW2 output voltage setting register (Standby mode). The default value here should be identical to SW2_VOLT[5:0] register.<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings |
| UNUSED        | 7 to 6 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 87. Register SW2\_SLP\_VOLT - ADDR 0x3A

| Name         | Bit    | R/W                 | Default | Description   |
|--------------|--------|---------------------|---------|---|
| SW2_SLP_VOLT | 5 to 0 | RW1S <sup>[1]</sup> | —       | SW2 output voltage setting register (Sleep mode). The default value here should be identical to SW2_VOLT[5:0] register.<br><b>000000</b> — See <a href="#">Table 23</a> for voltage settings<br><b>111111</b> — See <a href="#">Table 23</a> for voltage settings |
| UNUSED       | 7 to 6 | —                   | —       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 88. Register SW2\_CTRL - ADDR 0x3B

| Name        | Bit | R/W                 | Default | Description  |
|-------------|-----|---------------------|---------|--|
| SW2_EN      | 0   | RW1S <sup>[1]</sup> | 0       | Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Run mode<br><b>1</b> — Regulator enabled in Run mode   |
| SW2_STBY_EN | 1   | RW1S                | 0       | Enables buck regulator in Standby mode. User can turn regulator off by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP).<br><b>0</b> — Regulator disabled in Standby mode<br><b>1</b> — Regulator enabled in Standby mode |
| SW2_OMODE   | 2   | RW                  | 0       | Enables buck regulator in Sleep mode. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Sleep mode<br><b>1</b> — Regulator enabled in Sleep mode   |

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Table 88. Register SW2\_CTRL - ADDR 0x3B...continued

| Name            | Bit | R/W  | Default | Description   |
|-----------------|-----|------|---------|---|
| SW2_LPWR        | 3   | RW   | 0       | Enables the buck to enter Low-power mode during Standby and Sleep modes<br><b>0</b> — Regulator not in Low-power mode<br><b>1</b> — Regulator in Low-power mode during Standby or Sleep   |
| SW2_DVSSPEED    | 4   | RW1S | 0       | Controls slew rate of DVS transitions. Loaded from OTP and changeable by user after boot up. Not used when OTP_SW2_DVS_SEL = 1.<br><b>0</b> — DVS rate at 12.5 mV/2 $\mu$ s<br><b>1</b> — DVS rate at 12.5 mV/4 $\mu$ s   |
| SW2_FPWM_IN_DVS | 5   | RW   | 0       | Enables CCM operation during DVS down<br><b>0</b> — does not force FPWM during DVS<br><b>1</b> — forces regulator to track the DVS reference while it is falling rather than relying on the load current to pull the voltage low  |
| SW2_FPWM        | 6   | RW   | 0       | Forces buck to go into CCM mode<br><b>0</b> — Not in FPWM mode<br><b>1</b> — Forced in PWM mode irrespective of load current.   |
| SW2_RDIS_ENB    | 7   | RW1S | 0       | Controls discharge resistor on output when regulator disabled<br><b>0</b> — Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge.<br><b>1</b> — Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor. |

[1] Load from OTP fuse, Read and Write

Table 89. Register SW2\_CTRL1 - ADDR 0x3C

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| SW2_ILIM      | 1 to 0 | RW1S | 00      | Sets current limit of SW2 regulator<br><b>00</b> — Typical current limit of 1.0 A<br><b>01</b> — Typical current limit of 1.2 A<br><b>10</b> — Typical current limit of 1.5 A<br><b>11</b> — Typical current limit of 2.0 A |
| UNUSED        | 3 to 2 | —    | —       | Unused  |
| SW2_TMODE_SEL | 4      | RW   | 0       | <b>0</b> — TON control<br><b>1</b> — TOFF control   |
| UNUSED        | 7 to 5 | —    | —       | Unused  |

Table 90. Register SW3\_VOLT - ADDR 0x3E

| Name     | Bit    | R/W  | Default | Description   |
|----------|--------|------|---------|---|
| SW3_VOLT | 3 to 0 | RW1S | —       | SW3 voltage setting register (Run mode). Loaded from fuses. Read only because DVS is not supported in this regulator.<br><b>0000</b> — See <a href="#">Table 29</a> for voltage settings<br><b>1111</b> — See <a href="#">Table 29</a> for voltage settings |
| UNUSED   | 7 to 4 | —    | —       | Unused  |

Table 91. Register SW3\_STBY\_VOLT - ADDR 0x3F

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| SW3_STBY_VOLT | 3 to 0 | RW1S | —       | SW3 voltage setting register (Standby mode). Loaded from fuses. Read only because DVS is not supported in this regulator.<br><b>0000</b> — See <a href="#">Table 29</a> for voltage settings<br><b>1111</b> — See <a href="#">Table 29</a> for voltage settings |
| UNUSED        | 7 to 4 | —    | —       | Unused  |

Table 92. Register SW3\_SLP\_VOLT - ADDR 0x40

| Name         | Bit    | R/W  | Default | Description   |
|--------------|--------|------|---------|---|
| SW3_SLP_VOLT | 3 to 0 | RW1S | —       | SW3 voltage setting register (Sleep mode). Loaded from fuses. Read only because DVS is not supported in this regulator.<br><b>0000</b> — See <a href="#">Table 29</a> for voltage settings<br><b>1111</b> — See <a href="#">Table 29</a> for voltage settings |
| UNUSED       | 7 to 4 | —    | —       | Unused  |

Table 93. Register SW3\_CTRL - ADDR 0x41

| Name        | Bit | R/W  | Default | Description  |
|-------------|-----|------|---------|--|
| SW3_EN      | 0   | RW1S | 0       | Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Run mode<br><b>1</b> — Regulator enabled in Run mode   |
| SW3_STBY_EN | 1   | RW1S | 0       | Enables buck regulator in Standby mode. User can turn regulator off by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP).<br><b>0</b> — Regulator disabled in Standby mode<br><b>1</b> — Regulator enabled in Standby mode |
| SW3_OMODE   | 2   | RW   | 0       | Enables buck regulator in Sleep mode. User can turn regulator off by clearing this bit.<br><b>0</b> — Regulator disabled in Sleep mode<br><b>1</b> — Regulator enabled in Sleep mode   |
| SW3_LPWR    | 3   | RW   | 0       | Enables the buck to enter Low-power mode during Standby and Sleep modes<br><b>0</b> — Regulator not in Low-power mode<br><b>1</b> — Regulator in Low-power mode while in Standby or Sleep  |

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Table 93. Register SW3\_CTRL - ADDR 0x41...continued

| Name         | Bit | R/W  | Default | Description  |
|--------------|-----|------|---------|--|
| UNUSED       | 4   | —    | —       | Unused   |
| UNUSED       | 5   | —    | —       | Unused   |
| SW3_FPWM     | 6   | RW   | 0       | Forces buck to go into CCM mode<br><b>0</b> — Not in FPWM mode<br><b>1</b> — Forced in PWM mode irrespective of load current   |
| SW3_RDIS_ENB | 7   | RW1S | 0       | Controls discharge resistor on output when regulator is disabled<br><b>0</b> — Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge.<br><b>1</b> — Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor. |

Table 94. Register SW3\_CTRL1 - ADDR 0x42

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| SW3_ILIM      | 1 to 0 | RW1S | 00      | Sets current limit of SW3 regulator<br><b>00</b> — Typical current limit of 1.0 A<br><b>01</b> — Typical current limit of 1.2 A<br><b>10</b> — Typical current limit of 1.5 A<br><b>11</b> — Typical current limit of 2.0 A |
| UNUSED        | 3 to 2 | —    | —       | Unused  |
| SW3_TMODE_SEL | 4      | RW   | 0       | <b>0</b> — TON control<br><b>1</b> — TOFF control   |
| UNUSED        | 7 to 5 | —    | —       | Unused  |

Table 95. Register VSNVS\_CTRL - ADDR 0x48

| Name       | Bit    | R/W  | Default | Description  |
|------------|--------|------|---------|--|
| VSNVS_VOLT | 2 to 0 | RW1S | 000     | Not used in PF1510. Placeholder for future products.   |
| CLKPULSE   | 3      | RW   | 0       | Optional bit used for evaluation. Refer to IP block  |
| FORCEBOS   | 4      | RW   | 0       | Optional bit for evaluation<br><b>0</b> — BOS circuit activated only when VSYS < UVDET<br><b>1</b> — Forces best of supply circuit irrespective of UVDET   |
| LIBGDIS    | 5      | RW   | 0       | Use to reduce quiescent current in coin cell mode<br><b>0</b> — VSNVS local bandgap enabled in coin cell mode<br><b>1</b> — VSNVS local bandgap disabled in coin cell mode to save quiescent current |
| UNUSED     | 7 to 6 | —    | —       | Unused   |



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Table 96. Register VREFDDR\_CTRL - ADDR 0x4A

| Name            | Bit    | R/W  | Default | Description  |
|-----------------|--------|------|---------|--|
| VREFDDR_EN      | 0      | RW1S | 0       | <b>0</b> — Disables VREFDDR regulator<br><b>1</b> — Enables VREFDDR regulator. This is set by the OTP sequence.  |
| VREFDDR_STBY_EN | 1      | RW1S | 0       | The default value for this should be same as VREFDDREN<br><b>0</b> — Disables VREFDDR regulator in Standby mode<br><b>1</b> — Enables VREFDDR regulator in Standby mode if VREFDDREN = 1 |
| VREFDDR_OMODE   | 2      | RW   | 0       | <b>0</b> — Keeps VREFDDR off in Off mode<br><b>1</b> — Enables VREFDDR in Sleep mode if VREFDDREN = 1  |
| VREFDDR_LPWR    | 3      | RW   | 0       | <b>0</b> — Disables VREFDDR Low-power mode<br><b>1</b> — Enables VREFDDR Low-power mode  |
| UNUSED          | 7 to 4 | —    | —       | Unused   |

Table 97. Register LDO1\_VOLT - ADDR 0x4C

| Name      | Bit    | R/W  | Default | Description  |
|-----------|--------|------|---------|--|
| LDO1_VOLT | 4 to 0 | RW1S | —       | LDO1 output voltage setting register. Loaded from OTP.<br><b>00000</b> — See <a href="#">Table 33</a> for voltage settings<br><b>11111</b> — See <a href="#">Table 33</a> for voltage settings |
| UNUSED    | 7 to 5 | —    | —       | Unused   |

Table 98. Register LDO1\_CTRL - ADDR 0x4D

| Name          | Bit    | R/W  | Default | Description  |
|---------------|--------|------|---------|--|
| VLDO1_EN      | 0      | RW1S | 0       | Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator                    |
| VLDO1_STBY_EN | 1      | RW1S | 0       | Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator  |
| VLDO1_OMODE   | 2      | RW   | 0       | Enables LDO in Sleep mode<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator   |
| VLDO1_LPWR    | 3      | RW   | 0       | Forces LDO to Low-power mode in Sleep and Standby modes<br><b>0</b> — Not in Low-power mode during Standby and Sleep<br><b>1</b> — Regulator in Low-power mode during Standby and Sleep                      |
| LDO1_LS_EN    | 4      | RW1S | 0       | This is loaded from OTP_LDOy_LS_EN and changeable from 0 to 1 on power up. Changing from 1 to 0 is not allowed.<br><b>0</b> — Sets LDOy in LDO mode<br><b>1</b> — Sets LDOy to a load switch (fully on) mode |
| UNUSED        | 7 to 5 | —    | —       | Unused   |

Table 99. Register LDO2\_VOLT - ADDR 0x4F

| Name      | Bit    | R/W  | Default | Description  |
|-----------|--------|------|---------|--|
| LDO2_VOLT | 3 to 0 | RW1S | —       | LDO2 output voltage setting register. Loaded from OTP.<br><b>0000</b> — See <a href="#">Table 35</a> for voltage settings<br><b>1111</b> — See <a href="#">Table 35</a> for voltage settings |
| UNUSED    | 7 to 4 | —    | —       | Unused   |

Table 100. Register LDO2\_CTRL - ADDR 0x50

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| VLDO2_EN      | 0      | RW1S | 0       | Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator |
| VLDO2_STBY_EN | 1      | RW1S | 0       | Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator                                       |
| VLDO2_OMODE   | 2      | RW   | 0       | Enables LDO in Sleep mode<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator  |
| VLDO2_LPWR    | 3      | RW   | 0       | Forces LDO to Low-power mode in Sleep and Standby modes<br><b>0</b> — Not in Low-power mode during Standby and Sleep<br><b>1</b> — Regulator in Low-power mode during Standby and Sleep   |
| UNUSED        | 7 to 4 | —    | —       | Unused  |

Table 101. Register LDO3\_VOLT - ADDR 0x52

| Name      | Bit    | R/W  | Default | Description  |
|-----------|--------|------|---------|--|
| LDO3_VOLT | 4 to 0 | RW1S | —       | LDO3 output voltage setting register. Loaded from OTP.<br><b>00000</b> — See <a href="#">Table 33</a> for voltage settings<br><b>11111</b> — See <a href="#">Table 33</a> for voltage settings |
| UNUSED    | 7 to 5 | —    | —       | Unused   |

Table 102. Register LDO3\_CTRL - ADDR 0x53

| Name          | Bit | R/W  | Default | Description   |
|---------------|-----|------|---------|---|
| VLDO3_EN      | 0   | RW1S | 0       | Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn regulator off by clearing this bit.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator |
| VLDO3_STBY_EN | 1   | RW1S | 0       | Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN.<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator                                       |

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Table 102. Register LDO3\_CTRL - ADDR 0x53...continued

| Name        | Bit    | R/W  | Default | Description  |
|-------------|--------|------|---------|--|
| VLDO3_OMODE | 2      | RW   | 0       | Enables LDO in Sleep mode<br><b>0</b> — Disables regulator<br><b>1</b> — Enables regulator   |
| VLDO3_LPWR  | 3      | RW   | 0       | Forces LDO to Low-power mode in Sleep and Standby modes<br><b>0</b> — Not in Low-power mode during Standby and Sleep<br><b>1</b> — Regulator in Low-power mode during Standby and Sleep                      |
| LDO3_LS_EN  | 4      | RW1S | 0       | This is loaded from OTP_LDOy_LS_EN and changeable from 0 to 1 on power up. Changing from 1 to 0 is not allowed.<br><b>0</b> — Sets LDOy in LDO mode<br><b>1</b> — Sets LDOy to a load switch (fully on) mode |
| UNUSED      | 7 to 5 | —    | —       | Unused   |

Table 103. Register PWRCTRL0 - ADDR 0x58

| Name       | Bit    | R/W  | Default | Description  |
|------------|--------|------|---------|--|
| STANDBYDLY | 1 to 0 | RW   | 01      | Controls delay of Standby pin after synchronization<br><b>0</b> — No additional delay<br><b>1</b> — 32 kHz cycle additional delay<br><b>2</b> — 32 kHz cycle additional delay<br><b>3</b> — 32 kHz cycle additional delay  |
| STANDBYINV | 2      | RW   | 0       | Controls polarity of STANDBY pin<br><b>0</b> — Standby pin input active high<br><b>1</b> — Standby pin input active low  |
| POR_DLY    | 5 to 3 | RW1S | 000     | Controls delay of RESETBMCU pin after power up (loaded from OTP)<br><b>000</b> — RESETBMCU goes high 2 ms after last regulator<br><b>010</b> — RESETBMCU goes high 4 ms after last regulator<br><b>011</b> — RESETBMCU goes high 8 ms after last regulator<br><b>100</b> — RESETBMCU goes high 16 ms after last regulator<br><b>101</b> — RESETBMCU goes high 128 ms after last regulator<br><b>110</b> — RESETBMCU goes high 256 ms after last regulator<br><b>111</b> — RESETBMCU goes high 1024 ms after last regulator |
| TGRESET    | 7 to 6 | RW1S | 00      | Controls duration for which ONKEY has to be pushed low for a global reset (part goes to REGS_DISABLE)<br><b>00</b> — 4 s<br><b>01</b> — 8 s<br><b>10</b> — 12 s<br><b>11</b> — 16 s  |

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Table 104. Register PWRCTRL1 - ADDR 0x59

| Name         | Bit    | R/W | Default | Description   |
|--------------|--------|-----|---------|---|
| PWRONDBNC    | 1 to 0 | RW  | 00      | Controls debounce of PWRON when in push button mode (PWRON_CFG = 1)<br><b>00</b> — 31.25 ms falling edge; 31.25 ms rising edge<br><b>01</b> — 31.25 ms falling edge; 31.25 ms rising edge<br><b>10</b> — 125 ms falling edge; 31.25 ms rising edge<br><b>11</b> — 750 ms falling edge; 31.25 ms rising edge |
| ONKEYDBNC    | 3 to 2 | RW  | 00      | Controls debounce of ONKEY push button<br><b>00</b> — 31.25 ms falling edge; 31.25 ms rising edge<br><b>01</b> — 31.25 ms falling edge; 31.25 ms rising edge<br><b>10</b> — 125 ms falling edge; 31.25 ms rising edge<br><b>11</b> — 750 ms falling edge; 31.25 ms rising edge                              |
| PWRONRSTEN   | 4      | RW  | 0       | Enables going to REGS_DISABLE or Sleep mode when PWRON_CFG = 1. See <a href="#">Section 10 "PF1510 state machine"</a> for details.<br><b>0</b> — Long press on PWRON button does not take state to REGS_DISABLE or Sleep<br><b>1</b> — Long press on PWRON button takes state to REGS_DISABLE or Sleep      |
| RESTARTEN    | 5      | RW  | 0       | Enables restart of system when PWRON push button is held low for 5 s<br><b>0</b> — No impact<br><b>1</b> — When going to REGS_DISABLE via a long press of PWRON button, holding it low for 1 more second takes state back to RUN (equally, a 5 second push restarts the system)                             |
| REGSCPEN     | 6      | RW  | 0       | Shuts down LDO if it enters a current limit fault. Controls LDO1, LDO2 and LDO3.<br><b>0</b> — LDO does not shutdown in the event of a current limit fault. Continues to limit current.<br><b>1</b> — LDO is turned off when it encounters a current limit fault  |
| ONKEY_RST_EN | 7      | RW  | 1       | Enables turning off of system via ONKEY. See <a href="#">Section 10 "PF1510 state machine"</a> for details.<br><b>0</b> — ONKEY cannot be used to turn off or restart system<br><b>1</b> — ONKEY can be used to turn off or restart system  |

Table 105. Register PWRCTRL2 - ADDR 0x5A

| Name         | Bit    | R/W  | Default | Description   |
|--------------|--------|------|---------|---|
| UVDET        | 1 to 0 | RW1S | 00      | Sets UVDET threshold<br><b>00</b> — Rising 2.65 V; falling 2.55 V<br><b>01</b> — Rising 2.8 V; falling 2.7 V<br><b>10</b> — Rising 3.0 V; falling 2.9 V<br><b>11</b> — Rising 3.1 V; falling 3.0 V      |
| LOW_SYS_WARN | 3 to 2 | RW   | 00      | Sets LOW_SYS_WARN threshold<br><b>00</b> — Rising 3.3 V; falling 3.1 V<br><b>01</b> — Rising 3.5 V; falling 3.3 V<br><b>10</b> — Rising 3.7 V; falling 3.5 V<br><b>11</b> — Rising 3.9 V; falling 3.7 V |

Table 105. Register PWRCTRL2 - ADDR 0x5A...continued

| Name   | Bit    | R/W | Default | Description |
|--------|--------|-----|---------|-------------|
| UNUSED | 7 to 4 | —   | —       | Unused      |

Table 106. Register PWRCTRL3 - ADDR 0x5B

| Name          | Bit    | R/W | Default | Description  |
|---------------|--------|-----|---------|--|
| UNUSED        | 0      | RW  | 0       | Unused   |
| GOTO_CORE_OFF | 1      | RW  | 0       | Set this bit to go to CORE_OFF mode once in REGS_DISABLE state<br><b>0</b> — No impact<br><b>1</b> — PF1510 gracefully enters CORE_OFF mode when in REGS_DISABLE state |
| UNUSED        | 7 to 2 | —   | —       | Unused   |

Table 107. Register SW1\_PWRDN\_SEQ - ADDR 0x5F

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| SW1_PWRDN_SEQ | 2 to 0 | RW1S | 000     | This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.<br>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].<br>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once. |
| UNUSED        | 7 to 3 | —    | —       | Unused  |

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Table 108. Register SW2\_PWRDN\_SEQ - ADDR 0x60

| Name          | Bit    | R/W  | Default | Description  |
|---------------|--------|------|---------|--|
| SW2_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED        | 7 to 3 | —    | —       | Unused   |

Table 109. Register SW2\_PWRDN\_SEQ - ADDR 0x61

| Name          | Bit    | R/W  | Default | Description  |
|---------------|--------|------|---------|--|
| SW3_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED        | 7 to 3 | —    | —       | Unused   |

Table 110. Register LDO1\_PWRDN\_SEQ - ADDR 0x62

| Name           | Bit    | R/W  | Default | Description  |
|----------------|--------|------|---------|--|
| LDO1_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED         | 7 to 3 | —    | —       | Unused   |

Table 111. Register LDO2\_PWRDN\_SEQ - ADDR 0x63

| Name           | Bit    | R/W  | Default | Description  |
|----------------|--------|------|---------|--|
| LDO2_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED         | 7 to 3 | —    | —       | Unused   |

Table 112. Register LDO3\_PWRDN\_SEQ - ADDR 0x64

| Name           | Bit    | R/W  | Default | Description  |
|----------------|--------|------|---------|--|
| LDO3_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED         | 7 to 3 | —    | —       | Unused   |

Table 113. Register VREFDDR\_PWRDN\_SEQ - ADDR 0x65

| Name              | Bit    | R/W  | Default | Description  |
|-------------------|--------|------|---------|--|
| VREFDDR_PWRDN_SEQ | 2 to 0 | RW1S | 000     | <p>This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers.</p> <p>xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].</p> <p>When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.</p> |
| UNUSED            | 7 to 3 | —    | —       | Unused   |



Table 114. Register STATE\_INFO - ADDR 0x67

| Name   | Bit    | R/W | Default | Description  |
|--------|--------|-----|---------|--|
| STATE  | 5 to 0 | R   | 000000  | Indicates machine state<br><b>000000</b> — Wait state<br><b>001100</b> — Run state<br><b>001101</b> — Standby state<br><b>001110</b> — Sleep/LPSR state<br><b>101011</b> — REGS_DISABLE state<br>Other bits are reserved |
| UNUSED | 7 to 6 | —   | —       | Unused   |

Table 115. Register I2C\_ADDR - ADDR 0x68

| Name                    | Bit    | R/W | Default | Description   |
|-------------------------|--------|-----|---------|---|
| I2C_SLAVE_ADDR_L<br>SBS | 2 to 0 | R   | 000     | Loaded from fuses. But read only in functional space.<br><b>000</b> — Slave Address: 0x08<br><b>001</b> — Slave Address: 0x09<br><b>010</b> — Slave Address: 0x0A<br><b>011</b> — Slave Address: 0x0B<br><b>100</b> — Slave Address: 0x0C<br><b>101</b> — Slave Address: 0x0D<br><b>110</b> — Slave Address: 0x0E<br><b>111</b> — Slave Address: 0x0F |
| USE_DEFAULT_ADDR        | 7      | RW  | 0       | DEFAULT ADDR  |

Table 116. Register RC\_16MHZ - ADDR 0x6B

| Name            | Bit    | R/W | Default | Description   |
|-----------------|--------|-----|---------|---|
| REQ_16MHZ       | 0      | RW  | 0       | Enables 16 MHz clock<br><b>0</b> — 16 MHz clock enable controlled by state machine<br><b>1</b> — 16 MHz clock always enabled                                      |
| REQ_ACORE_ON    | 1      | RW  | 0       | Controls Analog core enable<br><b>0</b> — Analog core enable controlled by state machine<br><b>1</b> — Analog core always on                                      |
| REQ_ACORE_HIPWR | 2      | RW  | 0       | Controls Low-power mode of the analog core<br><b>0</b> — Analog core Low-power mode controlled by state machine<br><b>1</b> — Analog core never in Low-power mode |
| UNUSED          | 7 to 3 | —   | —       | Unused  |

Table 117. Register KEY1 - ADDR 0x6B

| Name | Bit    | R/W | Default | Description |
|------|--------|-----|---------|-------------|
| KEY1 | 7 to 0 | RW  | 0x00    | Unused      |

## 12.2 Specific Registers (Offset is 0x80)

Table 118. Register INT - ADDR 0x00

| Name  | Bit | R/W                 | Default | Description   |
|-------|-----|---------------------|---------|---|
| RSVD0 | 0   | RW1S <sup>[1]</sup> | 0       | Unused  |
| RSVD1 | 1   |                     |         |   |
| RSVD2 | 2   |                     |         |   |
| RSVD3 | 3   |                     |         |   |
| RSVD4 | 4   |                     |         |   |
| VIN_I | 5   | RW1S                | 0       | VIN interrupt<br><b>0</b> — The VIN_OK interrupt has not occurred or been cleared<br><b>1</b> — The VIN_OK interrupt has occurred<br><b>Reset condition</b> — VCOREDIG_RSTB |
| RSVD6 | 6   | RW1S                | 0       | Unused  |
| RSVD7 | 7   | RW1S                | 0       | Unused  |

[1] Load from OTP fuse, Read and Write

Table 119. Register INT\_MASK - ADDR 0x02

| Name  | Bit | R/W | Default | Description  |
|-------|-----|-----|---------|--|
| RSVD0 | 0   | RW  | 1       | Unused   |
| RSVD1 | 1   |     |         |  |
| RSVD2 | 2   |     |         |  |
| RSVD3 | 3   |     |         |  |
| RSVD4 | 4   |     |         |  |
| VIN_M | 5   | RW  | 1       | VIN interrupt mask<br><b>0</b> — Unmasked<br><b>1</b> — Masked<br><b>Reset condition</b> — VCOREDIG_RSTB |
| RSVD6 | 6   | RW  | 1       | Unused   |
| RSVD7 | 7   | RW  | 1       | Unused   |

Table 120. Register INT\_OK - ADDR 0x04

| Name  | Bit | R/W | Default | Description |
|-------|-----|-----|---------|-------------|
| RSVD0 | 0   | R   | 0       | Unused      |
| RSVD1 | 1   |     | 0       |             |
| RSVD2 | 2   |     | 1       |             |
| RSVD3 | 3   |     | 0       |             |
| RSVD4 | 4   |     | 0       |             |

Table 120. Register INT\_OK - ADDR 0x04...continued

| Name   | Bit | R/W | Default | Description  |
|--------|-----|-----|---------|--|
| VIN_OK | 5   | R   | 0       | Single bit VIN status indicator. See VIN_SNS for more information.<br><b>0</b> — The VIN input is invalid. For example, VIN_VALID = 0.<br><b>1</b> — The VIN input is valid. For example, VIN_VALID = 1.<br><b>Reset condition</b> — VCOREDIG_RSTB |
| RSVS6  | 6   | R   | 0       | Unused   |
| RSVD7  | 7   | R   | 1       | Unused   |

Table 121. Register VIN\_SNS - ADDR 0x06

| Name         | Bit    | R/W | Default | Description  |
|--------------|--------|-----|---------|--|
| RSVD[1:0]    | 1 to 0 | R   | 00      | Unused   |
| VIN_UVLO_SNS | 2      | R   | 1       | <b>0</b> — VIN > VIN_UVLO<br><b>1</b> — VIN < VIN_UVLO or when VIN is detached   |
| VIN2SYS_SNS  | 3      | R   | 1       | <b>0</b> — VIN > VSYS + VIN2SYS<br><b>1</b> — VIN < VSYS + VIN2SYS   |
| VIN_OVLO_SNS | 4      | R   | 0       | <b>0</b> — VIN < VIN_OVLO<br><b>1</b> — VIN > VIN_OVLO   |
| VIN_VALID    | 5      | R   | 0       | <b>0</b> — VIN is not valid<br><b>1</b> — VIN is valid, VIN > VIN_UVLO, VIN > VSYS + VIN2SYS, VIN < VIN_OVLO<br><b>Reset condition</b> — VCOREDIG_RSTB |
| RSVD6        | 6      | R   | 0       | Unused   |
| RSVD7        | 7      | R   | 0       | Unused   |

Table 122. Register FRONT\_END\_OPER- ADDR 0x09

| Name         | Bit    | R/W                 | Default | Description  |
|--------------|--------|---------------------|---------|--|
| FRONT_END_ON | 1 to 0 | RW1S <sup>[1]</sup> | 01      | Front-end LDO operation configuration<br><b>0</b> — Front-end LDO is OFF<br><b>1</b> — Front-end LDO is ON<br><b>2</b> — Reserved<br><b>3</b> — Reserved<br><b>Reset condition</b> — VCOREDIG_RSTB |
| RSVD2        | 2      | RW                  | 0       | Unused   |
| RSVD3        | 3      |                     | 0       |  |
| RSVD4        | 4      |                     | 0       |  |
| RSVD[7:5]    | 7 to 5 |                     | 000     |  |

[1] Load from OTP fuse, Read and Write

Table 123. Register FRONT\_END\_REG - ADDR 0x0F

| Name      | Bit    | R/W  | Default | Description  |
|-----------|--------|------|---------|--|
| RSVD[5:0] | 5 to 0 | RW1S | 101011  | Unused   |
| VSYSMIN   | 7 to 6 | RW1S | 00      | Minimum system regulation voltage ( $V_{SYS_{MIN}}$ )<br><b>0</b> — 3.5 V<br><b>1</b> — 3.7 V<br><b>2</b> — 4.3 V<br><b>3</b> — Reserved<br><b>Reset condition</b> — VCOREDIG_RSTB |

Table 124. Register VIN\_INLIM\_CNFG - ADDR 0x14

| Name      | Bit    | R/W  | Default | Description   |
|-----------|--------|------|---------|---|
| RSVD[2:0] | 2 to 0 | RW   | 000     | Unused  |
| VIN_ILIM  | 7 to 3 | RW1S | 01101   | Maximum input current limit selection. 5 bit adjustment from 10 mA to 1500 mA.<br><b>0</b> — 10 mA<br><b>1</b> — 15 mA<br><b>2</b> — 20 mA<br><b>3</b> — 25 mA<br><b>4</b> — 30 mA<br><b>5</b> — 35 mA<br><b>6</b> — 40 mA<br><b>7</b> — 45 mA<br><b>8</b> — 50 mA<br><b>9</b> — 100 mA<br><b>10</b> — 150 mA<br><b>11</b> — 200 mA<br><b>12</b> — 300 mA<br><b>13</b> — 400 mA<br><b>14</b> — 500 mA<br><b>15</b> — 600 mA<br><b>16</b> — 700 mA<br><b>17</b> — 800 mA<br><b>18</b> — 900 mA<br><b>19</b> — 1000 mA<br><b>20</b> — 1500 mA<br><b>21</b> — Reserved<br><b>22</b> — Reserved<br><b>23</b> — Reserved<br><b>24</b> — Reserved<br><b>25</b> — Reserved<br><b>26</b> — Reserved<br><b>27</b> — Reserved<br><b>28</b> — Reserved<br><b>29</b> — Reserved<br><b>30</b> — Reserved<br><b>31</b> — Reserved<br><b>Reset condition</b> — CHGPOK_RSTB |

Table 125. Register USB\_PHY\_LDO\_CNFG - ADDR 0x16

| Name      | Bit    | R/W  | Default | Description   |
|-----------|--------|------|---------|---|
| RSVD0     | 0      | RW1S | 1       | Unused  |
| USBPHY    | 1      | RW1S | 0       | USBPHY voltage setting register<br><b>0</b> — 3.3 V<br><b>1</b> — 4.9 V<br><b>Reset condition</b> — VCOREDIG_RSTB |
| USBPHYLDO | 2      | RW1S | 0       | USBPHY LDO enable<br><b>0</b> — Disabled<br><b>1</b> — Enabled<br><b>Reset condition</b> — VCOREDIG_RSTB          |
| RSVD3     | 3      | RW   | 0       | Unused  |
| RSVD[5:4] | 5 to 4 |      | 00      |   |
| RSVD[7:6] | 7 to 6 |      | 00      |   |

Table 126. Register DBNC\_DELAY\_TIME - ADDR 0x18

| Name         | Bit    | R/W  | Default | Description   |
|--------------|--------|------|---------|---|
| VIN_OV_TDB   | 1 to 0 | RW1S | 00      | VIN overvoltage debounce delay<br><b>0</b> — 10 $\mu$ s (reserved)<br><b>1</b> — 100 $\mu$ s<br><b>2</b> — 1 ms<br><b>3</b> — 10 ms<br><b>Reset condition</b> — VCOREDIG_RSTB |
| USB_PHY_TDB  | 3 to 2 | RW1S | 00      | USBPHY debounce timer - not used in PF1510<br><b>0</b> — 0 ms<br><b>1</b> — 16 ms<br><b>2</b> — 32 ms<br><b>3</b> — Not used<br><b>Reset condition</b> — VCOREDIG_RSTB        |
| SYS_WKUP_DLY | 5 to 4 | RW1S | 00      | System wake-up time<br><b>0</b> — 8.0 ms<br><b>1</b> — 16 ms<br><b>2</b> — 32 ms<br><b>3</b> — 100 ms<br><b>Reset condition</b> — VCOREDIG_RSTB                               |
| RSVD[7:6]    | 7 to 6 | RW   | 00      | Unused  |

Table 127. Register VIN2SYS\_CNFG - ADDR 0x1B

| Name          | Bit    | R/W  | Default | Description   |
|---------------|--------|------|---------|---|
| VIN2SYS_TDB   | 1 to 0 | RW1S | 00      | VIN to VSYS comparator debounce time<br><b>0</b> — Reserved<br><b>1</b> — 100 μs<br><b>2</b> — 1 ms<br><b>3</b> — 10 ms<br><b>Reset condition</b> — VCOREDIG_RSTB |
| VIN2SYS_THRSH | 2      | RW1S | 0       | VIN to VSYS comparator threshold setting<br><b>0</b> — 50 mV<br><b>1</b> — 175 mV<br><b>Reset condition</b> — VCOREDIG_RSTB                                       |
| RSVD[7:3]     | 7 to 3 | RW   | 00000   | Unused  |

### 12.3 Register PMIC bitmap

|                                      |
|--------------------------------------|
| VCOREDIG_PORB <sup>[1]</sup>         |
| PS_END_RSTB <sup>[2]</sup>           |
| REGS_DISABLE_TOG_RSTB <sup>[3]</sup> |

- [1] Bits reset by invalid VCOREDIG
- [2] Bits reset by PORB or RESETBMCU
- [3] Bits reset by pulse to REGS\_DISABLE mode

Table 128. Register PMIC bitmap

| Address | Register name | BITS[7:0] |                 |          |                     |         |                |                      |          |          |
|---------|---------------|-----------|-----------------|----------|---------------------|---------|----------------|----------------------|----------|----------|
|         |               | 7         | 6               | 5        | 4                   | 3       | 2              | 1                    | 0        |          |
| 0x00    | DEVICE_ID     | Name      | FAMILY[3:7]     |          |                     |         | DEVICE_ID[2:0] |                      |          |          |
|         |               | Reset     | 0               | 1        | 1                   | 1       | 1              | 0                    | 0        |          |
|         |               | Type      | R               | R        | R                   | R       | R              | R                    | R        |          |
| 0x01    | OTP_FLAVOR    | Name      | OTP_FLAVOR[5:0] |          |                     |         |                |                      |          |          |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 0                    | 0        |          |
|         |               | Type      | —               | —        | R                   | R       | R              | R                    | R        | R        |
| 0x02    | SILICON_REV   | Name      | FAB_FIN[7:6]    |          | FULL_LAYER_REV[5:3] |         |                | METAL_LAYER_REV[2:0] |          |          |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 1              | 0                    | 0        | 0        |
|         |               | Type      | R               | R        | R                   | R       | R              | R                    | R        | R        |
| 0x06    | INT_CATEGORY  | Name      | MISC_INT        | TEMP_INT | ONKEY_INT           | LDO_INT | SW3_INT        | SW2_INT              | SW1_INT  | VIN_INT  |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 0                    | 0        | 0        |
|         |               | Type      | R               | R        | R                   | R       | R              | R                    | R        | R        |
| 0x08    | SW_INT_STAT0  | Name      | —               | —        | —                   | —       | —              | SW3_LS_I             | SW2_LS_I | SW1_LS_I |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 0                    | 0        | 0        |
|         |               | Type      | —               | —        | —                   | —       | —              | RW1C                 | RW1C     | RW1C     |
| 0x09    | SW_INT_MASK0  | Name      | —               | —        | —                   | —       | —              | SW3_LS_M             | SW2_LS_M | SW1_LS_M |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 1                    | 1        | 1        |
|         |               | Type      | —               | —        | —                   | —       | —              | RW                   | RW       | RW       |
| 0x0A    | SW_INT_SENSE0 | Name      | —               | —        | —                   | —       | —              | SW3_LS_S             | SW2_LS_S | SW1_LS_S |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 0                    | 0        | 0        |
|         |               | Type      | —               | —        | —                   | —       | —              | R                    | R        | R        |
| 0x0B    | SW_INT_STAT1  | Name      | —               | —        | —                   | —       | —              | SW3_HS_I             | SW2_HS_I | SW1_HS_I |
|         |               | Reset     | 0               | 0        | 0                   | 0       | 0              | 0                    | 0        | 0        |

Power management integrated circuit (PMIC) for low power application processors

Table 128. Register PMIC bitmap...continued

| Address | Register name    |       | BITS[7:0] |   |           |            |                |           |             |                |                |
|---------|------------------|-------|-----------|---|-----------|------------|----------------|-----------|-------------|----------------|----------------|
|         |                  |       | 7         | 6 | 5         | 4          | 3              | 2         | 1           | 0              |                |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW1C        | RW1C           | RW1C           |
| 0x0C    | SW_INT_MASK1     | Name  | —         | — | —         | —          | —              | —         | SW3_HS_M    | SW2_HS_M       | SW1_HS_M       |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 1           | 1              | 1              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW          | RW             | RW             |
| 0x0D    | SW_INT_SENSE1    | Name  | —         | — | —         | —          | —              | —         | SW3_HS_S    | SW2_HS_S       | SW1_HS_S       |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | R           | R              | R              |
| 0x0E    | SW_INT_STAT2     | Name  | —         | — | —         | —          | —              | —         | —           | SW2_DVS_DONE_I | SW1_DVS_DONE_I |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | —           | RW1C           | RW1C           |
| 0x0F    | SW_INT_MASK2     | Name  | —         | — | —         | —          | —              | —         | —           | SW2_DVS_DONE_M | SW1_DVS_DONE_M |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 1              | 1              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | —           | RW             | RW             |
| 0x10    | SW_INT_SENSE2    | Name  | —         | — | —         | —          | —              | —         | —           | SW2_DVS_S      | SW1_DVS_S      |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | —           | R              | R              |
| 0x18    | LDO_INT_STAT0    | Name  | —         | — | —         | —          | —              | —         | LDO3_FAULTI | LDO2_FAULTI    | LDO1_FAULTI    |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW1C        | RW1C           | RW1C           |
| 0x19    | LDO_INT_MASK0    | Name  | —         | — | —         | —          | —              | —         | LDO3_FAULTM | LDO2_FAULTM    | LDO1_FAULTM    |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 1           | 1              | 1              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW          | RW             | RW             |
| 0x1A    | LDO_INT_SENSE0   | Name  | —         | — | —         | —          | —              | —         | LDO3_FAULTS | LDO2_FAULTS    | LDO1_FAULTS    |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | R           | R              | R              |
| 0x20    | TEMP_INT_STAT0   | Name  | —         | — | —         | —          | —              | —         | THERM125I   | —              | THERM110I      |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW1C        | —              | RW1C           |
| 0x21    | TEMP_INT_MASK0   | Name  | —         | — | —         | —          | —              | —         | THERM125M   | —              | THERM110M      |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 1         | 1           | 1              | 1              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | RW          | —              | RW             |
| 0x22    | TEMP_INT_SENSE0  | Name  | —         | — | —         | —          | —              | —         | THERM125S   | —              | THERM110S      |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              | 0              |
|         |                  | Type  | —         | — | —         | —          | —              | —         | R           | —              | R              |
| 0x24    | ONKEY_INT_STAT0  | Name  | —         | — | ONKEY_8SI | ONKEY_4SI  | ONKEY_3SI      | ONKEY_2SI | ONKEY_1SI   | ONKEY_PUSHI    |                |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              |                |
|         |                  | Type  | —         | — | RW1C      | RW1C       | RW1C           | RW1C      | RW1C        | RW1C           |                |
| 0x25    | ONKEY_INT_MASK0  | Name  | —         | — | ONKEY_8SM | ONKEY_4SM  | ONKEY_3SM      | ONKEY_2SM | ONKEY_1SM   | ONKEY_PUSHM    |                |
|         |                  | Reset | 0         | 0 | 1         | 1          | 1              | 1         | 1           | 1              |                |
|         |                  | Type  | —         | — | RW        | RW         | RW             | RW        | RW          | RW             |                |
| 0x26    | ONKEY_INT_SENSE0 | Name  | —         | — | ONKEY_8SS | ONKEY_4SS  | ONKEY_3SS      | ONKEY_2SS | ONKEY_1SS   | ONKEY_PUSHS    |                |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              |                |
|         |                  | Type  | —         | — | R         | R          | R              | R         | R           | R              |                |
| 0x28    | MISC_INT_STAT0   | Name  | —         | — | —         | SYS_OVLO_I | LOW_SYS_WARN_I | PWRON_I   | PWRDN_I     | PWRUP_I        |                |
|         |                  | Reset | 0         | 0 | 0         | 0          | 0              | 0         | 0           | 0              |                |
|         |                  | Type  | —         | — | —         | RW1C       | RW1C           | RW1C      | RW1C        | RW1C           |                |

Power management integrated circuit (PMIC) for low power application processors

Table 128. Register PMIC bitmap...continued

| Address | Register name    |       | BITS[7:0]          |          |                     |               |                |           |               |         |
|---------|------------------|-------|--------------------|----------|---------------------|---------------|----------------|-----------|---------------|---------|
|         |                  |       | 7                  | 6        | 5                   | 4             | 3              | 2         | 1             | 0       |
| 0x29    | MISC_INT_MASK0   | Name  | —                  | —        | —                   | SYS_OVLO_M    | LOW_SYS_WARN_M | PWRON_M   | PWRDN_M       | PWRUP_M |
|         |                  | Reset | 0                  | 0        | 0                   | 1             | 1              | 1         | 1             | 1       |
|         |                  | Type  | —                  | —        | —                   | RW            | RW             | RW        | RW            | RW      |
| 0x2A    | MISC_INT_SENSE0  | Name  | —                  | —        | —                   | SYS_OVLO_S    | LOW_SYS_WARN_S | PWRON_S   | PWRDN_S       | PWRUP_S |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | R             | R              | R         | R             | R       |
| 0x30    | COINCELL_CONTROL | Name  |                    |          | COINCHEN VCOIN[3:0] |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | RW            | RW             | RW        | RW            | RW      |
| 0x32    | SW1_VOLT         | Name  | SW1_VOLT[5:0]      |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x33    | SW1_STBY_VOLT    | Name  | SW1_STBY_VOLT[5:0] |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x34    | SW1_SLP_VOLT     | Name  | SW1_SLP_VOLT[5:0]  |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x35    | SW1_CTRL         | Name  | SW1_RDIS_ENB       | SW1_FPWM | SW1_FPWM_IN_DVS     | SW1_DVSSPEED  | SW1_LPWR       | SW1_OMODE | SW1_STBY_EN   | SW1_EN  |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | RW1S               | RW       | RW                  | RW1S          | RW             | RW        | RW1S          | RW1S    |
| 0x36    | SW1_CTRL1        | Name  | —                  | —        | —                   | SW1_TMODE_SEL | —              | —         | SW1_ILIM[1:0] |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | RW            | —              | —         | RW1S          | RW1S    |
| 0x38    | SW2_VOLT         | Name  | SW2_VOLT[5:0]      |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x39    | SW2_STBY_VOLT    | Name  | SW2_STBY_VOLT[5:0] |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x3A    | SW2_SLP_VOLT     | Name  | SW2_SLP_VOLT[5:0]  |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | RW1S                | RW1S          | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x3B    | SW2_CTRL         | Name  | SW2_RDIS_ENB       | SW2_FPWM | SW2_FPWM_IN_DVS     | SW2_DVSSPEED  | SW2_LPWR       | SW2_OMODE | SW2_STBY_EN   | SW2_EN  |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | RW1S               | RW       | RW                  | RW1S          | RW             | RW        | RW1S          | RW1S    |
| 0x3C    | SW2_CTRL1        | Name  | —                  | —        | —                   | SW2_TMODE_SEL | —              | —         | SW2_ILIM[1:0] |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | RW            | —              | —         | RW1S          | RW1S    |
| 0x3E    | SW3_VOLT         | Name  | SW3_VOLT[3:0]      |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | —             | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x3F    | SW3_STBY_VOLT    | Name  | SW3_STBY_VOLT[3:0] |          |                     |               |                |           |               |         |
|         |                  | Reset | 0                  | 0        | 0                   | 0             | 0              | 0         | 0             | 0       |
|         |                  | Type  | —                  | —        | —                   | —             | RW1S           | RW1S      | RW1S          | RW1S    |
| 0x40    | SW3_SLP_VOLT     | Name  | SW3_SLP_VOLT[3:0]  |          |                     |               |                |           |               |         |



Power management integrated circuit (PMIC) for low power application processors

Table 128. Register PMIC bitmap...continued

| Address | Register name | BITS[7:0] |              |          |              |                |                    |                 |                 |               |
|---------|---------------|-----------|--------------|----------|--------------|----------------|--------------------|-----------------|-----------------|---------------|
|         |               | 7         | 6            | 5        | 4            | 3              | 2                  | 1               | 0               |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW1S               | RW1S            | RW1S            | RW1S          |
| 0x41    | SW3_CTRL      | Name      | SW3_RDIS_ENB | SW3_FPWM | —            | SW3_DVSSPEED   | SW3_LPWR           | SW3_OMODE       | SW3_STBY_EN     | SW3_EN        |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | RW1S         | RW       | —            | RW1S           | RW                 | RW              | RW1S            | RW1S          |
|         |               | Name      | —            | —        | —            | SW3_TMODE_SEL  | —                  | —               | SW3_ILIM[1:0]   |               |
| 0x42    | SW3_CTRL1     | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | RW             | —                  | —               | RW1S            | RW1S          |
| 0x48    | VSNVS_CTRL    | Name      | —            | —        | LIBGDIS      | FORCEBOS       | CLKPULSE           | VSNVS_VOLT[2:0] |                 |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | RW           | RW             | RW                 | RW1S            | RW1S            | RW1S          |
|         |               | Name      | —            | —        | —            | —              | VREFDDR_LPWR       | VREFDDR_OMODE   | VREFDDR_STBY_EN | VREFDDR_EN    |
| 0x4A    | VREFDDR_CTRL  | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW                 | RW              | RW1S            | RW1S          |
| 0x4C    | LDO1_VOLT     | Name      | —            | —        | —            | LDO1_VOLT[4:0] |                    |                 |                 |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | RW1S           | RW1S               | RW1S            | RW1S            | RW1S          |
|         |               | Name      | —            | —        | —            | LDO1_LS_EN     | LDO1_LPWR          | LDO1_OMODE      | LDO1_STB_Y_EN   | VLDO1_EN      |
| 0x4D    | LDO1_CTRL     | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | RW1S           | RW                 | RW              | RW1S            | RW1S          |
| 0x4F    | LDO2_VOLT     | Name      | —            | —        | —            | LDO2_VOLT[3:0] |                    |                 |                 |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW1S               | RW1S            | RW1S            | RW1S          |
|         |               | Name      | —            | —        | —            | —              | LDO2_LPWR          | LDO2_OMODE      | LDO2_STB_Y_EN   | VLDO2_EN      |
| 0x50    | LDO2_CTRL     | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW                 | RW              | RW1S            | RW1S          |
| 0x52    | LDO3_VOLT     | Name      | —            | —        | —            | LDO3_VOLT[4:0] |                    |                 |                 |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW1S               | RW1S            | RW1S            | RW1S          |
|         |               | Name      | —            | —        | —            | LDO3_LS_EN     | LDO3_LPWR          | LDO3_OMODE      | LDO3_STB_Y_EN   | VLDO3_EN      |
| 0x53    | LDO3_CTRL     | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW1S               | RW              | RW              | RW1S          |
| 0x58    | PWRCTRL0      | Name      | TGRESET[7:6] |          | POR_DLY[5:3] |                |                    | STANDBYINV      | STANDBYDLY[1:0] |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 1             |
|         |               | Type      | RW1S         | RW1S     | RW1S         | RW1S           | RW1S               | RW              | RW              | RW            |
|         |               | Name      | ONKEY_RST_EN | REGSCPEN | RESTARTEN    | PWRONRSTEN     | ONKEYDBNC[3:2]     |                 | PWRONDBNC[1:0]  |               |
| 0x59    | PWRCTRL1      | Reset     | 1            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | RW           | RW       | RW           | RW             | RW                 | RW              | RW              | RW            |
| 015A    | PWRCTRL2      | Name      | —            | —        | —            | —              | LOW_SYS_WARN[3:2]  |                 | UVDET[1:0]      |               |
|         |               | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | —            | —        | —            | —              | RW                 | RW              | RW1S            | RW1S          |
|         |               | Name      | —            |          |              |                |                    |                 |                 | GOTO_CORE_OFF |
| 0x5B    | PWRCTRL3      | Reset     | 0            | 0        | 0            | 0              | 0                  | 0               | 0               | 0             |
|         |               | Type      | RW           | RW       | RW           | RW             | RW                 | RW              | RW              | RW            |
| 0x5F    | SW1_PWRDN_SEQ | Name      | —            | —        | —            | —              | SW1_PWRDN_SEQ[2:0] |                 |                 |               |

Power management integrated circuit (PMIC) for low power application processors

Table 128. Register PMIC bitmap...continued

| Address | Register name     | BITS[7:0] |                  |    |            |    |    |                          |              |           |
|---------|-------------------|-----------|------------------|----|------------|----|----|--------------------------|--------------|-----------|
|         |                   | 7         | 6                | 5  | 4          | 3  | 2  | 1                        | 0            |           |
|         |                   | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            | 0         |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | SW2_PWRDN_SEQ[2:0]       |              |           |
| 0x60    | SW2_PWRDN_SEQ     | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | SW3_PWRDN_SEQ[2:0]       |              |           |
| 0x61    | SW3_PWRDN_SEQ     | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | LDO1_PWRDN_SEQ[2:0]      |              |           |
| 0x62    | LDO1_PWRDN_SEQ    | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | LDO2_PWRDN_SEQ[2:0]      |              |           |
| 0x63    | LDO2_PWRDN_SEQ    | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | LDO3_PWRDN_SEQ[2:0]      |              |           |
| 0x64    | LDO3_PWRDN_SEQ    | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | —          | —  | —  | VREFDDR_PWRDN_SEQ[2:0]   |              |           |
| 0x65    | VREFDDR_PWRDN_SEQ | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW1S                     | RW1S         | RW1S      |
|         |                   | Name      | —                | —  | STATE[5:0] |    |    |                          |              |           |
| 0x67    | STATE_INFO        | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | R          | R  | R  | R                        | R            | R         |
|         |                   | Name      | USE_DEFAULT_ADDR | —  | —          | —  | —  | I2C_SLAVE_ADDR_LSBS[2:0] |              |           |
| 0x68    | I2C_ADDR          | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | RW               | —  | —          | —  | —  | R                        | R            | R         |
|         |                   | Name      | —                | —  | —          | —  | —  | —                        | —            | —         |
| 0x69    | IO_DRV0           | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | —                        | —            |           |
|         |                   | Name      | —                | —  | —          | —  | —  | —                        | —            | —         |
| 0x6A    | IO_DRV1           | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | —                        | —            |           |
|         |                   | Name      | —                | —  | —          | —  | —  | REQ_ACORE_HIPWR          | REQ_ACORE_ON | REQ_16MHZ |
| 0x6B    | RC_16MHZ          | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | —                | —  | —          | —  | —  | RW                       | RW           | RW        |
|         |                   | Name      | KEY1[7:0]        |    |            |    |    |                          |              |           |
| 0x6F    | KEY1              | Reset     | 0                | 0  | 0          | 0  | 0  | 0                        | 0            |           |
|         |                   | Type      | RW               | RW | RW         | RW | RW | RW                       | RW           | RW        |

### 12.4 Additional register bitmap

CHGPOK\_RSTB <sup>[1]</sup>  
 VCOREDIG\_RSTB <sup>[2]</sup>

- [1] Bits reset by invalid VIN
- [2] Bits reset by invalid VCOREDIG

**Table 129. Additional register bitmap**

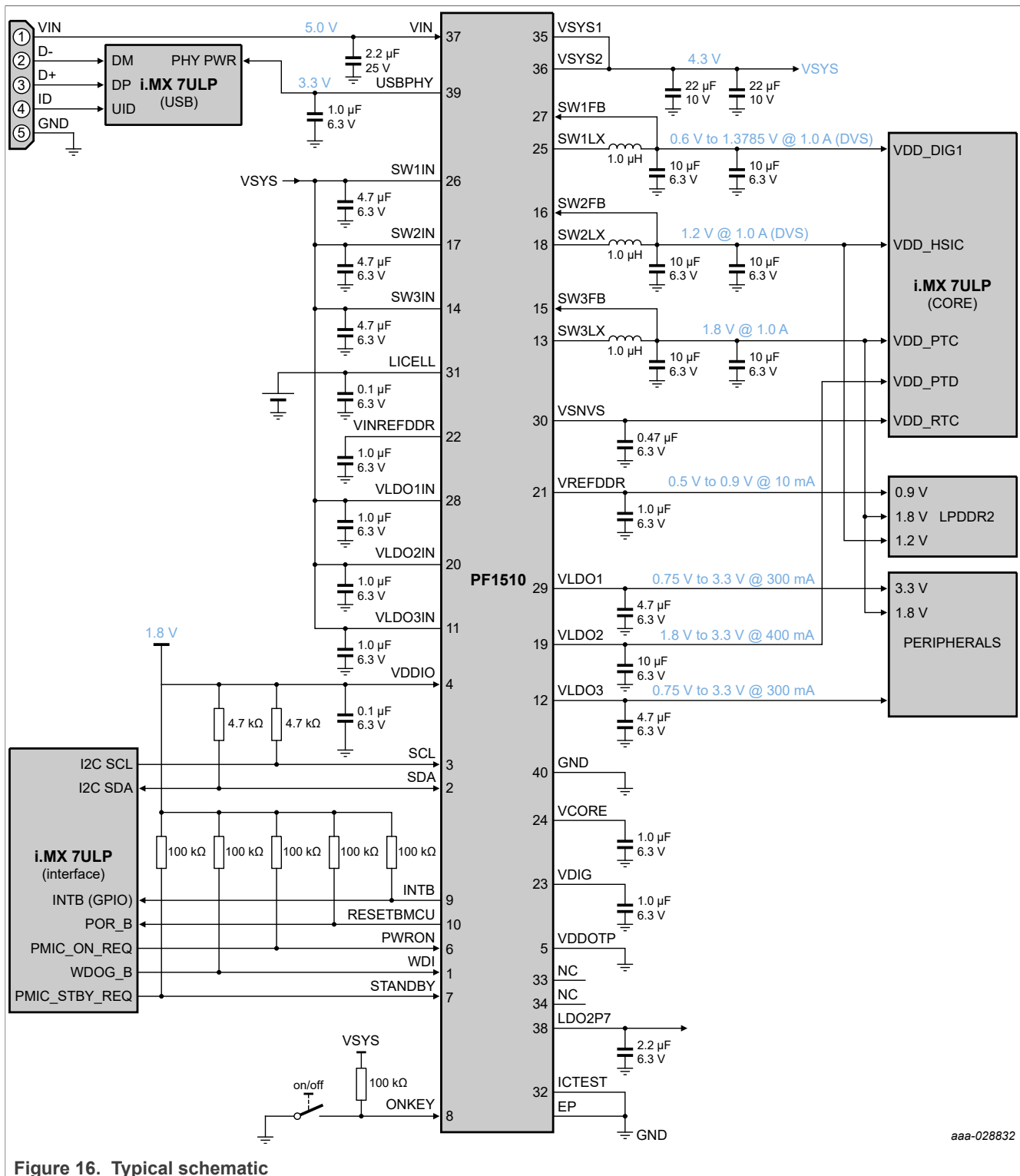
| Address | Register name    | BITS[7:0] |               |       |                   |              |                  |                  |                   |       |
|---------|------------------|-----------|---------------|-------|-------------------|--------------|------------------|------------------|-------------------|-------|
|         |                  | 7         | 6             | 5     | 4                 | 3            | 2                | 1                | 0                 |       |
| 0x00    | INT              | Name      | RSVD7         | RSVD6 | VIN_I             | RSVD4        | RSVD3            | RSVD2            | RSVD1             | RSVD0 |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 0                | 0                | 0                 | 0     |
|         |                  | Type      | RW1C          | RW1C  | RW1C              | RW1C         | RW1C             | RW1C             | RW1C              | RW1C  |
| 0x02    | INT_MASK         | Name      | RSVD7         | RSVD6 | VIN_M             | RSVD4        | RSVD3            | RSVD2            | RSVD1             | RSVD0 |
|         |                  | Reset     | 1             | 1     | 1                 | 1            | 1                | 1                | 1                 | 1     |
|         |                  | Type      | RW            | RW    | RW                | RW           | RW               | RW               | RW                | RW    |
| 0x04    | INT_OK           | Name      | RSVD7         | RSVD6 | VIN_OK            | RSVD4        | RSVD3            | RSVD2            | RSVD1             | RSVD0 |
|         |                  | Reset     | 1             | 0     | 0                 | 0            | 0                | 1                | 0                 | 0     |
|         |                  | Type      | R             | R     | R                 | R            | R                | R                | R                 | R     |
| 0x06    | VIN_SNS          | Name      | RSVD7         | RSVD6 | VIN2SYS_SNS       | VIN_OVLO_SNS | VIN_IN2SYS_SNS   | VIN_UVLO_SNS     | RSVD[1:0]         |       |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 1                | 1                | 0                 | 0     |
|         |                  | Type      | R             | R     | R                 | R            | R                | R                | R                 | R     |
| 0x09    | FRONT_END_OPER   | Name      | RSVD[7:5]     |       |                   | RSVD4        | RSVD3            | RSVD2            | FRONT_END_ON[1:0] |       |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 0                | 0                | 0                 | 1     |
|         |                  | Type      | RW            | RW    | RW                | RW           | RW               | RW               | RW1S              | RW1S  |
| 0x0F    | FRONT_END_REG    | Name      | VSYSMIN[7:6]  |       |                   | RSVD[5:0]    |                  |                  |                   |       |
|         |                  | Reset     | 0             | 0     | 1                 | 0            | 1                | 0                | 1                 | 1     |
|         |                  | Type      | RW1S          | RW1S  | RW1S              | RW1S         | RW1S             | RW1S             | RW1S              | RW1S  |
| 0x14    | VIN_INLIM_CNFG   | Name      | VIN_ILIM[7:3] |       |                   |              | RSVD[2:0]        |                  |                   |       |
|         |                  | Reset     | 0             | 1     | 1                 | 0            | 1                | 0                | 0                 | 0     |
|         |                  | Type      | RW1S          | RW1S  | RW1S              | RW1S         | RW1S             | RW               | RW                | RW    |
| 0x16    | USB_PHY_LDO_CNFG | Name      | RSVD[7:6]     |       | RSVD[5:4]         |              | RSVD3            | USBPHYLDO        | USBPHY            | RSVD0 |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 0                | 0                | 0                 | 1     |
|         |                  | Type      | RW            | RW    | RW                | RW           | RW               | RW1S             | RW1S              | RW1S  |
| 0x18    | DBNC_DELAY_TIME  | Name      | RSVD[7:6]     |       | SYS_WKUP_DLY[5:4] |              | USB_PHY_TDB[3:2] |                  | VIN_OV_TDB[1:0]   |       |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 0                | 0                | 0                 | 0     |
|         |                  | Type      | RW            | RW    | RW1S              | RW1S         | RW1S             | RW1S             | RW1S              | RW1S  |
| 0x1B    | VIN2SYS_CNFG     | Name      | RSVD[7:3]     |       |                   |              | VIN2SYS_THRSH    | VIN2SYS_TDB[1:0] |                   |       |
|         |                  | Reset     | 0             | 0     | 0                 | 0            | 0                | 0                | 0                 | 0     |
|         |                  | Type      | RW            | RW    | RW                | RW           | RW               | RW1S             | RW1S              | RW1S  |

## 13 Application details

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### 13.1 Example schematic

[Figure 16](#) shows a typical schematic of the PF1510 with key external components.



aaa-028832

Figure 16. Typical schematic

### 13.2 Bill of materials

The table below shows an example bill of materials to be used with the PF1510.

Table 130. Bill of materials

| Block   | Function                 | Description                                 | Qty |
|---------|--------------------------|---|-----|
| VCORE   | Analog IC supply         | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
| VDIG    | Digital IC supply        | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
| LDO2P7  | Analog supply            | CAP CER 2.2 $\mu$ F 6.3 V 20% X5R 0201      | 1   |
| USBPHY  | USB PHY output capacitor | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
| VIN     | VIN bypass capacitor     | CAP CER 2.2 $\mu$ F 25 V 20 % X5R 0402      | 1   |
| VSYS    | VSYS capacitor           | 22 $\mu$ F, 10 V, MLCC, X5R                 | 2   |
| VDDIO   | VDDIO bypass capacitor   | CAP CER 0.1 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
| Buck 1  | BUCK1 inductor           | 1.0 $\mu$ H, +/-20 %, 120 mOhm typ, 1700 mA | 1   |
|         | BUCK1 input capacitor    | 4.7 $\mu$ F, 6.3 V, MLCC, X5R               | 1   |
|         | BUCK1 output capacitor   | 10 $\mu$ F, 6.3 V, MLCC, X5R                | 2   |
| Buck 2  | BUCK2 inductor           | 1.0 $\mu$ H, +/-20 %, 120 mOhm typ, 1700 mA | 1   |
|         | BUCK2 input capacitor    | 4.7 $\mu$ F, 6.3 V, MLCC, X5R               | 1   |
|         | BUCK2 output capacitor   | 10 $\mu$ F, 6.3V, MLCC, X5R                 | 2   |
| Buck 3  | BUCK3 inductor           | 1.0 $\mu$ H, +/-20 %, 120 mOhm typ, 1700 mA | 1   |
|         | BUCK3 input capacitor    | 4.7 $\mu$ F, 6.3 V, MLCC, X5R               | 1   |
|         | BUCK3 output capacitor   | 10 $\mu$ F, 6.3 V, MLCC, X5R                | 2   |
| LDO1    | LDO1 input capacitor     | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
|         | LDO1 output capacitor    | 4.7 $\mu$ F, 6.3 V, MLCC, X5R               | 1   |
| LDO2    | LDO2 input capacitor     | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
|         | LDO2 output capacitor    | 10 $\mu$ F, 6.3 V, MLCC, X5R                | 1   |
| LDO3    | LDO3 input capacitor     | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
|         | LDO3 output capacitor    | 4.7 $\mu$ F, 6.3 V, MLCC, X5R               | 1   |
| VREFDDR | VREFDDR input capacitor  | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
|         | VREFDDR output capacitor | CAP CER 1.0 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |
| VSNVS   | VSNVS output capacitor   | CAP CER 0.47 $\mu$ F 6.3 V 20 % X5R 0201    | 1   |
| LICELL  | LICELL bypass capacitor  | CAP CER 0.1 $\mu$ F 6.3 V 20 % X5R 0201     | 1   |

### 13.3 PF1510 layout guidelines

#### 13.3.1 General board recommendations

- It is recommended to use an eight layer board stack-up arranged as follows:
  - High current signal
  - GND
  - Signal
  - Power
  - Power
  - Signal
  - GND

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**Power management integrated circuit (PMIC) for low power application processors**

- Allocate TOP and BOTTOM PCB layers for POWER ROUTING (high current signals), copper-pour the unused area.
- Use internal layers sandwiched between two GND planes for the SIGNAL routing.

**13.3.2 Component placement**

It is desirable to keep all component related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

**13.3.3 General routing requirements**

- Some recommended things to keep in mind for manufacturability:
  - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
  - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
  - Minimum allowed spacing between line and hole pad is 3.5 mils
  - Minimum allowed spacing between line and line is 3.0 mils
- Care must be taken with SWx<sub>FB</sub> pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the SWx<sub>IN</sub>, SWx<sub>LX</sub>. They could be also shielded.
- Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
- Avoid coupling traces between important signal/low noise supplies (like V<sub>CORE</sub>, V<sub>DIG</sub>) from any switching node (for example, SW1<sub>LX</sub>, SW2<sub>LX</sub>, SW3<sub>LX</sub>).
- Make sure that all components related to a specific block are referenced to the corresponding ground.

**13.3.4 Parallel routing requirements**

- I<sup>2</sup>C signal routing
  - CLK is the fastest signal of the system, so it must be given special care.
  - To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.
  - These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
  - Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

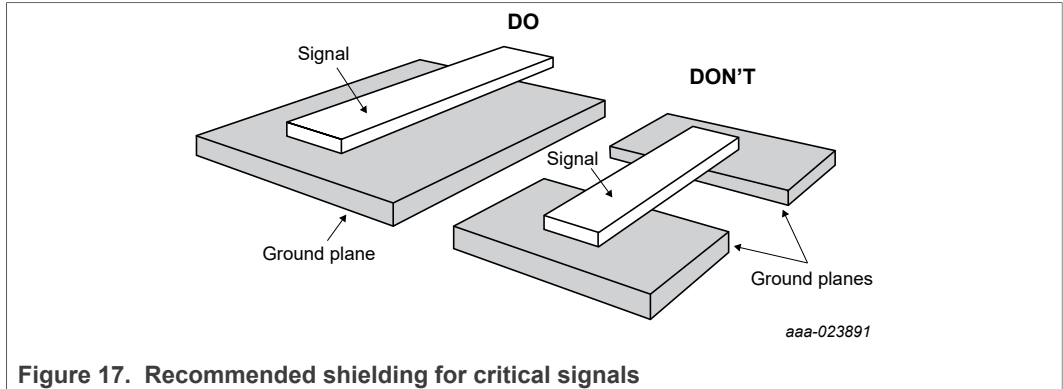


Figure 17. Recommended shielding for critical signals

13.3.5 Switching regulator layout recommendations

- Per design, the switching regulators in PF1510 are designed to operate with only one input bulk capacitor. However, it is recommended to add a high frequency filter input capacitor ( $C_{IN\_hf}$ ), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
- Make high-current ripple traces low-inductance (short, high W/L ratio).
- Make high-current traces wide or copper islands.

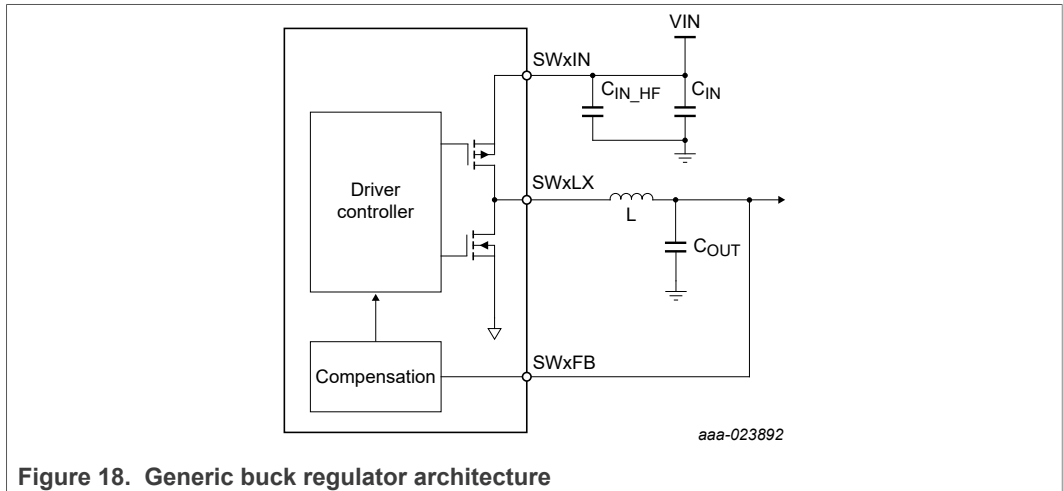


Figure 18. Generic buck regulator architecture



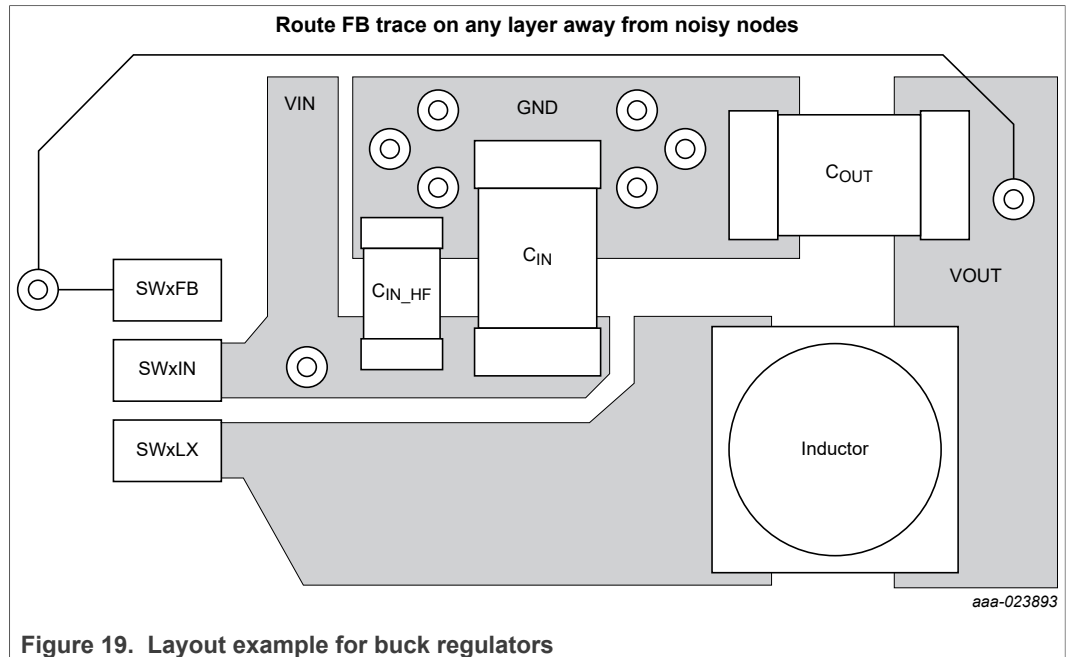


Figure 19. Layout example for buck regulators

## 13.4 Thermal information

### 13.4.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in [Table 3](#).

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol  $R_{\theta JA}$  or  $\theta_{JA}$  (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment.  $R_{\theta JMA}$  or  $\theta_{JMA}$  (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used.

The JEDEC standards can be consulted at <http://www.jedec.org/>.

### 13.4.2 Estimation of junction temperature

An estimation of the chip junction temperature  $T_J$  can be obtained from the equation:  $T_J = T_A + (R_{\theta JA} \times P_D)$  with:

$T_A$  = Ambient temperature for the package in °C

$R_{\theta JA}$  = Junction to ambient thermal resistance in °C/W

$P_D$  = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board  $R_{\theta JA}$  and the value obtained on a four layer board  $R_{\theta JMA}$ . Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

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**Power management integrated circuit (PMIC) for low power application processors**

At a known board temperature, the junction temperature  $T_J$  is estimated using the following equation  $T_J = T_B + (R_{\theta_{JB}} \times P_D)$  with

$T_B$  = Board temperature at the package perimeter in °C

$R_{\theta_{JB}}$  = Junction to board thermal resistance in °C/W

$P_D$  = Power dissipation in the package in W

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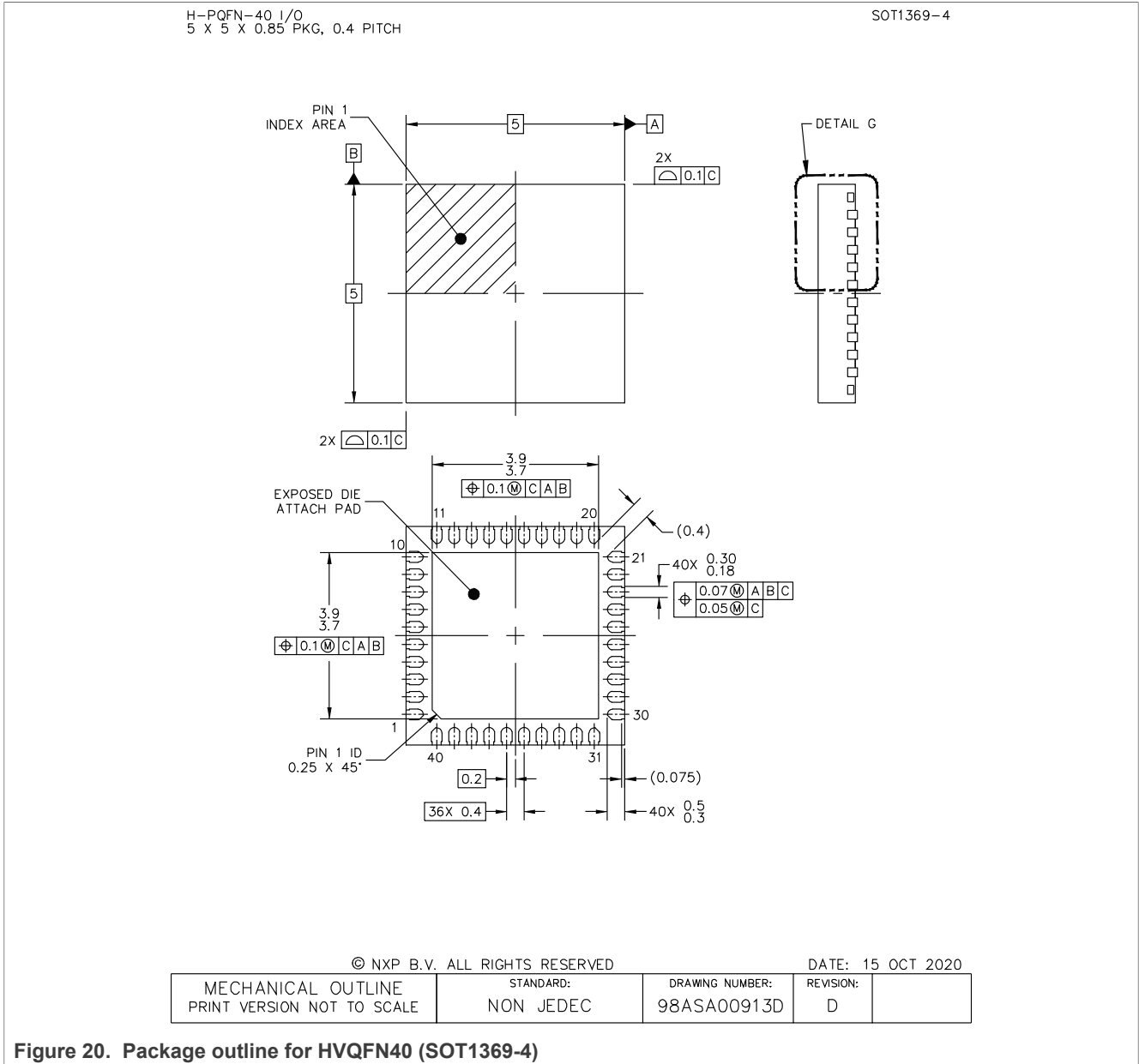
## 14 Packaging information

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The PF1510 uses a 40 QFN 5.0 mm x 5.0 mm with exposed pad, case number 98ASA00913D.

### 14.1 Packaging description

This drawing is available for download at <http://www.nxp.com>. Consult the most recently issued drawing before initiating or completing a design.



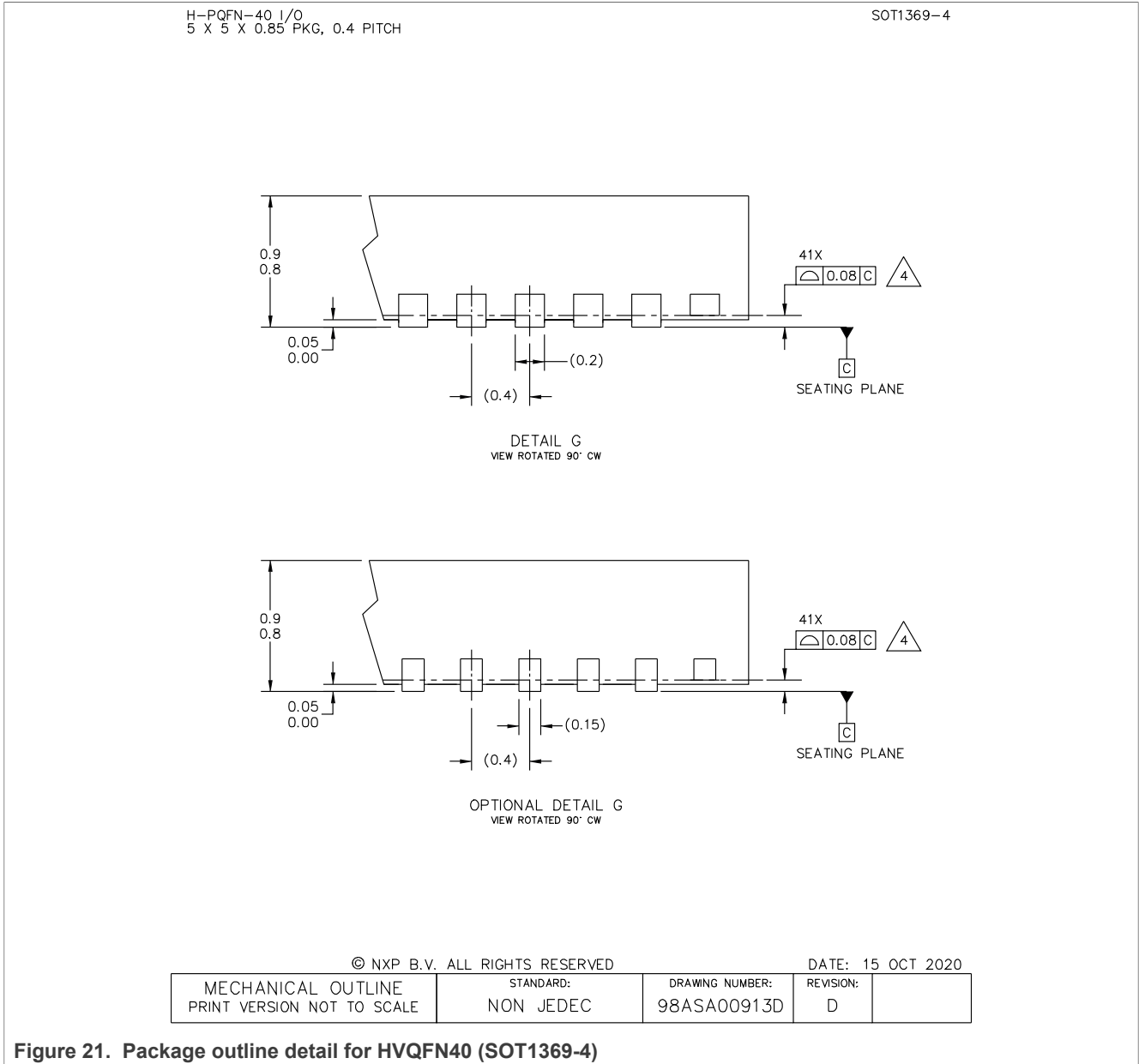



Figure 21. Package outline detail for HVQFN40 (SOT1369-4)

Power management integrated circuit (PMIC) for low power application processors

H-PQFN-40 I/O  
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-4

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

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DATE: 15 OCT 2020

|  |                        |                                |                |  |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA00913D | REVISION:<br>D |  |
|--|------------------------|--------------------------------|----------------|--|

Figure 22. Package outline notes for HVQFN40 (SOT1369-4)

## 15 Revision history

Table 131. Revision history

| Document ID   | Release date  | Data sheet status   | Change notice    | Supersedes   |
|---------------|---|---------------------|------------------|--------------|
| PF1510 v.4.0  | 20210305  | Product             | PCN 202012012F01 | PF1510 v.3.0 |
| Modifications | <ul style="list-style-type: none"> <li>• <a href="#">Section 14.1</a>: added "Optional Detail G with 0.15 mm lead edge package option" to package outline drawings</li> </ul>   |                     |                  |              |
| PF1510 v.3.0  | 20200407  | Product             | CIN 2020040011   | PF1510 v.2.0 |
| Modifications | <ul style="list-style-type: none"> <li>• <a href="#">Table 1</a>: added MC32PF1510A0EP and MC34PF1510A0EP (non-programmed parts)</li> </ul>   |                     |                  |              |
| PF1510 v.2.0  | 20190524  | Product             | CIN 2019040341   | PF1510 v.1.0 |
| Modifications | <ul style="list-style-type: none"> <li>• Changed data sheet status from advanced information to product</li> <li>• <a href="#">Table 2</a>, pin 38                             <ul style="list-style-type: none"> <li>– Changed Recommended connection from "Bypass with 1.0 capacitor to ground" to "Bypass with 2.2 μF capacitor to ground mandatory"</li> <li>– Changed Recommended connection when not used from "Leave floating" to "Bypass with 2.2 μF capacitor to ground mandatory"</li> </ul> </li> <li>• <a href="#">Section 7.5</a> <ul style="list-style-type: none"> <li>– Changed "It derives its power from either VSYS or a coin cell (only if the COIN_CELL bit is set)." to "It derives its power from either VSYS or a coin cell."</li> <li>– Changed "Upon subsequent removal of VSYS, with the coin cell attached and COIN_CELL set, VSNVS..." to "Upon subsequent removal of VSYS, with the coin cell attached, VSNVS..."</li> </ul> </li> <li>• <a href="#">Table 45</a> <ul style="list-style-type: none"> <li>– Changed <math>V_{IL}</math> max from "0.2 * VSNVS" to "0.4"</li> <li>– Changed <math>V_{IH}</math> min from "0.8 * VSNVS" to "1.4"</li> </ul> </li> <li>• Added <a href="#">Table 46</a></li> <li>• Added <a href="#">Table 47</a></li> <li>• <a href="#">Table 49</a> <ul style="list-style-type: none"> <li>– Changed <math>V_{IL}</math> max from "0.2 * VSYS" to "0.4"</li> <li>– Changed <math>V_{IH}</math> min from "0.8 * VSYS" to "1.4"</li> <li>– Changed "3.6" to "4.8"</li> </ul> </li> <li>• <a href="#">Figure 15</a> <ul style="list-style-type: none"> <li>– Removed step-down from VSYS and VSNVS lines</li> </ul> </li> <li>• <a href="#">Figure 16</a> <ul style="list-style-type: none"> <li>– Terminal 38, changed capacitor value from 1.0 μF to 2.2 μF</li> </ul> </li> <li>• <a href="#">Table 125</a> <ul style="list-style-type: none"> <li>– Changed USBPHYLDO description from "0 — Enabled" to "1 — Enabled"</li> </ul> </li> </ul> |                     |                  |              |
| PF1510 v.1.0  | 20180523  | Advance information | —                | —            |

## 16 Legal information

### 16.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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