Single Supply 3.0 V to 44 V Operational Amplifiers

MC34071,2,4,A
MC33071,2,4,A,
NCV33072,4,A

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74, NCV33072/74A series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

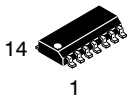
The MC33071/72/74, MC34071/72/74, NCV33072/74,A series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic SOIC, QFN and TSSOP surface mount packages.

Features

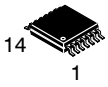
- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

SOIC−8
D SUFFIX
CASE 751

WQFN10
MT SUFFIX
CASE 510AJ



SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DTB SUFFIX
CASE 948G

ORDERING INFORMATION

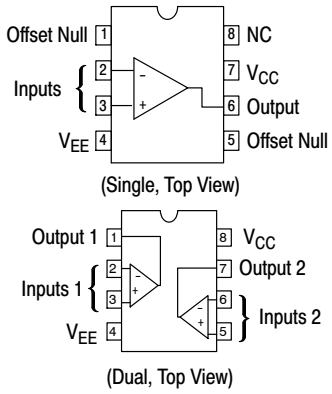
See detailed ordering and shipping information on page 18 of this data sheet.

DEVICE MARKING INFORMATION

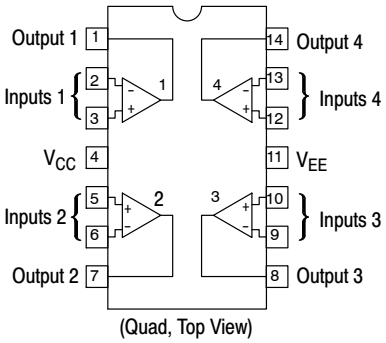
See general marking information in the device marking section on page 19 of this data sheet.

PIN CONNECTIONS

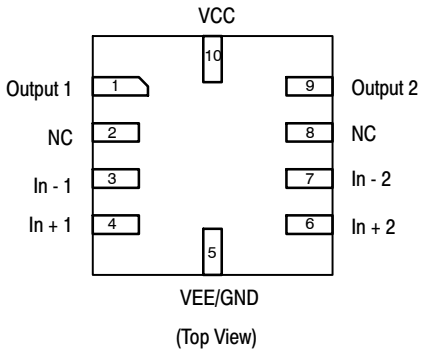
CASE 751



CASE 751A/CASE 948G



CASE 510AJ



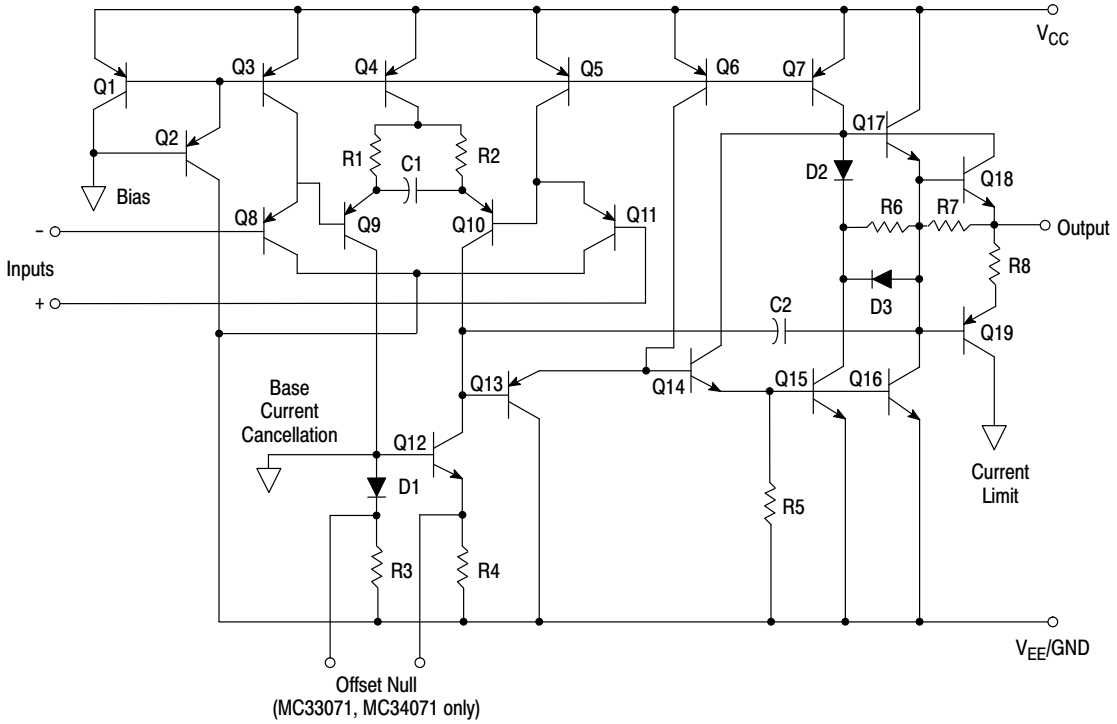


Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	Sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Capability, Dual and Quad (Note 3) Human Body Model Machine Model	 ESD_{HBM} ESD_{MM}	 2000 200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JEDEC standard: JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (JEDEC standard: JESD22−A115)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See Note 4 for T_A = T_{low} to T_{high})

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V) V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}	V_{IO}	 – – –	 0.5 0.5 –	 3.0 3.0 5.0	 – – –	 1.0 1.5 –	 5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = T_{low} to T_{high}	I_{IB}	 – –	 100 –	 500 700	 – –	 100 –	 500 700	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0V) T_A = +25°C T_A = T_{low} to T_{high}	I_{IO}	 – –	 6.0 –	 50 300	 – –	 6.0 –	 75 300	nA
Input Common Mode Voltage Range T_A = +25°C T_A = T_{low} to T_{high}	V_{ICR}	V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	A_{VOL}	 50 25	 100 –	 – –	 25 20	 100 –	 – –	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	V_{OH}	 3.7 13.6 13.4	 4.0 14 –	 – – –	 3.7 13.6 13.4	 4.0 14 –	 – – –	V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	V_{OL}	 – – –	 0.1 −14.7 –	 0.3 −14.3 −13.5	 – – –	 0.1 −14.7 –	 0.3 −14.3 −13.5	V
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C) Source Sink	I_{SC}	 10 20	 30 30	 – –	 10 20	 30 30	 – –	mA
Common Mode Rejection R_S ≤ 10 kΩ, V_{CM} = V_{ICR}, T_A = 25°C	CMR	80	97	–	70	97	–	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	–	70	97	–	dB
Power Supply Current (Per Amplifier, No Load) V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = T_{low} to T_{high}	I_D	 – – –	 1.6 1.9 –	 2.0 2.5 2.8	 – – –	 1.6 1.9 –	 2.0 2.5 2.8	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. T_{low} = −40°C for MC33071,2,4,/A, NCV33074/A T_{high} = +85°C for MC33071,2,4,/A, NCV33074/A
   = 0°C for MC34071,2,4,/A = +70°C for MC34071,2,4,/A
   = −40°C for MC34072,4/V, NCV33072,4A = +125°C for MC34072,4/V, NCV33072,4A, NCV34074V
   Case 510AJ T_{low}/T_{high} guaranteed by product characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non−Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF)	SR							V/μs
A_V = +1.0		8.0	10	–	8.0	10	–	
A_V = −1.0		–	13	–	–	13	–	
Setting Time (10 V Step, A_V = −1.0)	t_s							μs
To 0.1% (+1/2 LSB of 9−Bits)		–	1.1	–	–	1.1	–	
To 0.01% (+1/2 LSB of 12−Bits)		–	2.2	–	–	2.2	–	
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	–	3.5	4.5	–	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5.0%	BW	–	160	–	–	160	–	kHz
Phase margin	f_m							Deg
R_L = 2.0 kΩ		–	60	–	–	60	–	
R_L = 2.0 kΩ, C_L = 300 pF		–	40	–	–	40	–	
Gain Margin	A_m							dB
R_L = 2.0 kΩ		–	12	–	–	12	–	
R_L = 2.0 kΩ, C_L = 300 pF		–	4.0	–	–	4.0	–	
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	–	32	–	–	32	–	nV/$\sqrt{Hz}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	–	0.22	–	–	0.22	–	pA/$\sqrt{Hz}$
Differential Input Resistance V_{CM} = 0 V	R_{in}	–	150	–	–	150	–	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{in}	–	2.5	–	–	2.5	–	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	–	0.02	–	–	0.02	–	%
Channel Separation (f = 10 kHz)	–	–	120	–	–	120	–	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	–	30	–	–	30	–	W

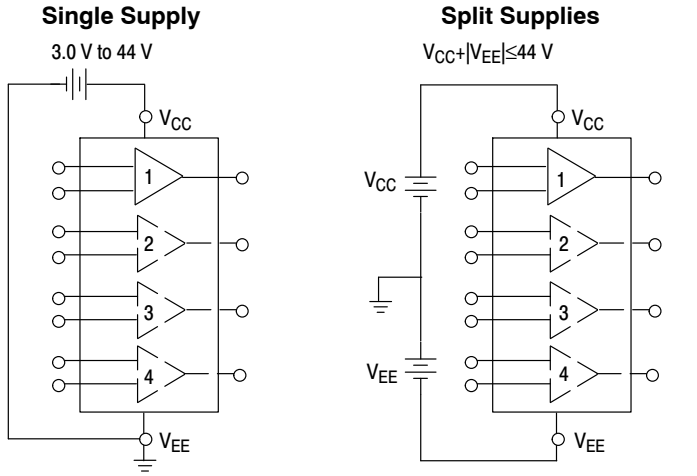
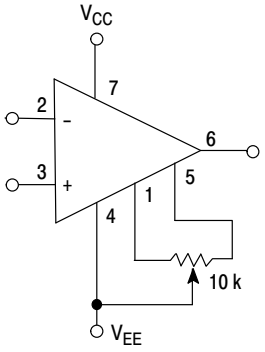


Figure 2. Power Supply Configurations



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).

Figure 3. Offset Null Circuit

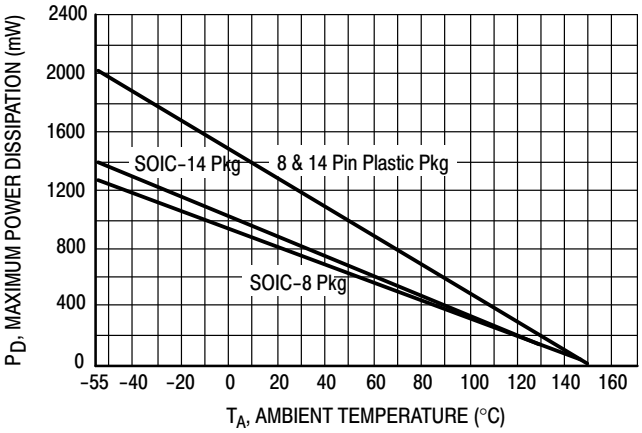


Figure 4. Maximum Power Dissipation versus Temperature for Package Types

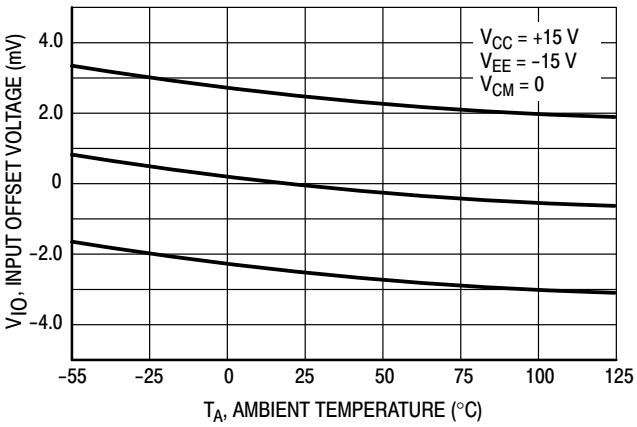


Figure 5. Input Offset Voltage versus Temperature for Representative Units

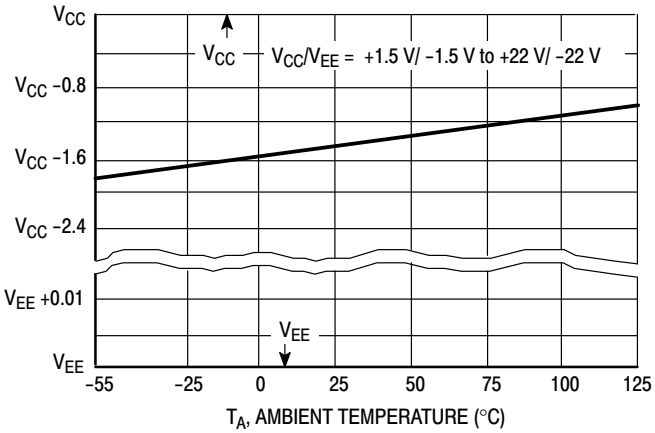


Figure 6. Input Common Mode Voltage Range versus Temperature

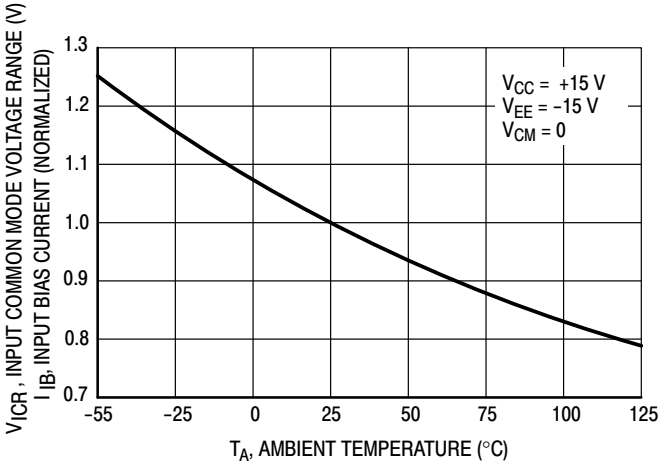


Figure 7. Normalized Input Bias Current versus Temperature

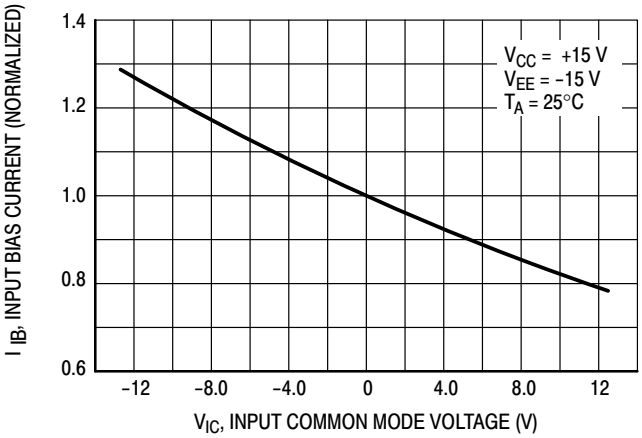


Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage

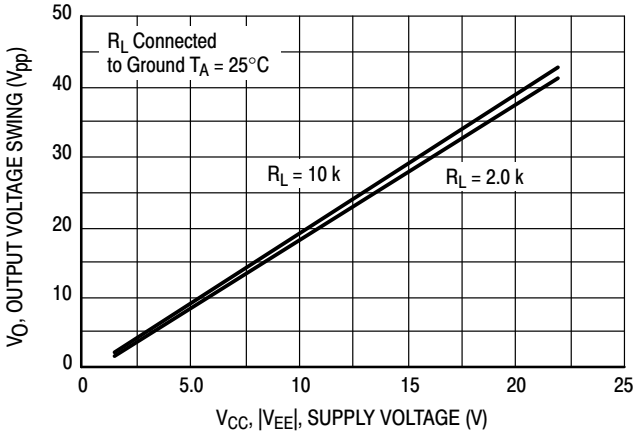


Figure 9. Split Supply Output Voltage Swing versus Supply Voltage

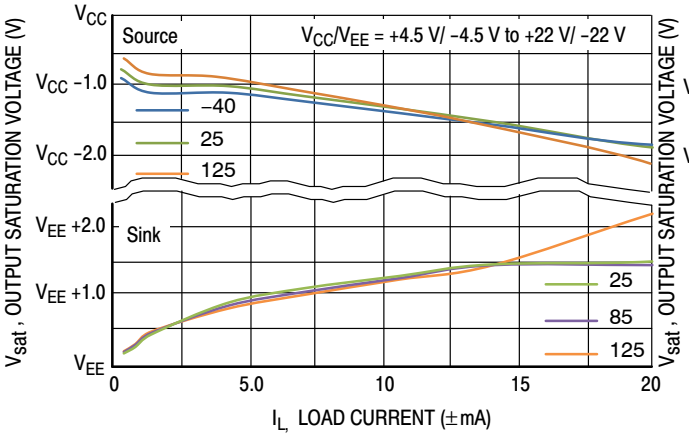


Figure 10. Split Supply Output Saturation versus Load Current

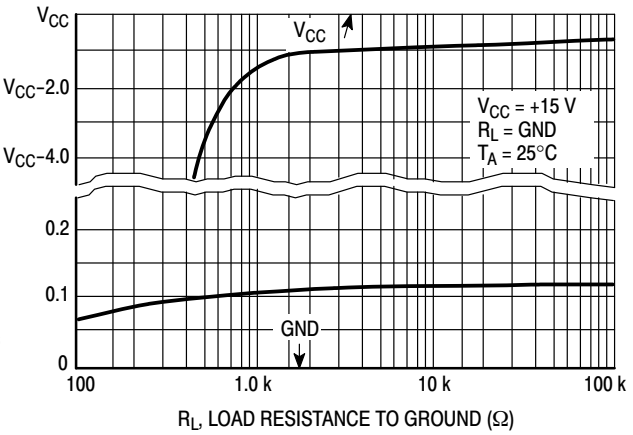


Figure 11. Single Supply Output Saturation versus Load Resistance to Ground

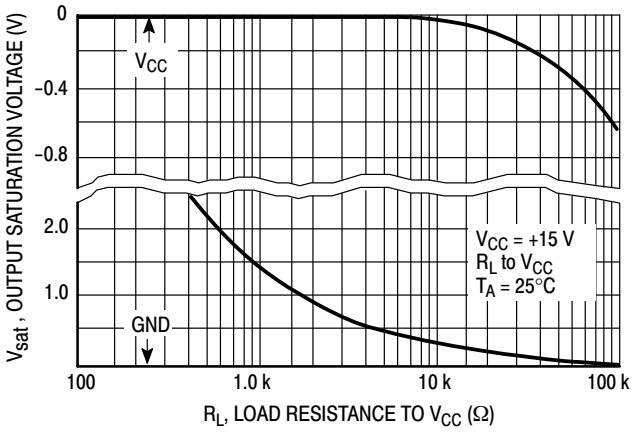


Figure 12. Single Supply Output Saturation versus Load Resistance to V_{CC}

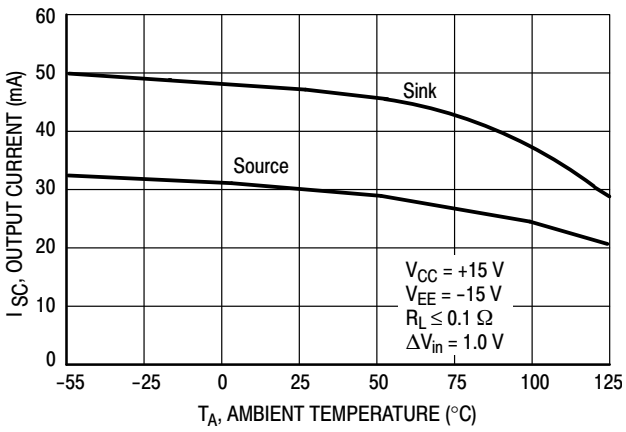


Figure 13. Output Short Circuit Current versus Temperature

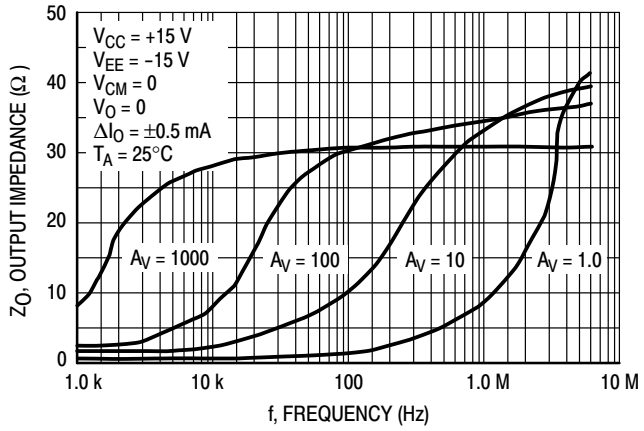


Figure 14. Output Impedance versus Frequency

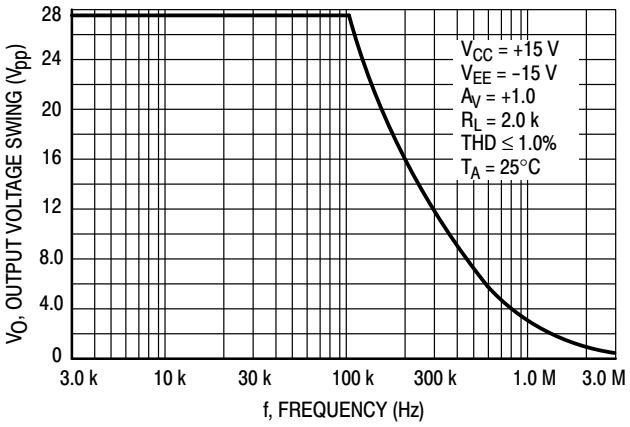


Figure 15. Output Voltage Swing versus Frequency

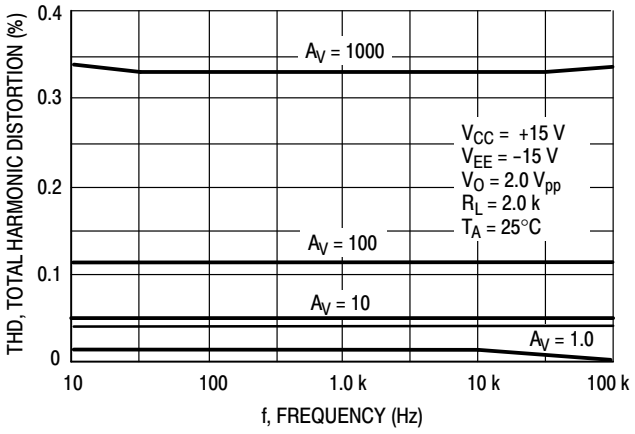


Figure 16. Total Harmonic Distortion versus Frequency

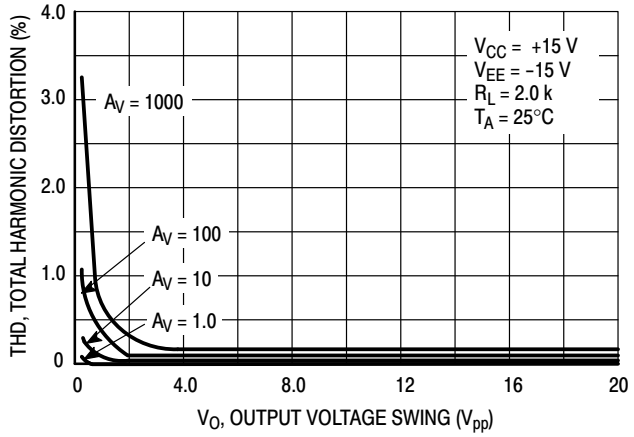


Figure 17. Total Harmonic Distortion versus Output Voltage Swing

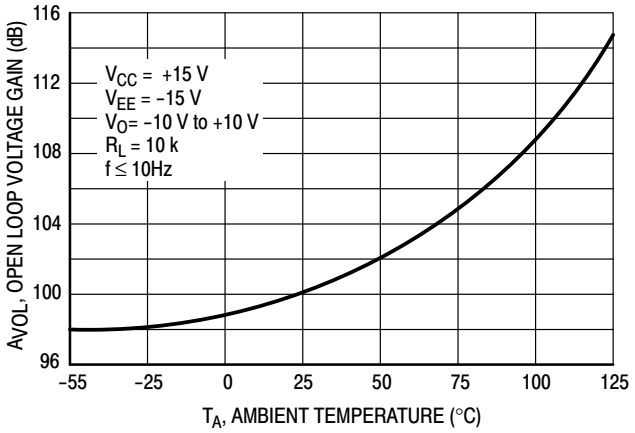


Figure 18. Open Loop Voltage Gain versus Temperature

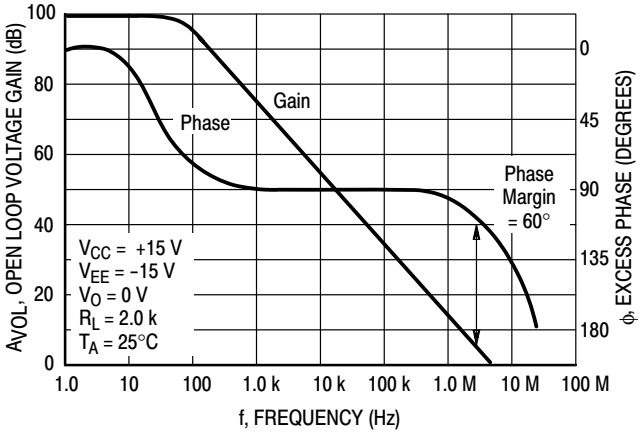


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

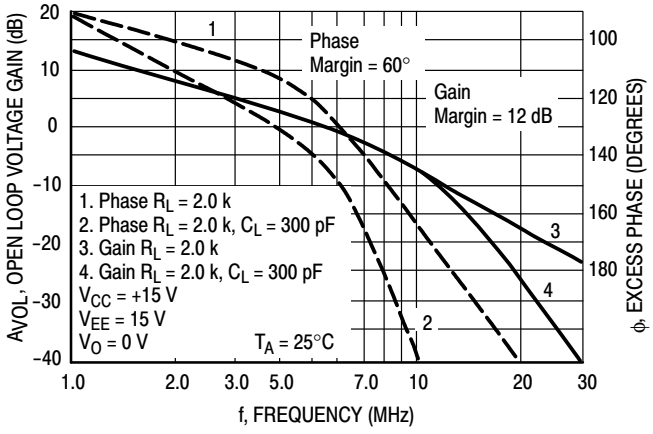


Figure 20. Open Loop Voltage Gain and Phase versus Frequency

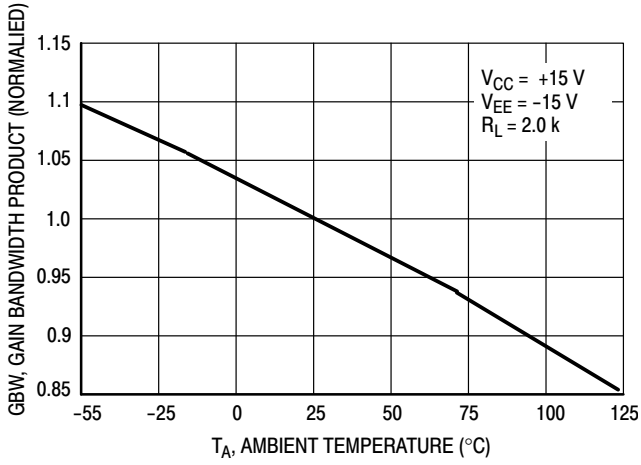


Figure 21. Normalized Gain Bandwidth Product versus Temperature

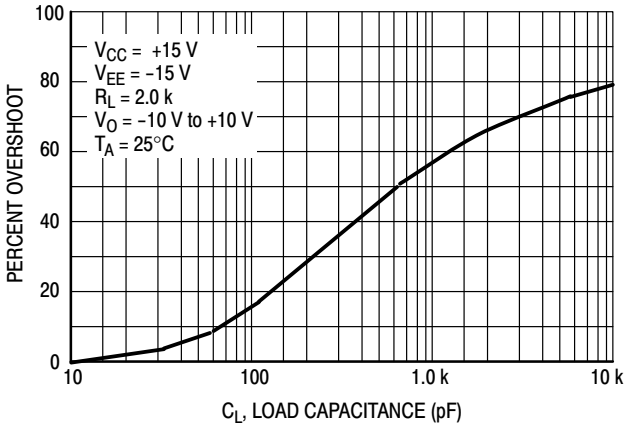


Figure 22. Percent Overshoot versus Load Capacitance

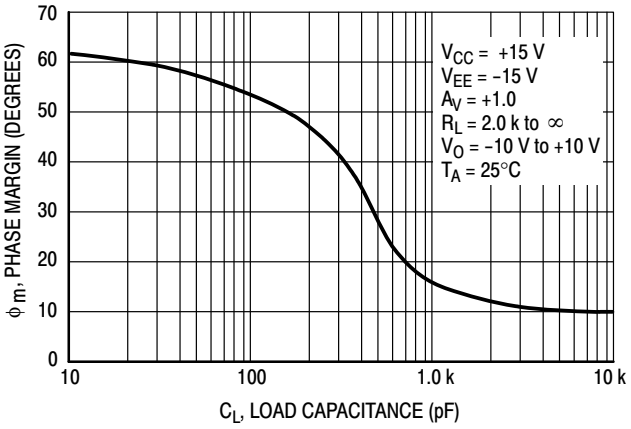


Figure 23. Phase Margin versus Load Capacitance

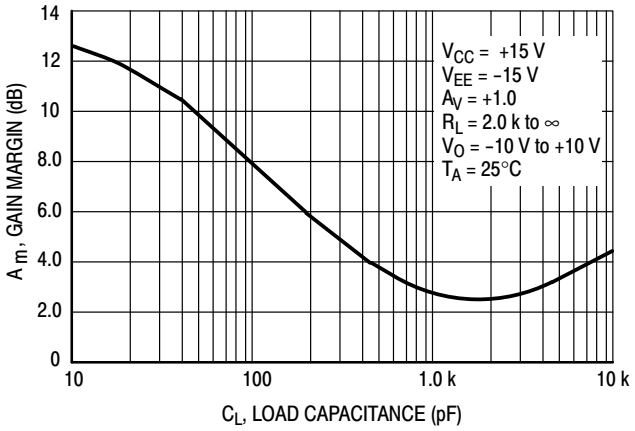


Figure 24. Gain Margin versus Load Capacitance

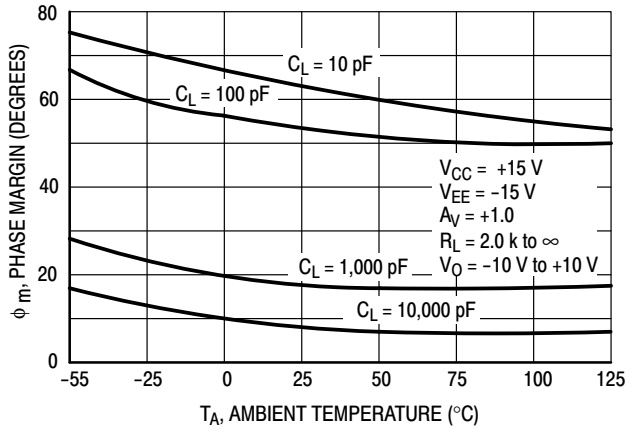


Figure 25. Phase Margin versus Temperature

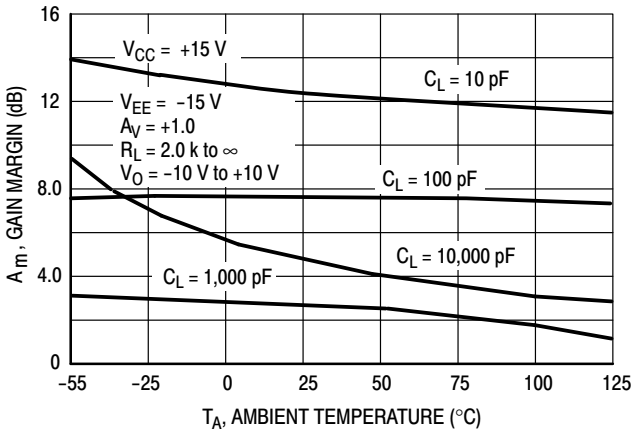


Figure 26. Gain Margin versus Temperature

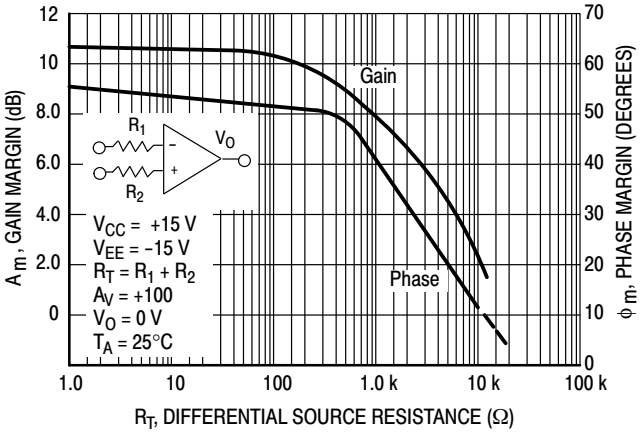


Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance

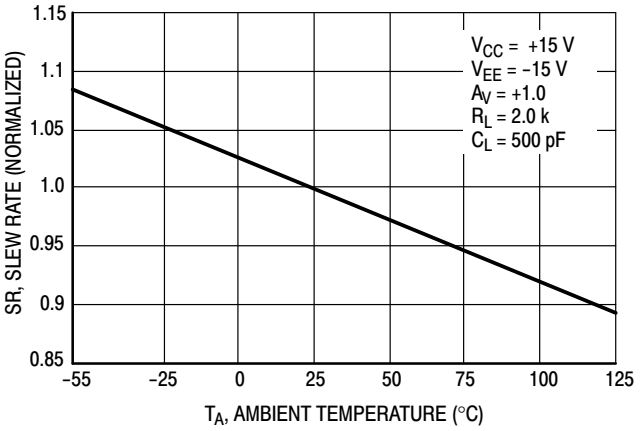


Figure 28. Normalized Slew Rate versus Temperature

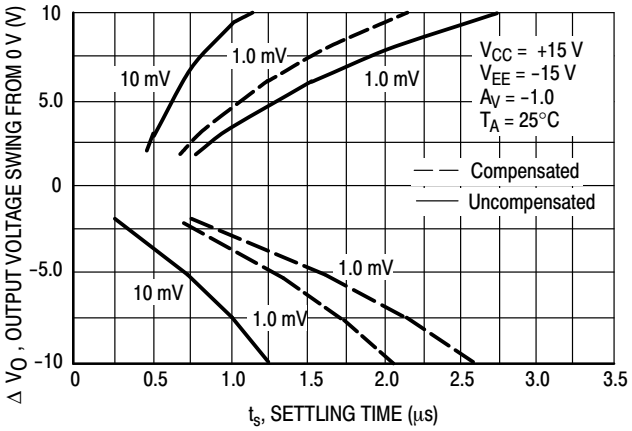


Figure 29. Output Settling Time

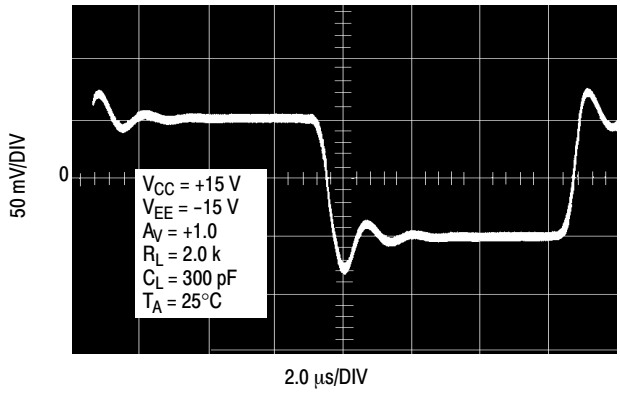


Figure 30. Small Signal Transient Response

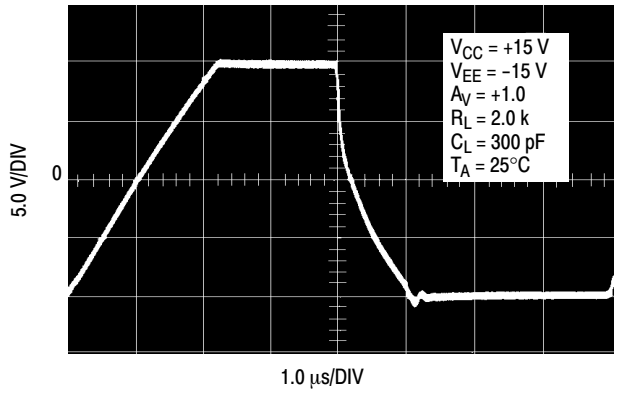


Figure 31. Large Signal Transient Response

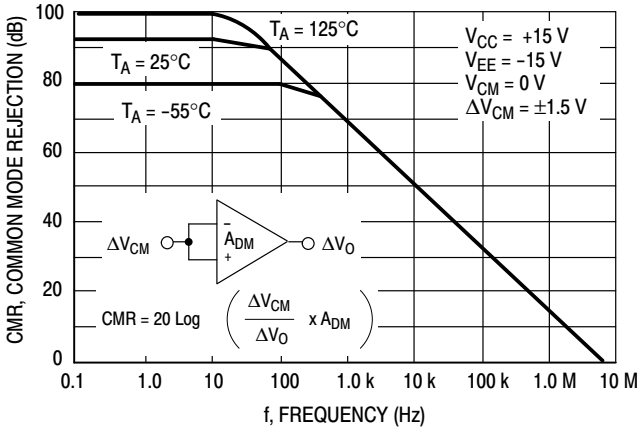


Figure 32. Common Mode Rejection versus Frequency

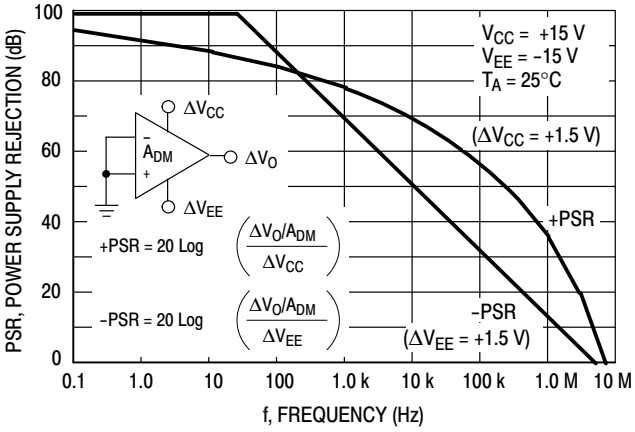


Figure 33. Power Supply Rejection versus Frequency

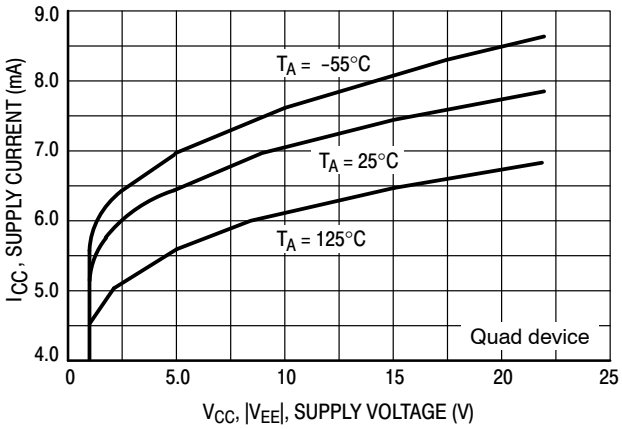


Figure 34. Supply Current versus Supply Voltage

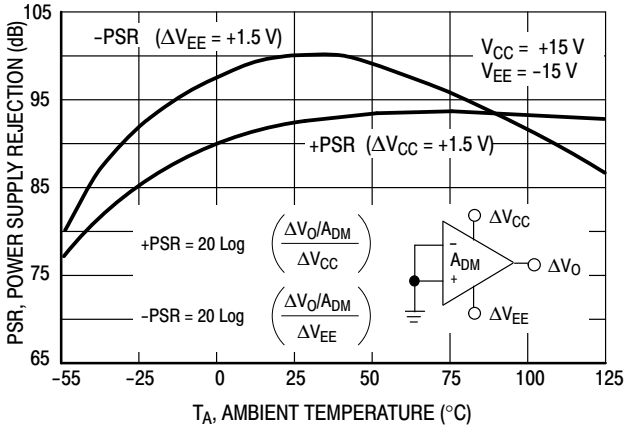


Figure 35. Power Supply Rejection versus Temperature

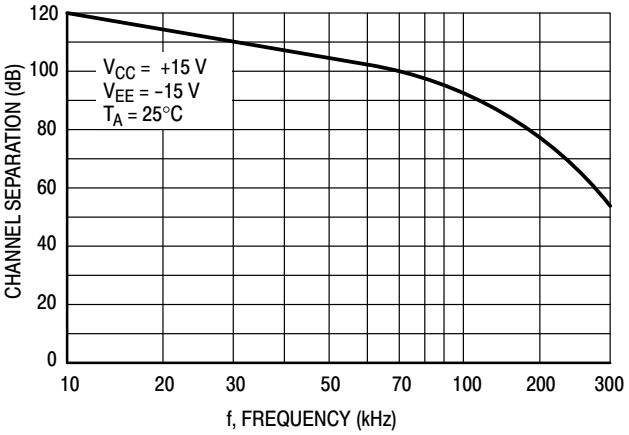


Figure 36. Channel Separation versus Frequency

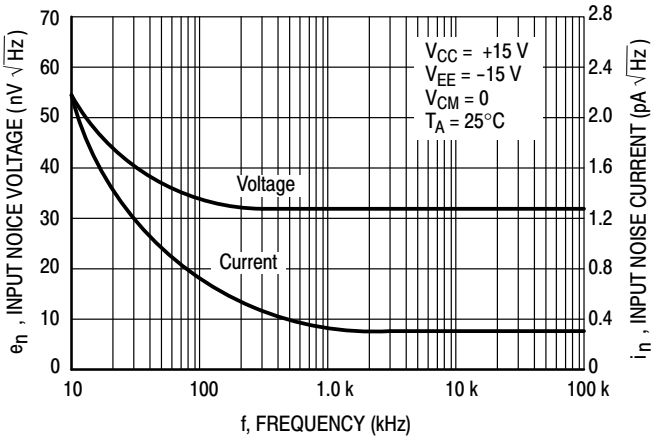


Figure 37. Input Noise versus Frequency

APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D−to−A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher

values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8−bits in 1.0 μs, and within 1/2 LSB of 12−bits in 2.2 μs for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/μs. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/μs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{pp} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull−down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 (≈V_{EE} +1.0 V). Thus for a given supply voltage, unprecedented peak−to−peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter−follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input−output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

(Typical Single Supply Applications V_{CC} = 5.0 V)

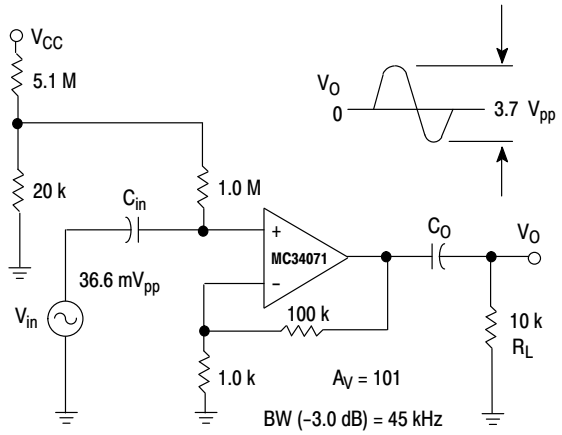


Figure 38. AC Coupled Noninverting Amplifier

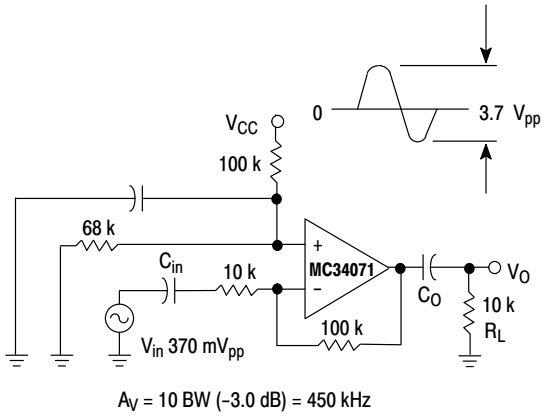


Figure 39. AC Coupled Inverting Amplifier

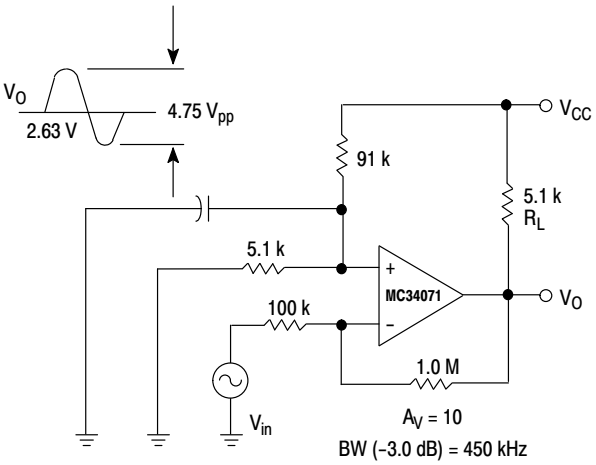


Figure 40. DC Coupled Inverting Amplifier Maximum Output Swing

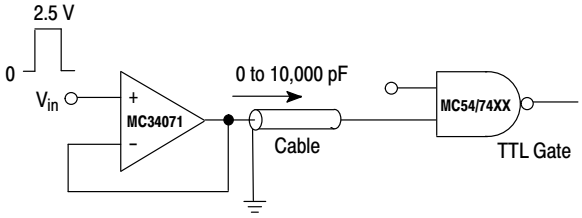


Figure 41. Unity Gain Buffer TTL Driver

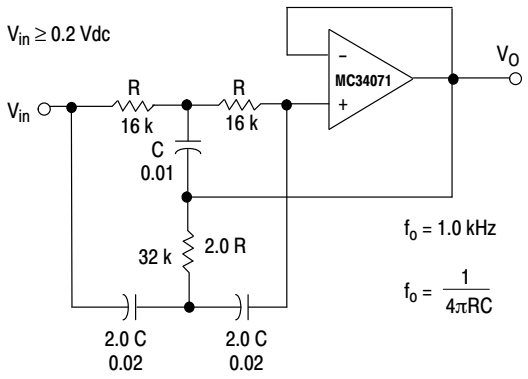
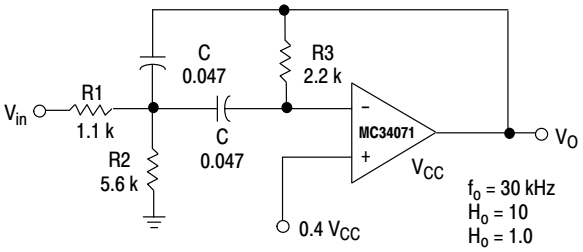


Figure 42. Active High−Q Notch Filter



Given f_o = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_o, Q, A_o, C

Then:

$$R3 = \frac{Q}{\pi f_o C} \quad R1 = \frac{R3}{2H_o} \quad R2 = \frac{R1\ R3}{4Q^2R1-R3}$$

For less than 10% error from operational amplifier $\frac{Q_o f_o}{GBW} < 0.1$

where f_o and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

Figure 43. Active Bandpass Filter

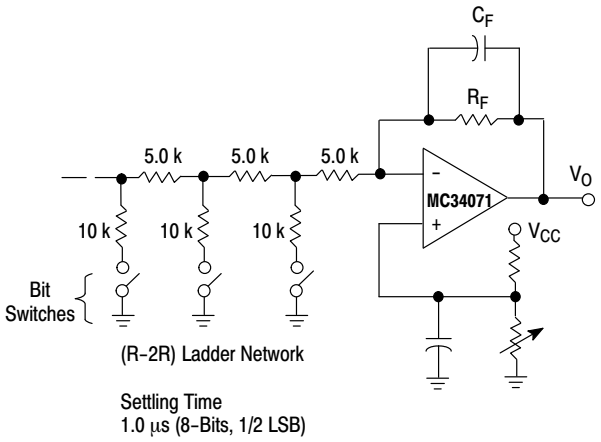


Figure 44. Low Voltage Fast D/A Converter

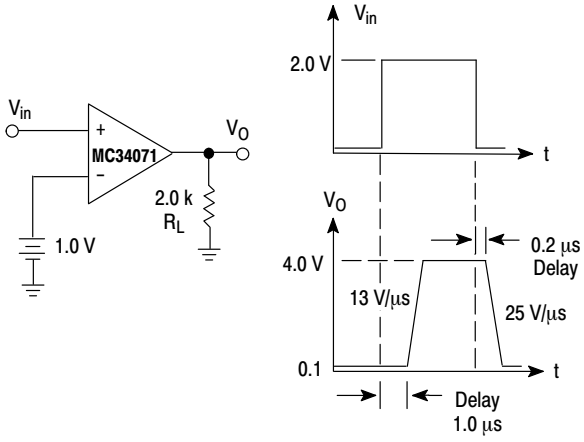


Figure 45. High Speed Low Voltage Comparator

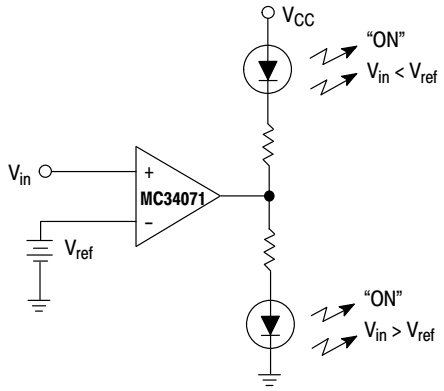


Figure 46. LED Driver

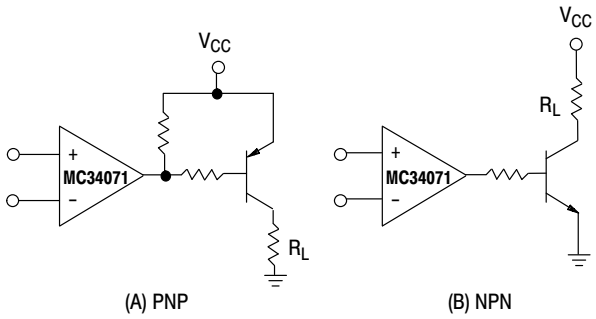


Figure 47. Transistor Driver

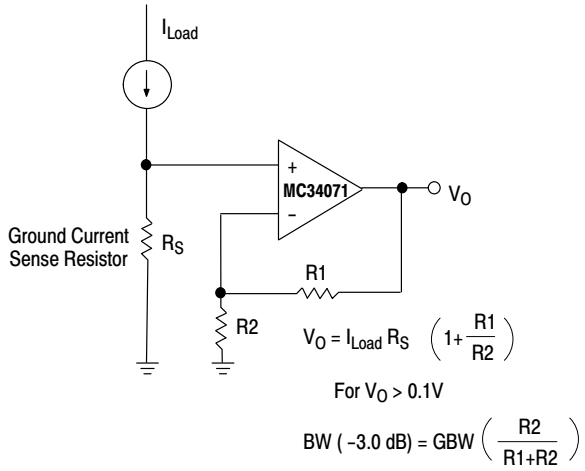


Figure 48. AC/DC Ground Current Monitor

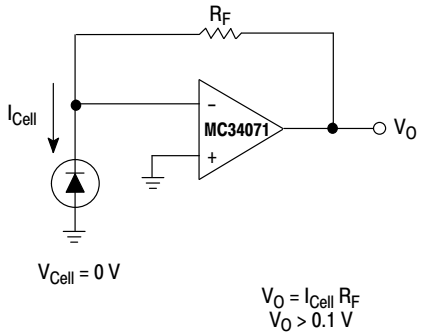


Figure 49. Photovoltaic Cell Amplifier

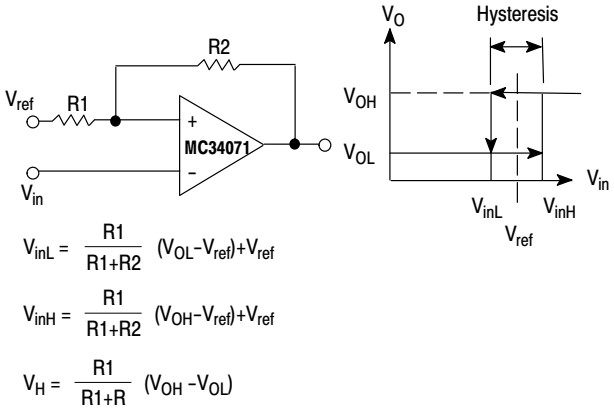


Figure 50. Low Input Voltage Comparator with Hysteresis

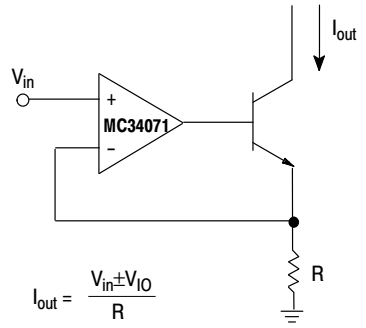


Figure 51. High Compliance Voltage to Sink Current Converter

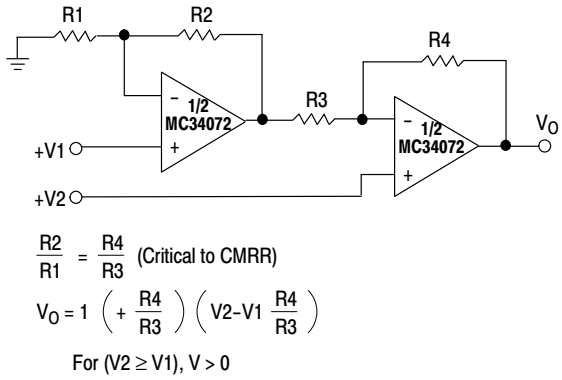


Figure 52. High Input Impedance Differential Amplifier

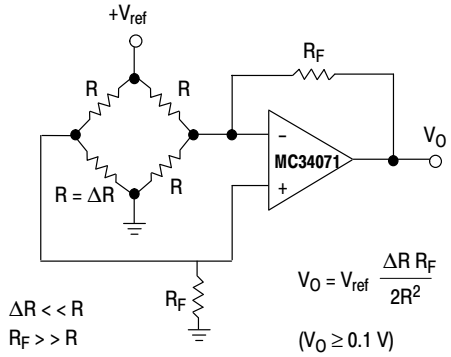


Figure 53. Bridge Current Amplifier

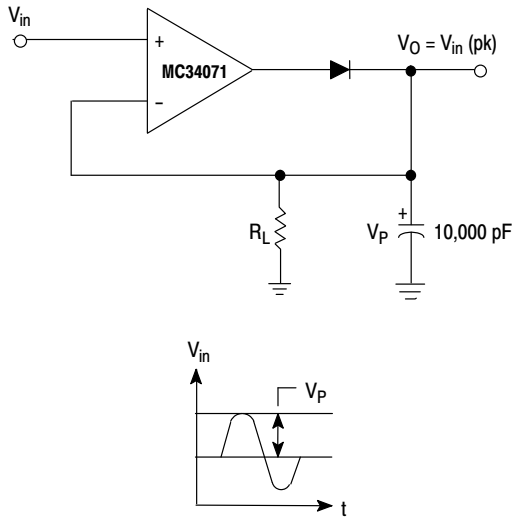


Figure 54. Low Voltage Peak Detector

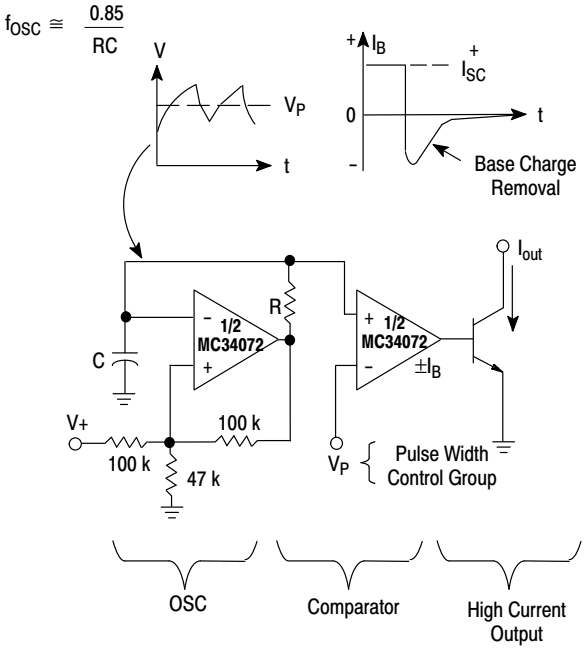


Figure 55. High Frequency Pulse Width Modulation

GENERAL ADDITIONAL APPLICATIONS INFORMATION V_S = ±15.0 V

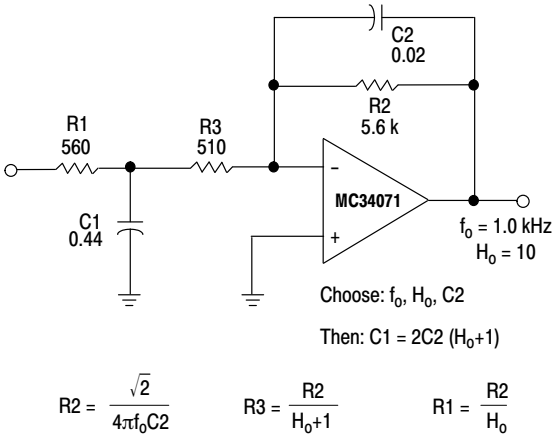


Figure 56. Second Order Low−Pass Active Filter

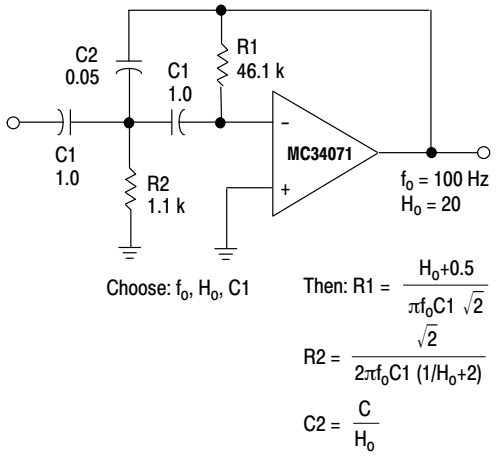


Figure 57. Second Order High−Pass Active Filter

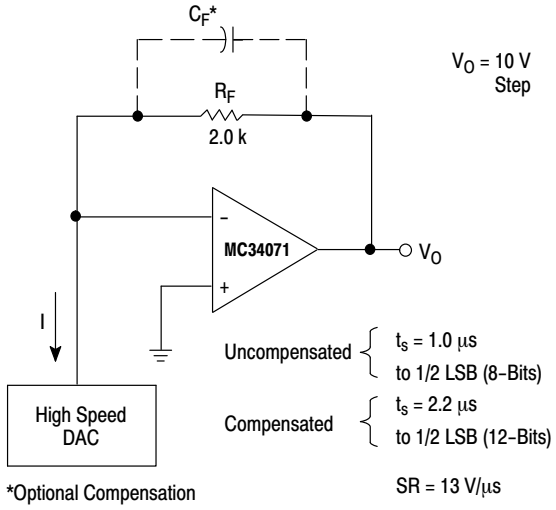


Figure 58. Fast Settling Inverter

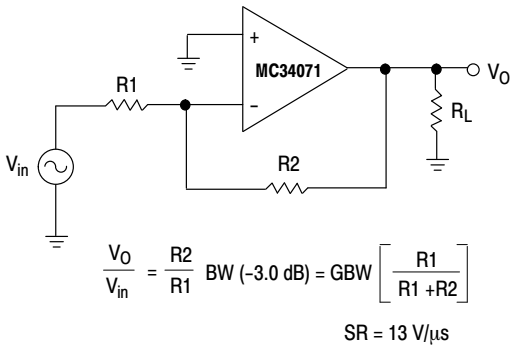


Figure 59. Basic Inverting Amplifier

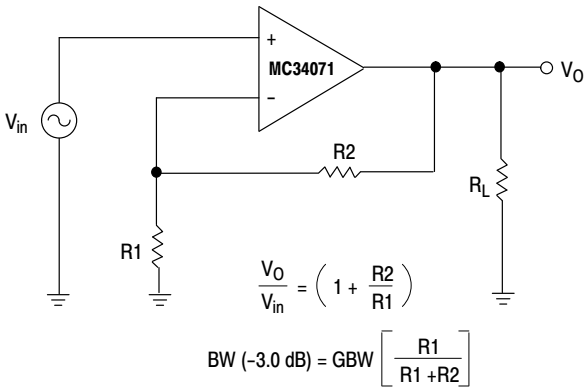


Figure 60. Basic Noninverting Amplifier

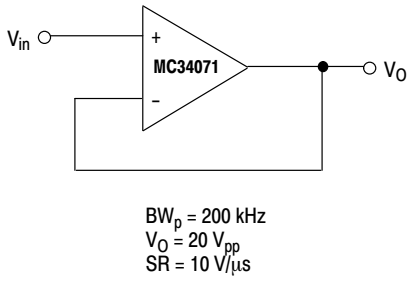


Figure 61. Unity Gain Buffer (A_V = +1.0)

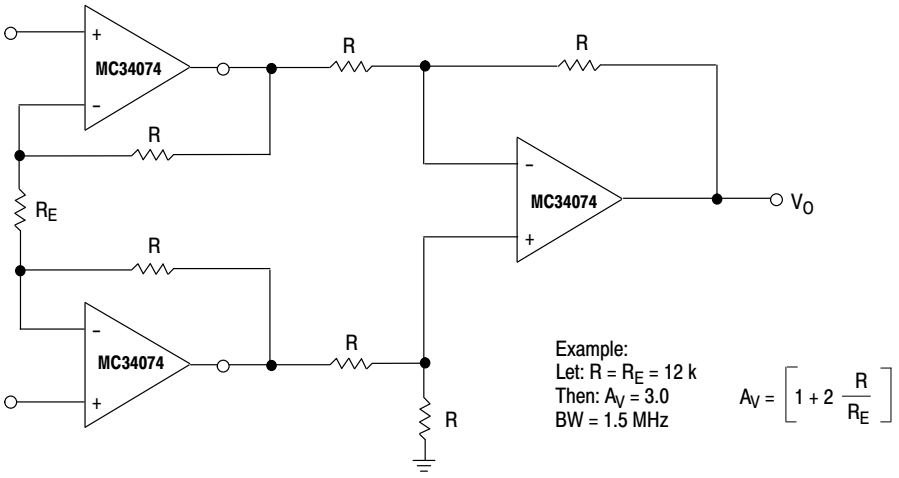
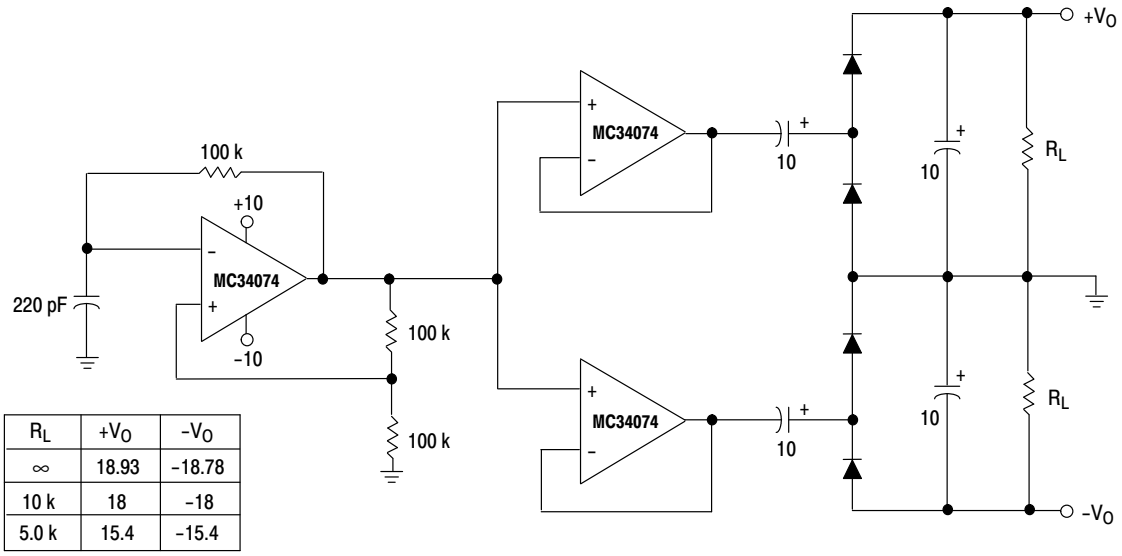


Figure 62. High Impedance Differential Amplifier



R_L	+V_O	-V_O
∞	18.93	−18.78
10 k	18	−18
5.0 k	15.4	−15.4

Figure 63. Dual Voltage Doubler

ORDERING INFORMATION

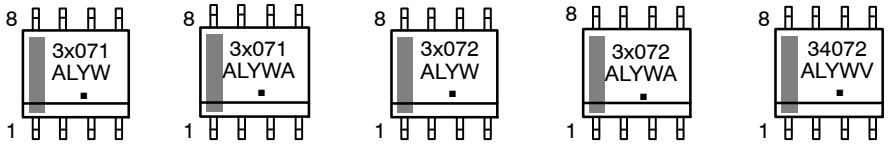
Op Amp Function	Device	Operating Temperature Range	Package	Shipping†
Single	MC34071DR2G	T_A = 0° to +70°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
	MC33071DR2G	T_A = −40° to +85°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
	MC33071ADR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
Dual	MC34072DR2G	T_A = 0° to +70°C	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
	MC34072ADR2G		SOIC−8 (Pb−Free)	
	MC34072AMTTBG		WQFN10 (Pb−Free)	3000 Units / Tape & Reel
	MC33072DR2G	T_A = −40° to +85°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
	MC33072ADR2G		SOIC−8 (Pb−Free)	
	MC34072VDR2G	T_A = −40° to +125°C	SOIC−8 (Pb−Free)	2500 / Tape & Reel
	NCV33072DR2G*		SOIC−8 (Pb−Free)	2500 / Tape & Reel
Quad	MC34074ADR2G	T_A = 0° to +70°C	SOIC−14 (Pb−Free)	2500 Units / Tape & Reel
	MC34074DR2G		SOIC−14 (Pb−Free)	
	MC33074DR2G	T_A = −40° to +85°C	SOIC−14 (Pb−Free)	2500 / Tape & Reel
	NCV33074DR2G*		SOIC−14 (Pb−Free)	
	MC33074ADR2G		SOIC−14 (Pb−Free)	2500 / Tape & Reel
	NCV33074ADR2G*		SOIC−14 (Pb−Free)	
	MC33074DTBR2G		TSSOP−14 (Pb−Free)	2500 / Tape & Reel
	MC33074ADTBR2G		TSSOP−14 (Pb−Free)	2500 / Tape & Reel
	NCV33074ADTBR2G*		TSSOP−14 (Pb−Free)	
	MC34074VDR2G	T_A = −40° to +125°C	SOIC−14 (Pb−Free)	2500 / Tape & Reel
	NCV34074VDR2G*		SOIC−14 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV prefix for automotive and other applications requiring unique site and control change requirements; AEC−Q100 qualified and PPAP capable.

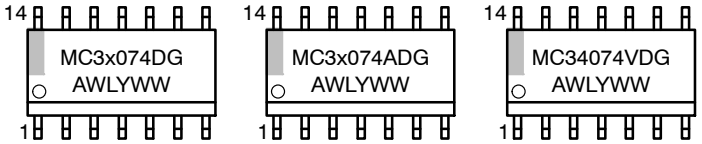
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751



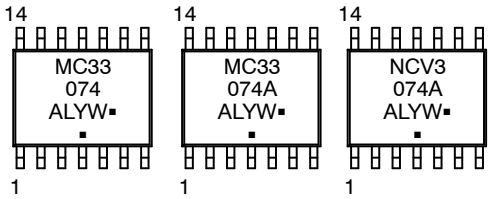
*applies to NCV33072DR2G

SOIC−14
D SUFFIX
CASE 751A

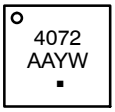


*applies to NCV34074VDR2G

TSSOP−14
DTB SUFFIX
CASE 948G



WQFN10
MT SUFFIX
CASE 510AJ



x	= 3 or 4
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

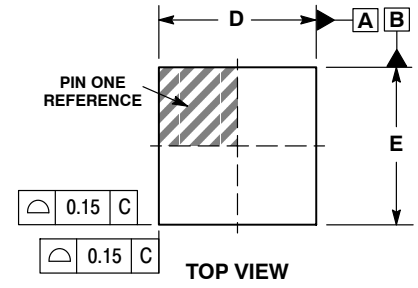
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

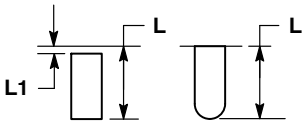
ON Semiconductor®

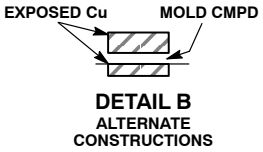
WQFN10 2.6x2.6, 0.5P
CASE 510AJ−01
ISSUE A

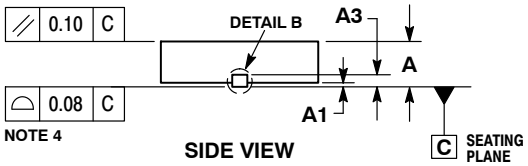
DATE 27 MAR 2009

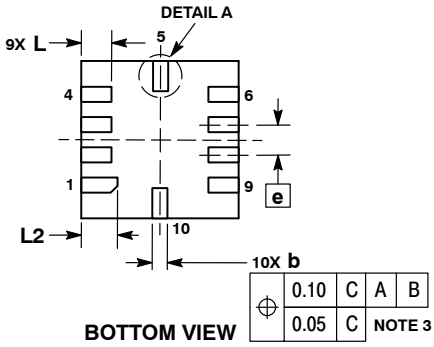
SCALE 2:1











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

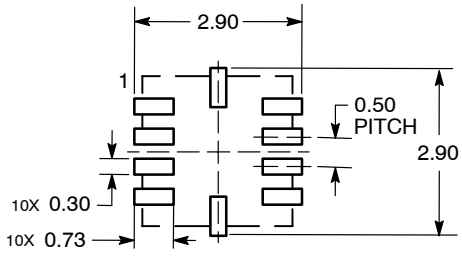
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.60 BSC	
E	2.60 BSC	
e	0.50 BSC	
L	0.45	0.55
L1	0.00	0.15
L2	0.55	0.65

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
AA = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON38696E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WQFN10 2.6X2.6, 0.5P**	**PAGE 1 OF 1**

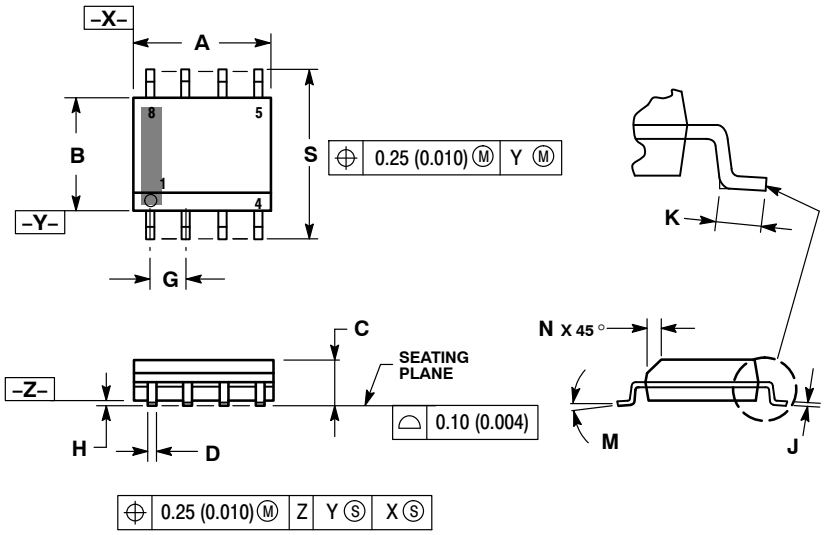
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

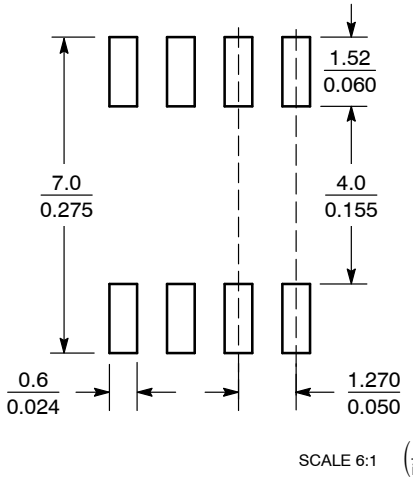
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

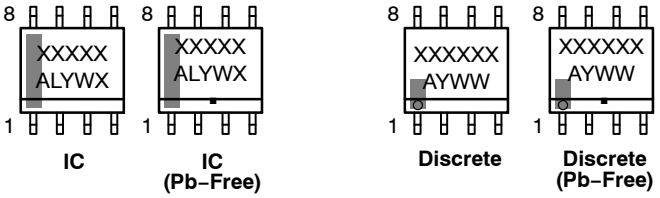
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

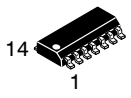
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

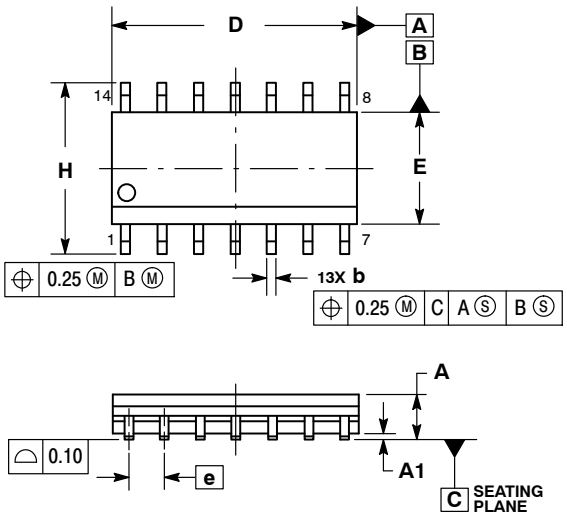
ON Semiconductor®

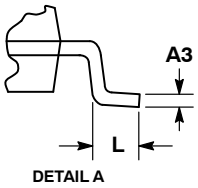


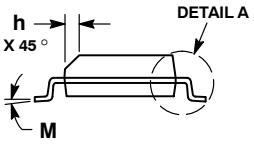
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



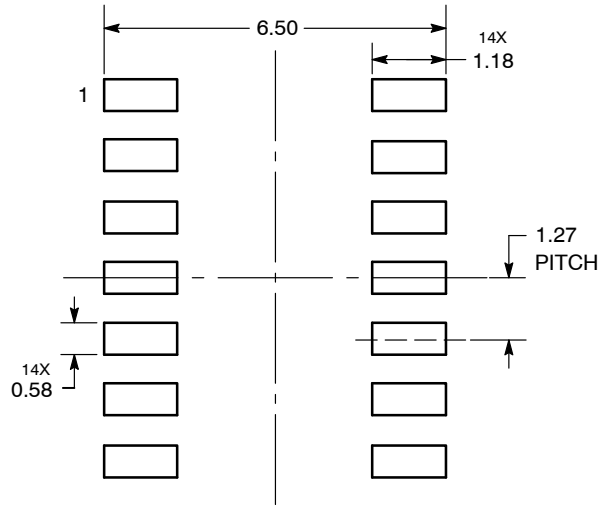




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

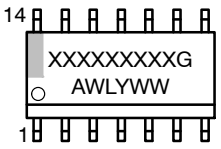
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	SOIC−14 NB		PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

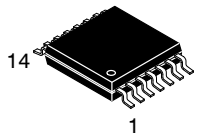
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

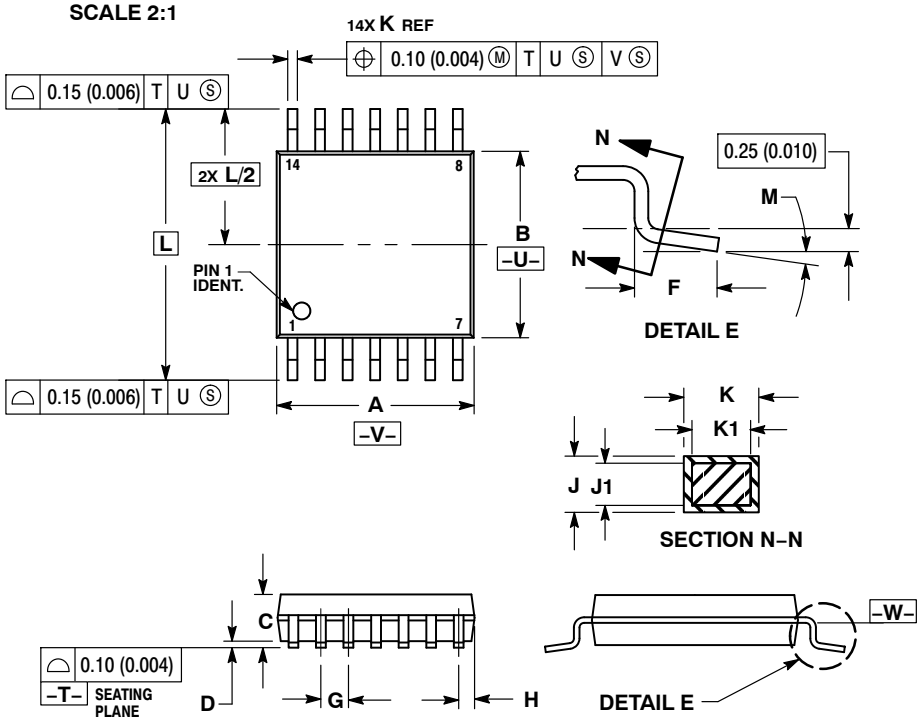
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



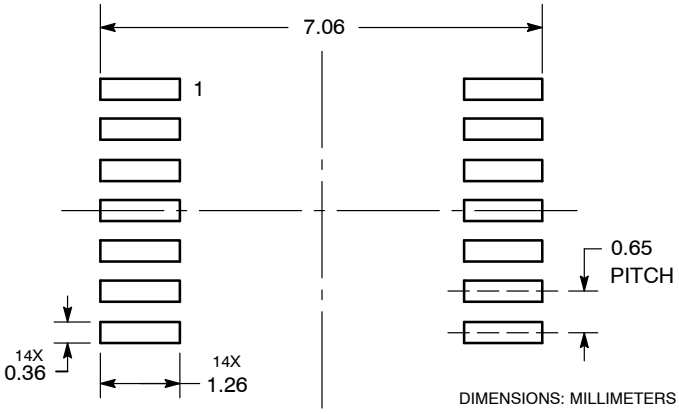
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

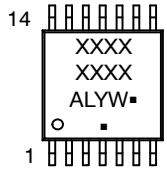
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**