MC33172 MC35172

Low power dual bipolar operational amplifiers

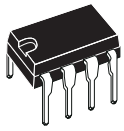
Features

- Good consumption/speed ratio: only 200 µA for 2.1 MHz, 2 V/µs
- Single (or dual) supply operation from +4 V to +44 V (±2 V to ±22V)
- Wide input common mode mode voltage range including V_{CC}-
- Low level output voltage close to V_{CC}- : 100 mV typical
- Pin-to-pin compatible with standard dual operational amplifiers

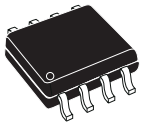
Description

The MC3x172 series are dual bipolar operational amplifiers offering both low consumption (200 µA/Amp) and good speed (2.1 MHz, 2 V/µs).

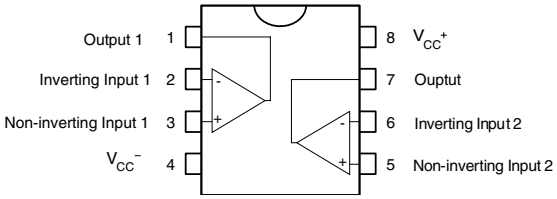
Moreover, the input common mode range extends down to the lower supply rail, allowing single supply operation from +4 V to +44 V.



N
DIP8
(Plastic package)



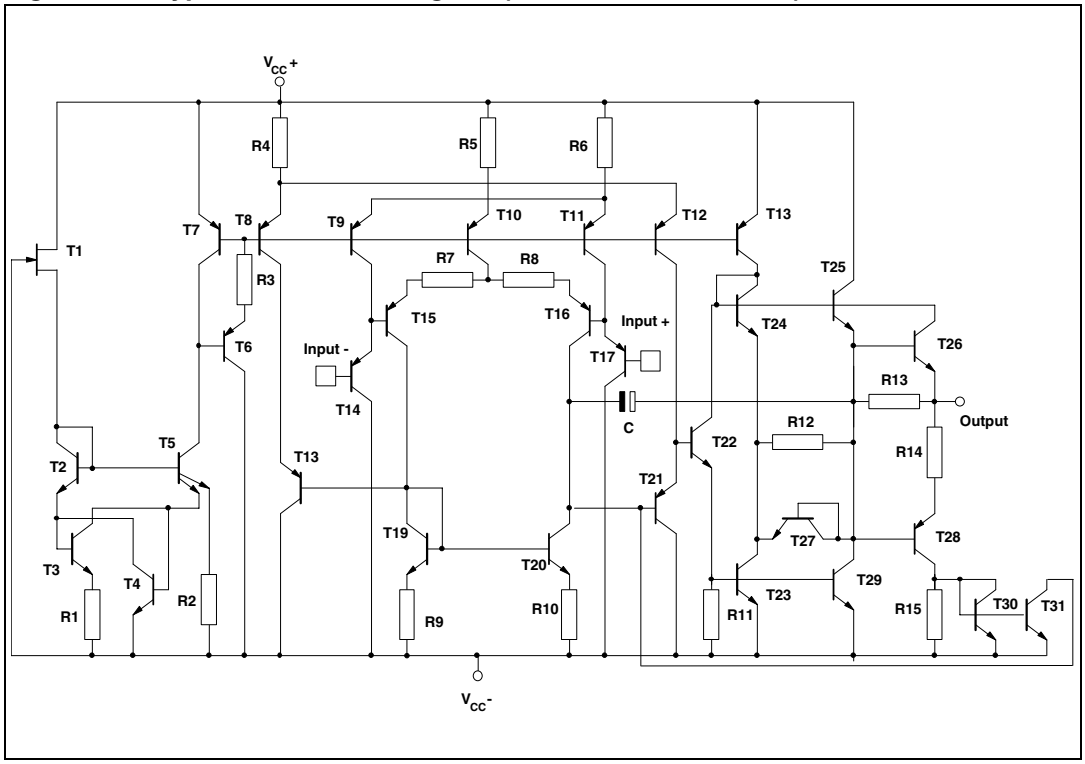
D
SO-8
(Plastic micropackage)



Pin connections
(top view)

1 Circuit schematics

Figure 1. Typical schematic diagram (1/2 MC33172/MC35172)



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±22	V
V_{id}	Differential input voltage	see note (1)	V
V_{in}	Input voltage	see note 1	V
	Output short-circuit duration	Indefinite	s
T_{oper}	Operating free-air temperature range MC33172 MC35172	 -40 to 105 -55 to 125	°C
R_{thja}	Thermal resistance junction to ambient(2) SO-8 DIP8	 125 85	°C/W
R_{thjc}	Thermal resistance junction to case(2) SO-8 DIP8	 40 41	°C/W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C
ESD	HBM: human body model(3)	2	kV
	MM: machine model(4)	200	V
	CDM: charged device model(5)	1	kV
	Latch-up immunity	Class A	

1. Either or both input voltages must not exceed the magnitude of V_{CC}.
2. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
3. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
5. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±2 to ±22	V

3 Electrical characteristics

Table 3. V_{CC}^+ = +15V, V_{CC}^- = -15V, R_L connected to Ground, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage V_{CC}^+ = +15V, V_{CC}^- = -15V, V_{ic} = 0V V_{CC}^+ = 5V, V_{CC}^- = 0V, V_{ic} = 0V, V_o = 1.4V V_{CC}^+ = +15V, V_{CC}^- = -15V, V_{ic} = 0V, $T_{min} \le T_{amb} \le T_{max}$		 1 1	 4.5 5 6.5	mV
DV_{io}	Input offset voltage drift		10		µV/°C
I_{io}	Input offset current (V_{ic} = 0V) $T_{min} \le T_{amb} \le T_{max}$		5	20 40	nA
I_{ib}	Input bias current (V_{ic} = 0V) $T_{min} \le T_{amb} \le T_{max}$		20	100 200	nA
A_{vd}	Large signal voltage gain (R_L = 10kΩ, V_o = ±10V) $T_{min} \le T_{amb} \le T_{max}$	50 25	100		V/mV
V_{OH}	High level output voltage V_{CC}^+= 5V, V_{CC}^-= 0V, R_L = 10kΩ V_{CC}^+= +15V, V_{CC}^- = -15V, R_L= 10kΩ V_{CC}^+= +15V, V_{CC}^-= -15V, R_L= 10kΩ, $T_{min} \le T_{amb} \le T_{max}$	 3.5 13.6 13.3	 4.2 14.2		V
V_{OL}	Low level output voltage V_{CC}^+= 5V, V_{CC}^-= 0V, R_L= 10kΩ V_{CC}^+= +15V, V_{CC}^-= -15V, R_L= 10kΩ V_{CC}^+= +15V, V_{CC}^-= -15V, R_L= 10kΩ, $T_{min} \le T_{amb} \le T_{max}$		 0.1 -14	 0.15 -13.6 -13.3	V
I_{sc}	Output short-circuit current (V_{id} = ±1V, V_o = 0V) Source Sink	 3 15	 6 27		mA
V_{icm}	Input common mode voltage range $T_{min} \le T_{amb} \le T_{max}$	V_{CC}^- to V_{CC}^+ - 1.8) V_{CC}^- to (V_{CC}^+ - 2.2)			V
CMR	Common-mode rejection ratio (V_{ic} = $V_{icm-min}$)	80	100		dB
SVR	Supply voltage rejection ratio (V_{CC} = ±5 to ±15V)	80	100		dB
I_{CC}	Supply current V_{CC}^+ = 5V, V_{CC}^- = 0V, no load V_{CC}^+ = +15V, V_{CC}^- = -15V, no load V_{CC}^+ = +15V, V_{CC}^- = -15V no load, $T_{min} \le T_{amb} \le T_{max}$		 200 220	 250 250 300	µA
SR	Slew rate (V_{in} = ±10V, R_L = 10kΩ, C_L = 100pF)	1.6	2		V/µs
GBP	Gain bandwidth product R_L = 10kΩ, C_L = 100pF, F= 100kHz	1.4	2.1		MHz
ϕm	Phase margin (R_L = 10kΩ, C_L = 100pF)		45		Degrees
e_n	Equivalent input noise voltage (F = 1kHz)		29		$\frac{nV}{\sqrt{Hz}}$
THD	Total harmonic distortion		0.05		%
V_{O1}/V_{O2}	Channel separation		120		dB

4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP8 package information

Figure 2. DIP8 package mechanical drawing

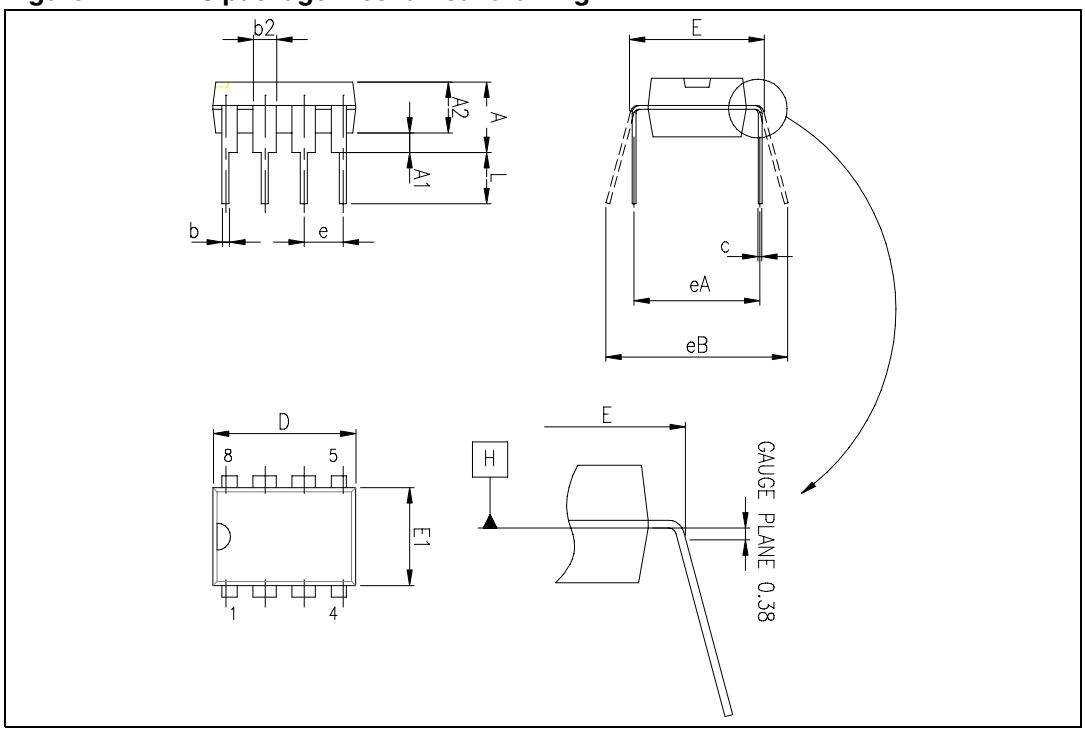


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

4.2 SO-8 package information

Figure 3. SO-8 package mechanical drawing

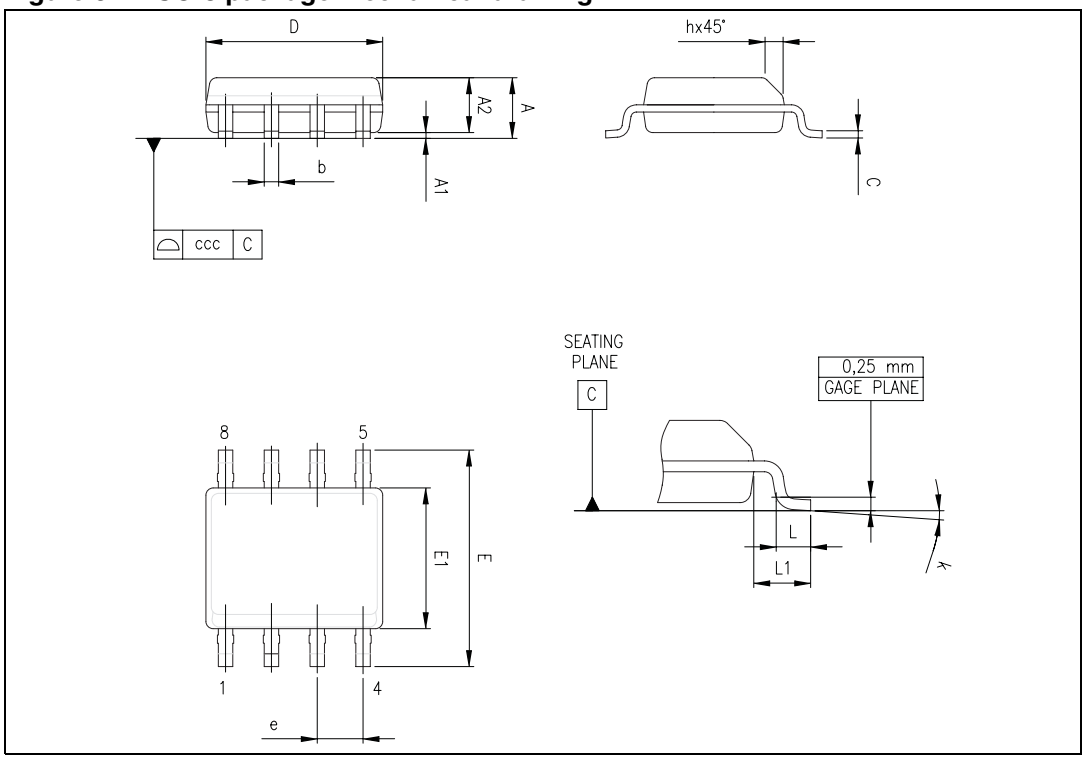


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

5 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
MC33172N	-40°C, +105°C	DIP8	Tape	MC33172N
MC33172D MC33172DT		SO-8	Tape or Tape & reel	33172
MC35172N	-55°C, +125°C	DIP8	Tape	MC35172N
MC35172D MC35172DT		SO-8	Tape or Tape & reel	35172

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
24-Nov-2001	1	Initial release.
01-Jul-2008	2	ESD values and latch-up immunity added in *Table 1: Absolute maximum ratings (AMR)*.