

# Low Voltage, Rail-to-Rail Operational Amplifiers

## MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages ( $\pm 0.9$  V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

### Features

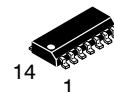
- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current ( $I_{SC} = 80$  mA, Typ)
- Low Supply Current ( $I_D = 0.9$  mA, Typ)
- 600  $\Omega$  Output Drive Capability
- Extended Operating Temperature Ranges ( $-40^\circ$  to  $+105^\circ\text{C}$  and  $-55^\circ$  to  $+125^\circ\text{C}$ )
- Typical Gain Bandwidth Product = 2.2 MHz
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant



SOIC-8  
D, VD SUFFIX  
CASE 751



Micro8  
DM SUFFIX  
CASE 846A



SOIC-14  
D, VD SUFFIX  
CASE 751A



TSSOP-14  
DTB SUFFIX  
CASE 948G

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

PIN CONNECTIONS

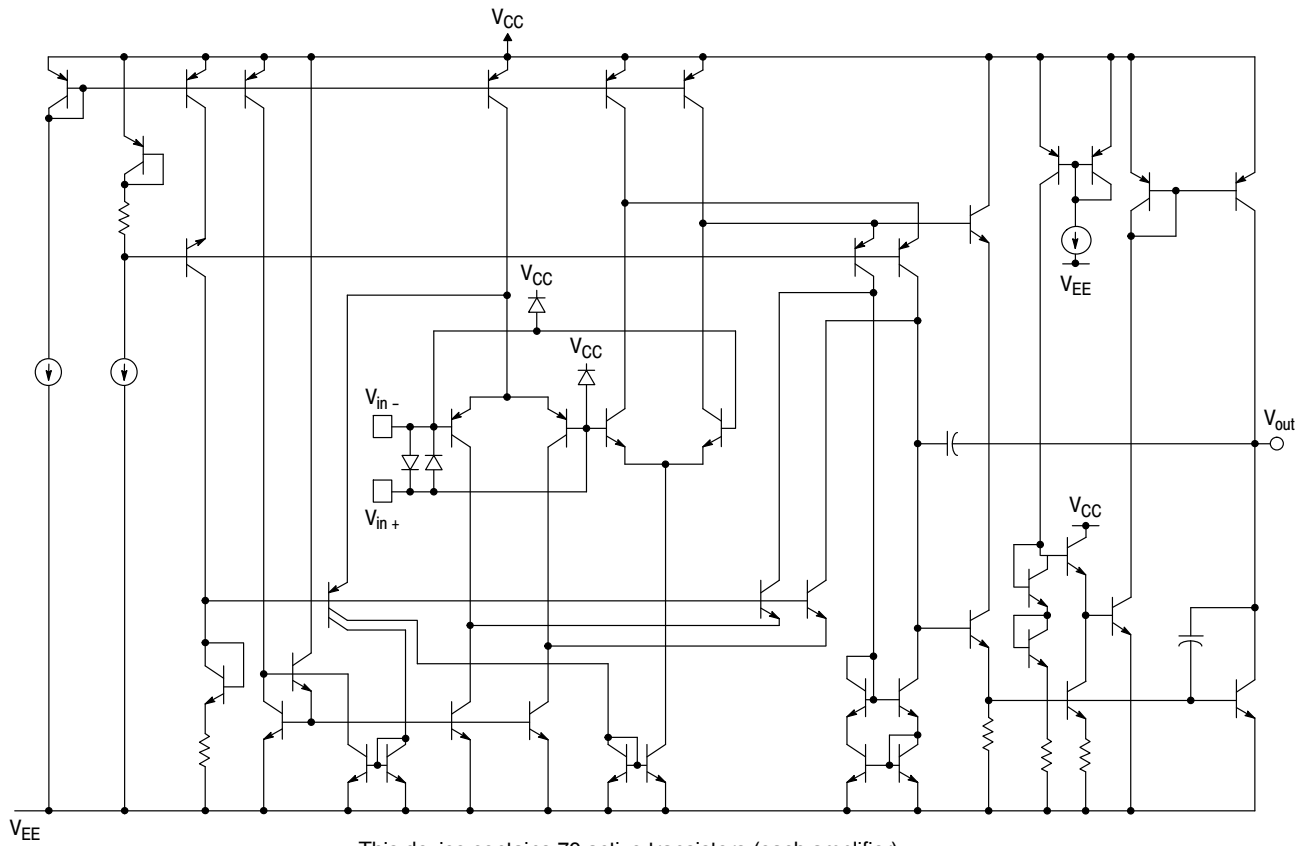
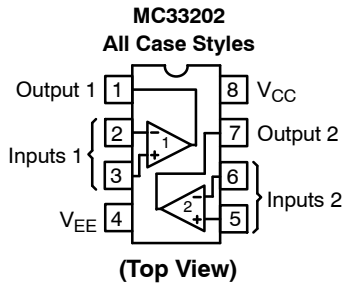
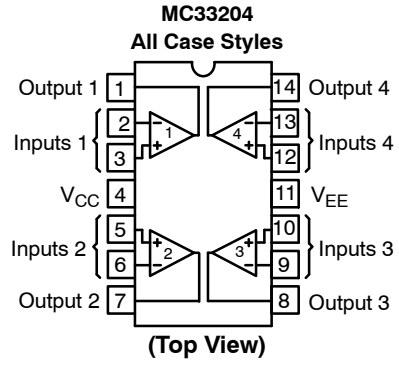
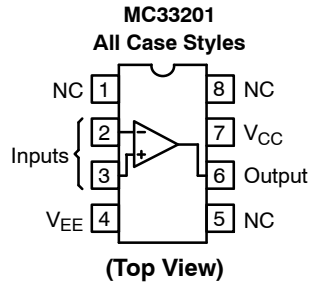


Figure 1. Circuit Schematic  
(Each Amplifier)

# MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

## MAXIMUM RATINGS

| Rating                                   | Symbol    | Value                                   | Unit |
|--|-----------|---|------|
| Supply Voltage ( $V_{CC}$ to $V_{EE}$ )  | $V_S$     | +13                                     | V    |
| Input Differential Voltage Range         | $V_{IDR}$ | Note 1                                  | V    |
| Common Mode Input Voltage Range (Note 2) | $V_{CM}$  | $V_{CC} + 0.5$ V to<br>$V_{EE} - 0.5$ V | V    |
| Output Short Circuit Duration            | $t_s$     | Note 3                                  | sec  |
| Maximum Junction Temperature             | $T_J$     | +150                                    | °C   |
| Storage Temperature                      | $T_{stg}$ | - 65 to +150                            | °C   |
| Maximum Power Dissipation                | $P_D$     | Note 3                                  | mW   |

## DC ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

| Characteristic  | $V_{CC} = 2.0$ V                  | $V_{CC} = 3.3$ V                  | $V_{CC} = 5.0$ V                   | Unit                   |
|---|-----------------------------------|-----------------------------------|------------------------------------|------------------------|
| Input Offset Voltage<br>$V_{IO(max)}$<br>MC33201, NCV33201V<br>MC33202, NCV33202, V<br>MC33204, NCV33204, V | $\pm 8.0$<br>$\pm 10$<br>$\pm 12$ | $\pm 8.0$<br>$\pm 10$<br>$\pm 12$ | $\pm 6.0$<br>$\pm 8.0$<br>$\pm 10$ | mV                     |
| Output Voltage Swing<br>$V_{OH}$ ( $R_L = 10$ k $\Omega$ )<br>$V_{OL}$ ( $R_L = 10$ k $\Omega$ )            | 1.9<br>0.10                       | 3.15<br>0.15                      | 4.85<br>0.15                       | $V_{min}$<br>$V_{max}$ |
| Power Supply Current<br>per Amplifier ( $I_D$ )   | 1.125                             | 1.125                             | 1.125                              | mA                     |

Specifications at  $V_{CC} = 3.3$  V are guaranteed by the 2.0 V and 5.0 V tests.  $V_{EE} = \text{GND}$ .

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5.0$ V, $V_{EE} = \text{Ground}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| Characteristic   | Figure | Symbol                   | Min                                  | Typ                                  | Max   | Unit                         |
|--|--------|--------------------------|--------------------------------------|--------------------------------------|---|------------------------------|
| Input Offset Voltage ( $V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V)<br>MC33201/NCV33201V: $T_A = +25^\circ\text{C}$<br>MC33201: $T_A = -40^\circ$ to $+105^\circ\text{C}$<br>MC33201V/NCV33201V: $T_A = -55^\circ$ to $+125^\circ\text{C}$<br>MC33202/NCV33202, V: $T_A = +25^\circ\text{C}$<br>MC33202/NCV33202: $T_A = -40^\circ$ to $+105^\circ\text{C}$<br>MC33202V/NCV33202V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ (Note 4)<br>MC33204/NCV33204V: $T_A = +25^\circ\text{C}$<br>MC33204: $T_A = -40^\circ$ to $+105^\circ\text{C}$<br>MC33204V/NCV33204V: $T_A = -55^\circ$ to $+125^\circ\text{C}$ (Note 4) | 3      | $ V_{IO} $               | -<br>-<br>-<br>-<br>-<br>-<br>-<br>- | -<br>-<br>-<br>-<br>-<br>-<br>-<br>- | 6.0<br>9.0<br>13<br>8.0<br>11<br>14<br>10<br>13<br>17 | mV                           |
| Input Offset Voltage Temperature Coefficient ( $R_S = 50$ $\Omega$ )<br>$T_A = -40^\circ$ to $+105^\circ\text{C}$<br>$T_A = -55^\circ$ to $+125^\circ\text{C}$   | 4      | $\Delta V_{IO}/\Delta T$ | -<br>-                               | 2.0<br>2.0                           | -<br>-  | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current ( $V_{CM} = 0$ V to 0.5 V, $V_{CM} = 1.0$ V to 5.0 V)<br>$T_A = +25^\circ\text{C}$<br>$T_A = -40^\circ$ to $+105^\circ\text{C}$<br>$T_A = -55^\circ$ to $+125^\circ\text{C}$  | 5, 6   | $ I_{IB} $               | -<br>-<br>-                          | 80<br>100<br>-                       | 200<br>250<br>500                                     | nA                           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
- The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
- Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded. (See Figure 2)
- All NCV devices are qualified for Automotive use.

# MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

## DC ELECTRICAL CHARACTERISTICS (cont.) ( $V_{CC} = +5.0\text{ V}$ , $V_{EE} = \text{Ground}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| Characteristic  | Figure   | Symbol                                       | Min                    | Typ                          | Max                    | Unit            |
|---|----------|--|------------------------|------------------------------|------------------------|-----------------|
| Input Offset Current ( $V_{CM} = 0\text{ V to } 0.5\text{ V}$ , $V_{CM} = 1.0\text{ V to } 5.0\text{ V}$ )<br>$T_A = +25^\circ\text{C}$<br>$T_A = -40^\circ\text{ to } +105^\circ\text{C}$<br>$T_A = -55^\circ\text{ to } +125^\circ\text{C}$ | –        | $ I_{IO} $                                   | –                      | 5.0<br>10<br>–               | 50<br>100<br>200       | nA              |
| Common Mode Input Voltage Range   | –        | $V_{ICR}$                                    | $V_{EE}$               | –                            | $V_{CC}$               | V               |
| Large Signal Voltage Gain ( $V_{CC} = +5.0\text{ V}$ , $V_{EE} = -5.0\text{ V}$ )<br>$R_L = 10\text{ k}\Omega$<br>$R_L = 600\ \Omega$   | 7        | $A_{VOL}$                                    | 50<br>25               | 300<br>250                   | –<br>–                 | kV/V            |
| Output Voltage Swing ( $V_{ID} = \pm 0.2\text{ V}$ )<br>$R_L = 10\text{ k}\Omega$<br>$R_L = 10\text{ k}\Omega$<br>$R_L = 600\ \Omega$<br>$R_L = 600\ \Omega$  | 8, 9, 10 | $V_{OH}$<br>$V_{OL}$<br>$V_{OH}$<br>$V_{OL}$ | 4.85<br>–<br>4.75<br>– | 4.95<br>0.05<br>4.85<br>0.15 | –<br>0.15<br>–<br>0.25 | V               |
| Common Mode Rejection ( $V_{in} = 0\text{ V to } 5.0\text{ V}$ )  | 11       | CMR  | 60                     | 90                           | –                      | dB              |
| Power Supply Rejection Ratio<br>$V_{CC}/V_{EE} = 5.0\text{ V/GND to } 3.0\text{ V/GND}$   | 12       | PSRR   | 500                    | 25                           | –                      | $\mu\text{V/V}$ |
| Output Short Circuit Current (Source and Sink)  | 13, 14   | $I_{SC}$                                     | 50                     | 80                           | –                      | mA              |
| Power Supply Current per Amplifier ( $V_O = 0\text{ V}$ )<br>$T_A = -40^\circ\text{ to } +105^\circ\text{C}$<br>$T_A = -55^\circ\text{ to } +125^\circ\text{C}$   | 15       | $I_D$  | –<br>–                 | 0.9<br>0.9                   | 1.125<br>1.125         | mA              |

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +5.0\text{ V}$ , $V_{EE} = \text{Ground}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| Characteristic   | Figure     | Symbol     | Min    | Typ            | Max    | Unit                      |
|--|------------|------------|--------|----------------|--------|---------------------------|
| Slew Rate<br>( $V_S = \pm 2.5\text{ V}$ , $V_O = -2.0\text{ V to } +2.0\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $A_V = +1.0$ )            | 16, 26     | SR         | 0.5    | 1.0            | –      | V/ $\mu\text{s}$          |
| Gain Bandwidth Product ( $f = 100\text{ kHz}$ )  | 17         | GBW        | –      | 2.2            | –      | MHz                       |
| Gain Margin ( $R_L = 600\ \Omega$ , $C_L = 0\text{ pF}$ )  | 20, 21, 22 | $A_M$      | –      | 12             | –      | dB                        |
| Phase Margin ( $R_L = 600\ \Omega$ , $C_L = 0\text{ pF}$ )   | 20, 21, 22 | $\theta_M$ | –      | 65             | –      | Deg                       |
| Channel Separation ( $f = 1.0\text{ Hz to } 20\text{ kHz}$ , $A_V = 100$ )   | 23         | CS         | –      | 90             | –      | dB                        |
| Power Bandwidth ( $V_O = 4.0\text{ V}_{pp}$ , $R_L = 600\ \Omega$ , $\text{THD} \leq 1\%$ )  |            | $BW_P$     | –      | 28             | –      | kHz                       |
| Total Harmonic Distortion ( $R_L = 600\ \Omega$ , $V_O = 1.0\text{ V}_{pp}$ , $A_V = 1.0$ )<br>$f = 1.0\text{ kHz}$<br>$f = 10\text{ kHz}$ | 24         | THD        | –<br>– | 0.002<br>0.008 | –<br>– | %                         |
| Open Loop Output Impedance<br>( $V_O = 0\text{ V}$ , $f = 2.0\text{ MHz}$ , $A_V = 10$ )   |            | $ Z_O $    | –      | 100            | –      | $\Omega$                  |
| Differential Input Resistance ( $V_{CM} = 0\text{ V}$ )  |            | $R_{in}$   | –      | 200            | –      | k $\Omega$                |
| Differential Input Capacitance ( $V_{CM} = 0\text{ V}$ )   |            | $C_{in}$   | –      | 8.0            | –      | pF                        |
| Equivalent Input Noise Voltage ( $R_S = 100\ \Omega$ )<br>$f = 10\text{ Hz}$<br>$f = 1.0\text{ kHz}$                                       | 25         | $e_n$      | –<br>– | 25<br>20       | –<br>– | nV/<br>$\sqrt{\text{Hz}}$ |
| Equivalent Input Noise Current<br>$f = 10\text{ Hz}$<br>$f = 1.0\text{ kHz}$   | 25         | $i_n$      | –<br>– | 0.8<br>0.2     | –<br>– | pA/<br>$\sqrt{\text{Hz}}$ |

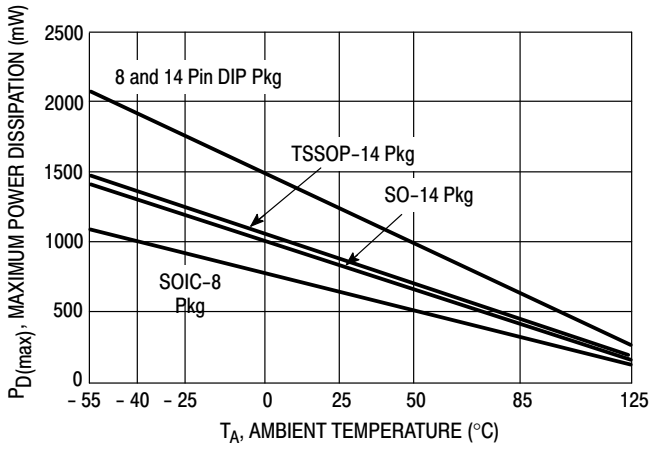


Figure 2. Maximum Power Dissipation versus Temperature

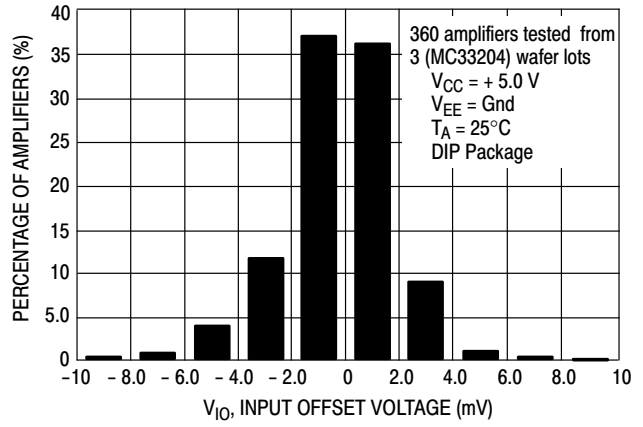


Figure 3. Input Offset Voltage Distribution

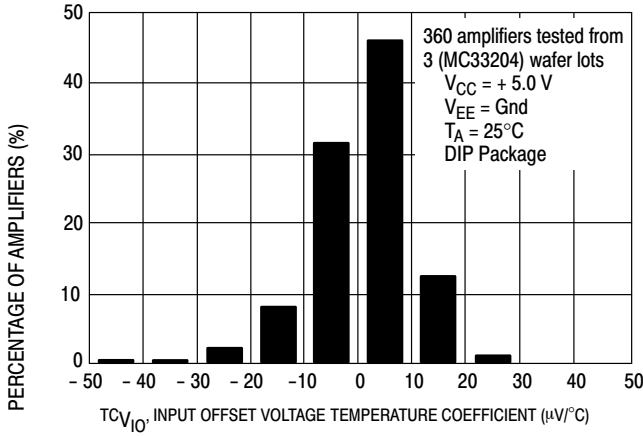


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

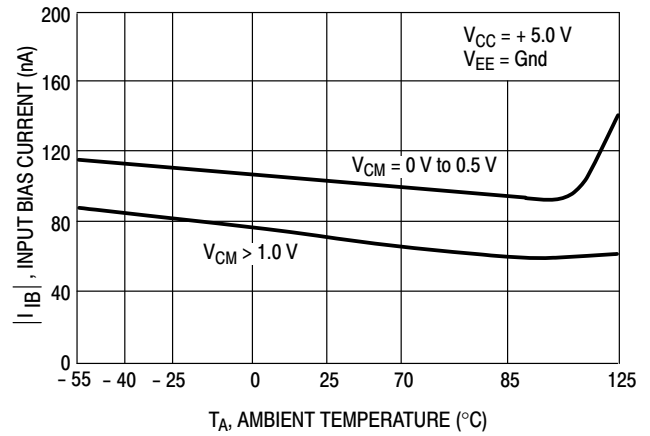


Figure 5. Input Bias Current versus Temperature

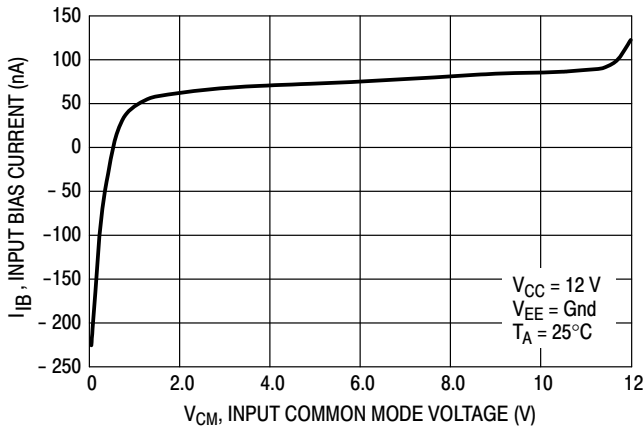


Figure 6. Input Bias Current versus Common Mode Voltage

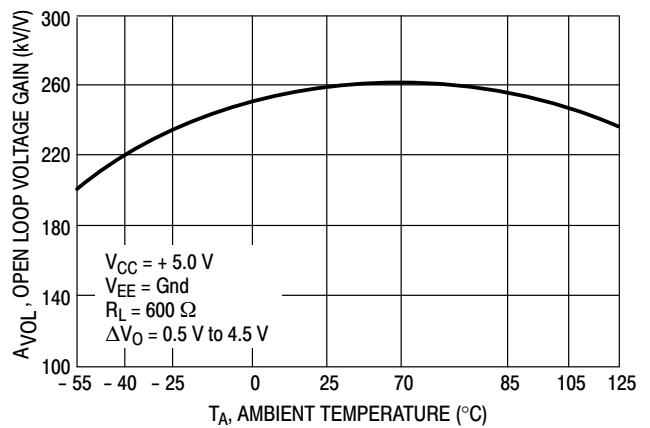


Figure 7. Open Loop Voltage Gain versus Temperature

MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

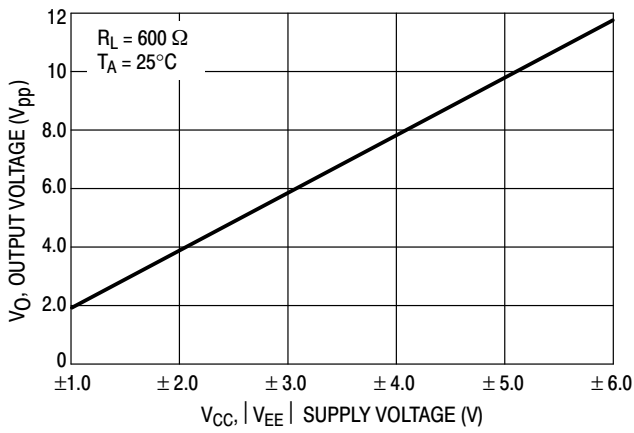


Figure 8. Output Voltage Swing versus Supply Voltage

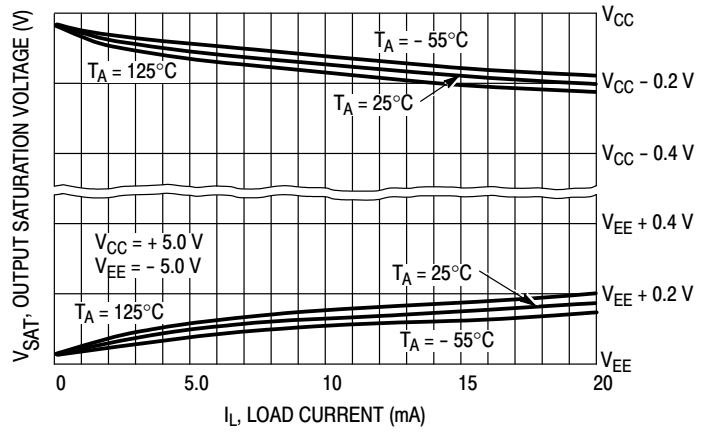


Figure 9. Output Saturation Voltage versus Load Current

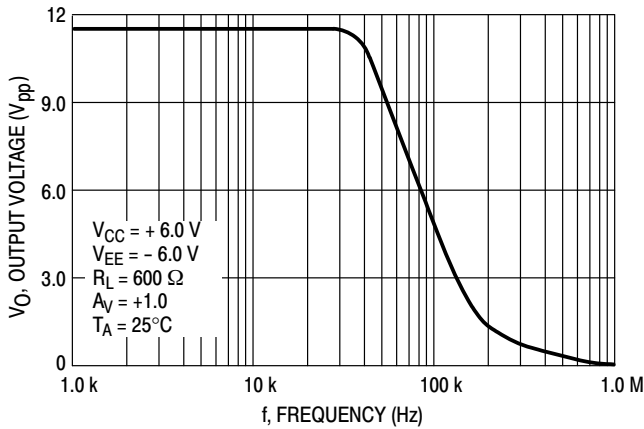


Figure 10. Output Voltage versus Frequency

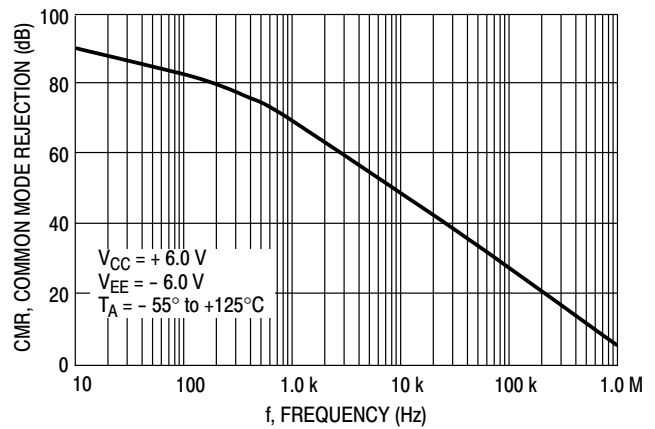


Figure 11. Common Mode Rejection versus Frequency

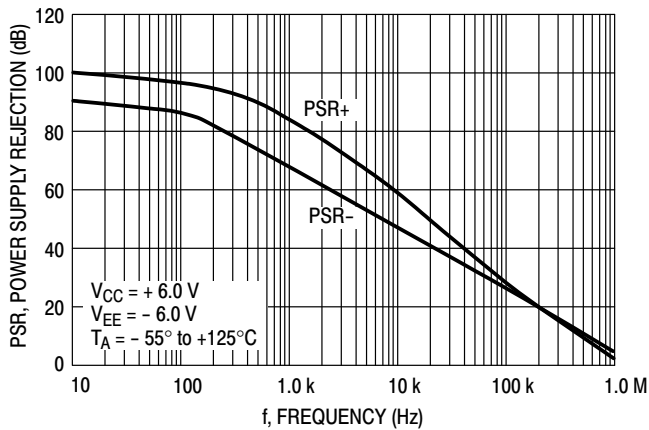


Figure 12. Power Supply Rejection versus Frequency

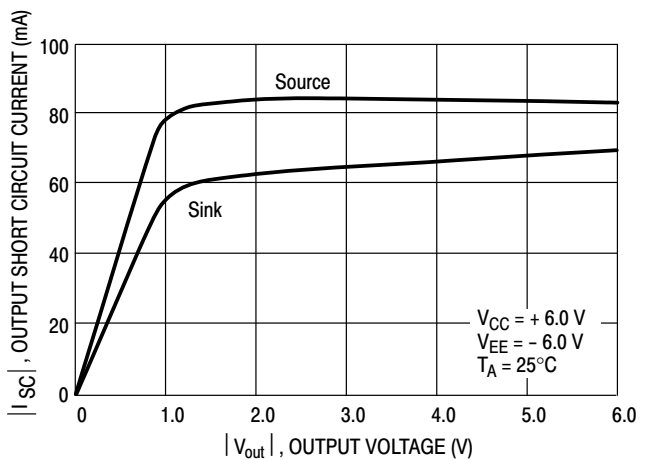


Figure 13. Output Short Circuit Current versus Output Voltage

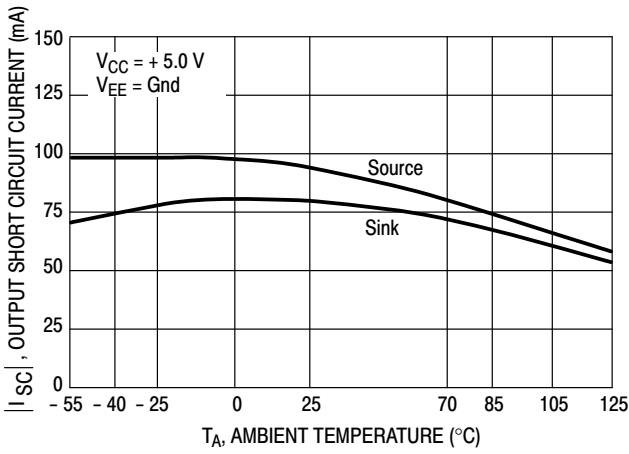


Figure 14. Output Short Circuit Current versus Temperature

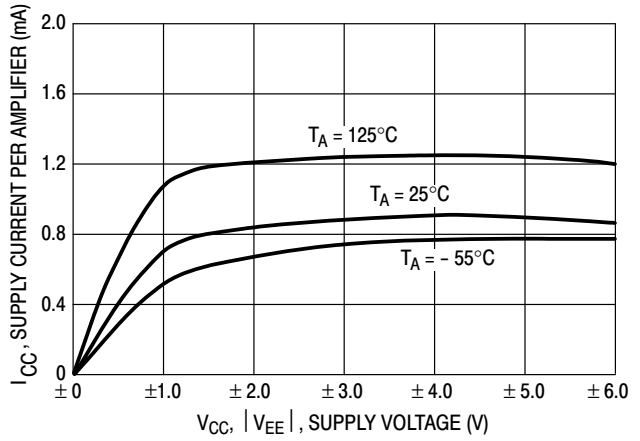


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

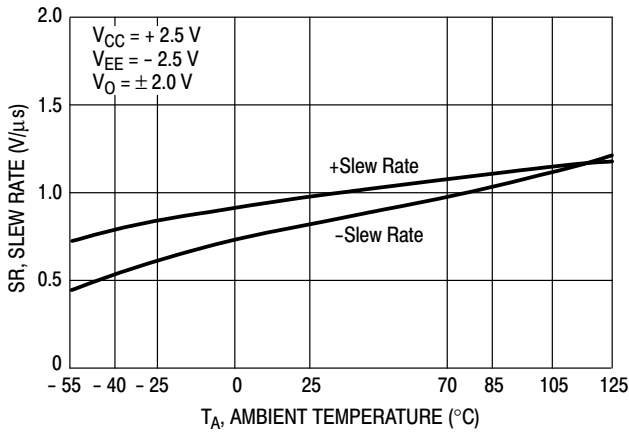


Figure 16. Slew Rate versus Temperature

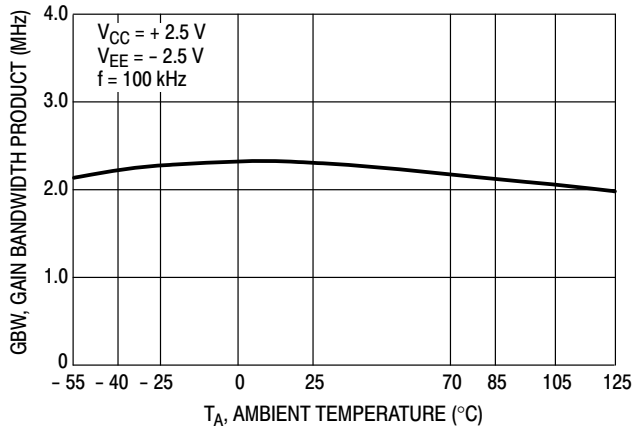


Figure 17. Gain Bandwidth Product versus Temperature

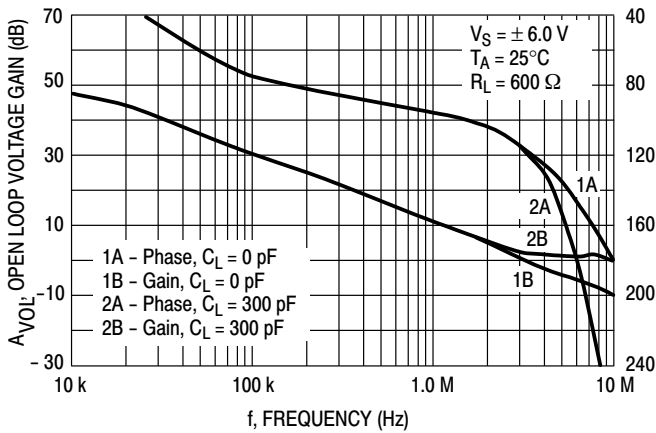


Figure 18. Voltage Gain and Phase versus Frequency

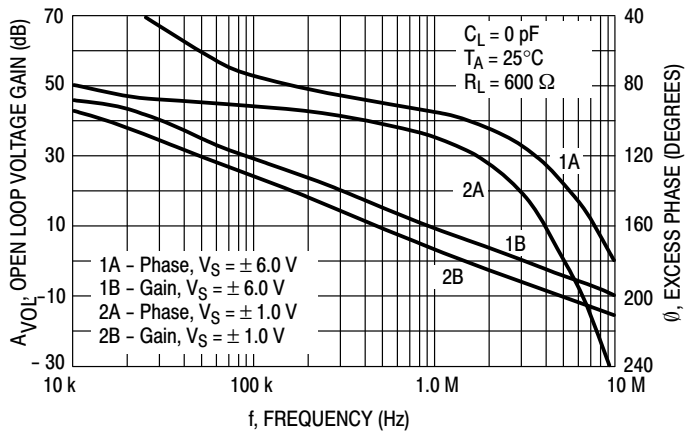


Figure 19. Voltage Gain and Phase versus Frequency

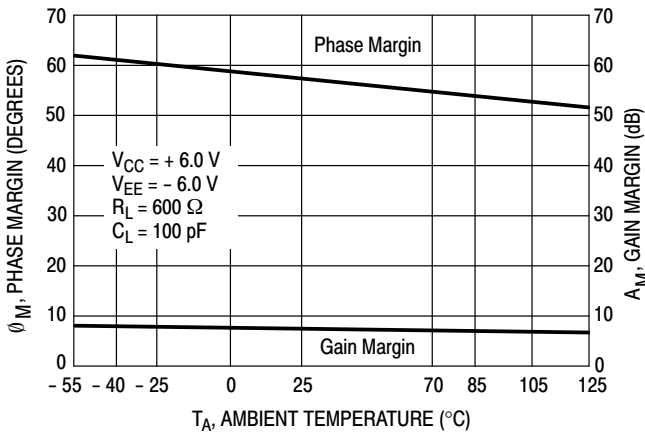


Figure 20. Gain and Phase Margin versus Temperature

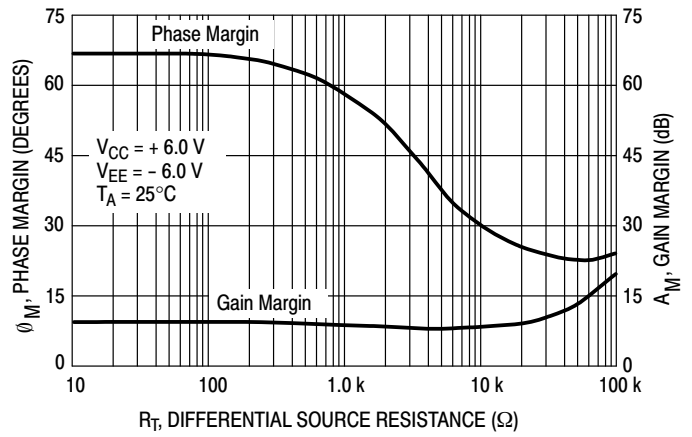


Figure 21. Gain and Phase Margin versus Differential Source Resistance

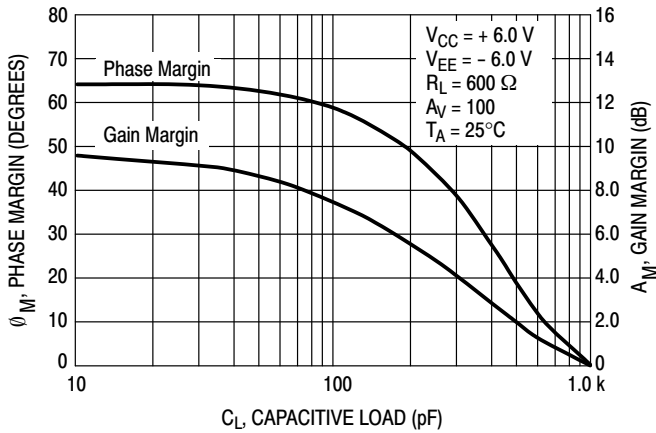


Figure 22. Gain and Phase Margin versus Capacitive Load

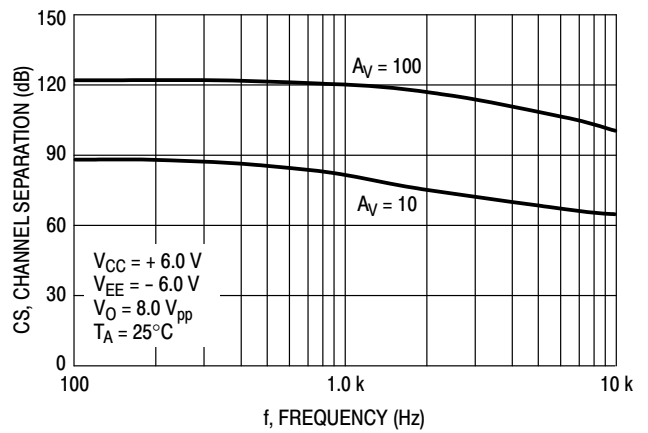


Figure 23. Channel Separation versus Frequency

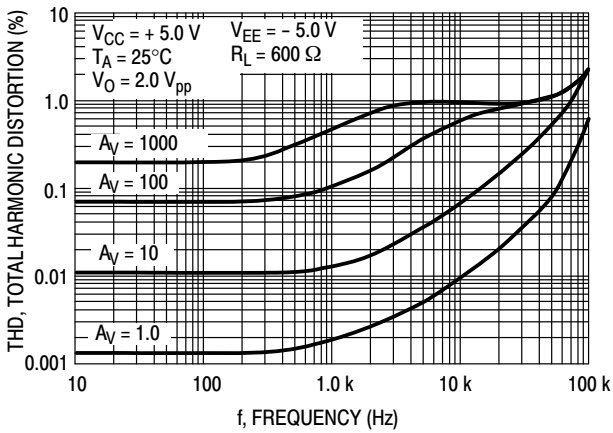


Figure 24. Total Harmonic Distortion versus Frequency

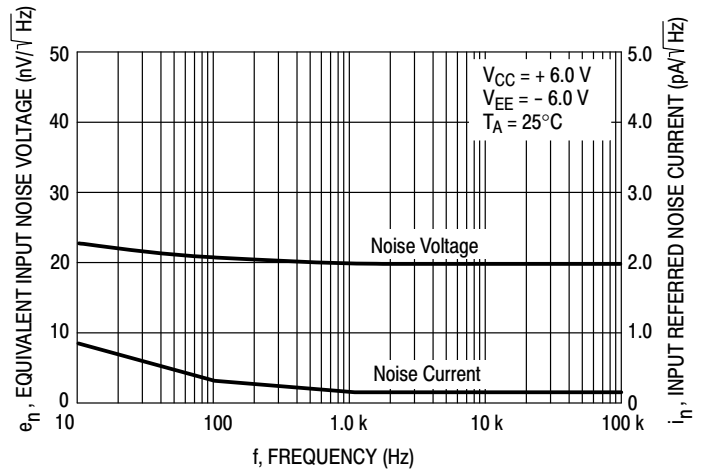


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency



DETAILED OPERATING DESCRIPTION

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from  $V_{CC}$  to  $V_{EE}$ , it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than  $V_{EE}$ , the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600  $\Omega$  loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

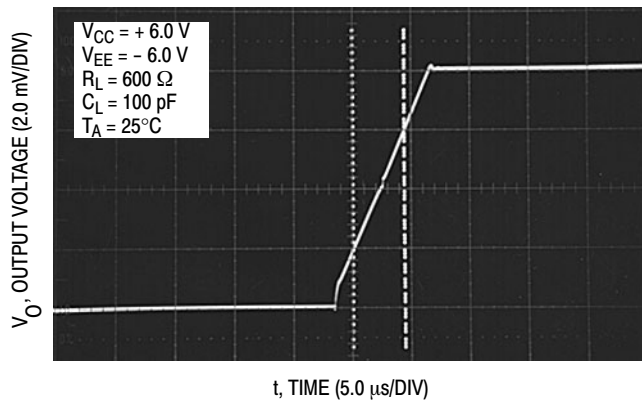


Figure 26. Noninverting Amplifier Slew Rate

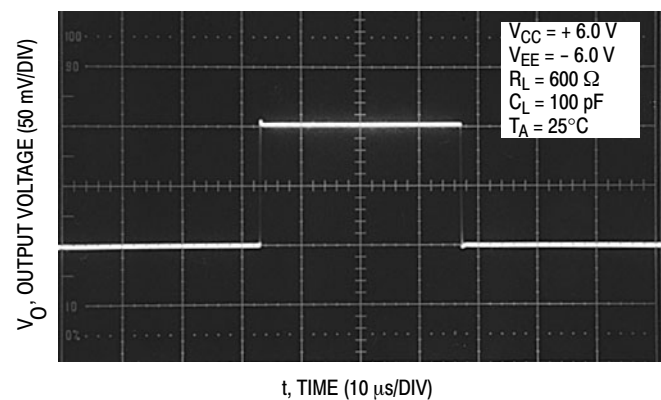


Figure 27. Small Signal Transient Response

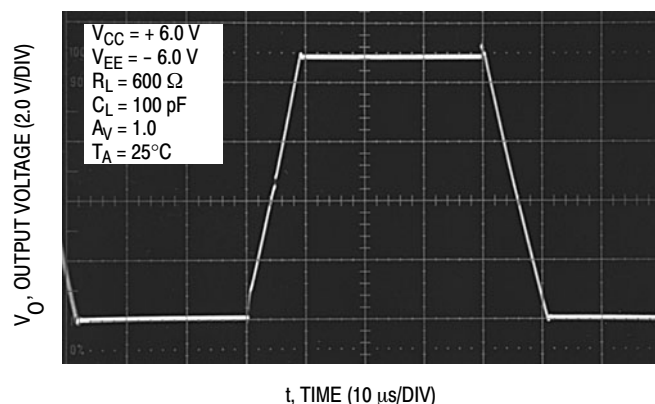


Figure 28. Large Signal Transient Response

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.

# MC33201, MC33202, MC33204, NCV33201, NCV33202, NCV33204

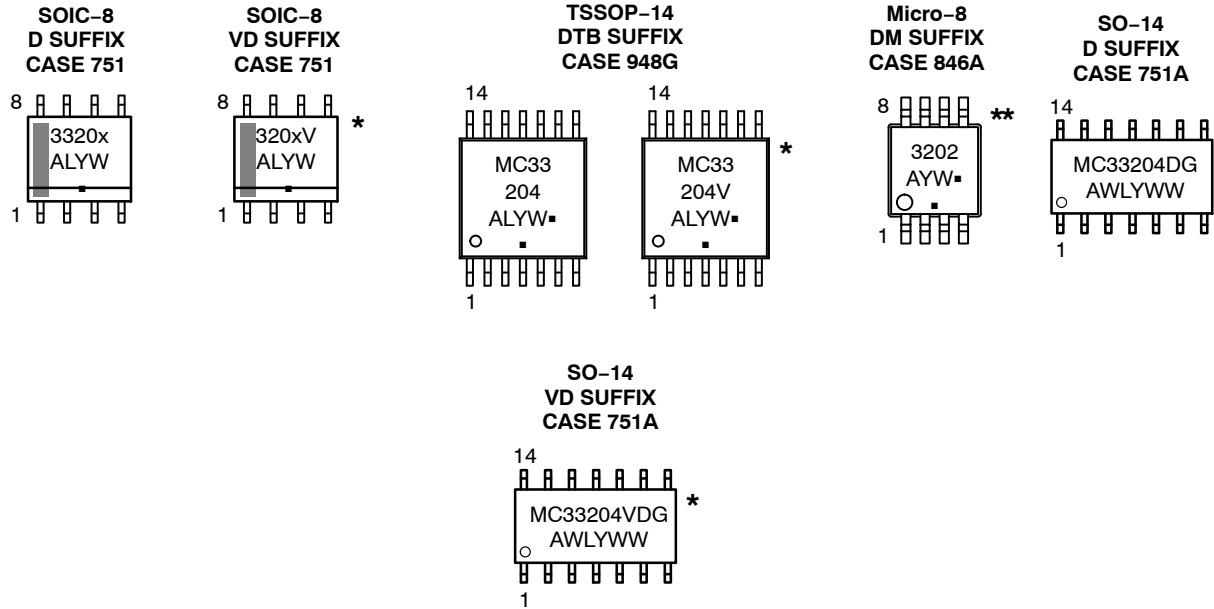
## ORDERING INFORMATION

| Operational Amplifier Function | Device          | Operating Temperature Range               | Package            | Shipping†                |
|--------------------------------|-----------------|---|--------------------|--------------------------|
| Single                         | MC33201DR2G     | $T_A = -40^\circ$ to $+105^\circ\text{C}$ | SOIC-8 (Pb-Free)   | 2500 / Tape & Reel       |
|                                | MC33201VDR2G    | $T_A = -55^\circ$ to $125^\circ\text{C}$  |                    | 2500 / Tape & Reel       |
|                                | NCV33201VDR2G   |   |                    | 2500 / Tape & Reel       |
| Dual                           | MC33202DR2G     | $T_A = -40^\circ$ to $+105^\circ\text{C}$ | SOIC-8 (Pb-Free)   | 2500 / Tape & Reel       |
|                                | MC33202DMR2G    |   | Micro-8 (Pb-Free)  | 4000 / Tape & Reel       |
|                                | NCV33202DMR2G*  |   |                    |                          |
|                                | MC33202VDR2G    | $T_A = -55^\circ$ to $125^\circ\text{C}$  | SOIC-8 (Pb-Free)   | 2500 / Tape & Reel       |
|                                | NCV33202VDR2G*  |   |                    |                          |
| Quad                           | MC33204DR2G     | $T_A = -40^\circ$ to $+105^\circ\text{C}$ | SO-14 (Pb-Free)    | 2500 Units / Tape & Reel |
|                                | MC33204DTBR2G   |   | TSSOP-14 (Pb-Free) | 2500 Units / Tape & Reel |
|                                | NCV33204DR2G*   | $T_A = -55^\circ$ to $125^\circ\text{C}$  | SO-14 (Pb-Free)    | 2500 Units / Tape & Reel |
|                                | NCV33204DTBR2G* |   | TSSOP-14 (Pb-Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

## MARKING DIAGRAMS



x = 1 or 2  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G = Pb-Free Package  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This marking diagram applies to NCV3320xV

\*\*This marking diagram applies to NCV33202DMR2G

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

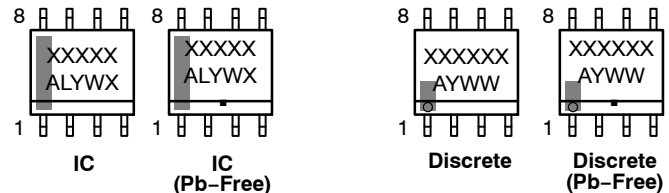
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

### Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020



TOP VIEW

NOTE 3



SIDE VIEW



END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

$\phi 0.08$  (0.003) M C B S A S

| DIM                  | MILLIMETERS |      |      |
|----------------------|-------------|------|------|
|                      | MIN.        | NOM. | MAX. |
| A                    | ---         | ---  | 1.10 |
| A1                   | 0.05        | 0.08 | 0.15 |
| <i>b</i>             | 0.25        | 0.33 | 0.40 |
| <i>c</i>             | 0.13        | 0.18 | 0.23 |
| <i>D</i>             | 2.90        | 3.00 | 3.10 |
| <i>E</i>             | 2.90        | 3.00 | 3.10 |
| <i>e</i>             | 0.65 BSC    |      |      |
| <i>H<sub>E</sub></i> | 4.75        | 4.90 | 5.05 |
| <i>L</i>             | 0.40        | 0.55 | 0.70 |



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

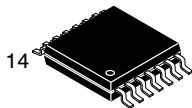
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

TSSOP-14 WB  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

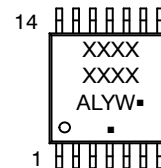


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

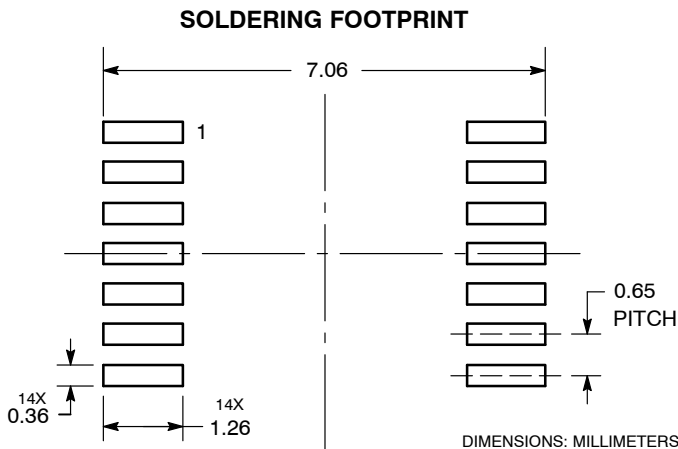
GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



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|------------------|-------------|--|
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| DESCRIPTION:     | TSSOP-14 WB | PAGE 1 OF 1  |

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