MC34262, MC33262

Power Factor Controllers

The MC34262/MC33262 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off−line power converter applications. These integrated circuits feature an internal startup timer for stand−alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle−by−cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual−in−line and surface mount plastic packages.

Features

- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 and TDA4817
- These are Pb−Free and Halide−Free Devices

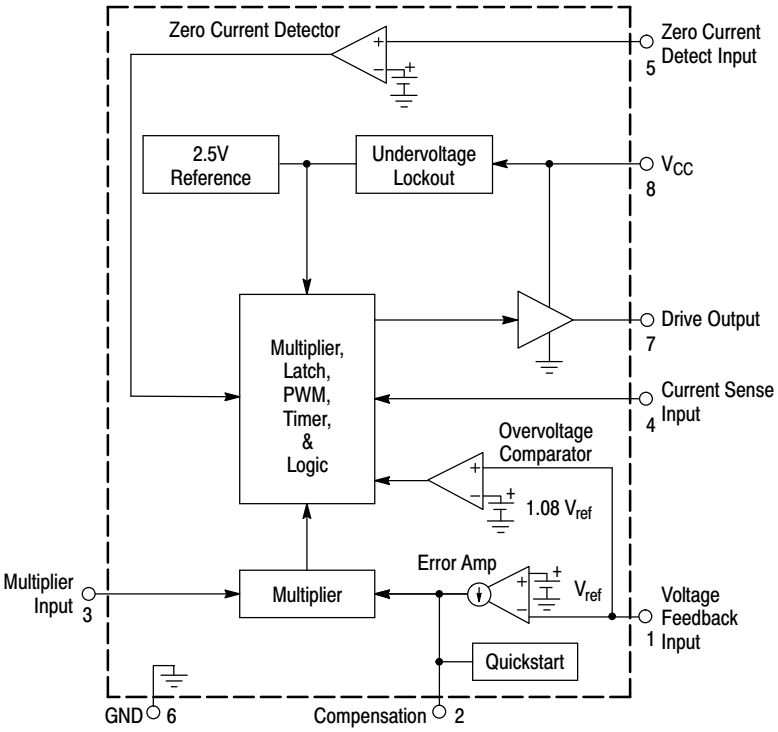

Figure 1. Simplified Block Diagram

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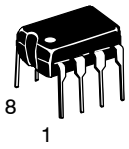
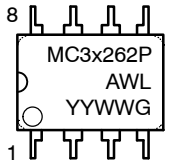
POWER FACTOR CONTROLLERS

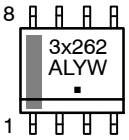
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

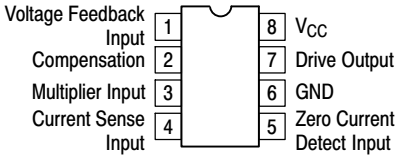


SOIC−8
D SUFFIX
CASE 751



x	= 3 or 4
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	−1.0 to +10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 −10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 4) MC34262 MC33262	T_A	 0 to + 85 − 40 to +105	°C
Storage Temperature	T_{stg}	− 65 to +150	°C
ESD Protection (Note 2) Human Body Model ESD Machine Model ESD Charged Device Model ESD	 HBM MM CDM	 2000 200 2000	 V V V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum package power dissipation limits must be observed.
2. ESD protection per JEDEC JESD22−A114−F for HBM, per JEDEC JESD22−A115−A for MM, and per JEDEC JESD22−C101D for CDM. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 3), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C T_A = T_{low} to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	 2.5 −	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	−	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	−	− 0.1	− 0.5	μA
Transconductance (T_A = 25°C)	g_m	80	100	130	μmho
Output Current Source (V_{FB} = 2.3 V) Sink (V_{FB} = 2.7 V)	I_O	 − −	 10 10	 − −	μA
Output Voltage Swing High State (V_{FB} = 2.3 V) Low State (V_{FB} = 2.7 V)	 $V_{OH(ea)}$ $V_{OL(ea)}$	 5.8 −	 6.4 1.7	 − 2.4	V
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.065 V_{FB}	1.08 V_{FB}	1.095 V_{FB}	V
MULTIPLIER					
Input Bias Current, Pin 3 (V_{FB} = 0 V)	I_{IB}	−	− 0.1	− 0.5	μA
Input Threshold, Pin 2	$V_{th(M)}$	1.05 $V_{OL(EA)}$	1.2 $V_{OL(EA)}$	−	V

3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. T_{low} = 0°C for MC34262 = −40°C for MC33262 T_{high} = +85°C for MC34262 = +105°C for MC33262.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V (Note 6), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 7), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
MULTIPLIER					
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.5)	 – –	V
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2}$ = $V_{th(M)}$ + 1.0 V) (Note 8)	K	0.43	0.65	0.87	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.33	1.6	1.87	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Input Clamp Voltage High State (I_{DET} = + 3.0 mA) Low State (I_{DET} = – 3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 – 1.0	V
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	–	– 0.15	–1.0	μA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	–	9.0	25	mV
Maximum Current Sense Input Threshold (Note 9)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output	$t_{PHL(in/out)}$	–	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V) Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – – 9.8 7.8	 0.3 2.4 10.3 8.4	 0.8 3.3 – –	V
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UVLO)}$	–	0.1	0.5	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	200	620	–	μs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	3.8	5.0	6.2	V
TOTAL DEVICE					
Power Supply Current Startup (V_{CC} = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)	I_{CC}	 – – –	 0.25 6.5 9.0	 0.4 12 20	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	V

5. Maximum package power dissipation limits must be observed.
6. Adjust V_{CC} above the startup threshold before setting to 12 V.
7. T_{low} = 0°C for MC34262 = –40°C for MC33262 T_{high} = +85°C for MC34262 = +105°C for MC33262.
8. $K = \frac{\text{Pin 4 Threshold}}{V_{Pin\ 3}\,(V_{Pin2} - V_{th(M)})}$
9. This parameter is measured with V_{FB} = 0 V, and $V_{Pin\ 3}$ = 3.0 V.

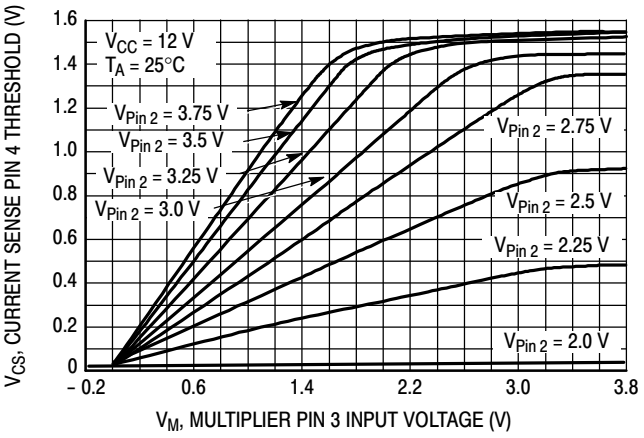


Figure 2. Current Sense Input Threshold versus Multiplier Input

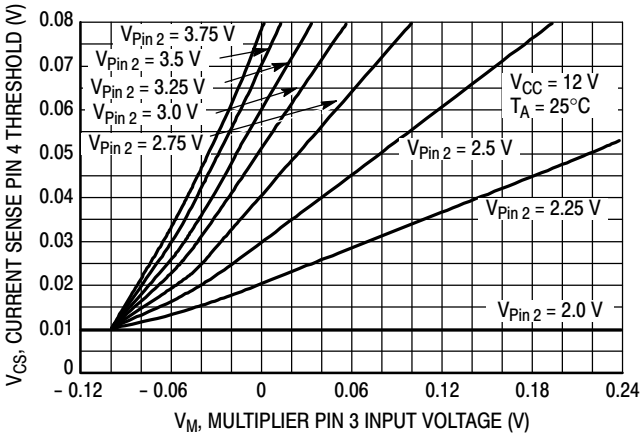


Figure 3. Current Sense Input Threshold versus Multiplier Input, Expanded View

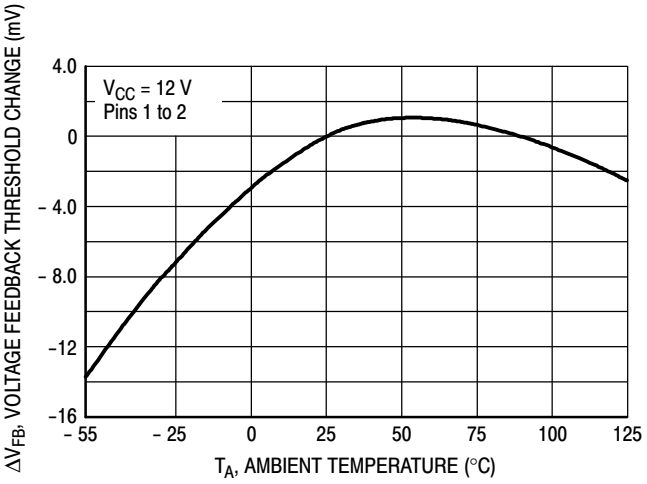


Figure 4. Voltage Feedback Input Threshold Change versus Temperature

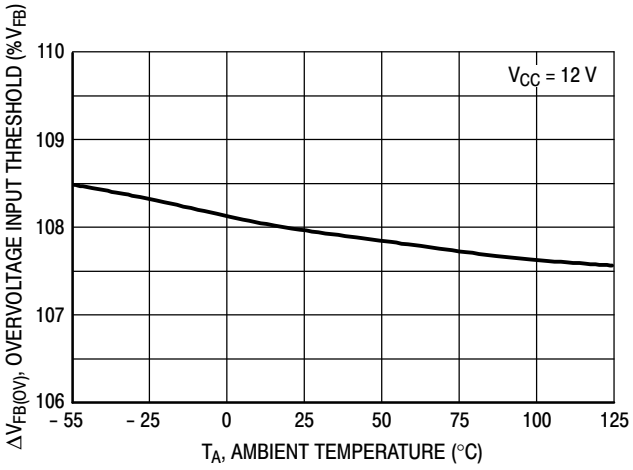


Figure 5. Overvoltage Comparator Input Threshold versus Temperature

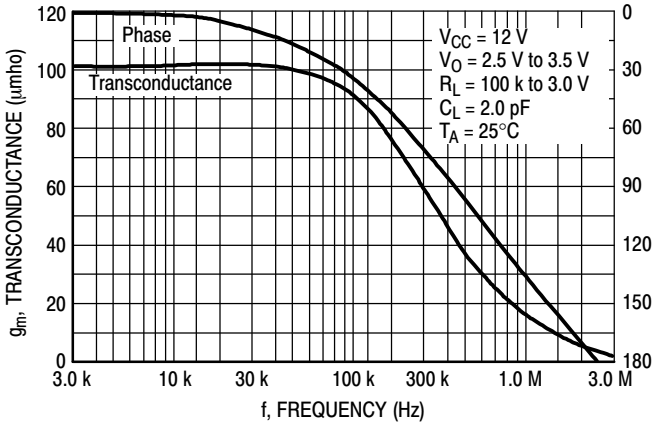


Figure 6. Error Amp Transconductance and Phase versus Frequency

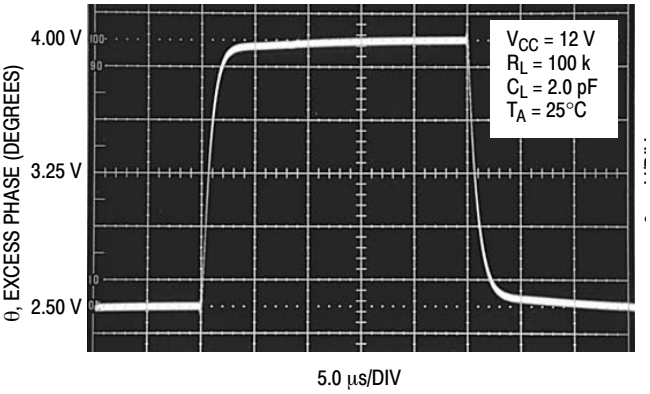


Figure 7. Error Amp Transient Response

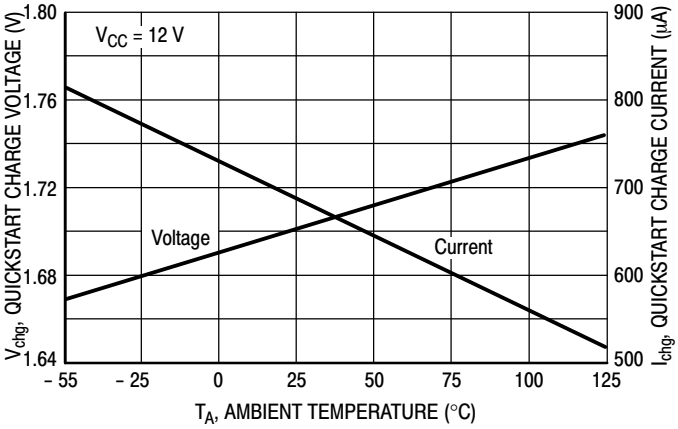


Figure 8. Quickstart Charge Current versus Temperature

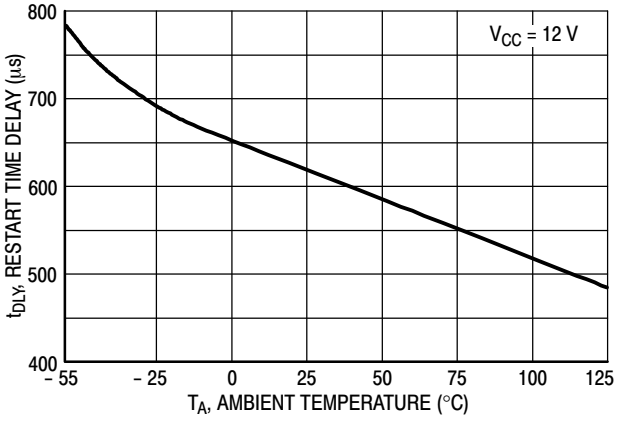


Figure 9. Restart Timer Delay versus Temperature

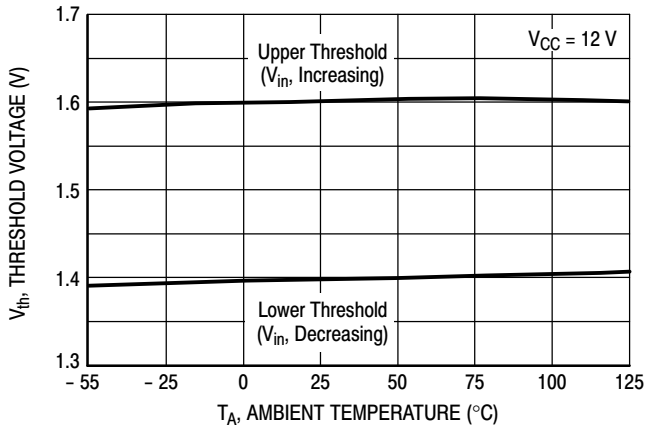


Figure 10. Zero Current Detector Input Threshold Voltage versus Temperature

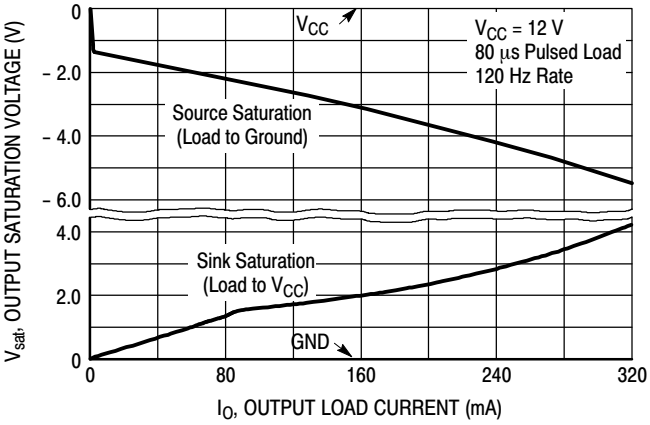


Figure 11. Output Saturation Voltage versus Load Current

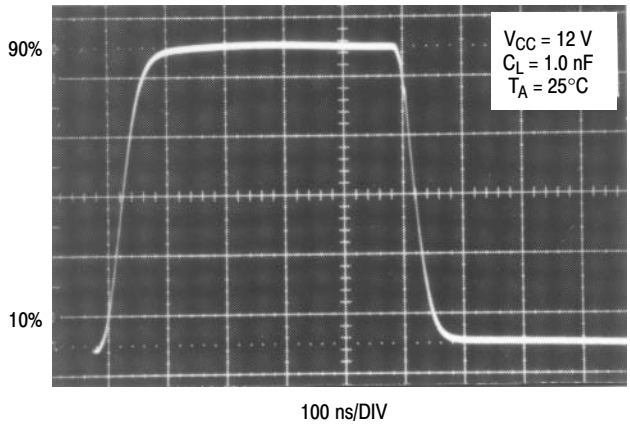


Figure 12. Drive Output Waveform

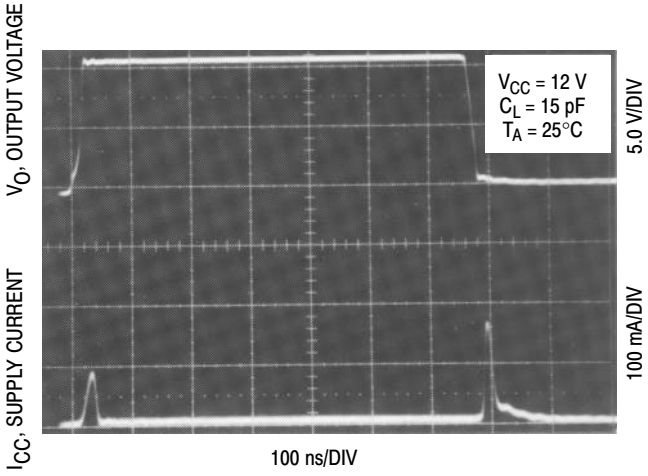


Figure 13. Drive Output Cross Conduction

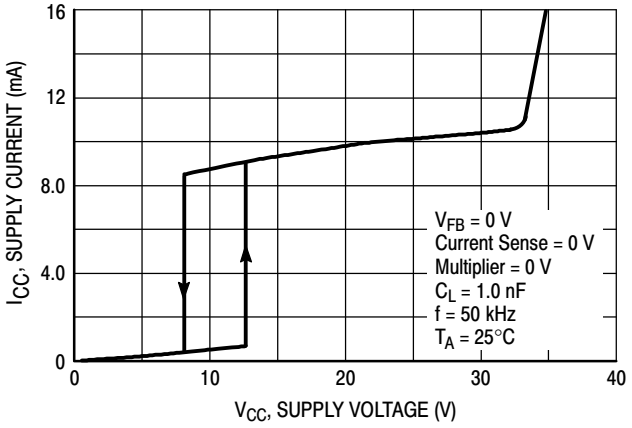


Figure 14. Supply Current versus Supply Voltage

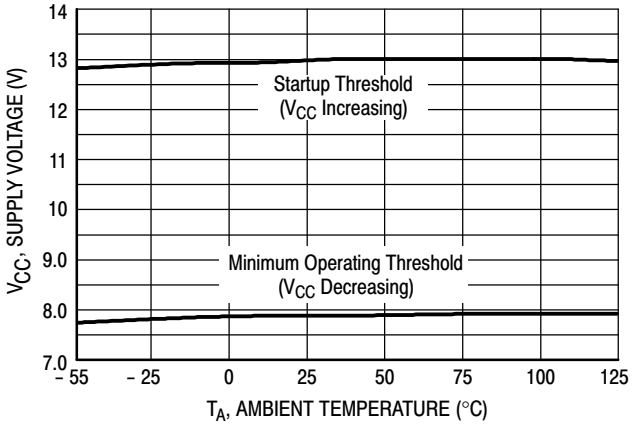


Figure 15. Undervoltage Lockout Thresholds versus Temperature

FUNCTIONAL DESCRIPTION

Introduction

With the goal of exceeding the requirements of legislation on line−current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple, cost−effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 16.

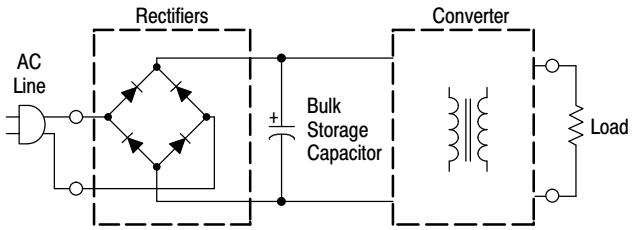


Figure 16. Uncorrected Power Factor Circuit

This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 17. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Power factor correction can be achieved with the use of either a passive or an active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing, with the boost converter being the most popular topology, Figure 18. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

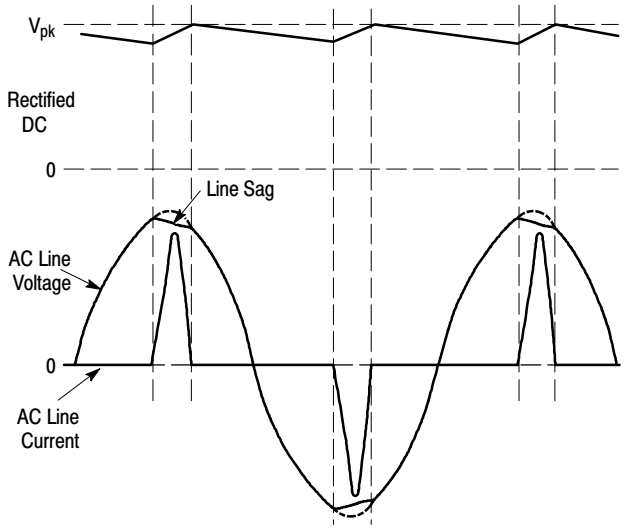


Figure 17. Uncorrected Power Factor Input Waveforms

The MC34262, MC33262 are high performance, critical conduction, current−mode power factor controllers specifically designed for use in off−line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage.

Operating Description

The MC34262, MC33262 contain many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagrams in Figures 20, 21, and 22 note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. The reasons for these differences will become apparent in the following discussion. A description of each of the functional blocks is given below.

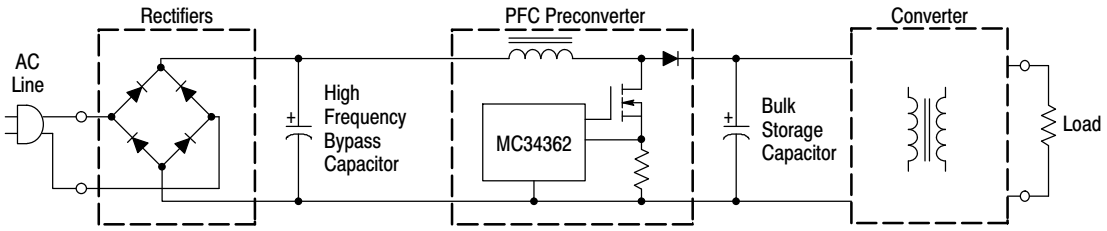


Figure 18. Active Power Factor Correction Preconverter

Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage−to−current gain. The amplifier features a typical gm of 100 μmhos (Figure 6). The noninverting input is internally biased at 2.5 V ± 2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is − 0.5 μA, which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amp monitors the average output voltage of the converter over several line cycles. The Error Amp output stage was designed to have a relatively constant transconductance over temperature. This allows the designer to define the compensated bandwidth over the intended operating temperature range. The output stage can sink and source 10 μA of current and is capable of swinging from 1.7 V to 6.4 V, assuring that the Multiplier can be driven over its entire dynamic range.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of of the Voltage Feedback Input pin by the Error Amplifier and by the Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C_3 must be large enough to keep the peak−to−peak ripple less than 16% of the average dc output. The Overvoltage Comparator input to Drive Output turn−off propagation delay is typically 400 ns. A comparison of startup overshoot without and with the Overvoltage Comparator circuit is shown in Figure 24.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac full wave rectified haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. The Multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0 V to 3.2 V for Pin 3, and 2.0 V to 3.75 V for Pin 2, Figures 2 and 3. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line, Figure 18. This has the effect of forcing the MOSFET on−time to track the input line voltage, resulting in a fixed Drive Output on−time, thus making the preconverter load appear to be resistive to the ac line. An approximation of the Current Sense Comparator threshold can be calculated from the following equation. This equation is accurate only under the given test condition stated in the electrical table.

$$V_{CS}, \text{ Pin 4 Threshold} \approx 0.65\ (V_{Pin\ 2} - V_{th(M)})\ V_{Pin\ 3}$$

A significant reduction in line current distortion can be attained by forcing the preconverter to switch as the ac line voltage crosses through zero. The forced switching is achieved by adding a controlled amount of offset to the Multiplier and Current Sense Comparator circuits. The equation shown below accounts for the built−in offsets and is accurate to within ten percent. Let $V_{th(M)}$ = 1.991 V

$$V_{CS}, \text{ Pin 4 Threshold} = 0.544\ (V_{Pin\ 2} - V_{th(M)})\ V_{Pin\ 3} + 0.0417\ (V_{Pin\ 2} - V_{th(M)})$$

Zero Current Detector

The MC34262 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on−time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn−on until the inductor current reaches zero, the output rectifier reverse recovery time becomes less critical, allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous, thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.4 V. To prevent false tripping, 200 mV of hysteresis is provided. Figure 10 shows that the thresholds are well−defined over temperature. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Current limit protection of the lower clamp transistor is provided in the event that the input pin is accidentally shorted to ground. The Zero Current Detector input to Drive Output turn−on propagation delay is typically 320 ns.

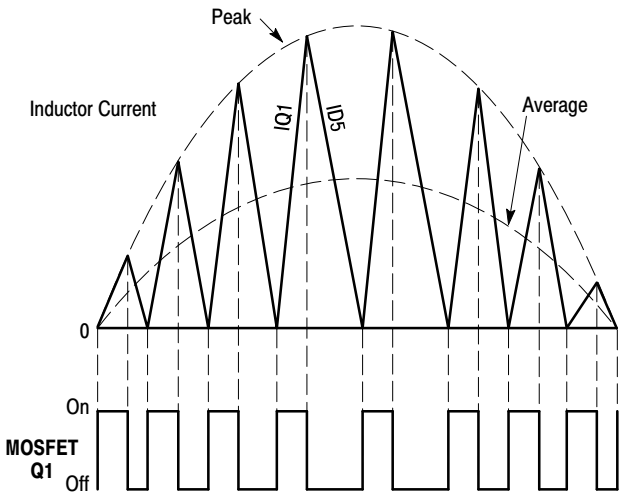


Figure 19. Inductor Current and MOSFET Gate Voltage Waveforms

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground−referenced sense resistor R_7 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 4 where:

$$I_{L(pk)} = \frac{\text{Pin 4 Threshold}}{R_7}$$

Abnormal operating conditions occur during preconverter startup at extremely high line or if output voltage sensing is lost. Under these conditions, the Multiplier output and Current Sense threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is limited to:

$$I_{pk(max)} = \frac{1.5\ V}{R_7}$$

An internal RC filter has been included to attenuate any high frequency noise that may be present on the current waveform. This filter helps reduce the ac line current distortion especially near the zero crossings. With the component values shown in Figure 21, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output turn−off propagation delay is typically less than 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand−alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 620 μs after the inductor current reaches zero. The restart time delay versus temperature is shown in Figure 9.

Undervoltage Lockout and Quickstart

An Undervoltage Lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 13 V and the lower threshold at 8.0 V. In the stand−by mode, with V_{CC} at 7.0 V, the required supply current is less than 0.4 mA. This large hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off−line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_4 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter. The supply current, startup, and operating voltage characteristics are shown in Figures 14 and 15.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C_1 will be discharged, holding the error amp output below the Multiplier threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor C_4 by diode D_6. If Pin 2 does not reach the multiplier threshold before C_4 discharges below the lower UVLO threshold, the converter will "hiccup" and experience a significant startup delay. The Quickstart circuit is designed to precharge C_1 to 1.7 V, Figure 8. This level is slightly below the Pin 2 Multiplier threshold, allowing immediate Drive Output switching and bootstrap operation when C_4 crosses the upper UVLO threshold.

Drive Output

The MC34262/MC33262 contain a single totem−pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pulldown resistor. The totem−pole output has been optimized to minimize cross−conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, helps to reduce the cross−conduction current and radiated noise by limiting the output rise and fall time. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

APPLICATIONS INFORMATION

The application circuits shown in Figures 20, 21 and 22 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current−mode boost converter that operates in critical conduction mode with a fixed on−time and variable off−time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 20 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of 80 W (230 V at 350 mA) with an associated power factor of approximately 0.998 at nominal line. Figures 21 and 22 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 21 provides an output power of 175 W (400 V at 440 mA) while Figure 22 provides 450 W (400 V at 1.125 A). Both circuits have an observed worst−case power factor of approximately 0.989. The input current and voltage waveforms of Figure 21 are shown in Figure 23 with operation at 115 Vac and 230 Vac. The data for each of the applications was generated with the test set−up shown in Figure 25.

Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.	Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\, Vac_{(LL)}^2}{\sqrt{2}\,V_O\,P_O}$
In theory the on−time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_5. Let Vac = $Vac_{(LL)}$ for initial t_{on} and t_{off} calculations.	Switch On−Time	$t_{on} = \frac{2\,P_O\,L_P}{\eta\, Vac^2}$
The off−time t_{off} is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off−Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert Sin\,\theta\rvert}} - 1$
The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, t_{off} approaches zero producing an increase in switching frequency.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.	Peak Switch Current	$R_7 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_5}{R_3} + 1\right)}$
The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 50 μA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_2$
The calculated peak−to−peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3.	Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(pp)} = I_O\sqrt{\left(\frac{1}{2\pi f_{ac}\,C_3}\right)^2 + ESR^2}$
The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C_1 may need to be increased. (See Figure 26)	Error Amplifier Bandwidth	$BW = \frac{gm}{2\,\pi\,C_1}$

The following converter characteristics must be chosen:

V_O − Desired output voltage — Vac − AC RMS line voltage

I_O − Desired output current — $Vac_{(LL)}$ − AC RMS low line voltage

ΔV_O − Converter output peak−to−peak ripple voltage

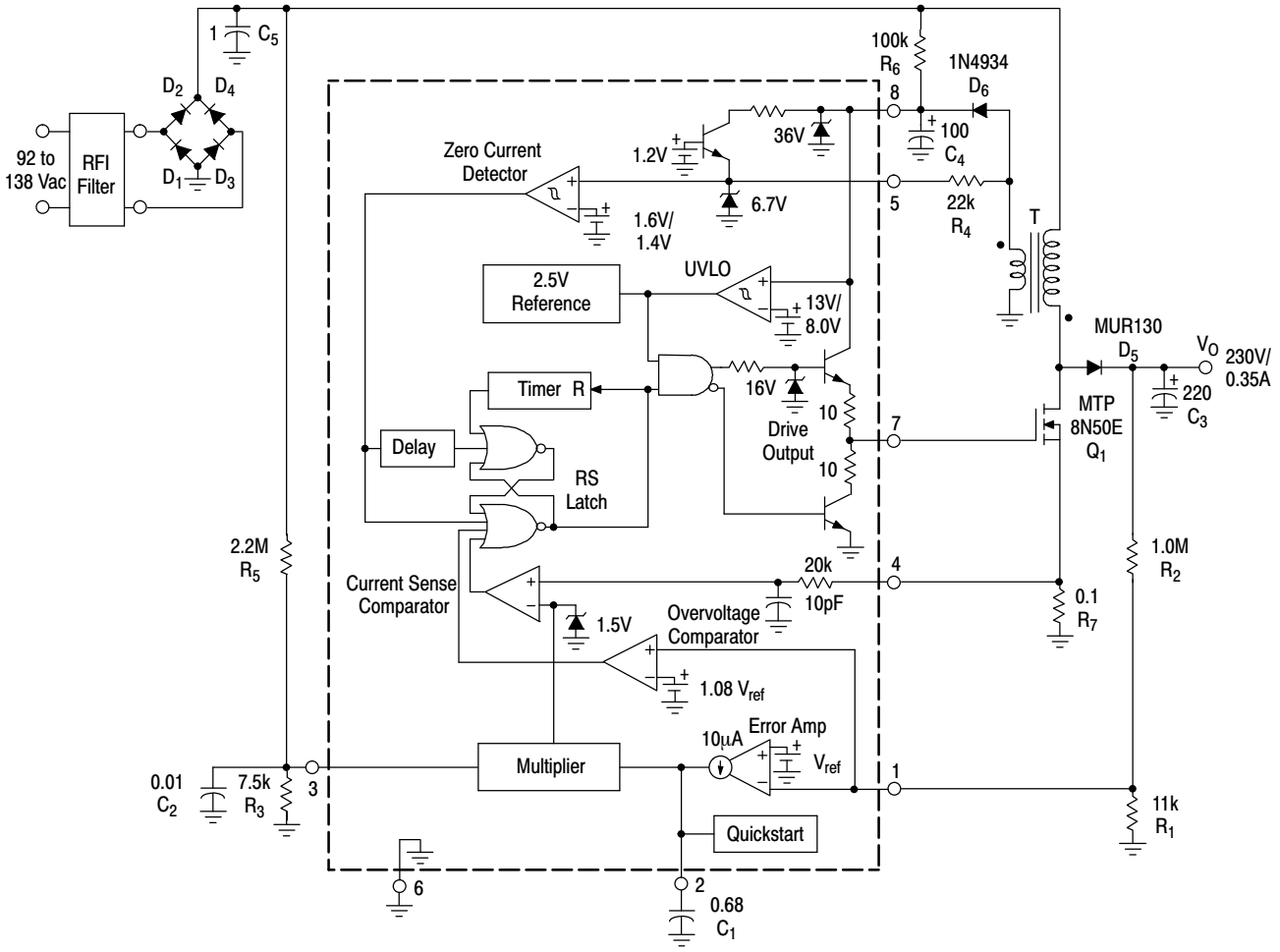


Figure 20. 80 W Power Factor Controller

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	85.9	0.999	0.93	2.6	0.08	1.6	0.84	0.95	4.0	230.7	0.350	80.8	94.0
100	85.3	0.999	0.85	2.3	0.13	1.0	1.2	0.73	4.0	230.7	0.350	80.8	94.7
110	85.1	0.998	0.77	2.2	0.10	0.58	1.5	0.59	4.0	230.7	0.350	80.8	94.9
120	84.7	0.998	0.71	3.0	0.09	0.73	1.9	0.58	4.1	230.7	0.350	80.8	95.3
130	84.4	0.997	0.65	3.9	0.12	1.7	2.2	0.61	4.1	230.7	0.350	80.8	95.7
138	84.1	0.996	0.62	4.6	0.16	2.4	2.3	0.60	4.1	230.7	0.350	80.8	96.0

This data was taken with the test set−up shown in Figure 25.

T = Coilcraft N2881−A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance (L_P) of 320 μH

Heatsink = AAVID Engineering Inc. 590302B03600, or 593002B03400

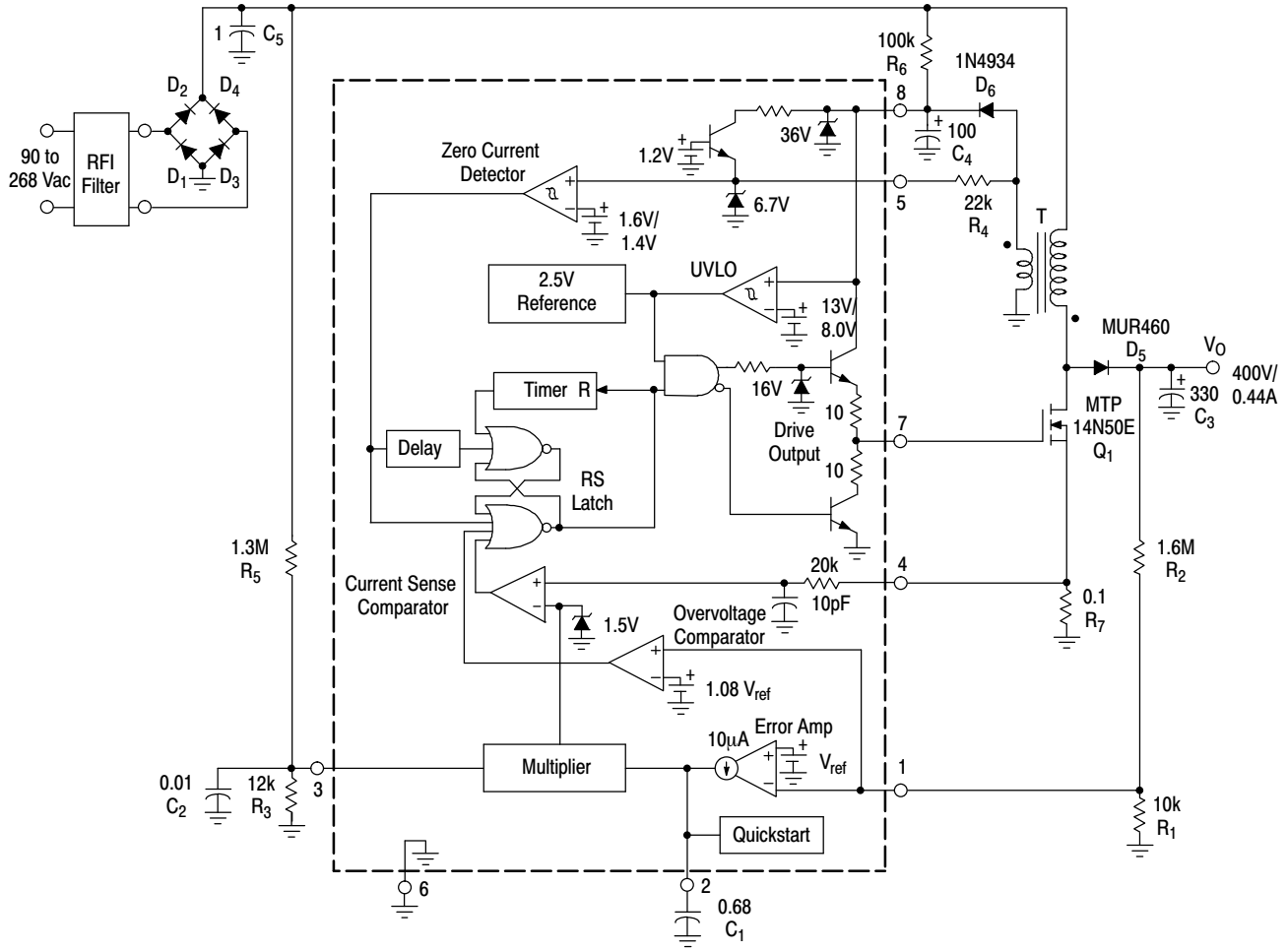


Figure 21. 175 W Universal Input Power Factor Controller

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	193.3	0.991	2.15	2.8	0.18	2.6	0.55	1.0	3.3	402.1	0.44	176.9	91.5
120	190.1	0.998	1.59	1.6	0.10	1.4	0.23	0.72	3.3	402.1	0.44	176.9	93.1
138	188.2	0.999	1.36	1.2	0.12	1.3	0.65	0.80	3.3	402.1	0.44	176.9	94.0
180	184.9	0.998	1.03	2.0	0.10	0.49	1.2	0.82	3.4	402.1	0.44	176.9	95.7
240	182.0	0.993	0.76	4.4	0.09	1.6	2.3	0.51	3.4	402.1	0.44	176.9	97.2
268	180.9	0.989	0.69	5.9	0.10	2.3	2.9	0.46	3.4	402.1	0.44	176.9	97.8

This data was taken with the test set−up shown in Figure 25.

T = Coilcraft N2880−A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42−15
Gap: 0.104″ total for a primary inductance (L_P) of 870 μH

Heatsink = AAVID Engineering Inc. 590302B03600

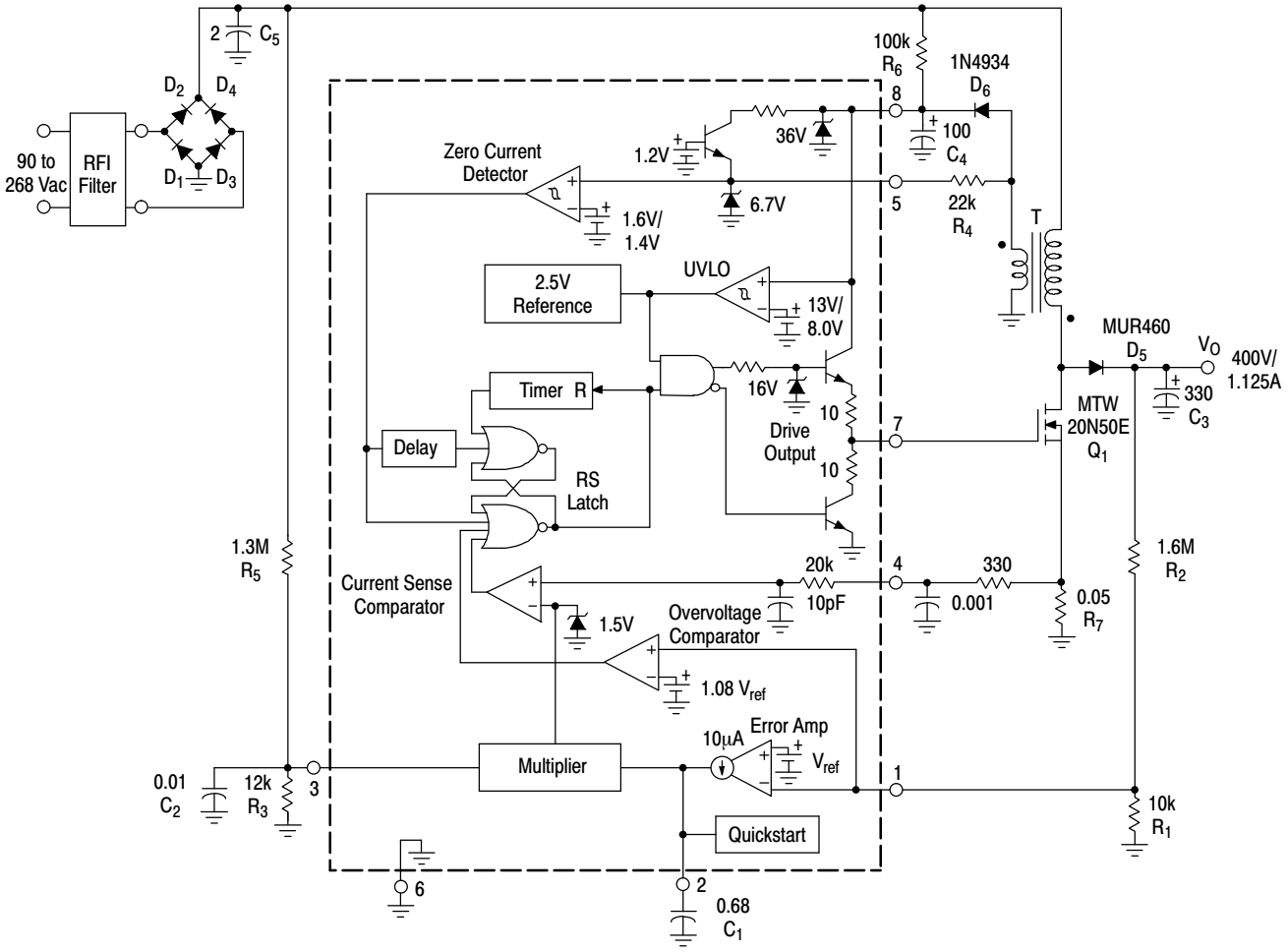


Figure 22. 450 W Universal Input Power Factor Controller

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	489.5	0.990	5.53	2.2	0.10	1.5	0.25	0.83	8.8	395.5	1.14	450.9	92.1
120	475.1	0.998	3.94	2.5	0.12	0.29	0.62	0.52	8.8	395.5	1.14	450.9	94.9
138	470.6	0.998	3.38	2.1	0.06	0.70	1.1	0.41	8.8	395.5	1.14	450.9	95.8
180	463.4	0.998	2.57	4.1	0.21	2.0	1.6	0.71	8.9	395.5	1.14	450.9	97.3
240	460.1	0.996	1.91	4.8	0.14	4.3	2.2	0.63	8.9	395.5	1.14	450.9	98.0
268	459.1	0.995	1.72	5.8	0.10	5.0	2.5	0.61	8.9	395.5	1.14	450.9	98.2

This data was taken with the test set−up shown in Figure 25.

T = Coilcraft P3657−A
Primary: 38 turns Litz wire, 1300 strands of #48 AWG, Kerrigan−Lewis, Chicago, IL
Secondary: 3 turns of # 20 AWG
Core: Coilcraft PT4220, EE 42−20
Gap: 0.180″ total for a primary inductance (L_P) of 190 μH

Heatsink = AAVID Engineering Inc. 604953B04000 Extrusion

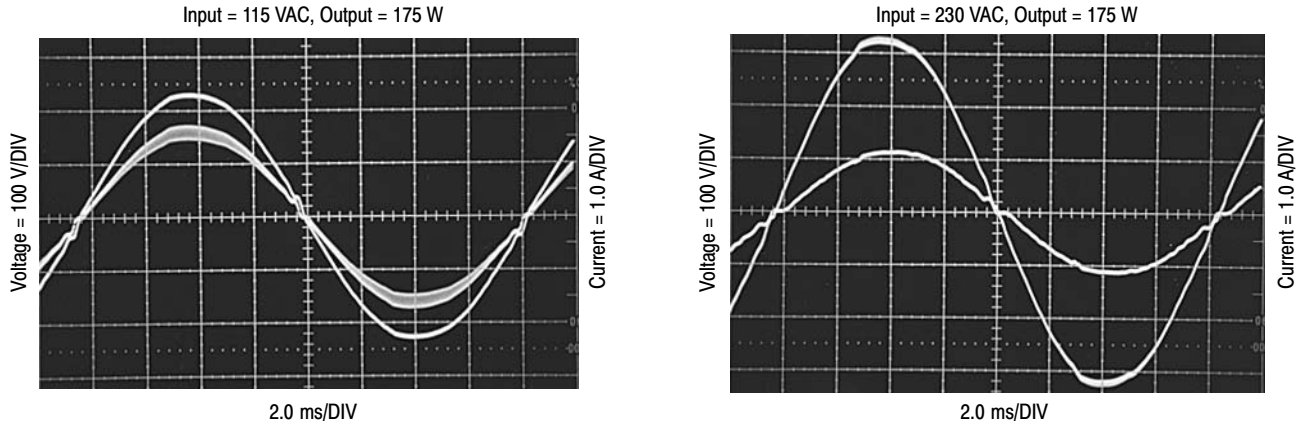


Figure 23. Power Factor Corrected Input Waveforms (Figure 21 Circuit)

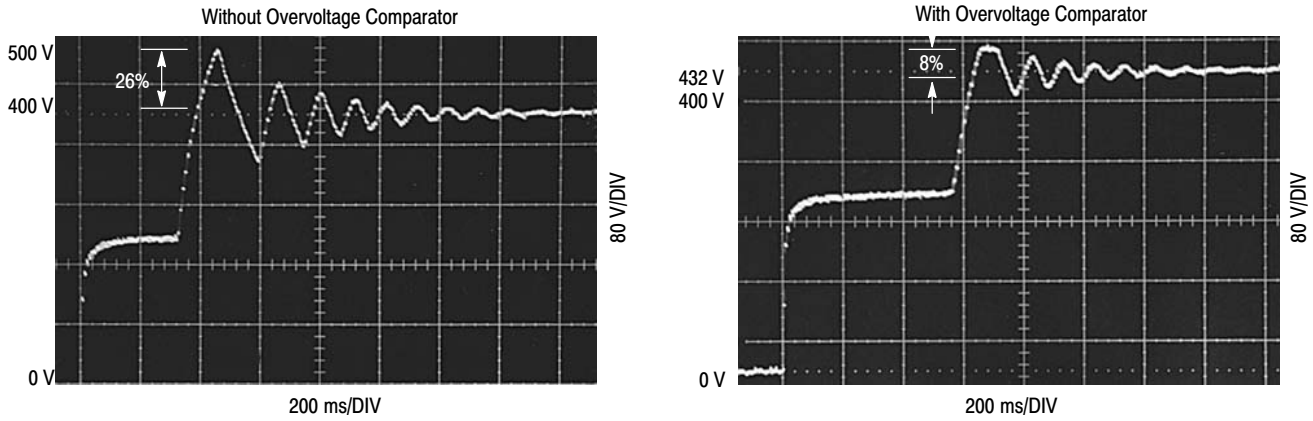


Figure 24. Output Voltage Startup Overshoot (Figure 21 Circuit)

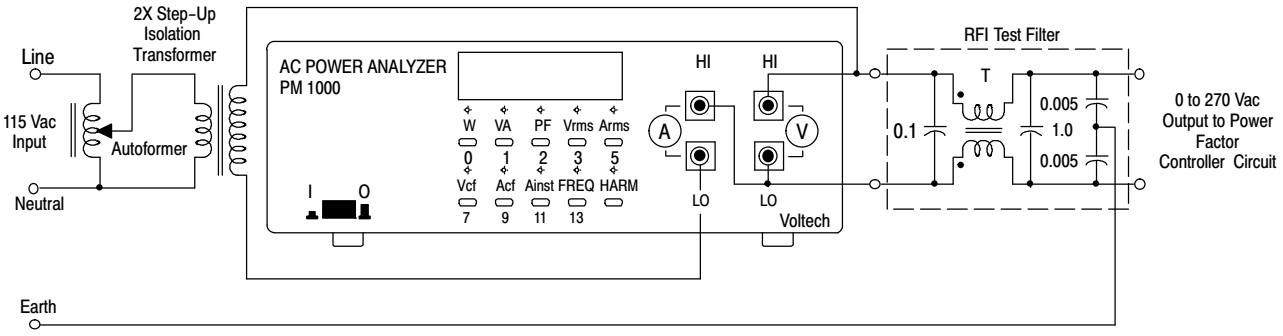


Figure 25. Power Factor Test Set−Up

An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 20 and 21 work well with commercially available two stage filters such as the Delta Electronics 03DPCG5. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common−mode transformer. Coilcraft CMT3−28−2 was used to test Figures 20 and 21. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A. Coilcraft CMT4−17−9was used to test Figure 22. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency η (%) was calculated without the power loss of the RFI filter.

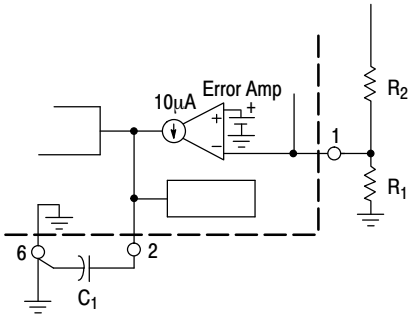


Figure 26. Error Amp Compensation

The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor C_1 must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to Pin 6. When operating at high ac line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, ≈ 2.0 V. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut−off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of C_1.

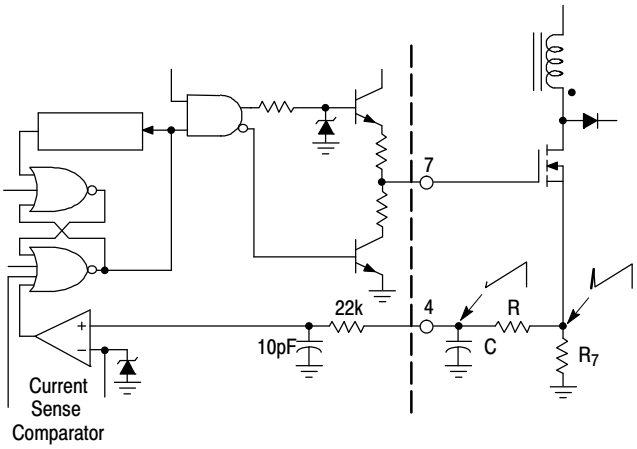


Figure 27. Current Waveform Spike Suppression

A narrow turn−on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The MC34262 provides an internal RC filter with a time constant of 220 ns. An additional external RC filter may be required in universal input applications that are above 200 W. It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.

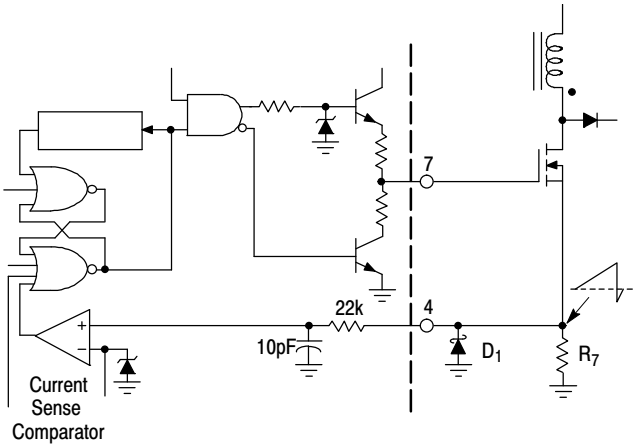
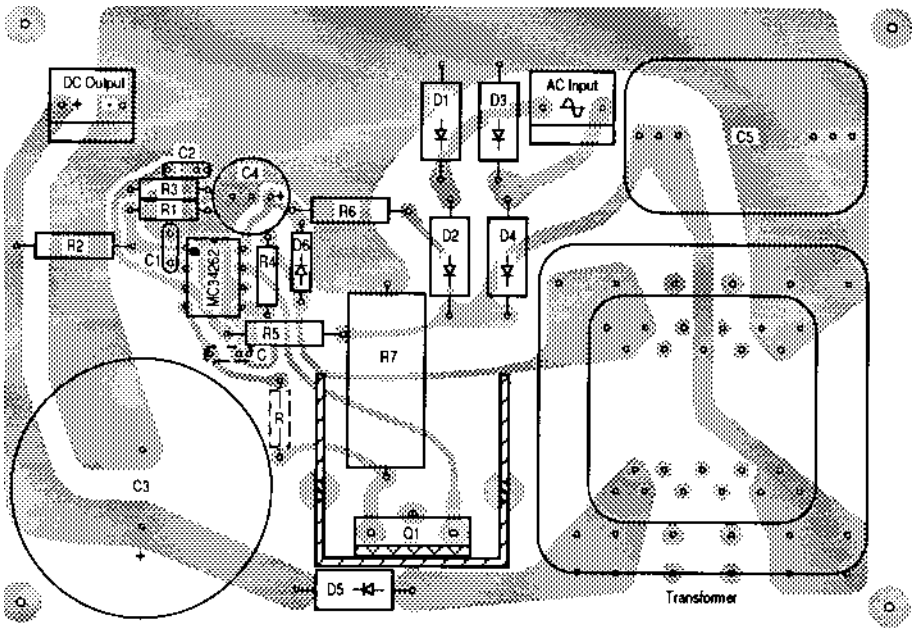
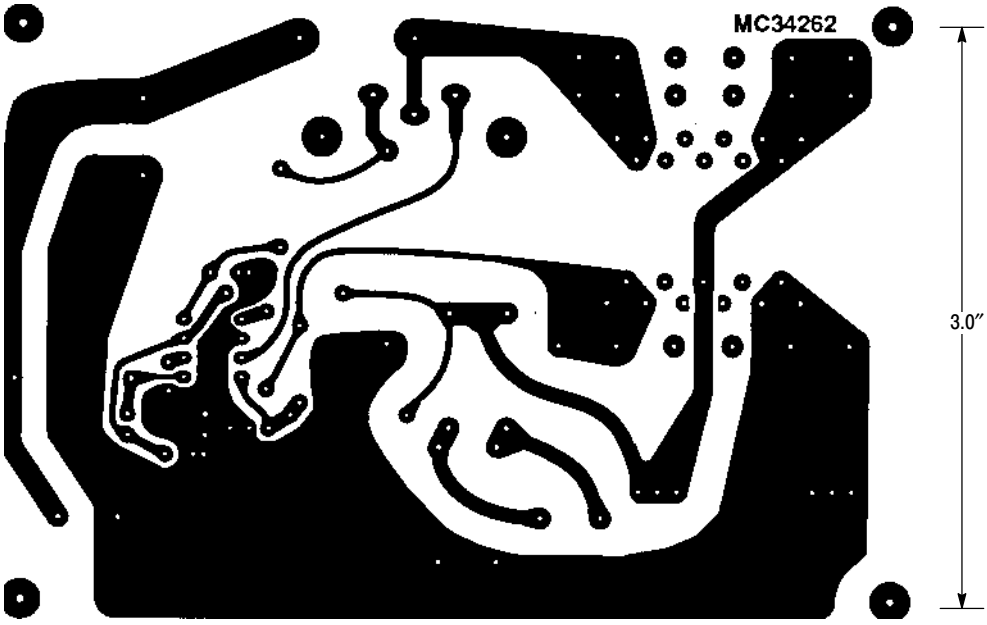


Figure 28. Negative Current Waveform Spike Suppression

A negative turn−off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor R_7, and if it is excessive, it can cause circuit instability. The addition of Schottky diode D_1 can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 27 may provide sufficient spike attenuation.



(Top View)



(Bottom View)

NOTE: Use 2 oz. copper laminate for optimum circuit performance.

Figure 29. Printed Circuit Board and Component Layout (Circuits of Figures 20 and 21)

DEVICE ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
MC34262DG	T_A = 0°C to +85°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC34262DR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC34262PG		PDIP−8 (Pb−Free)	50 Units / Rail
MC33262DG	T_A = −40°C to +105°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC33262DR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC33262PG		PDIP−8 (Pb−Free)	50 Units / Rail
MC33262CDR2G		SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

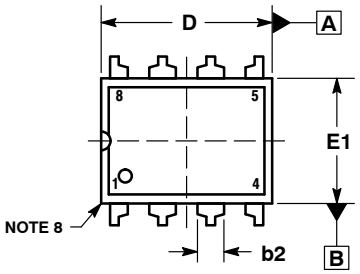
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

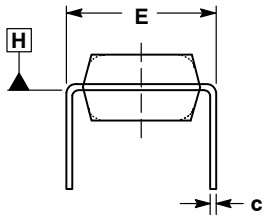
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

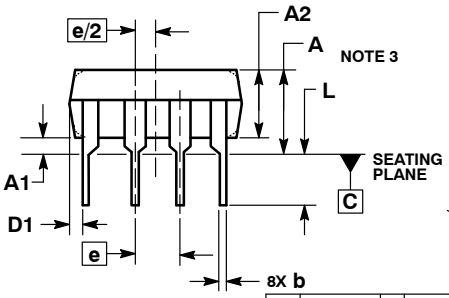
DATE 22 APR 2015



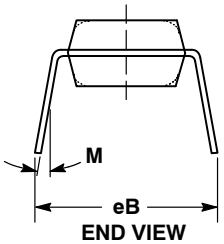
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



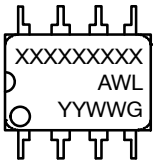
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

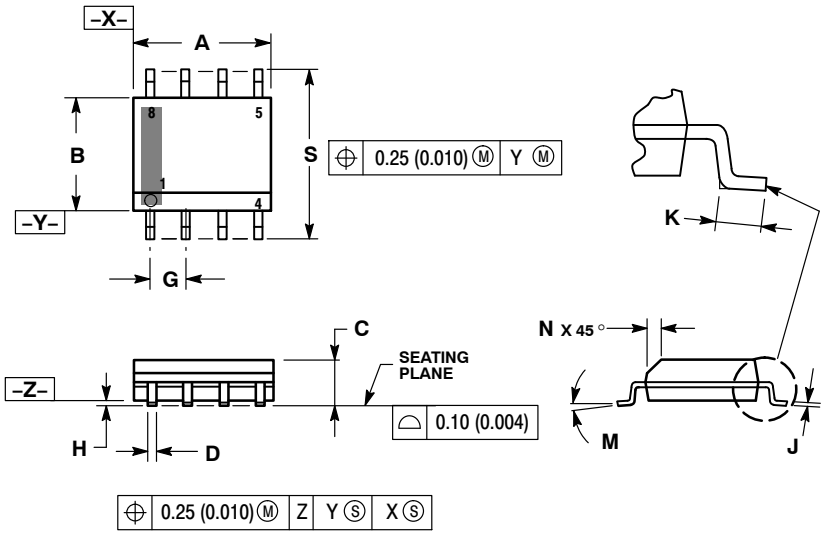
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

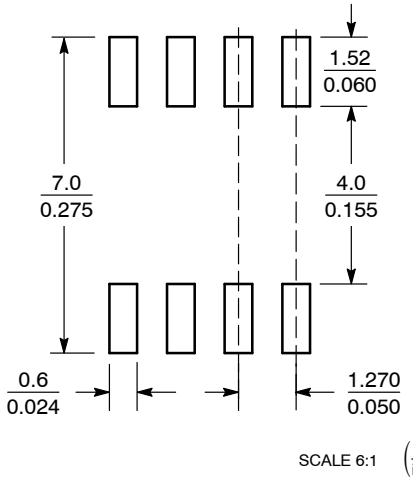
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

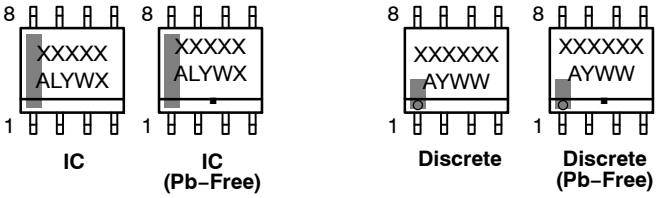
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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