

MC33272A, MC33274A, NCV33272A, NCV33274A



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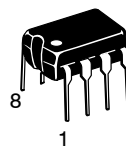
Operational Amplifiers, Single Supply, High Slew Rate, Low Input Offset Voltage

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

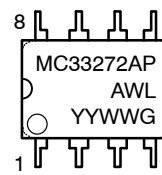
Features

- Input Offset Voltage Trimmed to 100 μ V (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 M Ω
- Low Noise: 18 nV/ $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/ μ s
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ -14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or \pm 1.5 V to \pm 18 V
- ESD Diodes Provide Added Protection to the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- Pb-Free Packages are Available

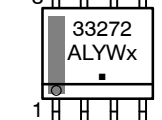
DUAL MARKING DIAGRAMS



PDIP-8
P SUFFIX
CASE 626

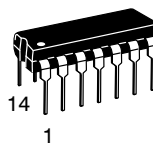


SOIC-8
D SUFFIX
CASE 751

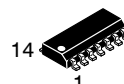
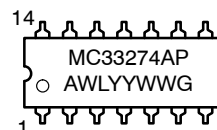


x = A for MC33272AD/DR2
= N for NCV33272ADR2

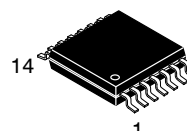
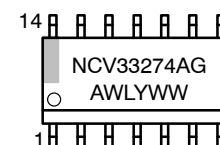
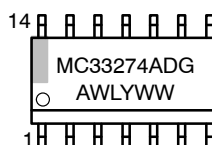
QUAD



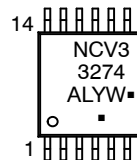
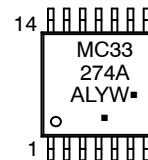
PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DTB SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

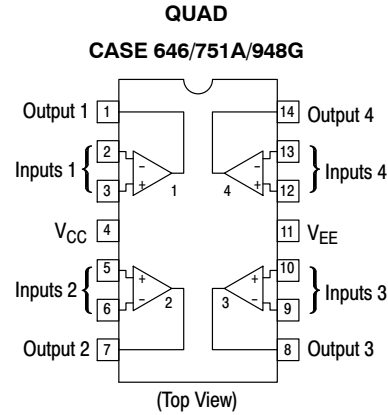
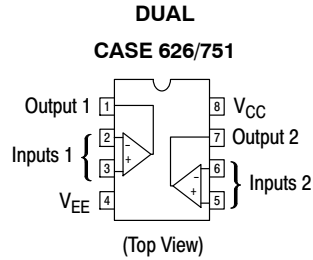
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

MC33272A, MC33274A, NCV33272A, NCV33274A

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC} to V _{EE}	+36	V
Input Differential Voltage Range	V _{IDR}	Note 1	V
Input Voltage Range	V _{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t _{SC}	Indefinite	sec
Maximum Junction Temperature	T _J	+150	°C
Storage Temperature	T _{stg}	-60 to +150	°C
ESD Protection at Any Pin	V _{esd}	2000 200	V
	- Human Body Model - Machine Model		
Maximum Power Dissipation	P _D	Note 2	mW
Operating Temperature Range	T _A	-40 to +85 -40 to +125	°C
	MC33272A, MC33274A NCV33272A, NCV33274A		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

MC33272A, MC33274A, NCV33272A, NCV33274A

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to } +85^\circ\text{C}$ $T_A = -40^\circ\text{ to } +125^\circ\text{C}$ (NCV33272A) $T_A = -40^\circ\text{ to } +125^\circ\text{C}$ (NCV33274A) ($V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$) $T_A = +25^\circ\text{C}$	3	$ V_{IO} $	-	0.1	1.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = -40^\circ\text{ to } +125^\circ\text{C}$	3	$\Delta V_{IO}/\Delta T$	-	2.0	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}\text{ to } T_{high}$	4, 5	I_{IB}	-	300	650	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}\text{ to } T_{high}$		$ I_{IO} $	-	3.0	65	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$	6	V_{ICR}	$V_{EE}\text{ to } (V_{CC} - 1.8)$			V
Large Signal Voltage Gain ($V_O = 0\text{ V to } 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}\text{ to } T_{high}$	7	A_{VOL}	90 86	100 -	- -	dB
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ ($V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$) $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$	8, 9, 12 10, 11	V_{O+} V_{O-} V_{O+} V_{O-} V_{OL} V_{OH}	13.4 - 13.4 - - 3.7	13.9 -13.9 14 -14.7 - -	- -13.5 - -14.1 0.2 5.0	V
Common Mode Rejection ($V_{in} = +13.2\text{ V to } -15\text{ V}$)	13	CMR	80	100	-	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15\text{ V}/ -15\text{ V}$, $+5.0\text{ V}/ -15\text{ V}$, $+15\text{ V}/ -5.0\text{ V}$	14, 15	PSR	80	105	-	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground) Source Sink	16	I_{SC}	+25 -25	+37 -37	- -	mA
Power Supply Current Per Amplifier ($V_O = 0\text{ V}$) ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = T_{low}\text{ to } T_{high}$ ($V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$) $T_A = +25^\circ\text{C}$	17	I_{CC}	-	2.15	2.75	mA
			-	-	3.0	
			-	-	2.75	

3. MC33272A, MC33274A $T_{low} = -40^\circ\text{C}$ $T_{high} = +85^\circ\text{C}$
 NCV33272A, NCV33274A $T_{low} = -40^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$

MC33272A, MC33274A, NCV33272A, NCV33274A

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0\text{ V}$)	18, 33	SR	8.0	10	-	$\text{V}/\mu\text{s}$
Gain Bandwidth Product ($f = 100\text{ kHz}$)	19	GBW	17	24	-	MHz
AC Voltage Gain ($R_L = 2.0\text{ k}\Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	20, 21, 22	A_{VO}	-	65	-	dB
Unity Gain Bandwidth (Open Loop)		BW	-	5.5	-	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	23, 24, 26	A_m	-	12	-	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$, $C_L = 0\text{ pF}$)	23, 25, 26	ϕ_m	-	55	-	Deg
Channel Separation ($f = 20\text{ Hz}$ to 20 kHz)	27	CS	-	-120	-	dB
Power Bandwidth ($V_O = 20\text{ V}_{pp}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)		BW_P	-	160	-	kHz
Total Harmonic Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_O = 3.0\text{ V}_{rms}$, $A_V = +1.0$)	28	THD	-	0.003	-	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 6.0\text{ MHz}$)	29	$ Z_O $	-	35	-	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)		R_{in}	-	16	-	$\text{M}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)		C_{in}	-	3.0	-	pF
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$)	30	e_n	-	18	-	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	31	i_n	-	0.5	-	$\text{pA}/\sqrt{\text{Hz}}$

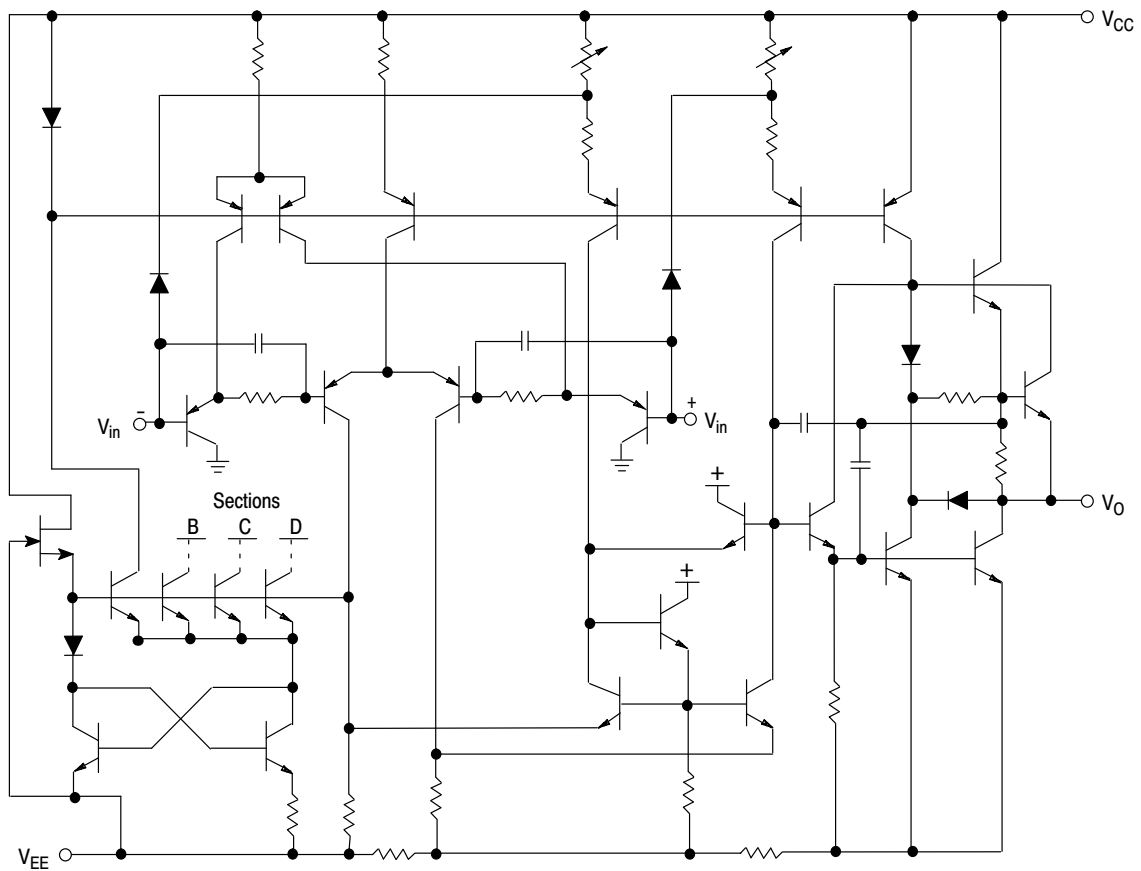


Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

MC33272A, MC33274A, NCV33272A, NCV33274A

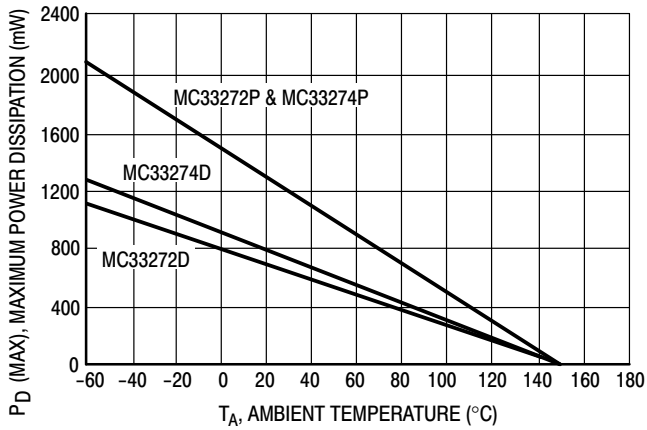


Figure 2. Maximum Power Dissipation versus Temperature



Figure 3. Input Offset Voltage versus Temperature for Typical Units

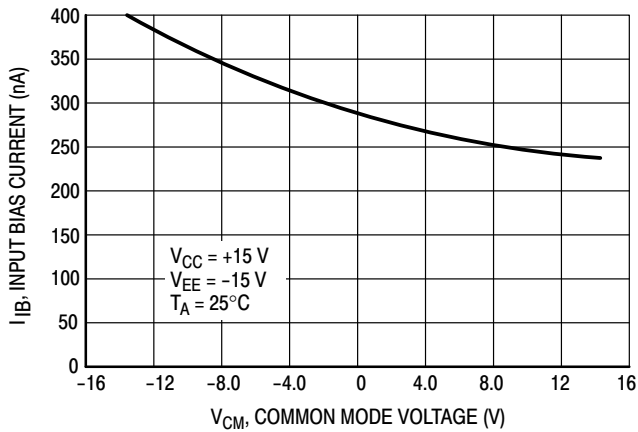


Figure 4. Input Bias Current versus Common Mode Voltage



Figure 5. Input Bias Current versus Temperature

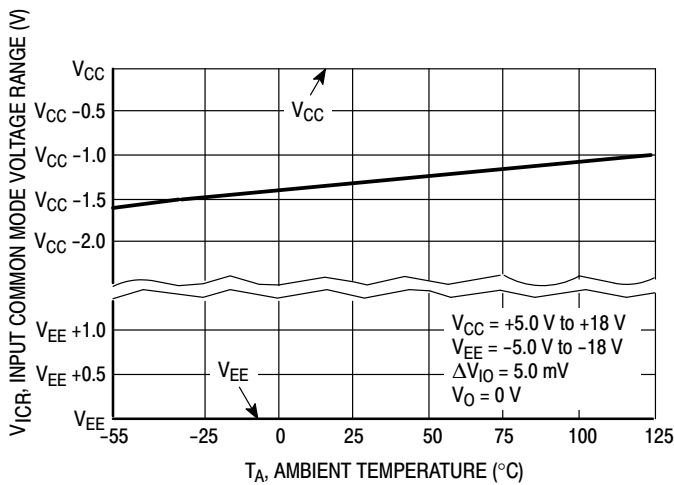


Figure 6. Input Common Mode Voltage Range versus Temperature



Figure 7. Open Loop Voltage Gain versus Temperature

MC33272A, MC33274A, NCV33272A, NCV33274A

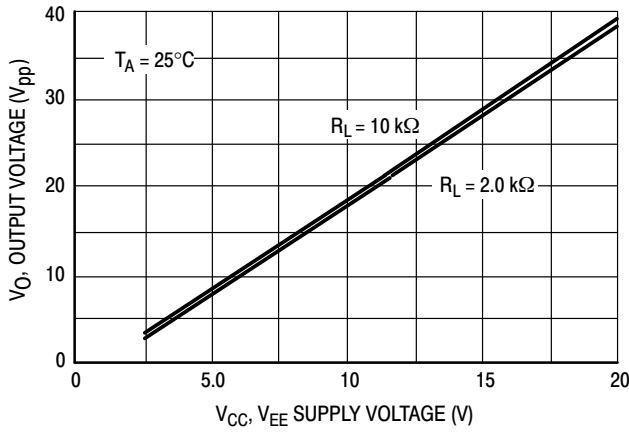


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

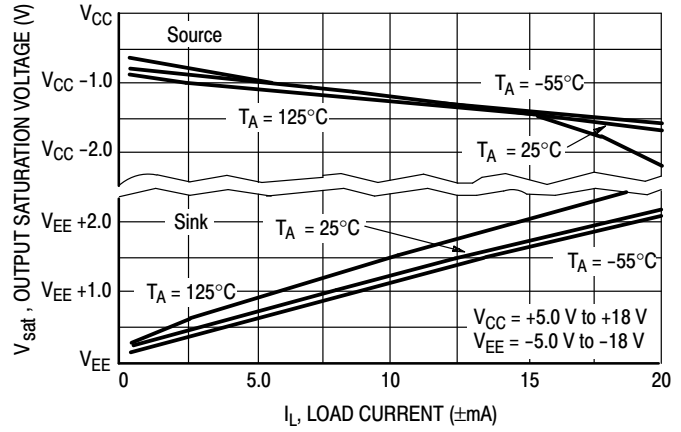


Figure 9. Split Supply Output Saturation Voltage versus Load Current

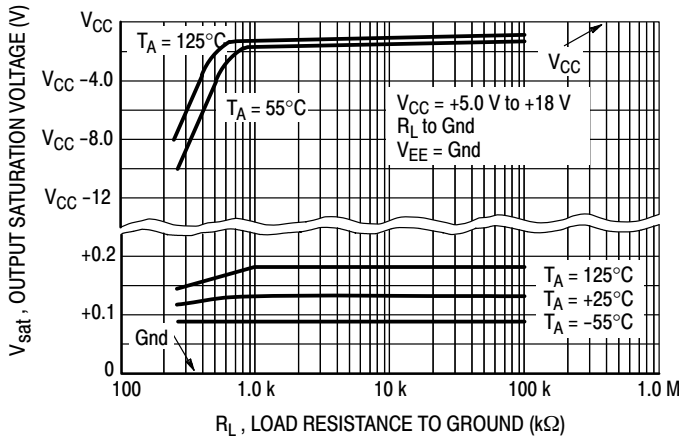


Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground

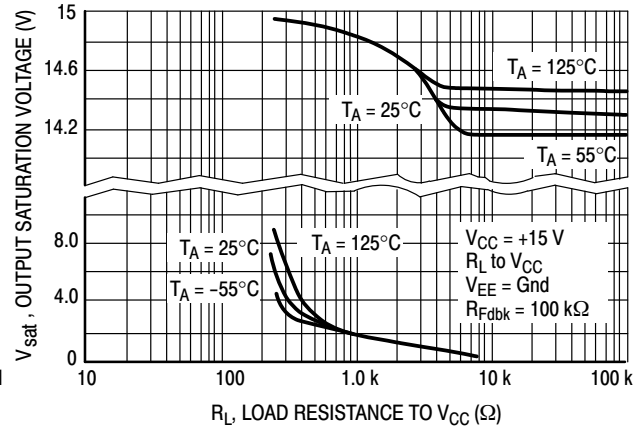


Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to VCC

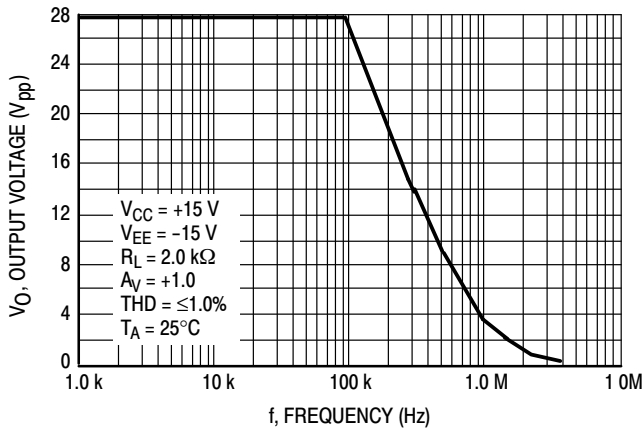


Figure 12. Output Voltage versus Frequency

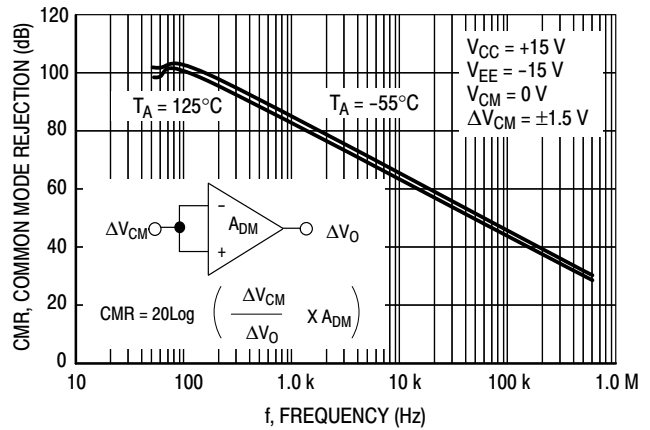


Figure 13. Common Mode Rejection versus Frequency

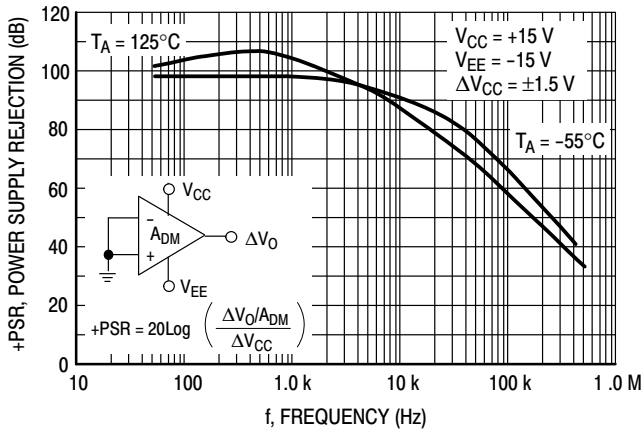


Figure 14. Positive Power Supply Rejection versus Frequency

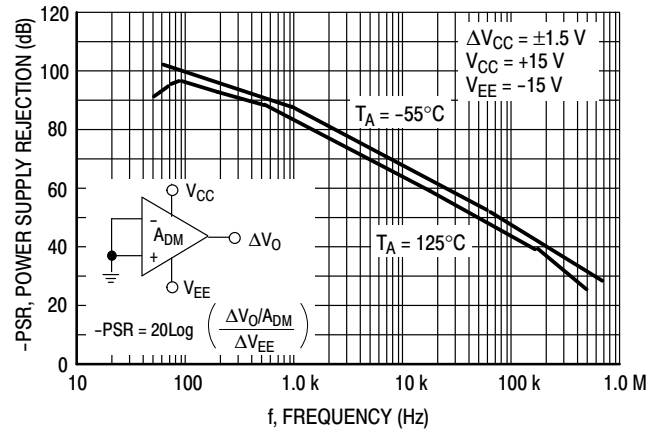


Figure 15. Negative Power Supply Rejection versus Frequency



Figure 16. Output Short Circuit Current versus Temperature



Figure 17. Supply Current versus Supply Voltage

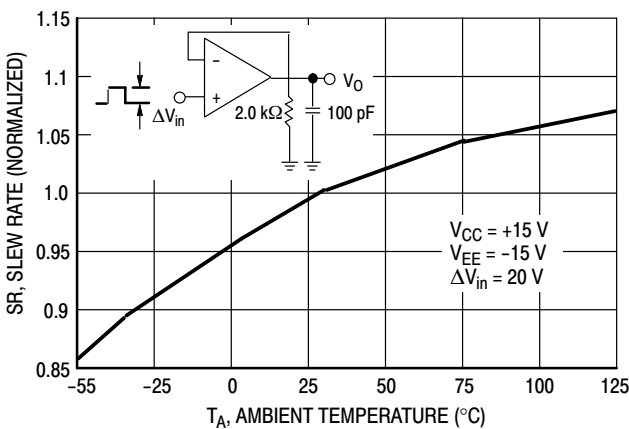


Figure 18. Normalized Slew Rate versus Temperature



Figure 19. Gain Bandwidth Product versus Temperature

MC33272A, MC33274A, NCV33272A, NCV33274A



Figure 20. Voltage Gain and Phase versus Frequency

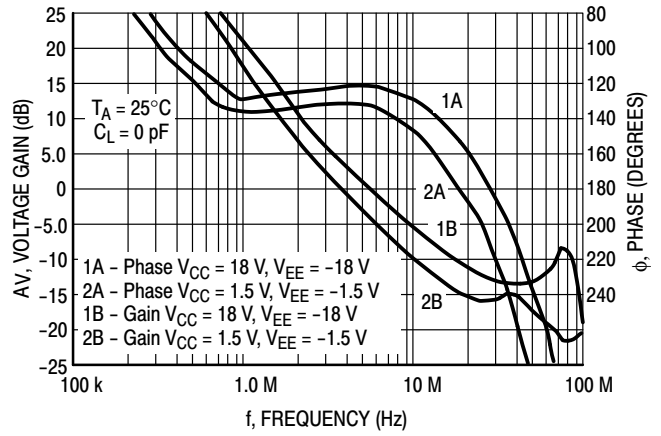


Figure 21. Gain and Phase versus Frequency

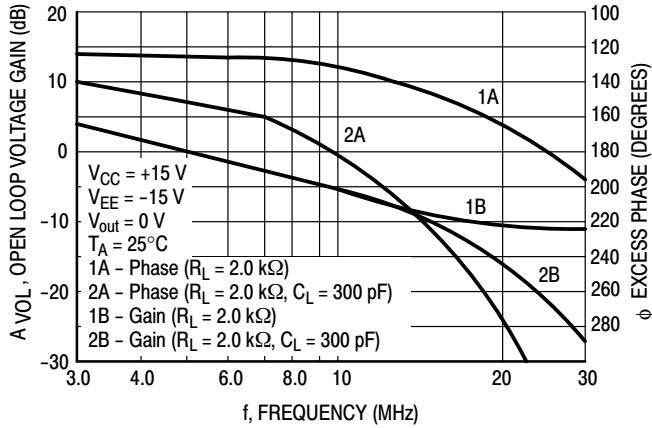


Figure 22. Open Loop Voltage Gain and Phase versus Frequency

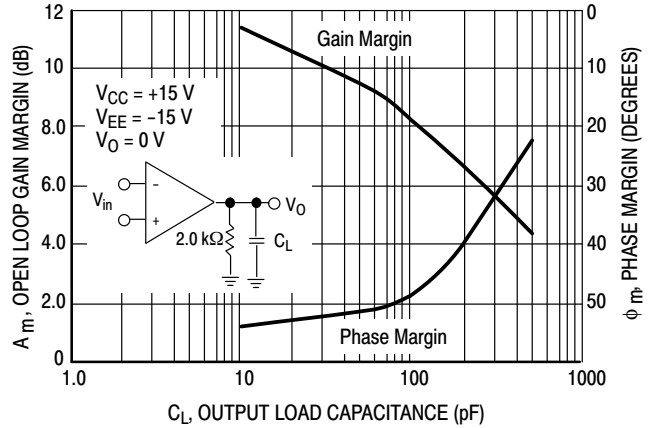


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

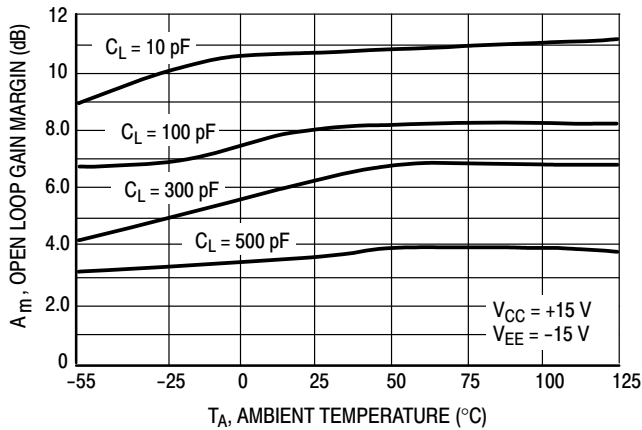


Figure 24. Open Loop Gain Margin versus Temperature

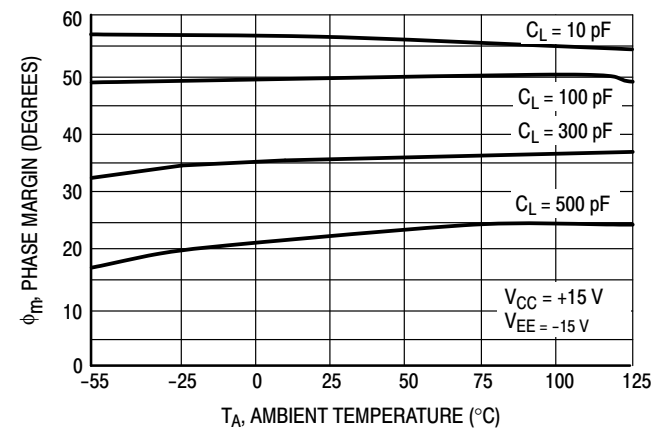


Figure 25. Phase Margin versus Temperature

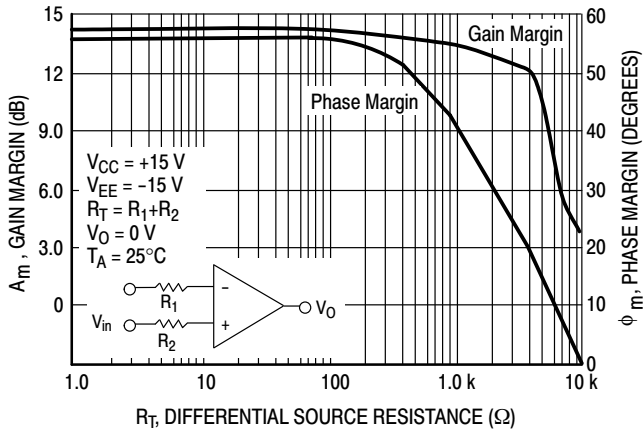


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

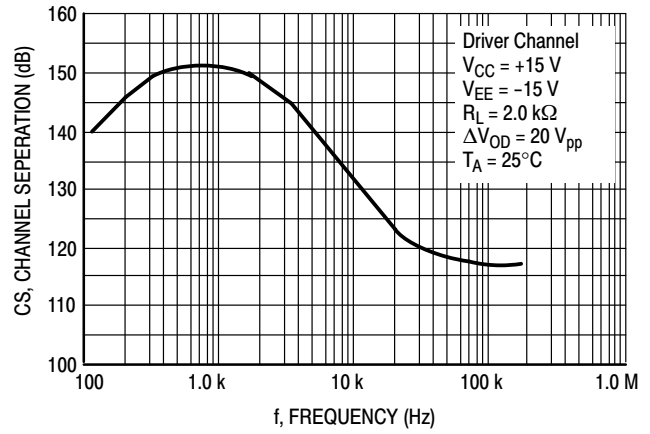


Figure 27. Channel Separation versus Frequency

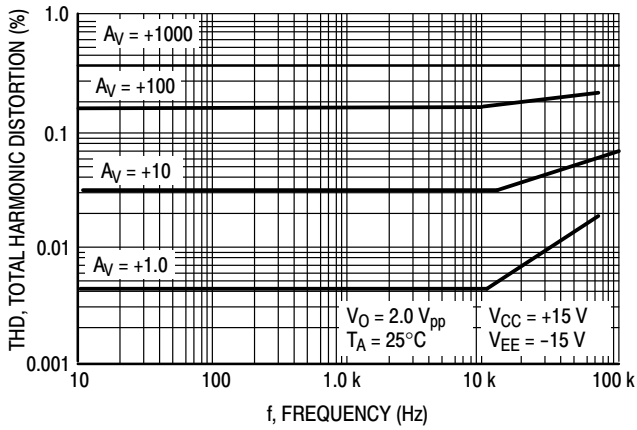


Figure 28. Total Harmonic Distortion versus Frequency

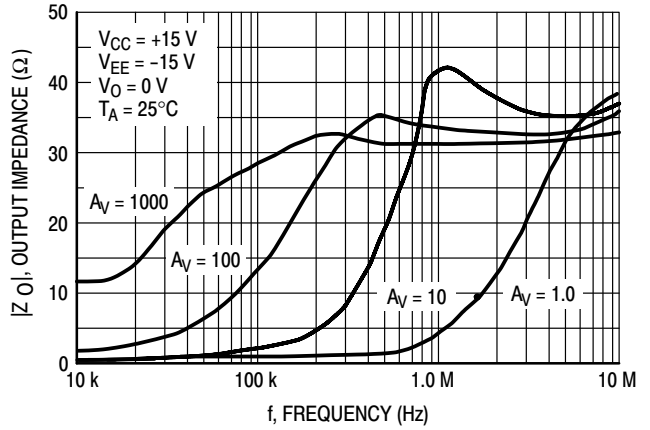


Figure 29. Output Impedance versus Frequency

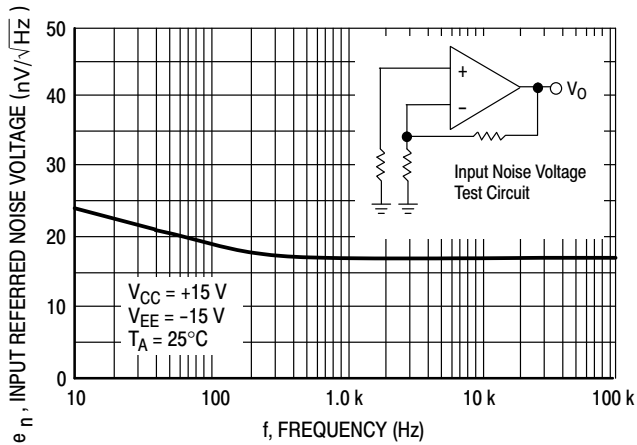


Figure 30. Input Referred Noise Voltage versus Frequency

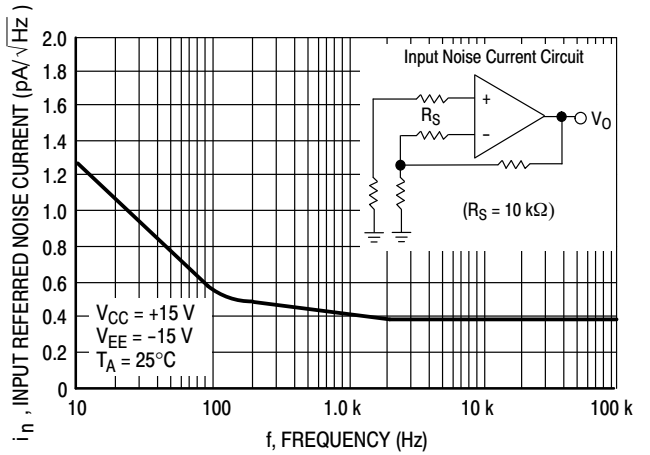


Figure 31. Input Referred Noise Current versus Frequency

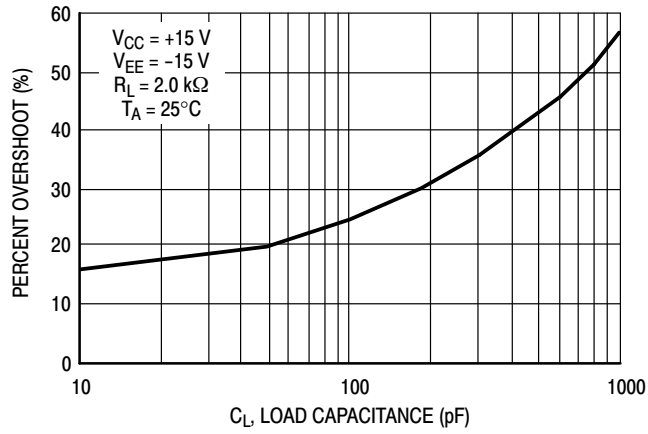


Figure 32. Percent Overshoot versus Load Capacitance

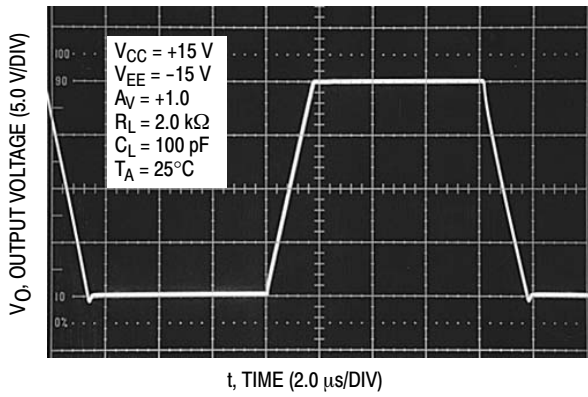


Figure 33. Non-inverting Amplifier Slew Rate for the MC33274

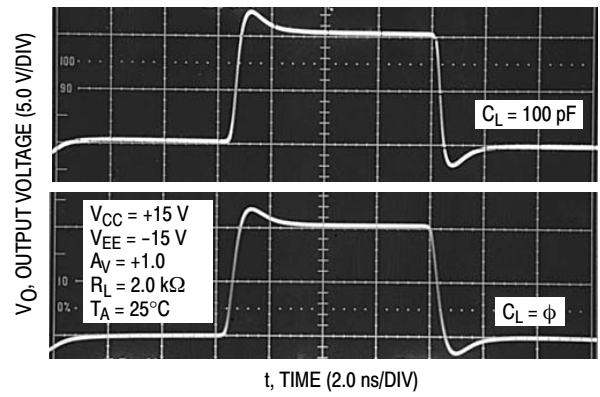


Figure 34. Non-inverting Amplifier Overshoot for the MC33274

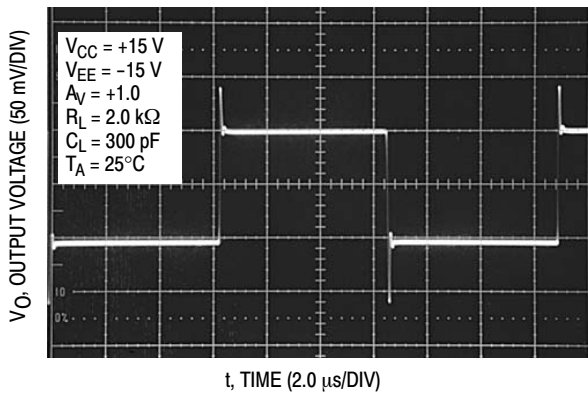


Figure 35. Small Signal Transient Response for MC33274

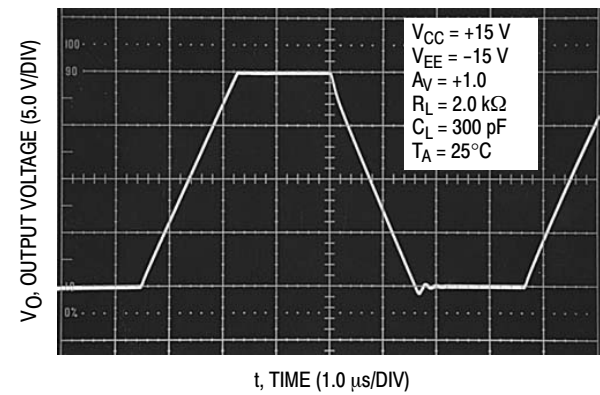


Figure 36. Large Signal Transient Response for MC33274

MC33272A, MC33274A, NCV33272A, NCV33274A

ORDERING INFORMATION

Device	Package	Shipping†
MC33272AD	SOIC-8	98 Units / Rail
MC33272ADG	SOIC-8 (Pb-Free)	
MC33272ADR2	SOIC-8	2500 / Tape & Reel
MC33272ADR2G	SOIC-8 (Pb-Free)	
MC33272AP	PDIP-8	50 Units / Rail
MC33272APG	PDIP-8 (Pb-Free)	
NCV33272ADR2*	SOIC-8	2500 / Tape & Reel
NCV33272ADR2G*	SOIC-8 (Pb-Free)	
MC33274AD	SOIC-14	55 Units / Rail
MC33274ADG	SOIC-14 (Pb-Free)	
MC33274ADR2	SOIC-14	2500 / Tape & Reel
MC33274ADR2G	SOIC-14 (Pb-Free)	
MC33274ADTBR2G	TSSOP-14 (Pb-Free)	
MC33274AP	PDIP-14	25 Units / Rail
MC33274APG	PDIP-14 (Pb-Free)	
NCV33274AD*	SOIC-14	55 Units / Rail
NCV33274ADG*	SOIC-14 (Pb-Free)	
NCV33274ADR2*	SOIC-14	2500 / Tape & Reel
NCV33274ADR2G*	SOIC-14 (Pb-Free)	
NCV33274ADTBR2G*	TSSOP-14 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

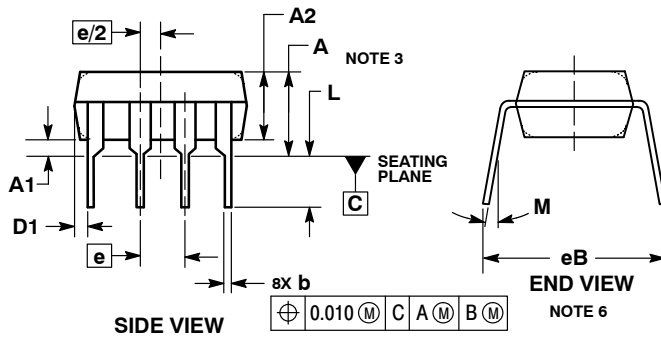
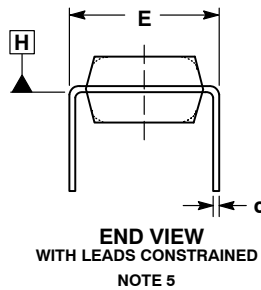
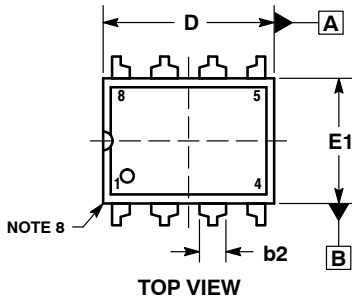
ON Semiconductor®



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

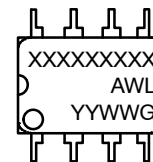


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM*

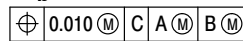


- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

- PIN 1. AC IN
- 2. DC + IN
- 3. DC - IN
- 4. AC IN
- 5. GROUND
- 6. OUTPUT
- 7. AUXILIARY
- 8. V_{CC}



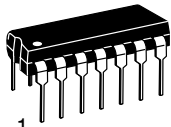
DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP-8	PAGE 1 OF 1

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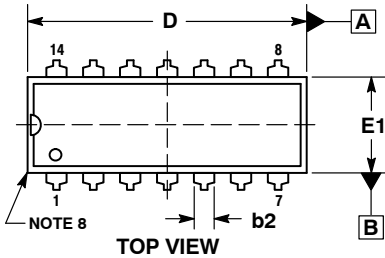
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

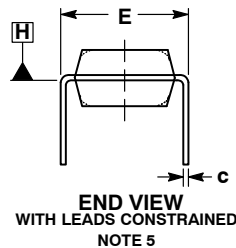


SCALE 1:1



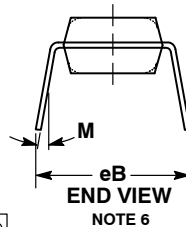
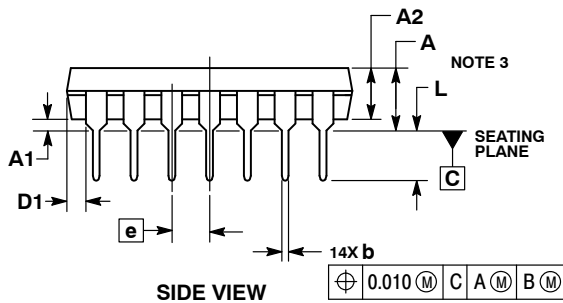
PDIP-14
CASE 646-06
ISSUE S

DATE 22 APR 2015



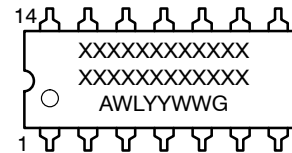
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
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7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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PDIP-14
CASE 646-06
ISSUE S

DATE 22 APR 2015

STYLE 1:
 PIN 1. COLLECTOR
 2. BASE
 3. EMITTER
 4. NO
 CONNECTION
 5. EMITTER
 6. BASE
 7. COLLECTOR
 8. COLLECTOR
 9. BASE
 10. EMITTER
 11. NO
 CONNECTION
 12. EMITTER
 13. BASE
 14. COLLECTOR

STYLE 2:
 CANCELLED

STYLE 3:
 CANCELLED

STYLE 4:
 PIN 1. DRAIN
 2. SOURCE
 3. GATE
 4. NO
 CONNECTION
 5. GATE
 6. SOURCE
 7. DRAIN
 8. DRAIN
 9. SOURCE
 10. GATE
 11. NO
 CONNECTION
 12. GATE
 13. SOURCE
 14. DRAIN

STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. NO CONNECTION
 5. SOURCE
 6. DRAIN
 7. GATE
 8. GATE
 9. DRAIN
 10. SOURCE
 11. NO CONNECTION
 12. SOURCE
 13. DRAIN
 14. GATE

STYLE 6:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 7:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON
 CATHODE

STYLE 8:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE


STYLE 9:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

STYLE 10:
 PIN 1. COMMON
 CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON
 CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 11:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 12:
 PIN 1. COMMON CATHODE
 2. COMMON ANODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. COMMON ANODE
 7. COMMON CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

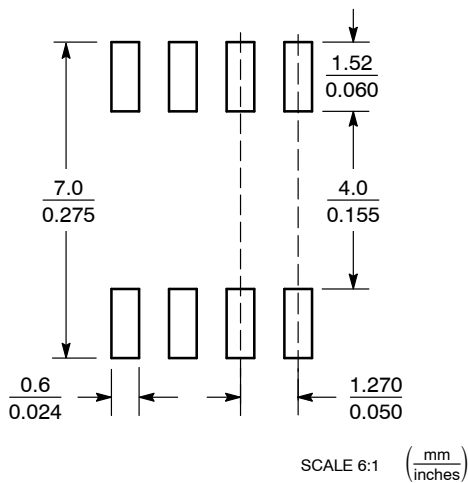


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

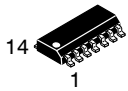
- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

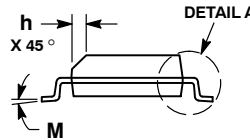
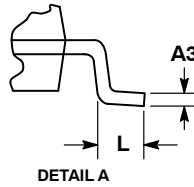
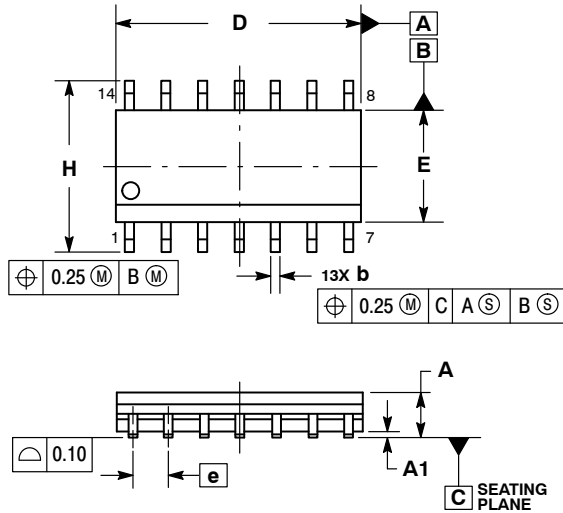
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SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

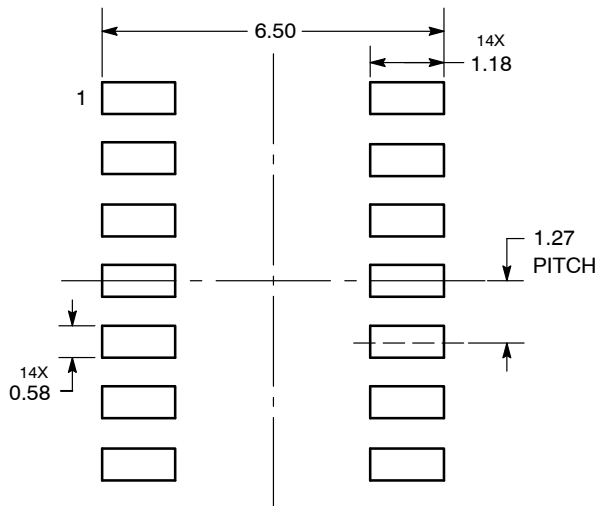


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

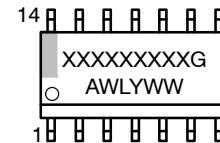
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE


STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

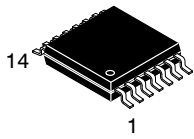
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

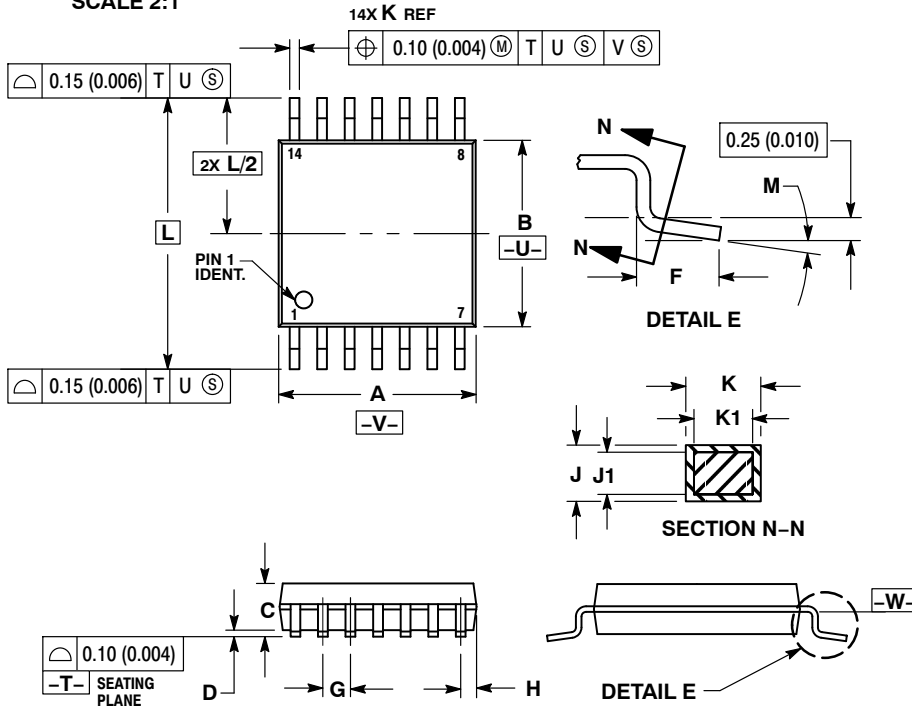
ON Semiconductor®



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

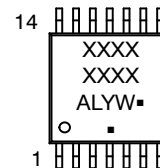


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

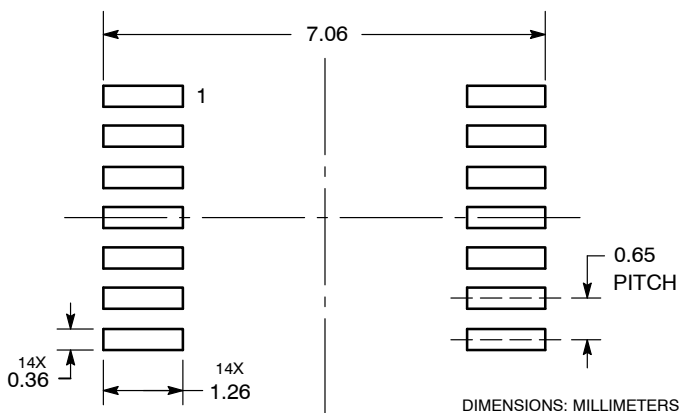


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT



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