



FS6500, FS4500: ASIL B

Safety power system basis chip with CAN FD and LIN transceivers

Rev. 3 — 14 April 2021

Product short data sheet

1 General description

The FS6500/FS4500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) and/or LIN transceivers, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32 μ A) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS6500/FS4500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL B).

The built-in CAN FD interface fulfills the ISO 11898-2⁽¹²⁾ and -5⁽¹³⁾ standards. The LIN interface fulfills LIN protocol specifications 2.0, 2.1⁽²²⁾, 2.2⁽²³⁾, and SAE J2602-2⁽²⁴⁾.

High temperature capability up to $T_A = 125\text{ }^\circ\text{C}$ and $T_J = 150\text{ }^\circ\text{C}$, compliant with AEC-Q100 Grade 1 automotive qualification.

2 Features and benefits

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V, or 3.3 V
- Linear voltage regulator dedicated to MCU Analog/Digital (A/D) reference voltage or I/Os supply (V_{CCA}), 5.0 V, or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT
- Five configurable I/Os

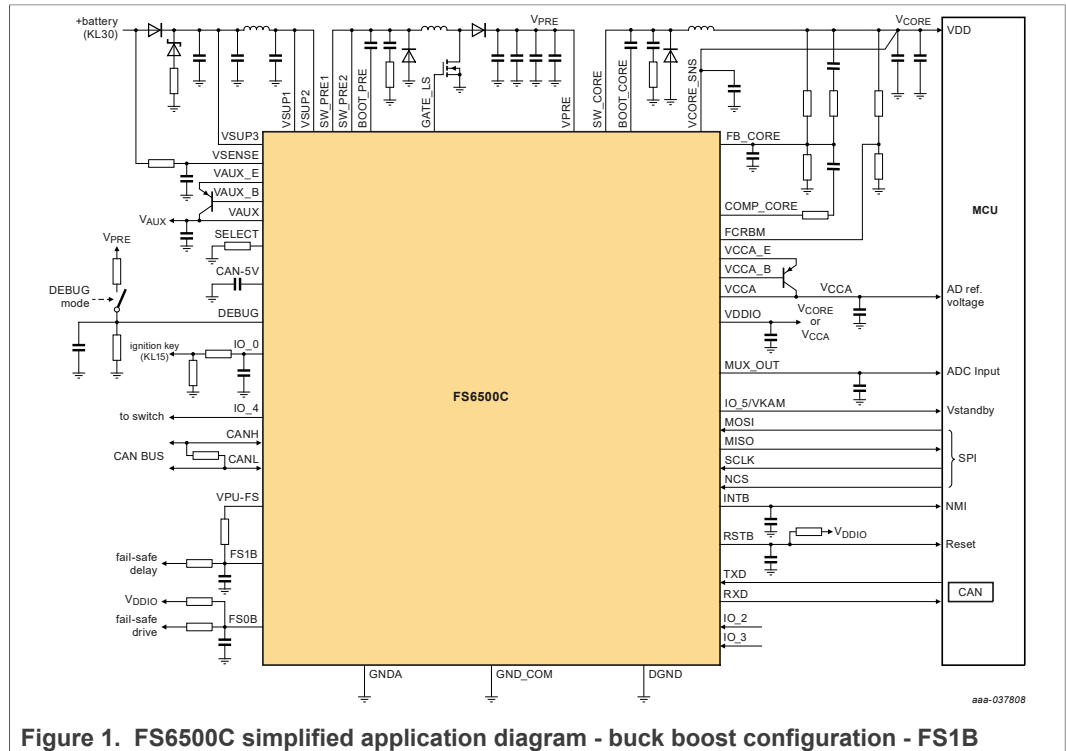
3 Applications

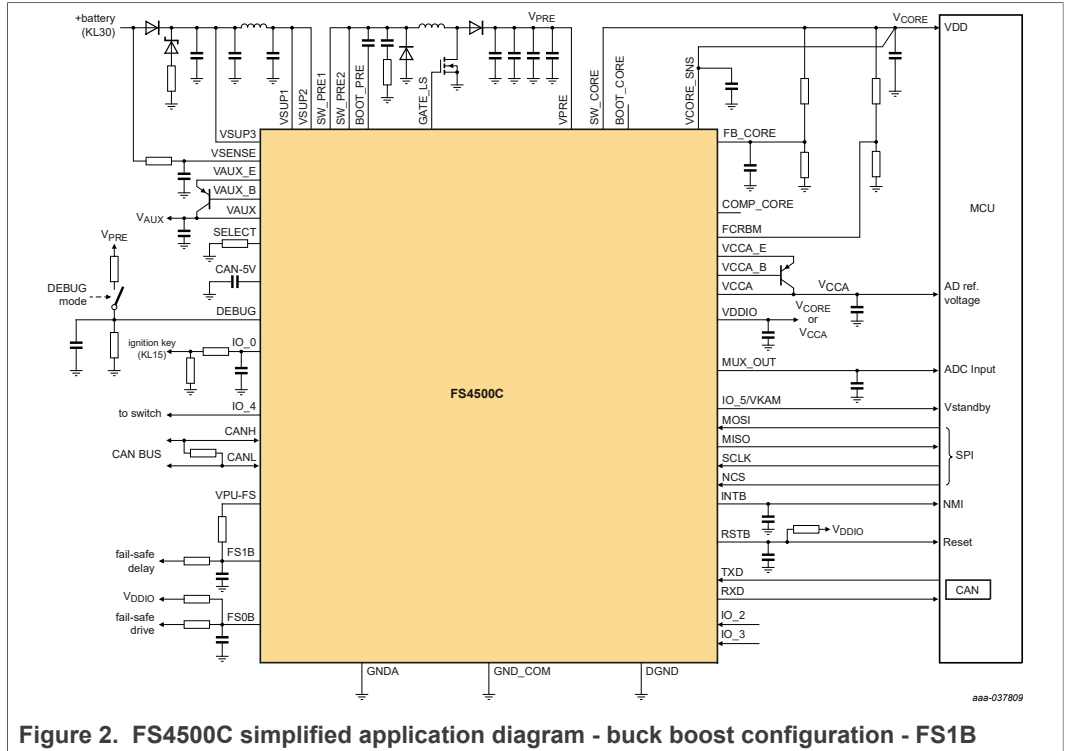
- Drive Train Electrification (BMS, Hybrid EV and HEV, Inverter, DC-DC, Alternator Starter)
- Drive Train - Chassis and Safety (Active Suspension, Steering, Safety Domain Gateway)
- Power Train (EMS, TCU, Gear Box)
- ADAS (LDW, Radar, Sensor Fusion Safety area)



- On board charger
- Motor control

4 Simplified application diagrams





5 Ordering information

5.1 Part number definition

MC33FS c 5 x y z AE/R2

Table 1. Part number breakdown

| Code | Option | Variable | Description |
|------|----------|---------------------------|----------------|
| c | 4 series | V _{CORE} type | Linear |
| | 6 series | | DC-DC |
| x | 0 | V _{CORE} current | 0.5 A or 0.8 A |
| | 1 | | 1.5 A |
| | 2 | | 2.2 A |
| y | 5 | Functions | None |
| | 6 | | FS1B |
| | 7 | | LDT |
| | 8 | | FS1B and LDT |
| z | N | Physical interface | None |
| | C | | CAN FD |
| | K | | LIN only |
| | L | | CAN FD and LIN |

5.2 Part numbers list

Table 2. Orderable part variations

| Part Number | Temperature (T _A) | Package | FS1B | LDT | VCORE | VCORE type | VKAM On | CAN FD | LIN | ASIL | Notes |
|---------------|-------------------------------|-------------------------|-------|-------|--------|------------|---------|--------|-----|------|-------|
| MC33FS4505NAE | -40 °C to 125 °C | 48-pin LQFP exposed pad | 0 | 0 | 0.5 A | Linear | by SPI | 0 | 0 | B | [1] |
| MC33FS4505CAE | | | 0 | 0 | 0.5 A | Linear | by SPI | 1 | 0 | B | |
| MC33FS4505KAE | | | 0 | 0 | 0.5 A | Linear | By SPI | 0 | 1 | B | |
| MC33FS4505LAE | | | 0 | 0 | 0.5 A | Linear | By SPI | 1 | 1 | B | |
| MC33FS4506NAE | | | 1 | 0 | 0.5 A | Linear | by SPI | 0 | 0 | B | |
| MC33FS4506CAE | | | 1 | 0 | 0.5 A | Linear | by SPI | 1 | 0 | B | |
| MC33FS4507NAE | | | 0 | 1 | 0.5 A | Linear | by SPI | 0 | 0 | B | |
| MC33FS4507CAE | | | 0 | 1 | 0.5 A | Linear | by SPI | 1 | 0 | B | |
| MC33FS4507KAE | | | 0 | 1 | 0.5 A | Linear | by SPI | 0 | 1 | B | |
| MC33FS4507LAE | | | 0 | 1 | 0.5 A | Linear | by SPI | 1 | 1 | B | |
| MC33FS4508NAE | | | 1 | 1 | 0.5 A | Linear | by SPI | 0 | 0 | B | |
| MC33FS4508CAE | | | 1 | 1 | 0.5 A | Linear | by SPI | 1 | 0 | B | |
| MC33FS6505NAE | | | 0 | 0 | 0.8 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6505CAE | | | 0 | 0 | 0.8 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6505KAE | | | 0 | 0 | 0.8 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6505LAE | | | 0 | 0 | 0.8 A | DC-DC | by SPI | 1 | 1 | B | |
| MC33FS6506NAE | | | 1 | 0 | 0.8 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6506CAE | | | 1 | 0 | 0.8 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6507NAE | | | 0 | 1 | 0.8 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6507CAE | | | 0 | 1 | 0.8 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6507KAE | | | 0 | 1 | 0.8 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6507LAE | | | 0 | 1 | 0.8 A | DC-DC | by SPI | 1 | 1 | B | |
| MC33FS6508NAE | | | 1 | 1 | 0.8 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6508CAE | | | 1 | 1 | 0.8 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6515NAE | | | 0 | 0 | 1.5 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6515CAE | | | 0 | 0 | 1.5 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6515KAE | | | 0 | 0 | 1.5 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6515LAE | | | 0 | 0 | 1.5 A | DC-DC | by SPI | 1 | 1 | B | |
| MC33FS6516NAE | | | 1 | 0 | 1.5 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6516CAE | | | 1 | 0 | 1.5 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6517NAE | | | 0 | 1 | 1.5 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6517CAE | | | 0 | 1 | 1.5 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6517KAE | | | 0 | 1 | 1.5 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6517LAE | 0 | 1 | 1.5 A | DC-DC | by SPI | 1 | 1 | B | | | |
| MC33FS6518NAE | 1 | 1 | 1.5 A | DC-DC | by SPI | 0 | 0 | B | | | |
| MC33FS6518CAE | 1 | 1 | 1.5 A | DC-DC | by SPI | 1 | 0 | B | | | |
| MC33FS6525NAE | 0 | 0 | 2.2 A | DC-DC | by SPI | 0 | 0 | B | | | |
| MC33FS6525CAE | 0 | 0 | 2.2 A | DC-DC | by SPI | 1 | 0 | B | | | |

Table 2. Orderable part variations...continued

| Part Number | Temperature (T _A) | Package | FS1B | LDT | VCORE | VCORE type | VKAM On | CAN FD | LIN | ASIL | Notes |
|---------------|-------------------------------|---------|------|-----|-------|------------|---------|--------|-----|------|-------|
| MC33FS6525KAE | | | 0 | 0 | 2.2 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6525LAE | | | 0 | 0 | 2.2 A | DC-DC | by SPI | 1 | 1 | B | |
| MC33FS6526NAE | | | 1 | 0 | 2.2 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6526CAE | | | 1 | 0 | 2.2 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6527NAE | | | 0 | 1 | 2.2 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6527CAE | | | 0 | 1 | 2.2 A | DC-DC | by SPI | 1 | 0 | B | |
| MC33FS6527KAE | | | 0 | 1 | 2.2 A | DC-DC | by SPI | 0 | 1 | B | |
| MC33FS6527LAE | | | 0 | 1 | 2.2 A | DC-DC | by SPI | 1 | 1 | B | |
| MC33FS6528NAE | | | 1 | 1 | 2.2 A | DC-DC | by SPI | 0 | 0 | B | |
| MC33FS6528CAE | | | 1 | 1 | 2.2 A | DC-DC | by SPI | 1 | 0 | B | |

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Block diagram

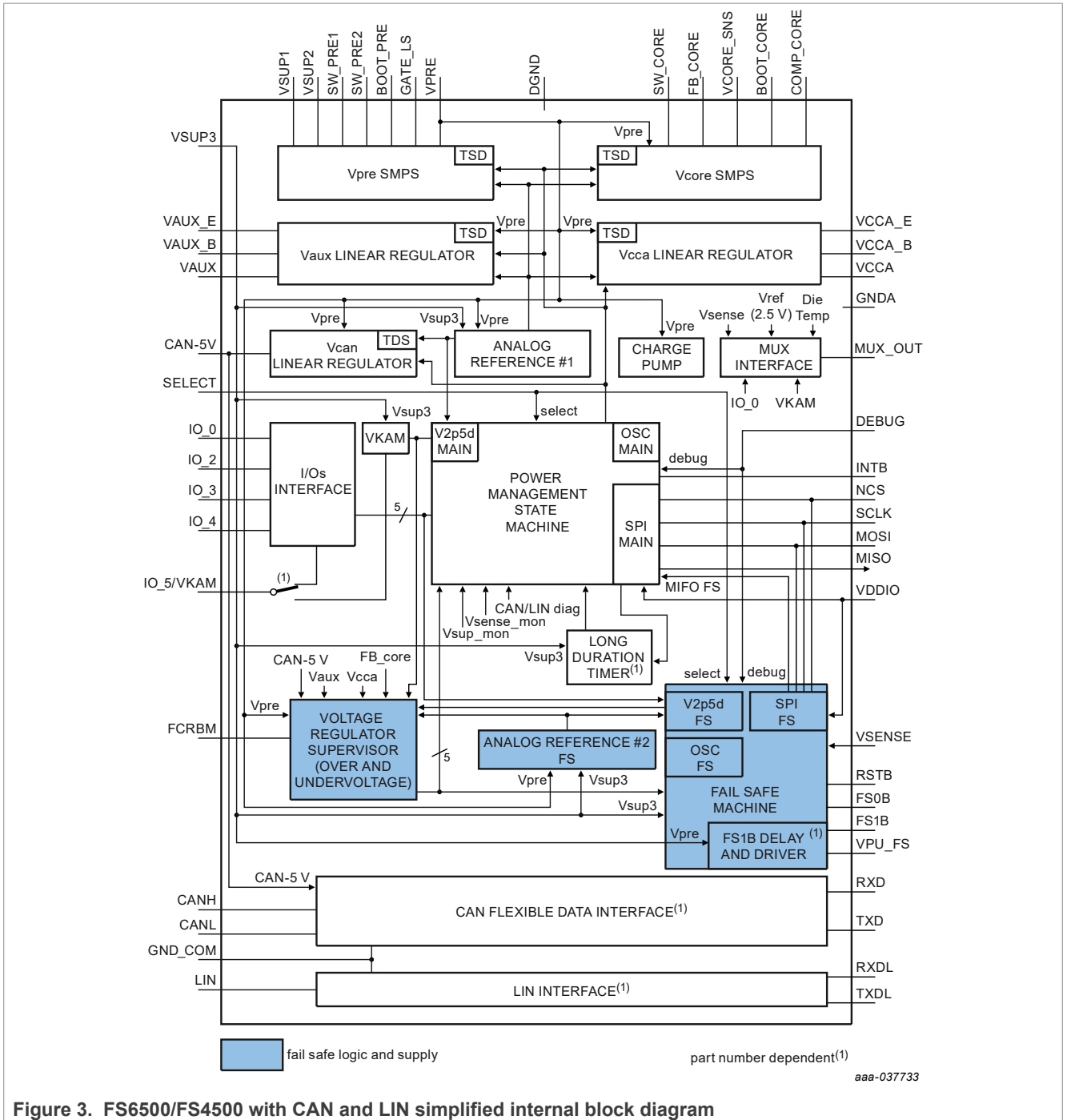
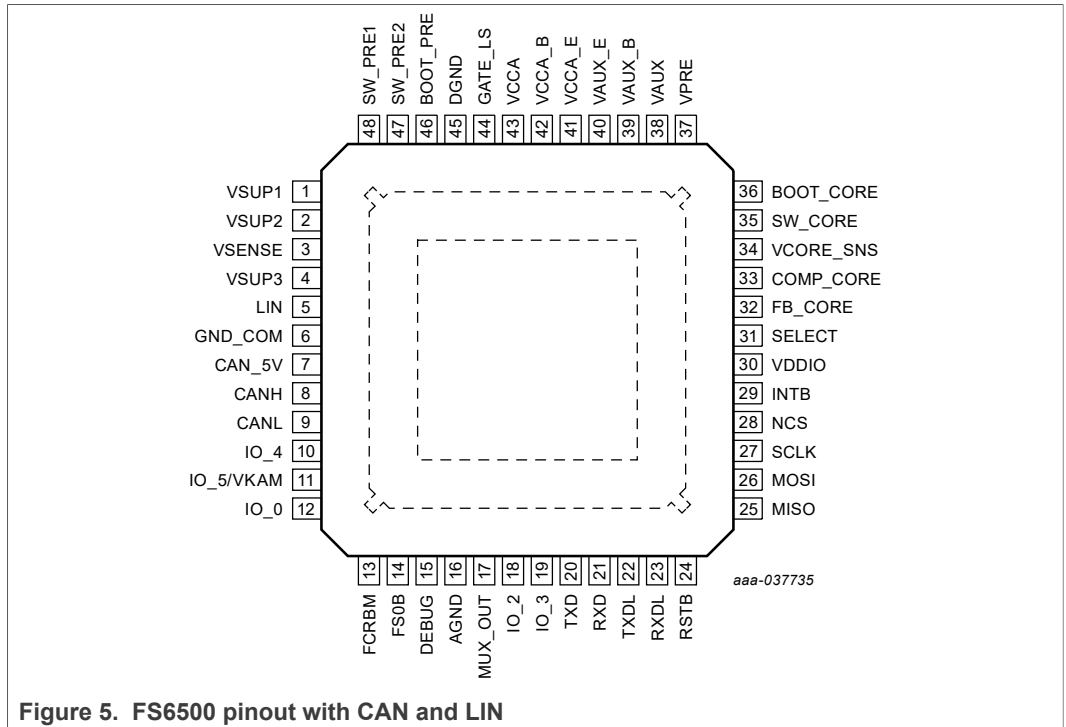
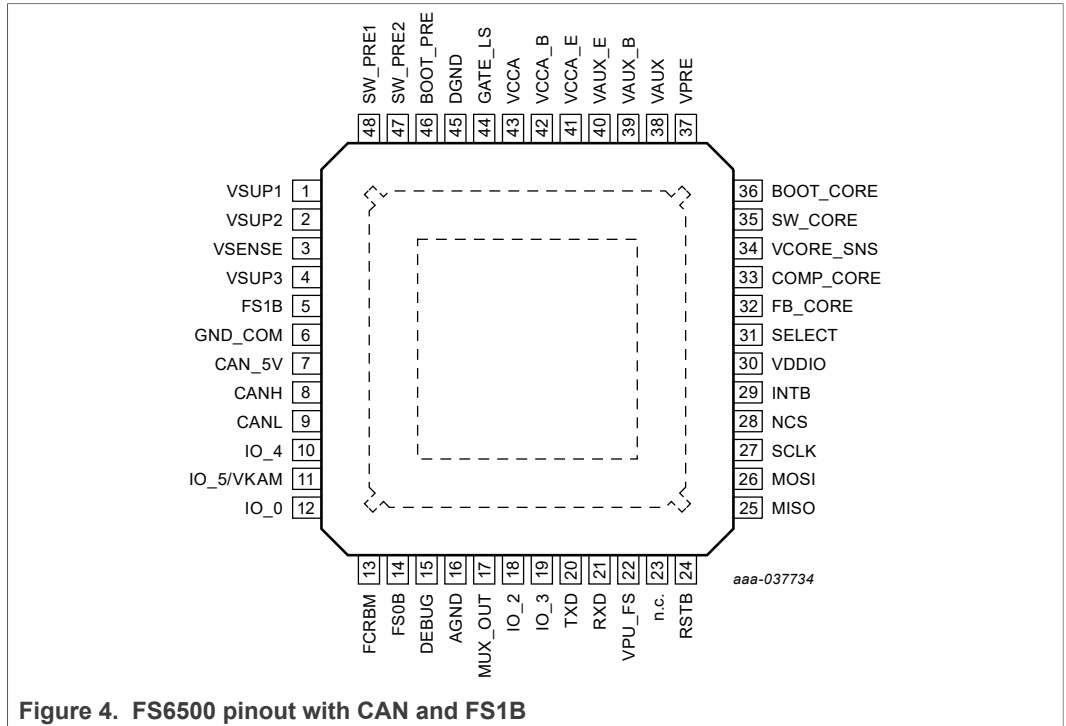


Figure 3. FS6500/FS4500 with CAN and LIN simplified internal block diagram

7 Pinning information

7.1 Pinning information



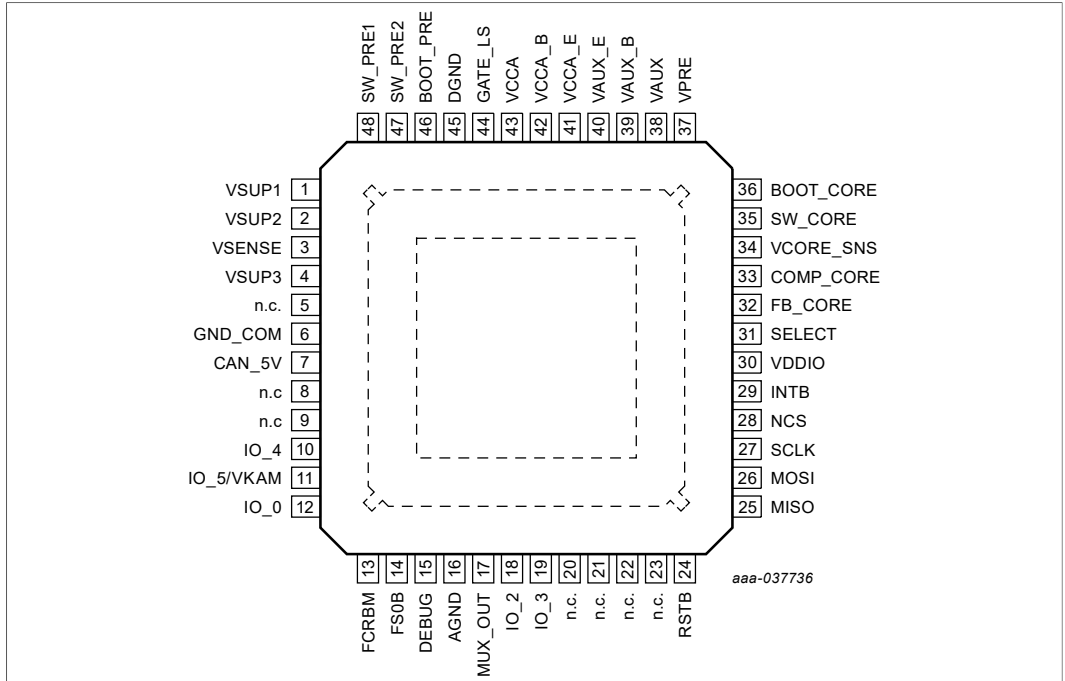


Figure 6. FS6500 pinout without CAN, without LIN

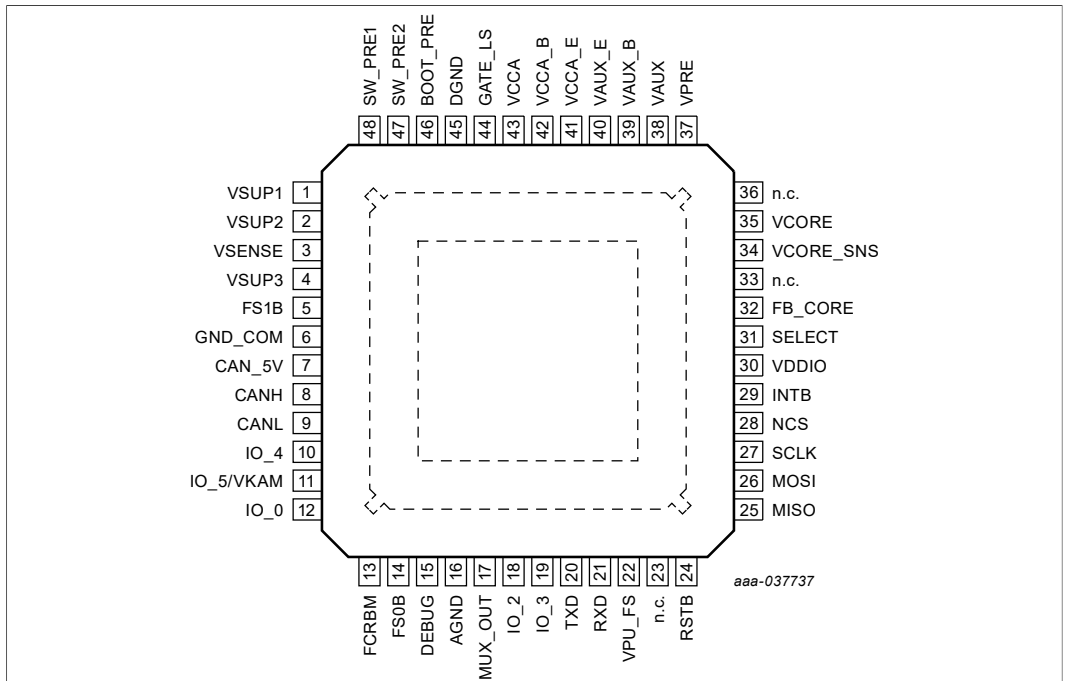


Figure 7. FS4500 pinout with CAN and FS1B

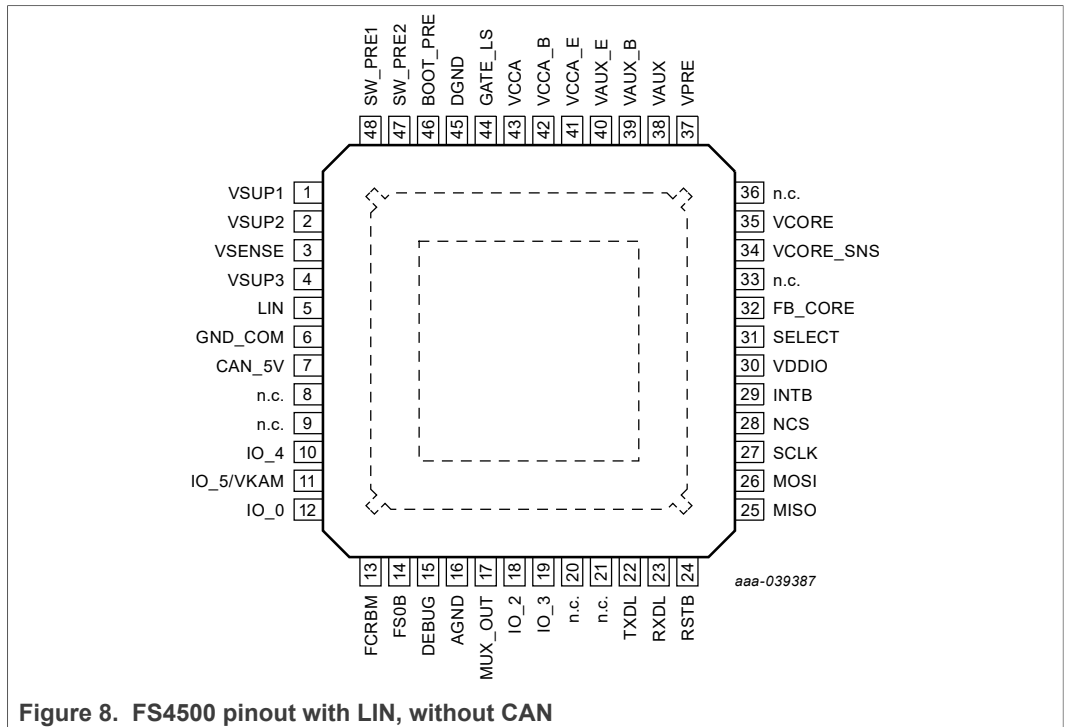


Figure 8. FS4500 pinout with LIN, without CAN

7.2 Pin description

A functional description of each pin can be found in the full data sheet.

Table 3. FS6500/FS4500 pin definition

| Pin number | Pin name | Type | Definition |
|---|----------|----------|--|
| 1 | VSUP1 | A_IN | Power supply of the device. An external reverse battery protection diode in series is mandatory |
| 2 | VSUP2 | A_IN | Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally. |
| 3 | VSENSE | A_IN | Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode. |
| 4 | VSUP3 | A_IN | Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter. |
| 5 | LIN | A_IN/OUT | LIN single-wire bus transmitter and receiver. |
| | or FS1B | D_OUT | Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure. |
| LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open. | | | |
| 6 | GND_COM | GROUND | Dedicated ground for physical layers |
| 7 | CAN_5V | A_OUT | Output voltage for the embedded CAN FD interface |
| 8 | CANH | A_IN/OUT | CAN output high. If CAN function is not used, this pin must be left open. |
| 9 | CANL | A_IN/OUT | CAN output low. If CAN function is not used, this pin must be left open. |

Table 3. FS6500/FS4500 pin definition...continued

| Pin number | Pin name | Type | Definition |
|------------|-----------|-----------------------|--|
| 10 | IO_4 | D_IN A_OUT | Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver Digital input: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_5). Wake-up capability: Can be selectable to wake-up on edges or levels. Output gate driver: Can drive a logic level low-side NMOS transistor. Controlled by the SPI. |
| 11 | IO_5/VKAM | A_IN D_IN A_OUT | Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. Analog input: Pin status can be read through the MUX output terminal Digital input: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_4). Wake-up capability: Can be selectable to wake-up on edges or levels. Supply output: Provide keep alive memory supply in low-power mode |
| 12 | IO_0 | A_IN D_IN | Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) Analog input: Pin status can be read through the MUX output terminal Digital input: Pin status can be read through the SPI. Wake-up capability: Can be selectable to wake-up on edges or levels. |
| 13 | FCRBM | A_IN | Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V _{CORE} (in parallel to the one used to set the V _{CORE} voltage). If not used, this pin must be connected directly to FB_CORE. |
| 14 | FS0B | D_OUT | First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure. |
| 15 | DEBUG | D_IN | Debug mode entry input |
| 16 | AGND | GROUND | Analog ground connection |
| 17 | MUX_OUT | A_OUT | Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI. |
| 18 19 | IO_2:3 | D_IN | Digital input pin with wake-up capability (logic level compatible) Digital input: Pin status can be read through the SPI. Wake-up capability: Can be selectable to wake-up on edges or levels. |
| 20 | TXD | D_IN | Transceiver input from the MCU which controls the state of the CAN-bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open. |
| 21 | RXD | D_OUT | Receiver output which reports the state of the CAN-bus to the MCU If CAN function is not used, this pin must be left open. |
| 22 | TXDL | D_IN | Transceiver input from the MCU controlling the state of the LIN bus. Internal pull-up to VDDIO. |
| | or VPU_FS | A_OUT | Pull-up output for FS1B function. LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open. |
| 23 | RXDL | D_OUT | Receiver output reporting the state of the LIN bus to the MCU. If LIN function is not used, this pin must be left open. |

Table 3. FS6500/FS4500 pin definition...continued

| Pin number | Pin name | Type | Definition |
|------------|-----------|----------|--|
| 24 | RSTB | D_OUT | This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure. |
| 25 | MISO | D_OUT | SPI bus. Master input slave output |
| 26 | MOSI | D_IN | SPI bus. Master output slave input |
| 27 | SCLK | D_IN | SPI Bus. Serial clock |
| 28 | NCS | D_IN | Not chip select (active low) |
| 29 | INTB | D_OUT | This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO. |
| 30 | VDDIO | A_IN | Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os. |
| 31 | SELECT | D_IN | Hardware selection pin for VAUX and VCCA output voltages |
| 32 | FB_CORE | A_IN | VCORE voltage feedback. Input of the error amplifier. |
| 33 | COMP_CORE | A_OUT | Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC). |
| 34 | VCORE_SNS | A_IN | VCORE input voltage sense |
| 35 | SW_CORE | A_OUT | VCORE output switching point for FS6500 series |
| | or VCORE | A_OUT | VCORE output voltage for FS4500 series |
| 36 | BOOT_CORE | A_IN/OUT | Bootstrap capacitor for VCORE internal NMOS gate drive. For FS4500 series, this pin must be left open (NC). |
| 37 | VPRE | A_IN | VPRE input voltage sense |
| 38 | VAUX | A_OUT | VAUX output voltage. External PNP ballast transistor. Collector connection |
| 39 | VAUX_B | A_OUT | VAUX voltage regulator. External PNP ballast transistor. Base connection |
| 40 | VAUX_E | A_OUT | VAUX voltage regulator. External PNP ballast transistor. Emitter connection |
| 41 | VCCA_E | A_OUT | VCCA voltage regulator. External PNP ballast transistor. Emitter connection |
| 42 | VCCA_B | A_OUT | VCCA voltage regulator. External PNP ballast transistor. Base connection |
| 43 | VCCA | A_OUT | VCCA output voltage. External PNP ballast transistor. Collector connection |
| 44 | GATE_LS | A_OUT | Low-side MOSFET gate drive for non-inverting buck-boost configuration |
| 45 | DGND | GROUND | Digital ground connection |
| 46 | BOOT_PRE | A_IN/OUT | Bootstrap capacitor for the VPRE internal NMOS gate drive |
| 47 | SW_PRE2 | A_OUT | Second pre-regulator output switching point |
| 48 | SW_PRE1 | A_OUT | First pre-regulator output switching point |

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Value | Unit | Notes |
|---|---|-------------|------|-------|
| Electrical ratings | | | | |
| V _{SUP1/2/3} | DC voltage at power supply pins | -1.0 to 40 | V | [1] |
| V _{SENSE} | DC voltage at battery sense pin (with ext R in series mandatory) | -14 to 40 | V | |
| V _{SW1,2} | DC voltage at SW_PRE1 and SW_PRE2 Pins | -1.0 to 40 | V | |
| V _{PRE} | DC voltage at VPRE Pin | -0.3 to 8 | V | |
| V _{GATE_LS} | DC voltage at Gate_LS pin | -0.3 to 8 | V | |
| V _{BOOT_PRE} | DC voltage at BOOT_PRE pin | -1.0 to 50 | V | |
| V _{SW_CORE} | DC voltage at SW_CORE pin | -1.0 to 8 | V | |
| V _{CORE_SNS} | DC voltage at V _{CORE_SNS} pin | 0.0 to 8 | V | |
| V _{BOOT_CORE} | DC voltage at BOOT_CORE pin | 0.0 to 15 | V | |
| V _{FB_CORE} | DC voltage at FB_CORE pin | -0.3 to 2.5 | V | |
| V _{COMP_CORE} | DC voltage at COMP_CORE pin | -0.3 to 2.5 | V | |
| V _{FCRBM} | DC voltage at FCRBM pin | -0.3 to 8 | V | |
| V _{AUX_B,E} | DC voltage at VAUX_B, VAUX_E pins | -0.3 to 40 | V | |
| V _{AUX} | DC voltage at VAUX pin | -2.0 to 40 | V | |
| V _{CCA_B,E} | DC voltage at VCCA_B, VCCA_E pins | -0.3 to 8 | V | |
| V _{CCA} | DC voltage at VCCA pin | -0.3 to 8 | V | |
| V _{DDIO} | DC voltage at VDDIO pin | -0.3 to 8 | V | |
| V _{CAN_5V} | DC voltage on CAN_5V pin | -0.3 to 8 | V | |
| V _{PU_FS} | DC voltage at VPU_FS pin | -0.3 to 8 | V | |
| V _{FSxB} | DC voltage at FS0B, FS1B pins (with ext R in series mandatory) | -0.3 to 40 | V | |
| V _{DEBUG} | DC voltage at DEBUG pin | -0.3 to 40 | V | |
| V _{IO_0,4} | DC voltage at IO_0, IO_4 pins (with ext R in series mandatory) | -0.3 to 40 | V | |
| V _{IO_5} | DC voltage at IO_5 pin | -0.3 to 20 | V | |
| V _{KAM} | DC voltage at VKAM pin | -0.3 to 8 | V | |
| V _{DIG} | DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, RXDL, TXDL, IO_2, IO_3 pins | -0.3 to 8 | V | |
| V _{SELECT} | DC voltage at SELECT pin | -0.3 to 8 | V | |
| V _{BUS_CAN} | DC voltage on CANL, CANH pins | -27 to 40 | V | |
| I _{Isense} | V _{SENSE} maximum current capability | -5.0 to 5.0 | mA | |
| I _{IO_0, 4, 5} | IOs maximum current capability (IO_0, IO_4, IO_5) | -5.0 to 5.0 | mA | |
| ESD voltage | | | | |
| Human body model (JESD22/A114)^[19] – 100 pF, 1.5 kΩ | | | | |
| V _{ESD-HBM1} | • All pins | ±2.0 | kV | [2] |
| V _{ESD-HBM2} | • VSUP1, 2, 3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG | ±4.0 | kV | |
| V _{ESD-HBM3} | • CANH, CANL | ±6.0 | kV | |
| V _{ESD-HBM4} | • LIN | ±8.0 | kV | |

Table 4. Maximum ratings ...continued

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Value | Unit | Notes |
|--|---|------------|------|-------|
| Charge device model (JESD22/C101)⁽²⁰⁾: | | | | |
| V _{ESD-CDM1} | • All pins | ±500 | V | |
| V _{ESD-CDM2} | • Corner pins | ±750 | V | |
| System level ESD (gun test) | | | | |
| | • VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B | | | |
| V _{ESD-GUN1} | 330 Ω/150 pF unpowered according to IEC 61000-4-2: ⁽¹⁶⁾ | ±8.0 | kV | |
| V _{ESD-GUN2} | 330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance | ±8.0 | kV | |
| V _{ESD-GUN3} | 2.0 kΩ/150 pF unpowered according to ISO 10605 ⁽¹⁵⁾ | ±8.0 | kV | |
| V _{ESD-GUN4} | 2.0 kΩ/330 pF powered according to ISO 10605 ⁽¹⁵⁾ | ±8.0 | kV | |
| | • CANH, CANL | | | |
| V _{ESD-GUN5} | 330 Ω/150 pF unpowered according to IEC 61000-4-2: ⁽¹⁶⁾ | ±15.0 | kV | |
| V _{ESD-GUN6} | 330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance | ±12.0 | kV | |
| V _{ESD-GUN7} | 2.0 kΩ/150 pF unpowered according to ISO 10605 ⁽¹⁵⁾ | ±15.0 | kV | |
| V _{ESD-GUN8} | 2.0 kΩ/330 pF powered according to ISO 10605 ⁽¹⁵⁾ | ±12.0 | kV | |
| | • LIN | | | |
| V _{ESD-GUN9} | 330 Ω/150 pF unpowered according to IEC 61000-4-2: ⁽¹⁶⁾ | ±12.0 | kV | |
| V _{ESD-GUN10} | 330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay conformance | ±12.0 | kV | |
| V _{ESD-GUN11} | 2.0 kΩ/150 pF unpowered according to ISO 10605 ⁽¹⁵⁾ | ±12.0 | kV | |
| V _{ESD-GUN12} | 2.0 kΩ/330 pF powered according to ISO 10605 ⁽¹⁵⁾ | ±12.0 | kV | |
| Thermal ratings | | | | |
| T _A | Ambient temperature | -40 to 125 | °C | |
| T _J | Junction temperature | -40 to 150 | °C | |
| T _{STG} | Storage temperature | -55 to 150 | °C | |
| Thermal resistance | | | | |
| R _{θJA} | Thermal resistance junction to ambient | 30 | °C/W | [3] |
| R _{θJCTOP} | Thermal resistance junction to case top | 23.8 | °C/W | [4] |
| R _{θJCBOTTOM} | Thermal resistance junction to case bottom | 0.9 | °C/W | [5] |

[1] All V_{SUPS} (V_{SUP1/2/3}) must be connected to the same supply (Figure 1).

[2] Compared to AGND.

[3] Per JEDEC JESD51-6⁽¹⁷⁾ with the board (JESD51-7)⁽¹⁸⁾ horizontal.

[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1)⁽²¹⁾.

[5] Thermal resistance between the die and the solder pad on the bottom of the packaged based on simulation without any interface resistance.

9 Packaging

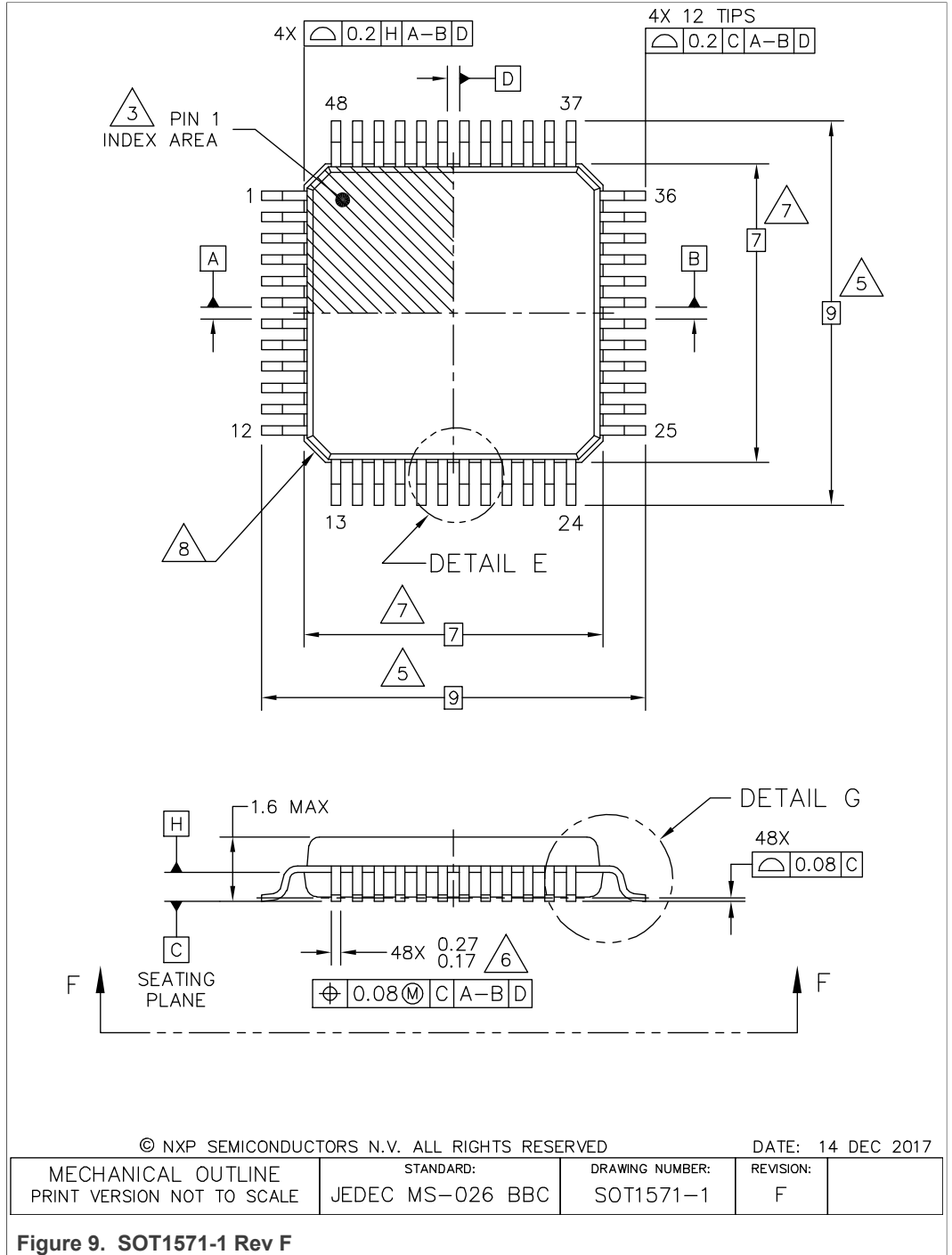
9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 5. Package mechanical dimensions

| Package | Suffix | Package outline drawing number |
|--|--------|--------------------------------|
| 7.0 × 7.0, 48-Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad | AE | 98ASA00173D |

9.2 Package outline



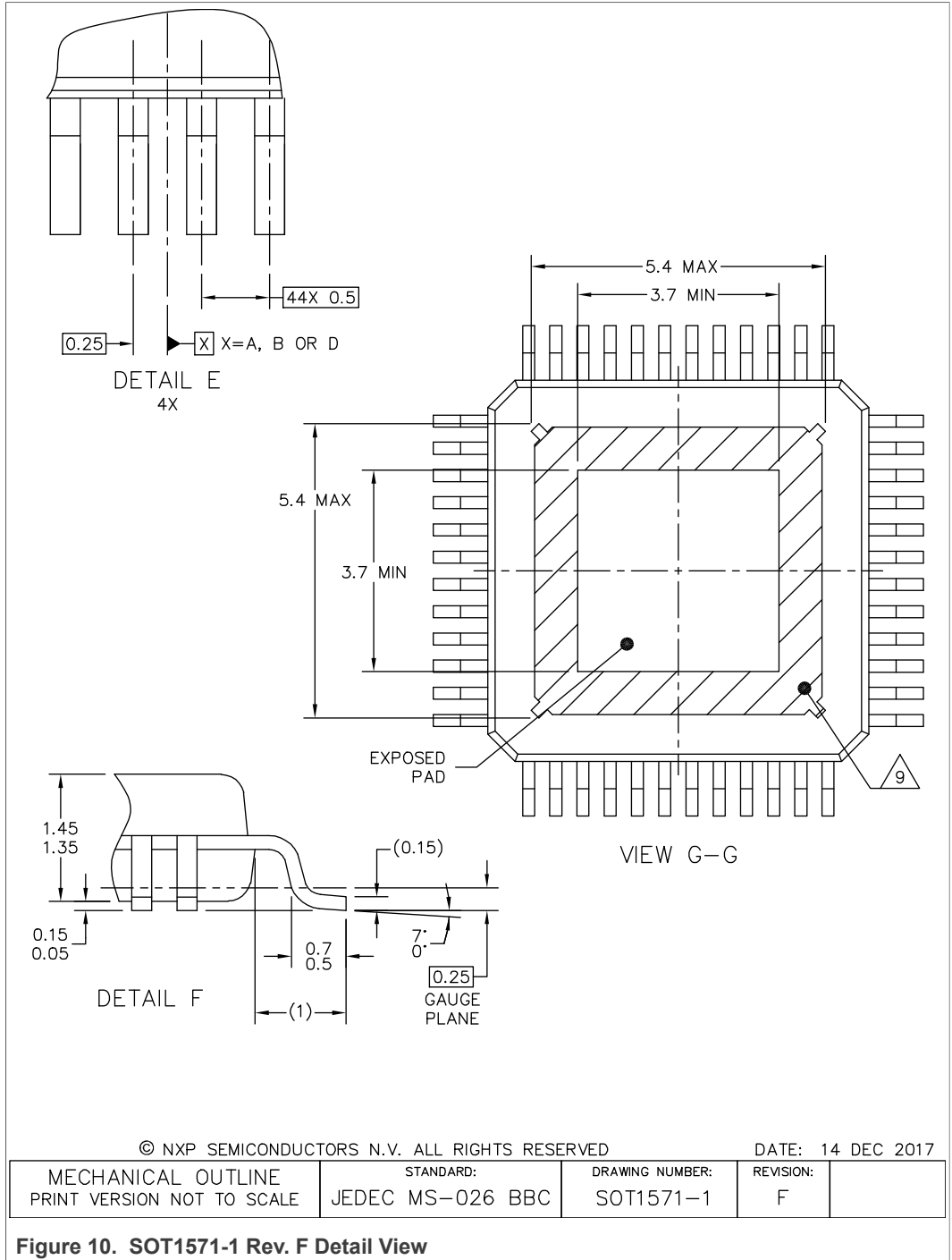
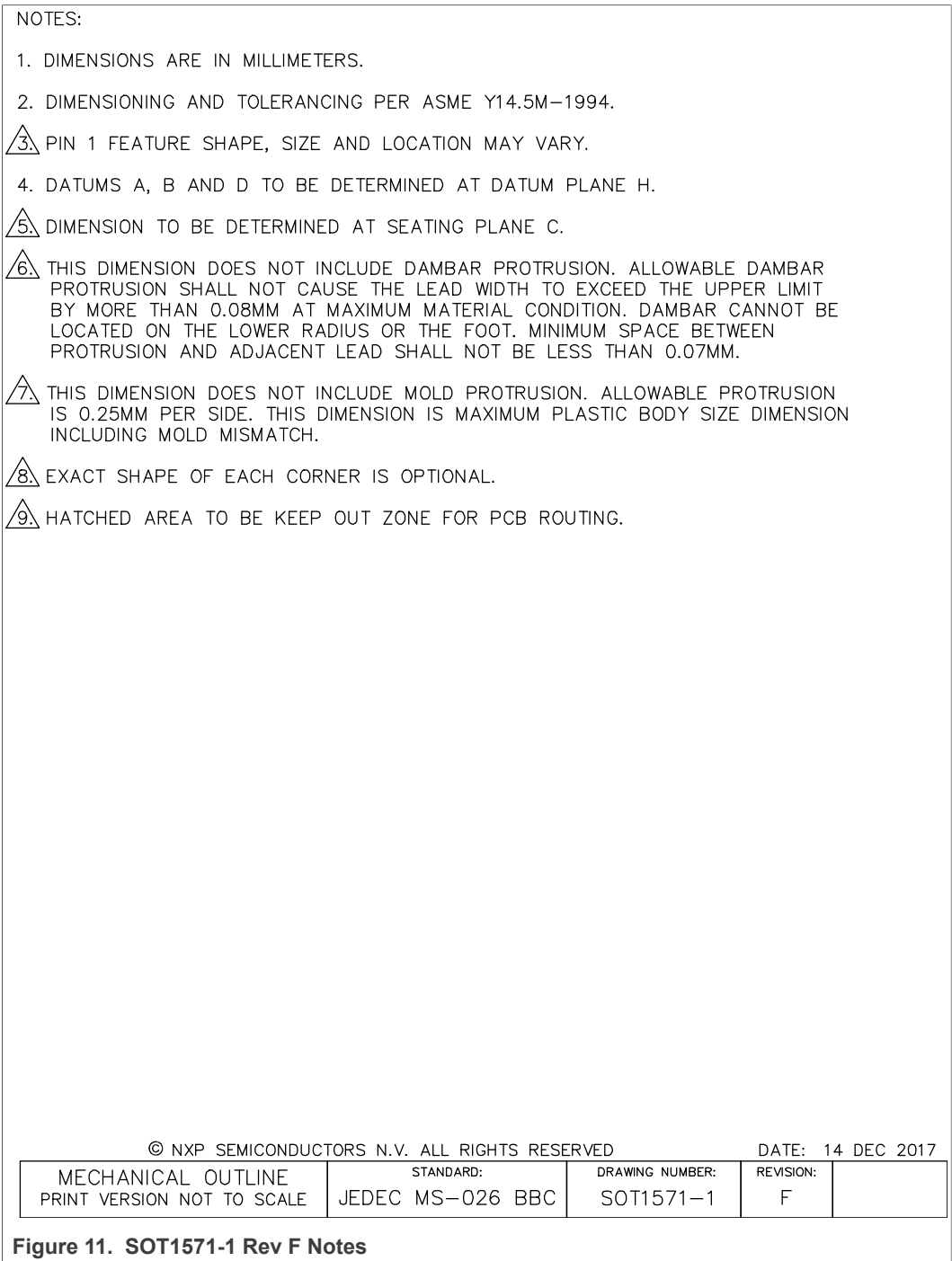
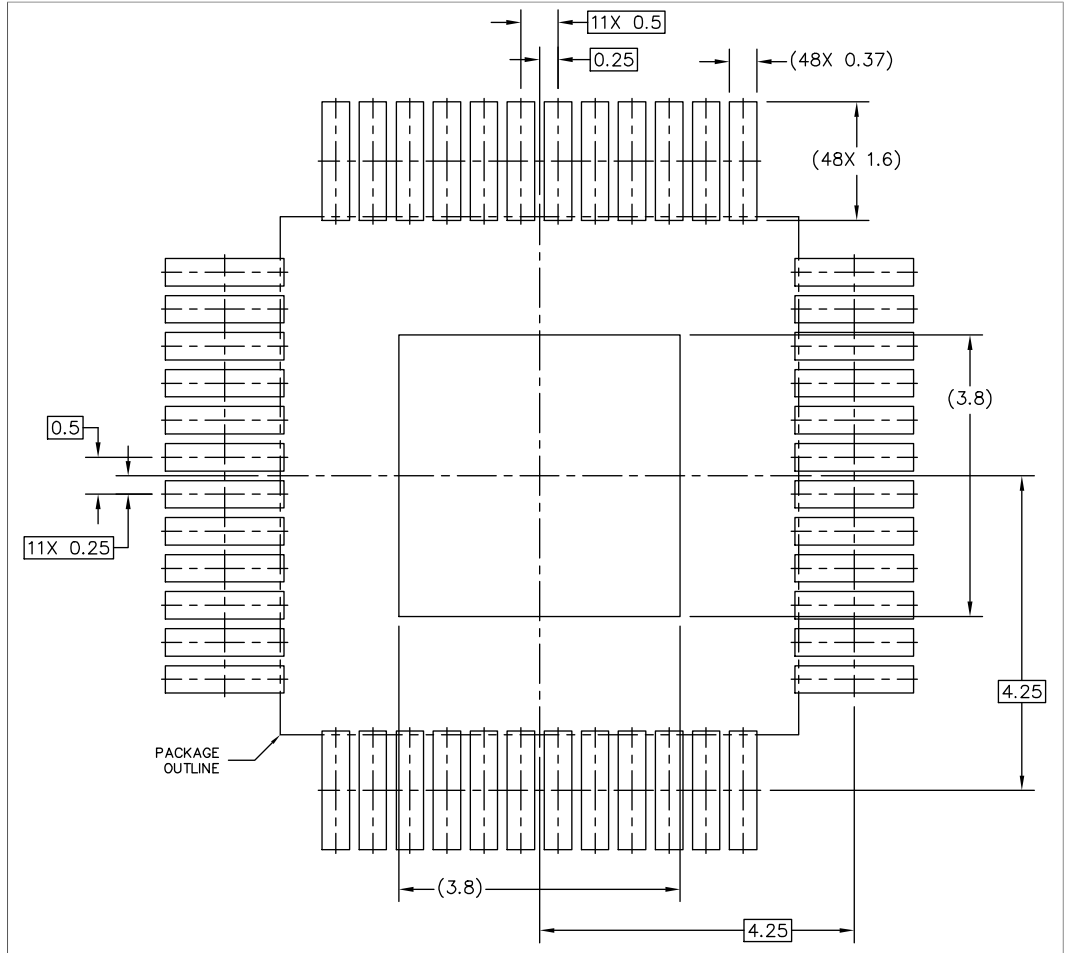


Figure 10. SOT1571-1 Rev. F Detail View



10 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

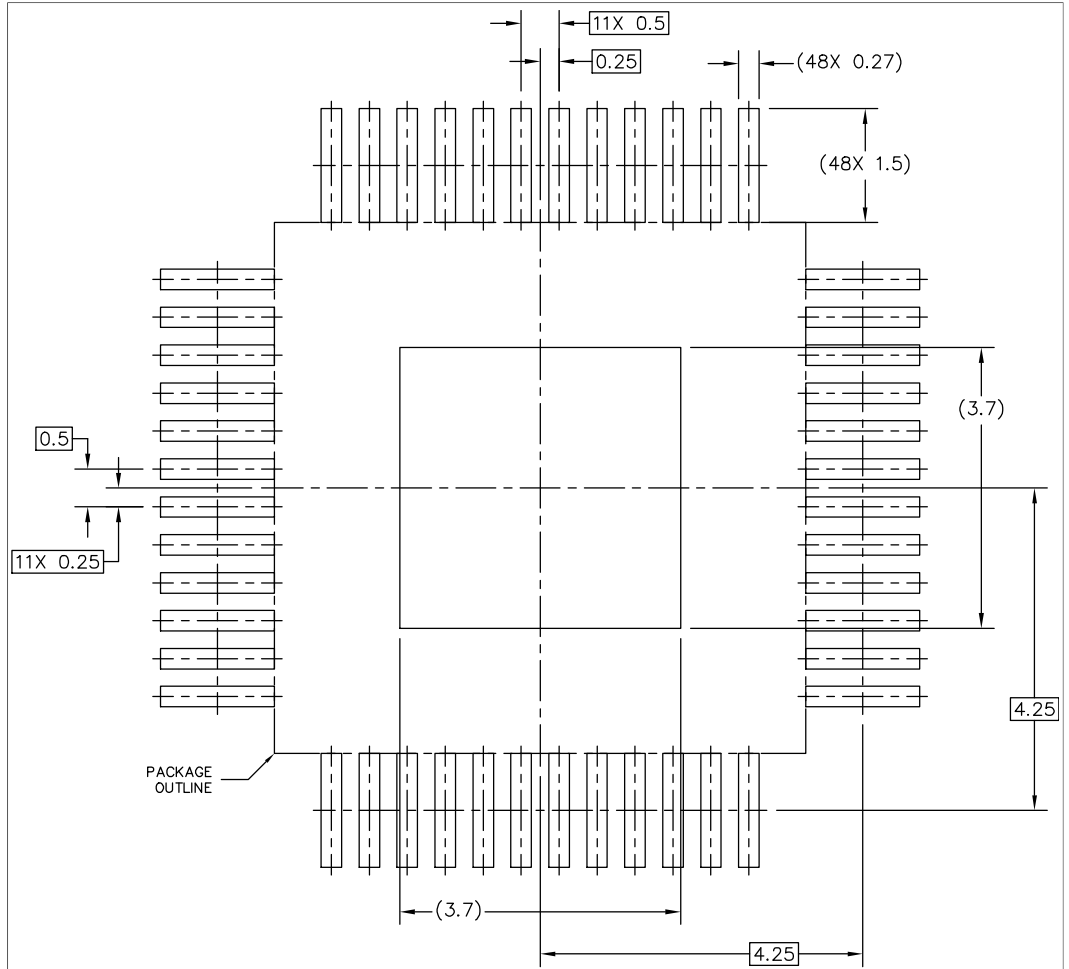
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 14 DEC 2017

| | | | |
|--|-------------------------------|------------------------------|----------------|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: JEDEC MS-026 BBC | DRAWING NUMBER: SOT1571-1 | REVISION: F |
|--|-------------------------------|------------------------------|----------------|

Figure 12. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

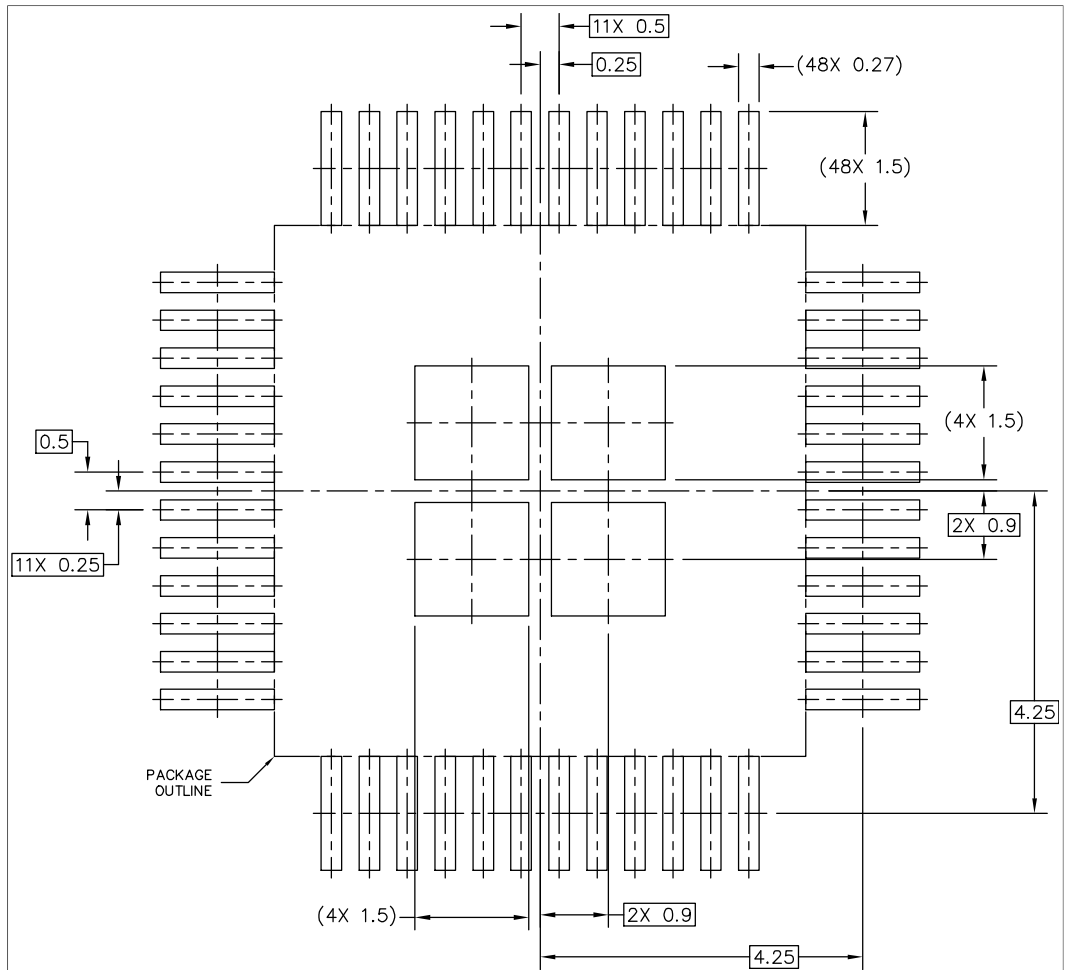
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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| | | | | |
|--|-------------------------------|------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: JEDEC MS-026 BBC | DRAWING NUMBER: SOT1571-1 | REVISION: F | |
|--|-------------------------------|------------------------------|----------------|--|

Figure 13. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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| | | | | |
|--|-------------------------------|------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: JEDEC MS-026 BBC | DRAWING NUMBER: SOT1571-1 | REVISION: F | |
|--|-------------------------------|------------------------------|----------------|--|

Figure 14. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil

11 References

Obtain additional information on related NXP products and application solutions through the documents and URLs listed below.

- (1) **AN5238** - FS6500 and FS4500 Safe System Basis Chip Hardware Design and Product Guidelines - Application Note
<https://www.nxp.com/AN5238-DOWNLOAD>
- (2) **AN4388** - Quad Flat Package (QFP)
https://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
- (3) **FS6500-FS4500PDTCALC** - Power dissipation tool (Excel File)
https://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx
- (4) **V_{CORE} compensation network simulation tool (CNC)**^[1]
- (5) **FMEDA** - FS6500/FS4500 ASILB FMEDA^[1]
- (6) **UM11498** - FS6500/FS4500 ASILB Safety manual – user guide
- (7) **KITFS6507LAEVEM** - FS6507, System Basis Chip, ASIL B, DC-DC 0.8 A Vcore, LDT, CAN, LIN
<https://www.nxp.com/KITFS6507LAEVEM>
- (8) **KITFS4508CAEEVEM** - FS4508, System Basis Chip, ASIL B, Linear 0.5 A Vcore, FS1b, LDT, CAN
<https://www.nxp.com/KITFS4508CAEEVEM>
- (9) **FS6500 product summary page** -
<https://www.nxp.com/FS6500>
- (10) **FS4500 product summary page** -
<https://www.nxp.com/FS4500>
- (11) **Analog power management homepage** -
<https://www.nxp.com/products/power-management>
- (12) **ISO 11898-2:2003** - Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit
<https://www.iso.org/standard/33423.html>
- (13) **ISO 11898-5:2007** - Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode
<https://www.iso.org/contents/data/standard/04/12/41284.html>
- (14) **ISO 7637-2:2011** - Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only
<https://www.iso.org/standard/50925.html>
- (15) **ISO 10605:2008** - Road vehicles — Test methods for electrical disturbances from electrostatic discharge
<https://www.iso.org/standard/41937.html>
- (16) **IEC 61000-4-2:2008** - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
<https://webstore.iec.ch/publication/4189>
- (17) **JESD51-6** - INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR)
- (18) **JESD51-7** - HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES
- (19) **JESD22-A114F** - ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)
- (20) **JESD22-C101F** - FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS
- (21) **MIL-STD-883-1, Method 1012.1** - TEST METHOD STANDARD MICROCIRCUITS

- (22) **LIN Specification Package Revision 2.1:2006**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN-Spec_Pac2_1.pdf
- (23) **LIN Specification Package Revision 2.2A:2010**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN_2.2A.pdf
- (24) **SAE J2602-2:201211 - LIN Network for Vehicle Applications Conformance Test**
https://www.sae.org/standards/content/j2602/2_201211/

[1] Available upon request.

12 Revision history

Table 6. Revision history

| Document ID | Release date | Data sheet status | Supersedes |
|------------------------------|---|-------------------|------------------------------|
| FS6500-FS4500SDS-ASILB v.3.0 | 20210414 | Product | FS6500-FS4500SDS-ASILB v.2.0 |
| Modifications | <ul style="list-style-type: none"> • Section 1: replaced "0.8 A" by "1.5 A" • Section 2: replaced "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A) or LDO (0.5 A)" to "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)" • Section 5: updated Table 1 and Table 2 (added new part numbers) | | |
| FS6500-FS4500SDS-ASILB v.2.0 | 20210111 | Product | FS6500-FS4500SDS-ASILB v.1.3 |
| Modifications | <ul style="list-style-type: none"> • Revised data sheet status from "Preliminary" to "Product". • Section 5.2, revised Table 2 changing "PC33..." parts to "MC33..." • Section 7.2, pin number 11, removed "VKAM can be enabled or disabled by default at power up. The differentiation is made by part numbers." | | |
| FS6500-FS4500SDS-ASILB v.1.3 | 20201106 | Preliminary | — |
| Modifications | <ul style="list-style-type: none"> • Initial release (Short data sheet version aligned to full data sheet, FS6500, FS4500: ASILB, v.1.3) | | |

13 Legal information

13.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Tables

| | | | | | |
|---------|------------------------------------|---|---------|-------------------------------------|----|
| Tab. 1. | Part number breakdown | 3 | Tab. 4. | Maximum ratings | 12 |
| Tab. 2. | Orderable part variations | 4 | Tab. 5. | Package mechanical dimensions | 14 |
| Tab. 3. | FS6500/FS4500 pin definition | 9 | Tab. 6. | Revision history | 22 |

Figures

| | | | | | |
|---------|---|---|----------|--|----|
| Fig. 1. | FS6500C simplified application diagram - buck boost configuration - FS1B | 2 | Fig. 8. | FS4500 pinout with LIN, without CAN | 9 |
| Fig. 2. | FS4500C simplified application diagram - buck boost configuration - FS1B | 3 | Fig. 9. | SOT1571-1 Rev F | 15 |
| Fig. 3. | FS6500/FS4500 with CAN and LIN simplified internal block diagram | 6 | Fig. 10. | SOT1571-1 Rev. F Detail View | 16 |
| Fig. 4. | FS6500 pinout with CAN and FS1B | 7 | Fig. 11. | SOT1571-1 Rev F Notes | 17 |
| Fig. 5. | FS6500 pinout with CAN and LIN | 7 | Fig. 12. | SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern | 18 |
| Fig. 6. | FS6500 pinout without CAN, without LIN | 8 | Fig. 13. | SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area | 19 |
| Fig. 7. | FS4500 pinout with CAN and FS1B | 8 | Fig. 14. | SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil | 20 |