FS84/FS85C

Fail-safe system basis chip with multiple SMPS and LDO

Rev. 7 — 7 May 2021 Product brief

1 About this document

This Product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant FS84_FS85 full data sheet, available via the NXP DocStore at https://www.docstore.nxp.com.

2 General description

The FS85/FS84 device family is developed in compliance with ASIL D process, FS84 is ASIL B capable and FS85 is ASIL D capable. All device options are pin to pin and software compatible.

The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard and is qualified in compliance with AEC-Q100 rev H (Grade1, MSL3).

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

3 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on device options (see** Table 1**)**: low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.

- **Based on device options (see Table 1)**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode (power down) with very low quiescent current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

4 Applications

- Radar (corner radar, imaging radar, ...)
- Vision (mono camera, stereo camera, night vision, ...)
- ADAS domain controller
- Infotainment
- V2x

5 Ordering information

Table 1. Device options

Device options	BUCK1	BUCK2	BUCK3	FCCU	VMONx	ASIL
FS8400	Yes	No	No	No	up to 2	B
FS8405	Yes	No	No	optional	up to 4	B
FS8410	Yes	No	Yes	No	up to 2	B
FS8415	Yes	No	Yes	optional	up to 4	B
FS8420	Yes	Yes	No	No	up to 2	B
FS8425	Yes	Yes	No	optional	up to 4	B
FS8430	Yes	Yes	Yes	No	up to 2	B
FS8435	Yes	Yes	Yes	optional	up to 4	B
FS8500	Yes	No	No	Yes	up to 4	D
FS8510	Yes	No	Yes	Yes	up to 4	D
FS8520	Yes	Yes	No	Yes	up to 4	D
FS8530	Yes	Yes	Yes	Yes	up to 4	D

Table 2. Ordering information

Part number [1] [2][3]	Application target	Package		
		Name	Description	Version
MC33FS8400G0ES MC33FS8400G0KS	Superset covering FS8400 configurations	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; wettable flank, 56 terminals; 0.5 mm pitch, 8 mm x 8 mm x 0.85 mm body See Section 13.1 "Package outline" for differences.	SOT684-23
MC33FS8400G5ES MC33FS8400G5KS	Camera			
MC33FS8405G0ES MC33FS8405G0KS	Superset covering FS8405 configurations			
MC33FS8410G0ES MC33FS8410G0KS	Superset covering FS8410 configurations			
MC33FS8410G3ES MC33FS8410G3KS	Radar with NXP S32R274 MCU			
MC33FS8410G6ES MC33FS8410G6KS	Gateway with NXP MPC5748G MCU			
MC33FS8415G0ES MC33FS8415G0KS	Superset covering FS8415 configurations			
MC33FS8415GJES MC33FS8415GJKS	For Radar with NXP S32R294 + TEF810x for 12 V/24 V application [4]			
MC33FS8415GYES MC33FS8415GYKS	For Radar with NXP S32R294 + TEF810x/ TEF82xx for 12 V/24 V application			
MC33FS8420G0ES MC33FS8420G0KS	Superset covering FS8420 configurations			
MC33FS8425G0ES MC33FS8425G0KS	Superset covering FS8425 configurations			
MC33FS8430G0ES MC33FS8430G0KS	Superset covering FS8430 configurations			
MC33FS8430G1ES MC33FS8430G1KS	Camera with NXP S32V MCU and PF8x PMIC			
MC33FS8430G2ES MC33FS8430G2KS	Camera with NXP S32V MCU			
MC33FS8430G4ES MC33FS8430G4KS	Camera			
MC33FS8435G0ES MC33FS8435G0KS	Superset covering FS8435 configurations			
MC33FS8500A0ES MC33FS8500A0KS	Superset covering FS8500 configurations			
MC33FS8510A0ES MC33FS8510A0KS	Superset covering FS8510 configurations			
MC33FS8510A2ES MC33FS8510A2KS	Domain controller			
MC33FS8510D3ES MC33FS8510D3KS	Battery monitoring system			
MC33FS8520A0ES MC33FS8520A0KS	Superset covering FS8520 configurations			
MC33FS8530A0ES MC33FS8530A0KS	Superset covering FS8530 configurations			
MC33FS8530A1ES MC33FS8530A1KS	Camera			
MC33FS8530A4ES MC33FS8530A4KS	Imaging radar with NXP S32R MCU			

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Step-cut wettable flank for part numbers ending in ES
Dimple wettable flank for part numbers ending in KS

[3] The part numbers with KS suffix are recommended for new designs.
[4] FS8415GY part is recommended for new designs

A0 and G0 parts are non-programmed OTP configurations. Pre-programmed OTP configurations (other than BUCK regulators and ASIL level) are managed through part number extension: A1 to FZ for FS85 and G1 to LZ for FS84.

For a custom OTP configuration, contact you local NXP sales representative.

6 Simplified application diagram

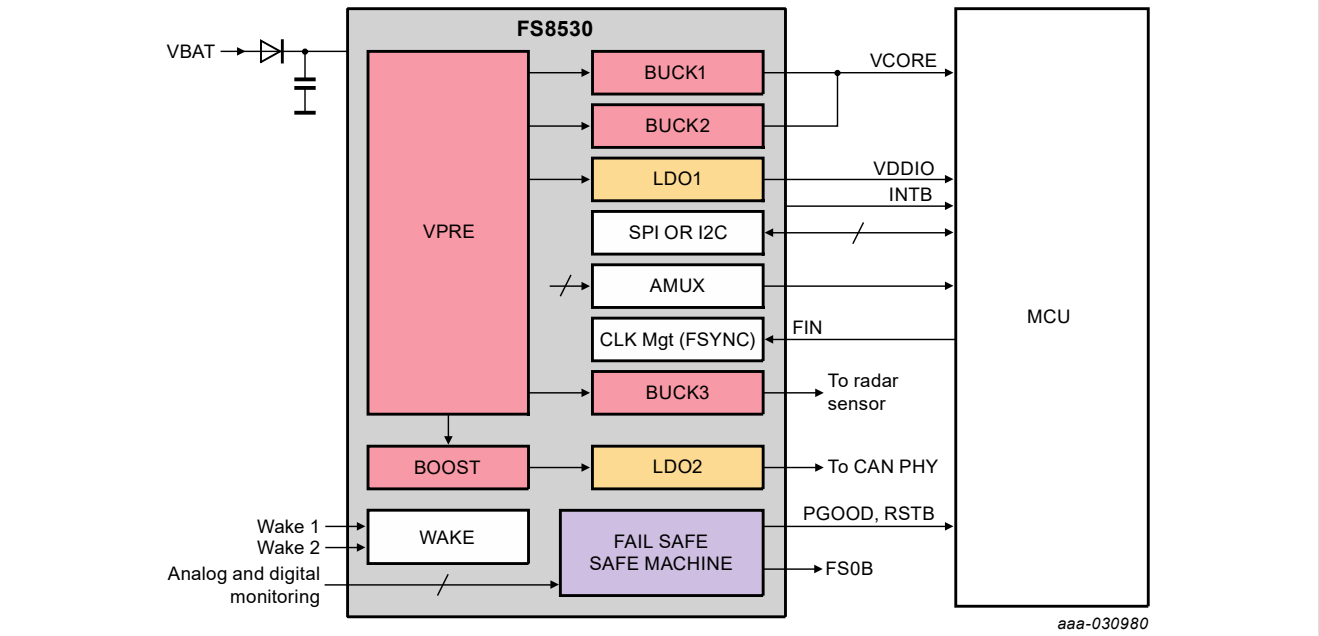


Figure 1. FS8530 superset device of the family

7 Pinning information

7.1 Pinning

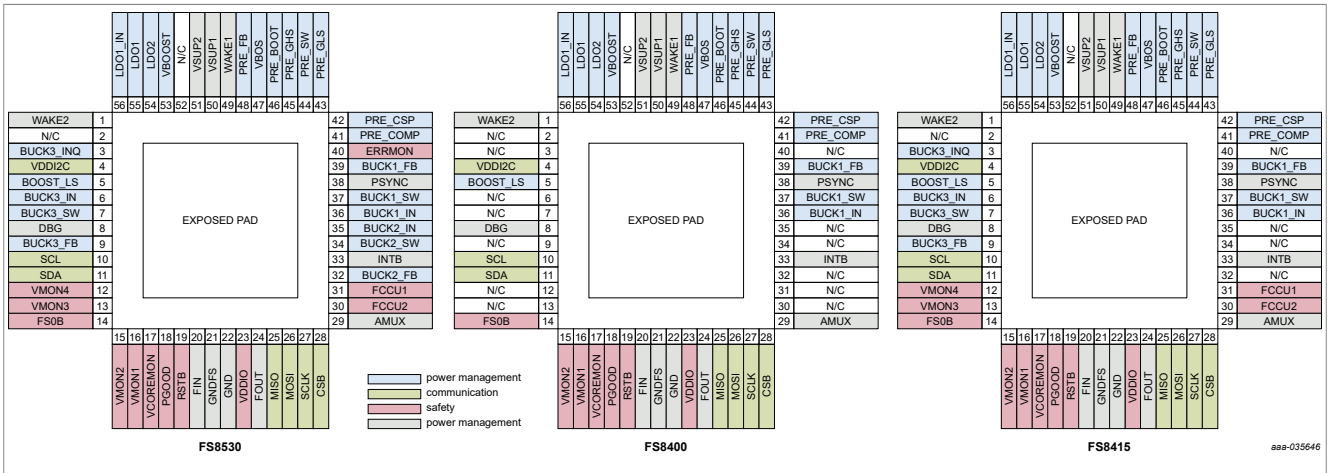


Figure 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description [1]
WAKE2	1	A_IN / D_IN	Wake-up input 2 An external serial resistor is required if WAKE2 is a global pin
N/C	2	N/C	Not connected pin
BUCK3_INQ	3	A_IN	Low voltage Buck3 quiet input voltage
VDDI2C	4	A_IN	Input voltage for I2C buffers
BOOST_LS	5	A_IN	Boost low-side drain of internal MOSFET
BUCK3_IN	6	A_IN	Low voltage Buck3 input voltage
BUCK3_SW	7	A_OUT	Low voltage Buck3 switching node
DBG	8	A_IN	Debug mode entry
BUCK3_FB	9	A_IN	Low voltage Buck3 voltage feedback
SCL	10	D_IN	I2C bus Clock input
SDA	11	D_IN/OUT	I2C bus Bidirectional data line
VMON4	12	A_IN	Voltage monitoring input 4
VMON3	13	A_IN	Voltage monitoring input 3
FS0B	14	D_OUT	Fail-safe output 0 Active low Open drain structure
VMON2	15	A_IN	Voltage monitoring input 2
VMON1	16	A_IN	Voltage monitoring input 1
VCOREMON	17	A_IN	VCORE monitoring input: Must be connected to Buck1 output voltage
PGOOD	18	D_OUT	Power good output Active low Pull up to VDDIO mandatory
RSTB	19	D_OUT	Reset output Active low The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault condition. Pull up to VDDIO mandatory
FIN	20	D_IN	Frequency synchronization input
GNDFS	21	GND	Fail-safe ground
GND	22	GND	Main ground
VDDIO	23	A_IN	Input voltage for SPI, FOUT and AMUX buffers Allow voltage compatibility with MCU I/Os
FOUT	24	D_OUT	Frequency synchronization output
MISO	25	D_OUT	SPI bus Master input slave output
MOSI	26	D_IN	SPI bus Master output slave Input
SCLK	27	D_IN	SPI bus Clock input
CSB	28	D_IN	Chip select (active low)

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description [1]
AMUX	29	A_OUT	Multiplexed output to connect to MCU ADC Selection of the analog parameter through SPI or I2C
FCCU2	30	D_IN	MCU error monitoring input 2
FCCU1	31	D_IN	MCU error monitoring input 1
BUCK2_FB	32	A_IN	Low voltage Buck2 voltage feedback
INTB	33	D_OUT	Interrupt output
BUCK2_SW	34	A_OUT	Low voltage Buck2 switching node
BUCK2_IN	35	A_IN	Low voltage Buck2 input voltage
BUCK1_IN	36	A_IN	Low voltage Buck1 input voltage
BUCK1_SW	37	A_OUT	Low voltage Buck1 switching node
PSYNC	38	D_IN/OUT	Power synchronization input/output
BUCK1_FB	39	A_IN	Low voltage Buck1 voltage feedback
ERRMON	40	D_IN	External IC error monitoring input
PRE_COMP	41	A_IN	VPRE compensation network
PRE_CSP	42	A_IN	VPRE positive current sense input
PRE_GLS	43	A_OUT	VPRE low-side gate driver for external MOSFET
PRE_SW	44	A_IN	VPRE switching node
PRE_GHS	45	A_OUT	VPRE high-side gate driver for external MOSFET
PRE_BOOT	46	A_IN/OUT	VPRE bootstrap capacitor
VBOS	47	A_OUT	Best of supply output voltage
PRE_FB	48	A_IN	VPRE voltage feedback and negative current sense input
WAKE1	49	A_IN / D_IN	Wake up input 1 An external serial resistor is required if WAKE1 is a global pin
VSUP1	50	A_IN	Power supply 1 of the device An external reverse battery protection diode in series is mandatory
VSUP2	51	A_IN	Power supply 2 of the device An external reverse battery protection diode in series is mandatory
N/C	52	N/C	Not connected pin
VBOOST	53	A_IN	VBOOST voltage feedback
LDO2	54	A_OUT	Linear regulator 2 output voltage
LDO1	55	A_OUT	Linear regulator 1 output voltage
LDO1_IN	56	A_IN	Linear regulator 1 input voltage
EP	57	GND	Expose pad (BUCK1, BUCK2 and BUCK3 low-side GNDs are connected to the expose pad) Must be connected to GND

[1] See Connection of unused pins for connection of unused pins.

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage ratings					
VSUP1/2	DC voltage	power supply VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC voltage	WAKE1,2 pins; external serial resistor mandatory	−1.0	60	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	60	V
	Transient voltage < 20 ns		−3.0	60	V
VMONx, FS0B	DC voltage	VMON1,2,3,4, VCOREMON, FS0B pins	−0.3	60	V
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	−0.3	65.5	V
DBG	DC voltage	DBG pin	−0.3	10	V
BOOST_LS	DC voltage	BOOST_LS pin	−0.3	8.5	V
VBOOST, LDO1_IN	DC voltage	VBOOST, LDO1_IN pins	−0.3	6.5	V
BUCKx_IN	DC voltage	BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ	−1.0	5.5	V
BUCKx_IN	Transient voltage < 3 µs	BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ	−1.0	6.5	V
BUCKx_SW	Transient voltage < 20 ns	BUCK1_SW, BUCK2_SW, BUCK3_SW	−3.0	6.5	V
All other pins	DC voltage	at all other pins	−0.3	5.5	V
Current ratings					
I_WAKE	Maximum current capability	WAKE1,2	−5.0	5.0	mA
I_SUP	Maximum current capability	VSUP1,2	−5.0	—	mA

9 Electrostatic discharge

9.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model at 100 pF and 1.5 kΩ. This protection is ensured at all pins.

9.2 Charged device model

The device is protected up to ±500 V, according to the AEC Q100 - 011 charged device model standard. This protection is ensured at all pins.

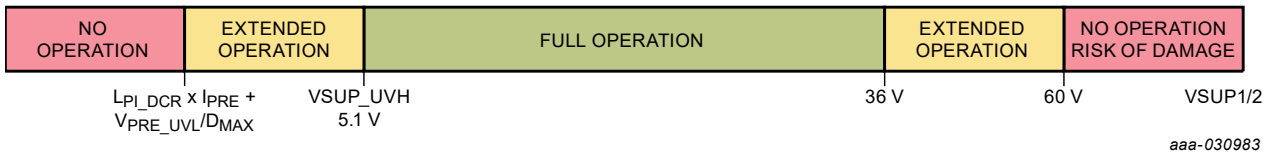
9.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2, FS0B pins.

10 Operating range



Assumptions

L_{PI_DCR} = 30 mΩ
D_{MAX} = 98.18 % with F_{PRE_SW} = 455 kHz and $T_{PRE\_OFF\_MIN}$ = 40 ns
I_{PRE} = 3.0 A
V_{RBD} = 0.56 V
VBAT_min = 3.4 V when VPRE = V_{PRE_UVL}

Figure 3. Operating range

- Below VSUP_UVH threshold, the extended operation range depends on VPRE output voltage configuration and external components.
  - When VPRE is configured at 5.0 V, VPRE may not remain in its regulation range.
  - VSUP minimum voltage depends on external components (L_{PI_DCR}) and application conditions (I_{PRE}, F_{PRE_SW}).
- When VPRE is switching at 455 kHz, the FS85/FS84 maximum continuous operating voltage is 36 V. It has been validated at 48 V for limited duration of 15 minutes at room temperature to satisfy the jump start requirement of 24 V applications. It can sustain 58 V load dump without external protection.
- When VPRE is switching at 2.2 MHz, the FS85/FS84 maximum continuous operating voltage is 18 V. It will be validated at 26 V for limited duration of 2 minutes at room temperature to satisfy the jump start requirement of 12 V applications and 35 V load dump.

11 Thermal ratings

Table 5. Thermal ratings

Symbol	Parameter	Conditions		Min	Max	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient	2s2p circuit board	[1]	—	31	°C/W
$R_{\theta JA}$	Thermal resistance junction to ambient	2s6p circuit board	[1]	—	23	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s2p circuit board	[1]	—	15	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s6p circuit board	[1]	—	10	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom	between the die and the solder pad on the bottom of the package	[1]	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal resistance junction to package top	between package top and the junction temperature	[1]	—	3	°C/W
T_A	Ambient temperature (Grade 1)			−40	125	°C
T_J	Junction temperature (Grade 1)			−40	150	°C
T_{STG}	Storage temperature			−55	150	°C

[1] per JEDEC JESD51-2 and JESD51-8

12 Characteristics

Table 6. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
I_{SUP_NORMAL}	Current in Normal mode, all regulators ON (I_{OUT} = 0)	—	15	25	mA
$I_{SUP\_STANDBY}$	Current in Standby mode, all regulators OFF except VBOS	—	5	10	mA
I_{SUP_OFF1}	Current in OFF mode (Power Down), T_A < 85 °C	—	10	15	µA
I_{SUP_OFF2}	Current in OFF mode (Power Down), T_A = 125 °C	—	—	25	µA
V_{SUP_UV7}	VSUP undervoltage threshold (7.0 V)	7.2	7.5	7.8	V
V_{SUP_UVH}	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 0	4.7	—	5.1	V
	VSUP undervoltage threshold high (during power up and Vsup rising) OTP_VSUP_CFG = 1	6.0	—	6.4	V
V_{SUP_UVL}	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 0	4.0	—	4.4	V
	VSUP undervoltage threshold low (during power up and Vsup falling) OTP_VSUP_CFG = 1	5.3	—	5.7	V
T_{SUP_UV}	V_{SUP_UV7}, V_{SUP_UVH} and V_{SUP_UVL} filtering time	6.0	10	15	µs

13 Package information

FS85/FS84 package is a QFN (sawn), thermally enhanced wettable flanks, 8 x 8 x 0.85 mm, 0.5 mm pitch, 56 pins.

13.1 Package outline

13.1.1 Step-cut wettable flank

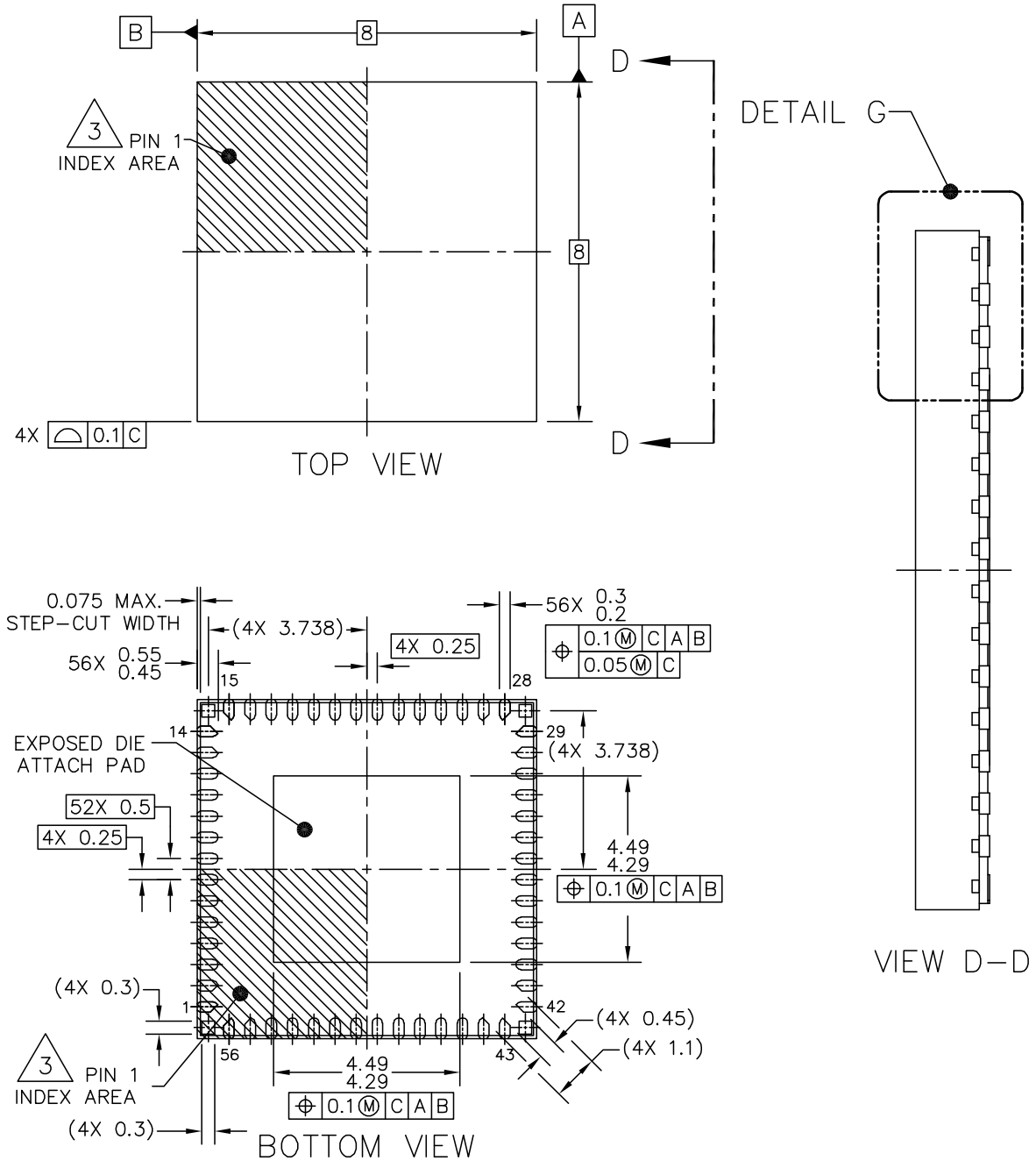


Figure 4. Package outline for HVQFN56 (SOT684-23, Step-cut)

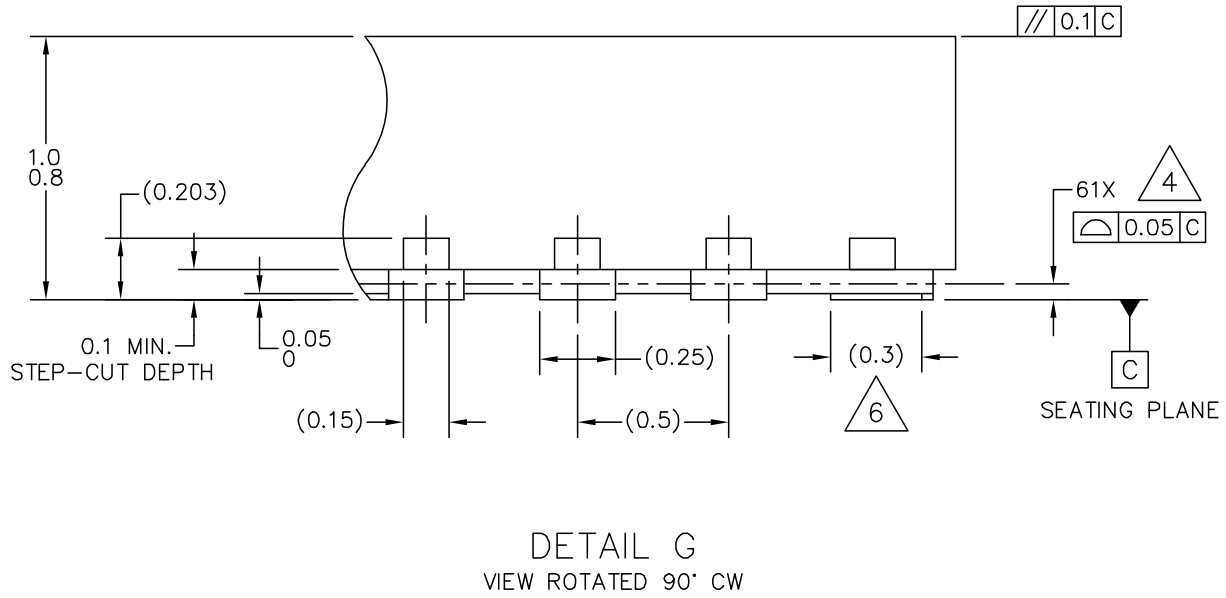


Figure 5. Package outline detail for HVQFN56 (SOT684-23, Step-cut)

13.1.2 Dimple wettable flank

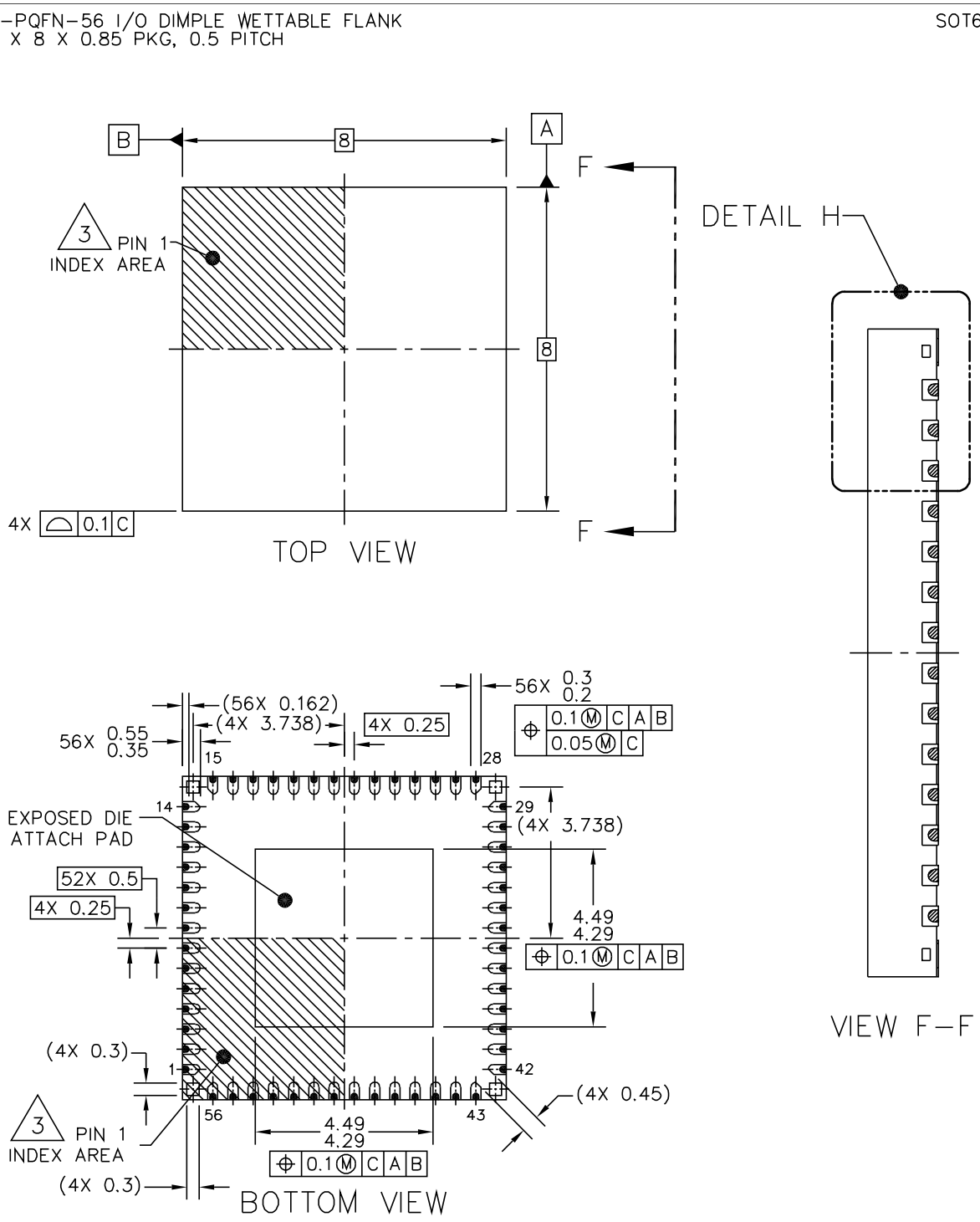


Figure 6. Package outline for HVQFN56 (SOT684-23, Dimple)

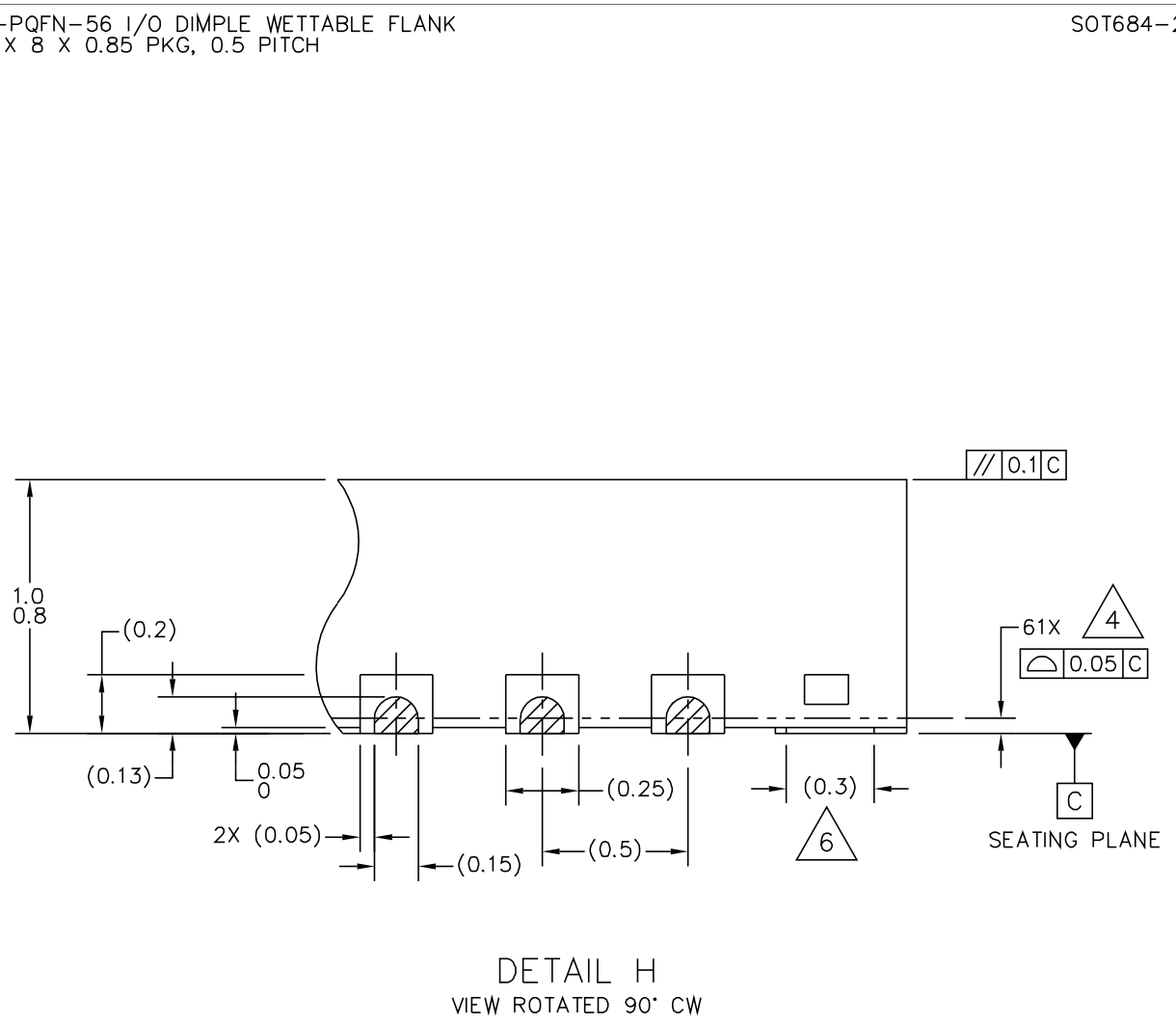


Figure 7. Package outline detail for HVQFN56 (SOT684-23, Dimple)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 8. Package outline notes for HVQFN56 (SOT684-23)

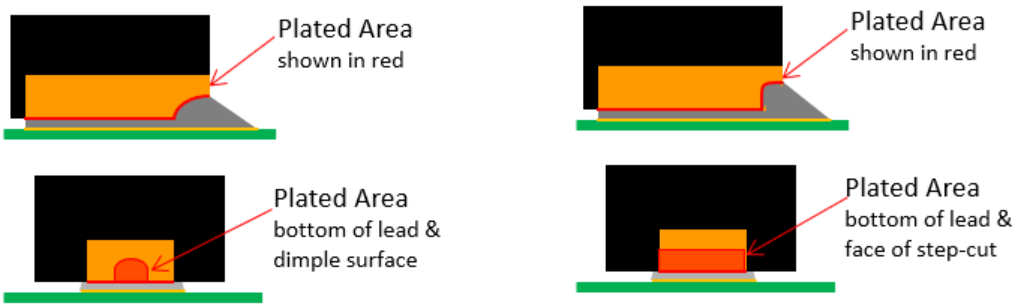
13.1.3 Package comparison

Table 7. Package comparison

Item	Dimple wettable flank	Step-cut wettable flank
Package size (x,y,z)	8x8x0.85 mm3	8x8x0.85 mm3

Table 7. Package comparison...*continued*

Item	Dimple wettable flank	Step-cut wettable flank
Package	QFN56 8*8	QFN56 8*8
Epoxy	EN4900G*	EN4900G*
Wire	AuPdCu Wire 1.3mil	AuPdCu Wire 1.3mil
Compound	CEL-9240HF10AN4	G700LA fine catalyst
Lead frame	PPF+RT	SN Plated
Wettable flank	Dimple solution	Step Cut
Part number	MC33FS85XXXXKS	MC33FS85XXXXES
MSL / Reflow ℃	3 / 260	3 / 260



13.2 Landing pad information

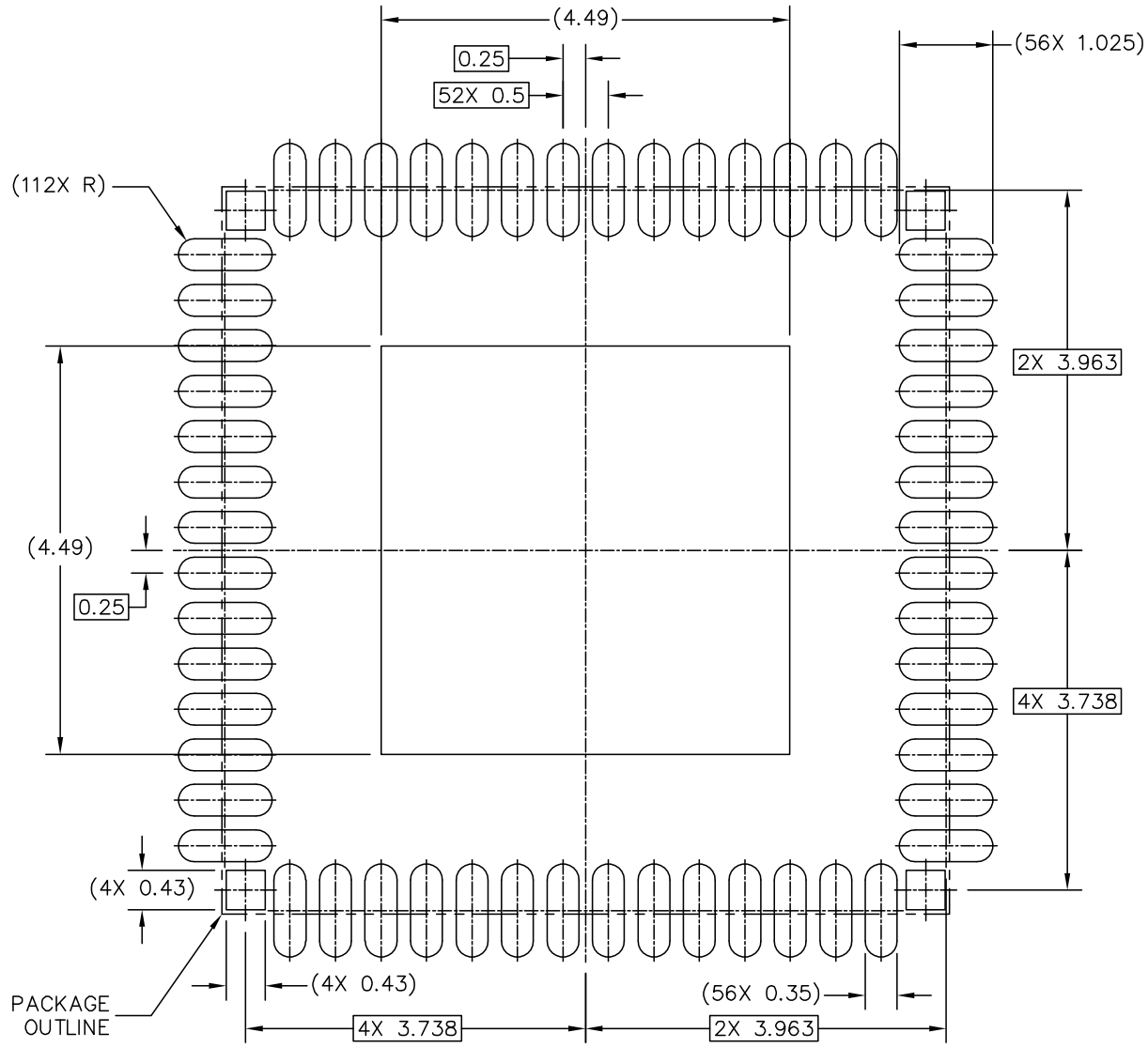


Figure 9. Solder mask pattern

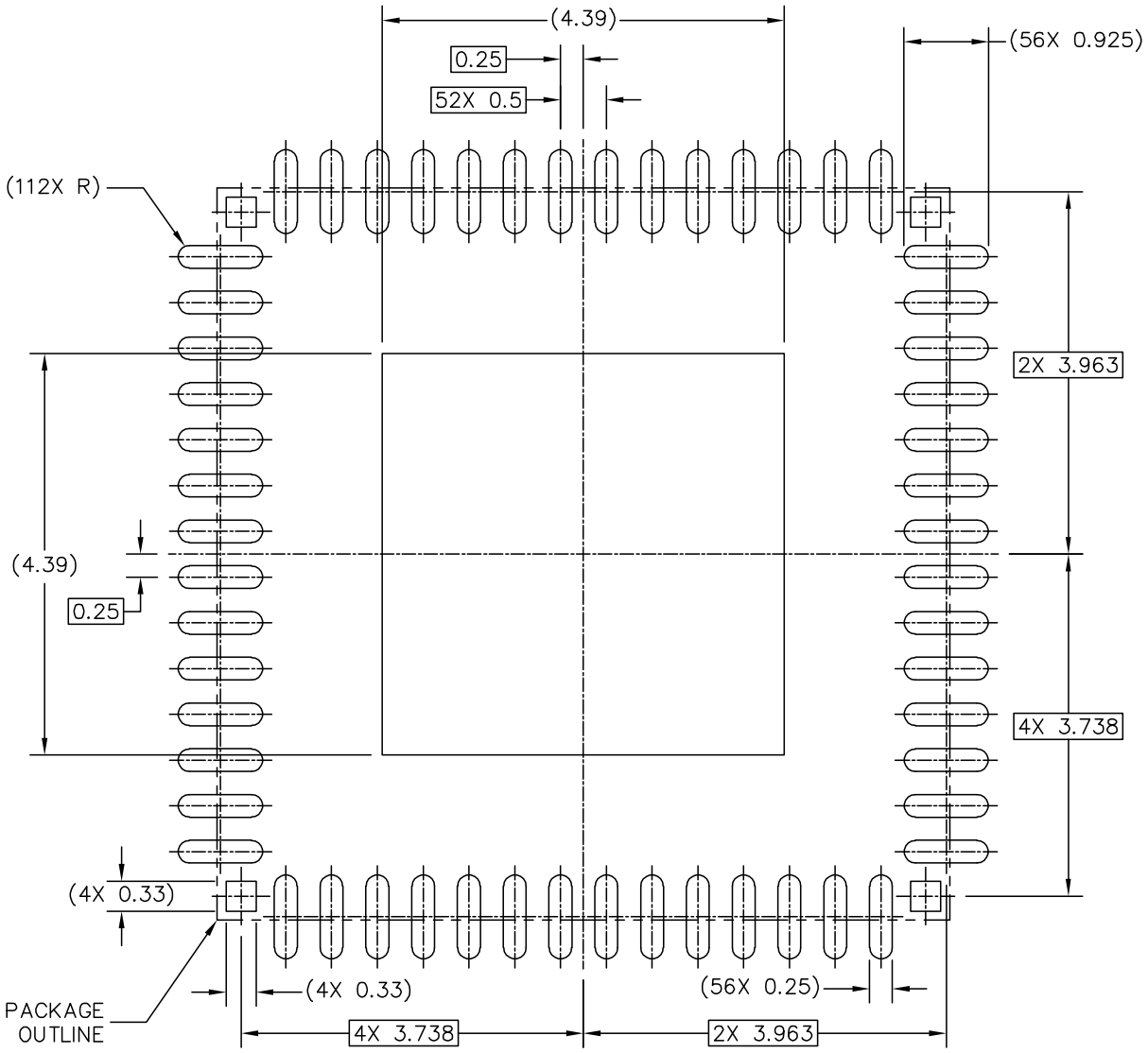


Figure 10. I/O pads and solderable area

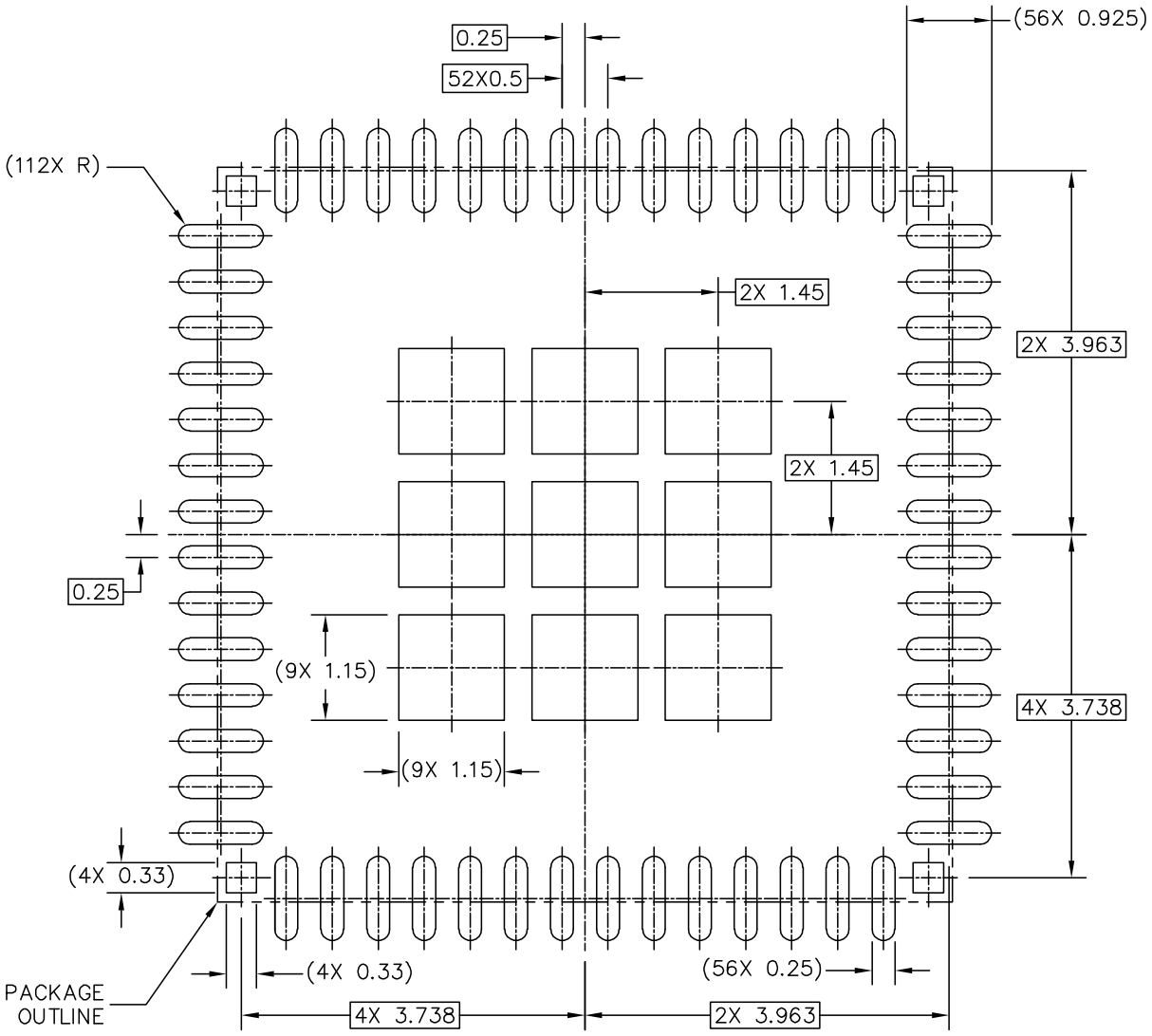


Figure 11. Solder paste stencil

14 References

[1] **FS8400** — Safety System Basis Chip for S32 Microcontrollers, fit for ASIL B
http://www.nxp.com/FS8400

[2] **FS8500** — Safety System Basis Chip for S32 Microcontroller, fit for ASIL D
http://www.nxp.com/FS8500

[3] **FS85_PDTCALC** — VPRE compensation network calculation and power dissipation tool (Excel file)
https://www.nxp.com/downloads/en/calculators/FS85-PDTCALC.xlsx

[4] **FS85_FMEDA** — FMEDA analysis [1]

[5] **FS85_VPRE_Simplis_Model** Simplis model for stability and transient simulations [1]

[6] **KITFS85FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS85FRDMEVM

[7] **KITFS85SKTEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS85SKTEVM

[8] **KITFS85AEEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS85AEEVM

[9] **AN12333** — FS84, FS85 product guidelines application note
https://www.nxp.com/webapp/sps/download/mod_download.jsp?colCode=AN12333

[10] **FS85_FS84_OTP_Config.xlsm** — OTP configuration file
https://www.nxp.com/webapp/Download?colCode=FS85-FS84-OTP

[11] **FS85_FS84SMUG** — Safety manual [1]

[12] **ES_FS84_FS85** — Errata sheet
https://www.nxp.com/webapp/Download?colCode=ES-FS84-FS85

[1] Contact NXP sales representative.

15 Legal information

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