



35FS4500, 35FS6500: ASIL B

Grade 0 safety power system basis chip with CAN FD transceiver

Rev. 2 — 14 April 2021

Product short data sheet

1 General description

The 35FS4500/35FS6500 ASIL B SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) transceiver, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32 μ A) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 1.5 A).

The 35FS4500/35FS6500 ASIL B includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL B).

The built-in CAN FD interface fulfills the ISO 11898-2⁽¹¹⁾ and -5⁽¹²⁾ standards.

High temperature capability up to $T_A = 150\text{ }^\circ\text{C}$ and $T_J = 175\text{ }^\circ\text{C}$, compliant with AEC-Q100 Grade 0 automotive qualification.

2 Features and benefits

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A or 1.5 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V, or 3.3 V
- Linear voltage regulator dedicated to MCU Analog/Digital (A/D) reference voltage or I/Os supply (V_{CCA}), 5.0 V, or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, IOs, LDT
- Five configurable I/Os

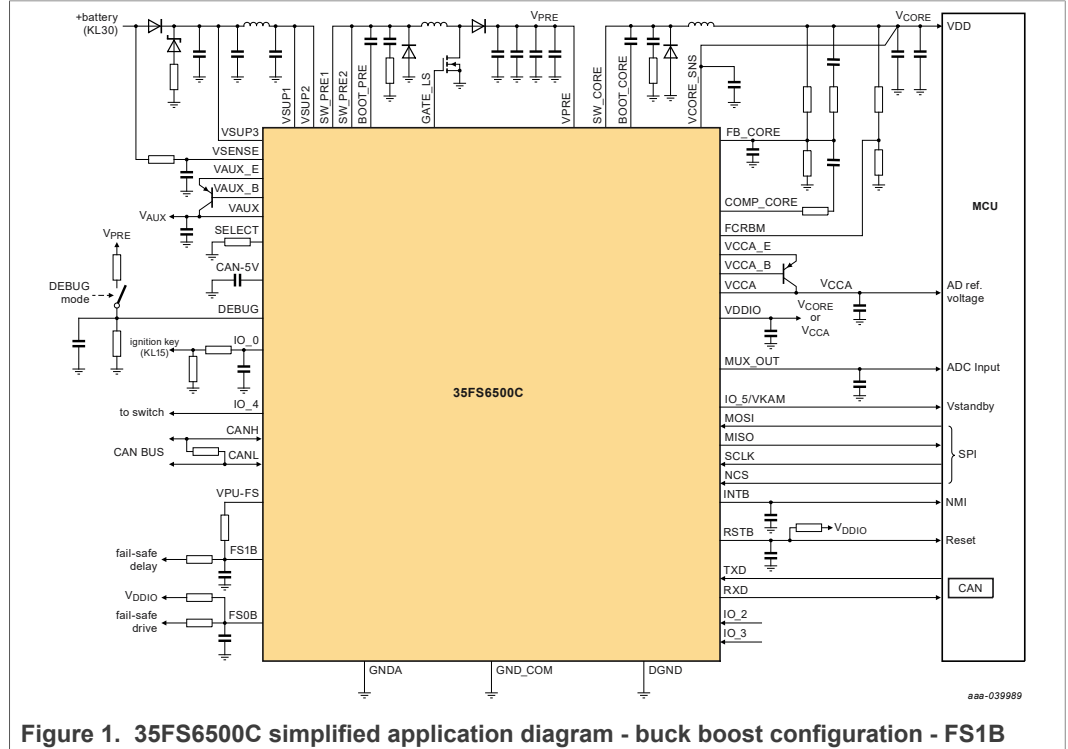
3 Applications

- T_A up to 150 $^\circ\text{C}$ and T_J up to 175 $^\circ\text{C}$
- Drive Train Electrification (BMS, Hybrid EV and HEV, Inverter, DC-DC, Alternator Starter)
- Drive Train - Chassis and Safety (Active Suspension, Steering, Safety Domain Gateway)
- Power Train (EMS, TCU, Gear Box)
- ADAS (LDW, Radar, Sensor Fusion Safety area)



- On board charger
- Motor control

4 Simplified application diagrams



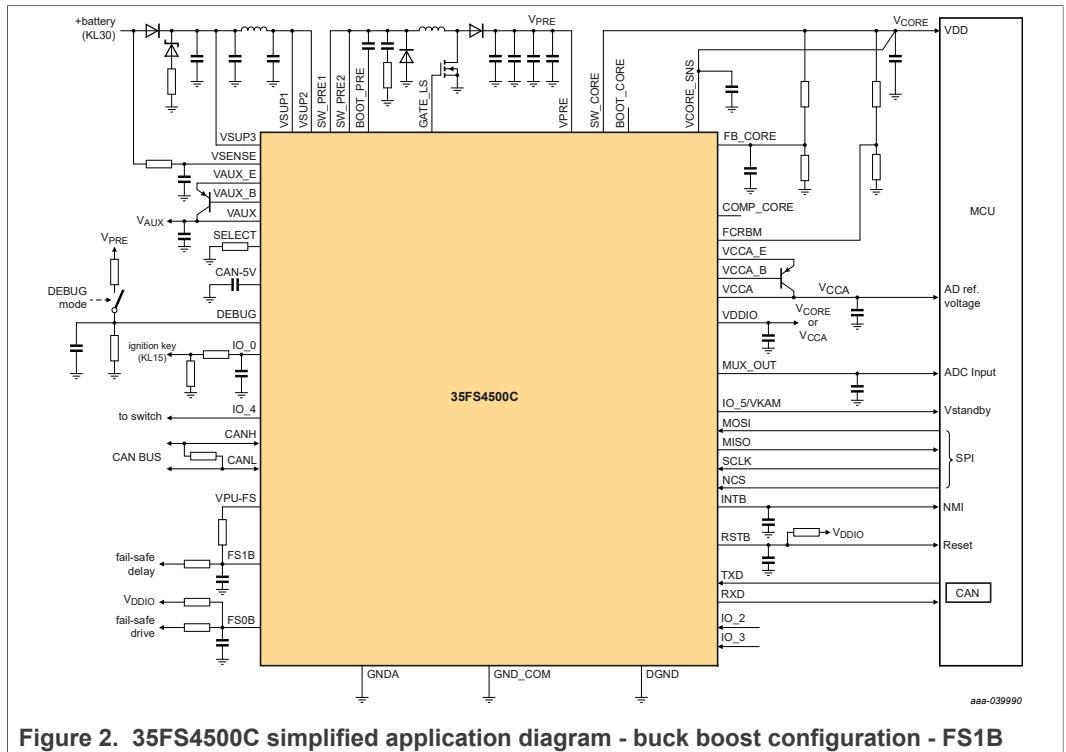


Figure 2. 35FS4500C simplified application diagram - buck boost configuration - FS1B

5 Ordering information

5.1 Part number definition

MC35FS c 5 x y z AE/R2

Table 1. Part number breakdown

Code	Option	Variable	Description
c	4 series	V _{CORE} type	Linear
	6 series		DC-DC
x	0	V _{CORE} current	0.5 A or 0.8 A
	1		1.5 A
y	5	Functions	None
	6		FS1B
	7		LDT
	8		FS1B and LDT
z	N	Physical interface	None
	C		CAN FD

5.2 Part numbers list

Table 2. Orderable part variations

Part Number	Temperature (T _A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM On	CAN FD	ASIL	Notes
MC35FS4505NAE	-40 °C to 150 °C	48-pin LQFP exposed pad	0	0	0.5 A	Linear	by SPI	0	B	[1]
MC35FS4505CAE			0	0	0.5 A	Linear	by SPI	1	B	
MC35FS4506NAE			1	0	0.5 A	Linear	by SPI	0	B	
MC35FS4506CAE			1	0	0.5 A	Linear	by SPI	1	B	
MC35FS4507NAE			0	1	0.5 A	Linear	by SPI	0	B	
MC35FS4507CAE			0	1	0.5 A	Linear	by SPI	1	B	
MC35FS4508NAE			1	1	0.5 A	Linear	by SPI	0	B	
MC35FS4508CAE			1	1	0.5 A	Linear	by SPI	1	B	
MC35FS6505NAE			0	0	0.8 A	DC-DC	by SPI	0	B	
MC35FS6505CAE			0	0	0.8 A	DC-DC	by SPI	1	B	
MC35FS6506NAE			1	0	0.8 A	DC-DC	by SPI	0	B	
MC35FS6506CAE			1	0	0.8 A	DC-DC	by SPI	1	B	
MC35FS6507NAE			0	1	0.8 A	DC-DC	by SPI	0	B	
MC35FS6507CAE			0	1	0.8 A	DC-DC	by SPI	1	B	
MC35FS6508NAE			1	1	0.8 A	DC-DC	by SPI	0	B	
MC35FS6508CAE			1	1	0.8 A	DC-DC	by SPI	1	B	
MC35FS6515NAE			0	0	1.5 A	DC-DC	by SPI	0	B	
MC35FS6515CAE			0	0	1.5 A	DC-DC	by SPI	1	B	
MC35FS6516NAE			1	0	1.5 A	DC-DC	by SPI	0	B	
MC35FS6516CAE			1	0	1.5 A	DC-DC	by SPI	1	B	
MC35FS6517NAE	0	1	1.5 A	DC-DC	by SPI	0	B			
MC35FS6517CAE	0	1	1.5 A	DC-DC	by SPI	1	B			
MC35FS6518NAE	1	1	1.5 A	DC-DC	by SPI	0	B			
MC35FS6518CAE	1	1	1.5 A	DC-DC	by SPI	1	B			

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Block diagram

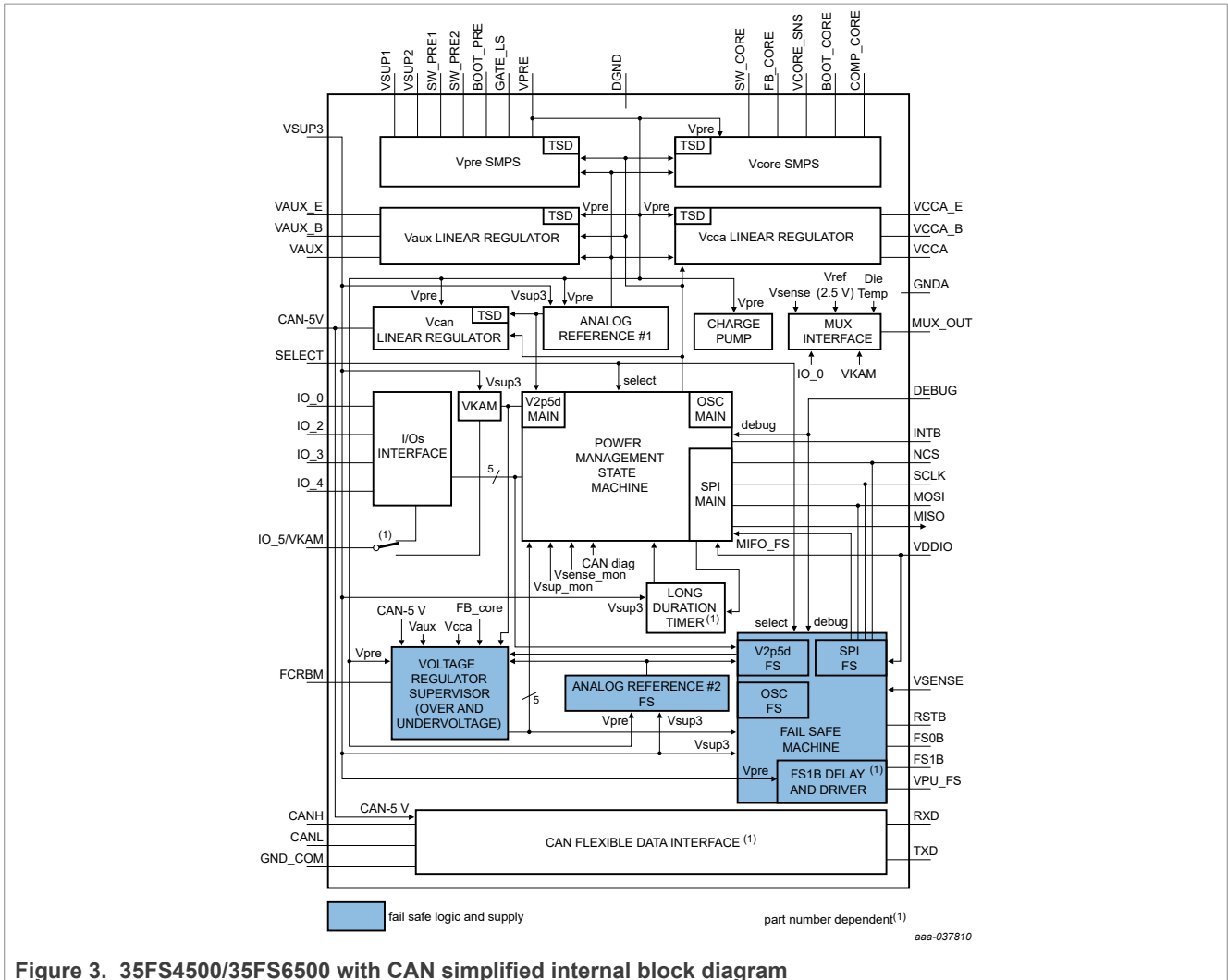
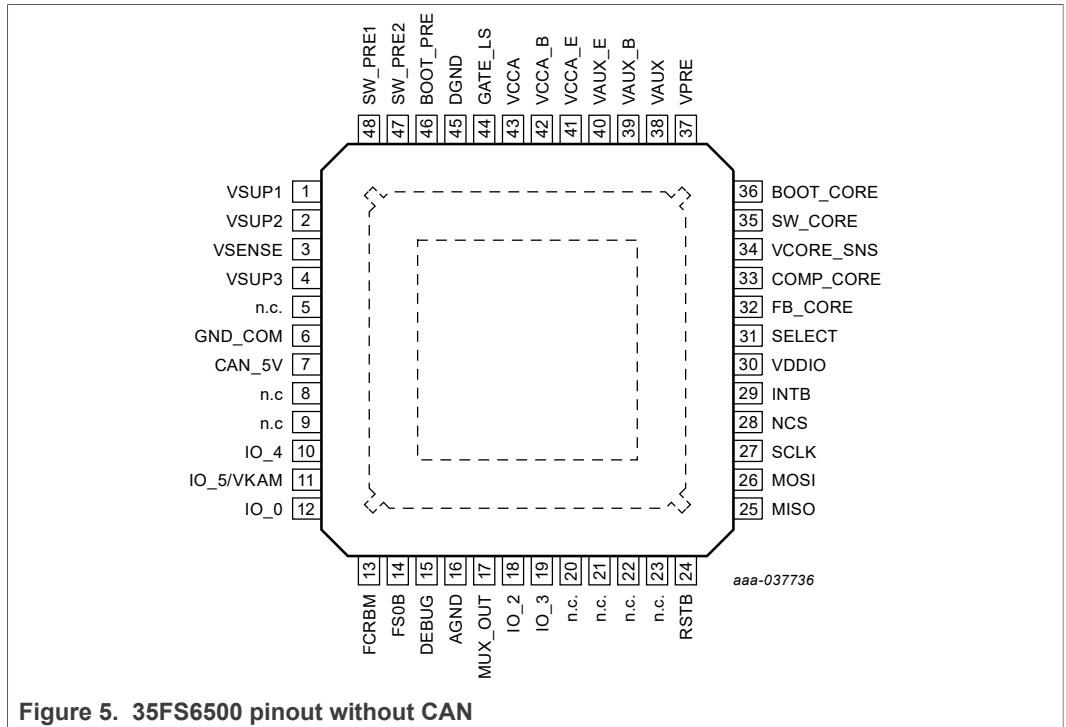
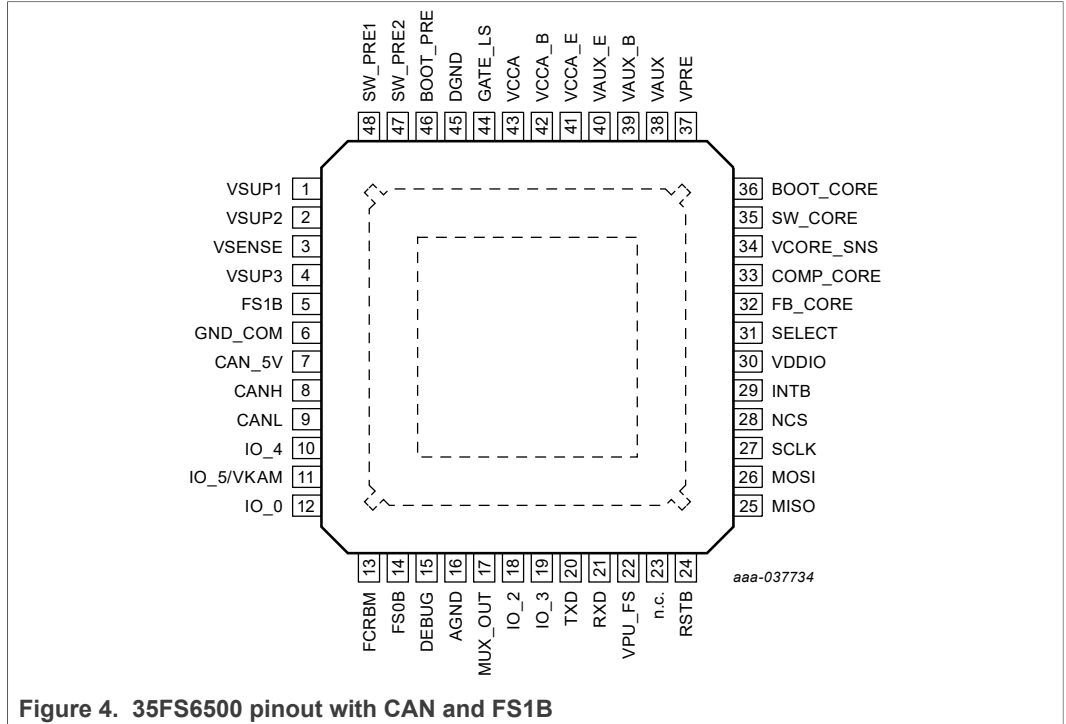


Figure 3. 35FS4500/35FS6500 with CAN simplified internal block diagram

7 Pinning information

7.1 Pinning information



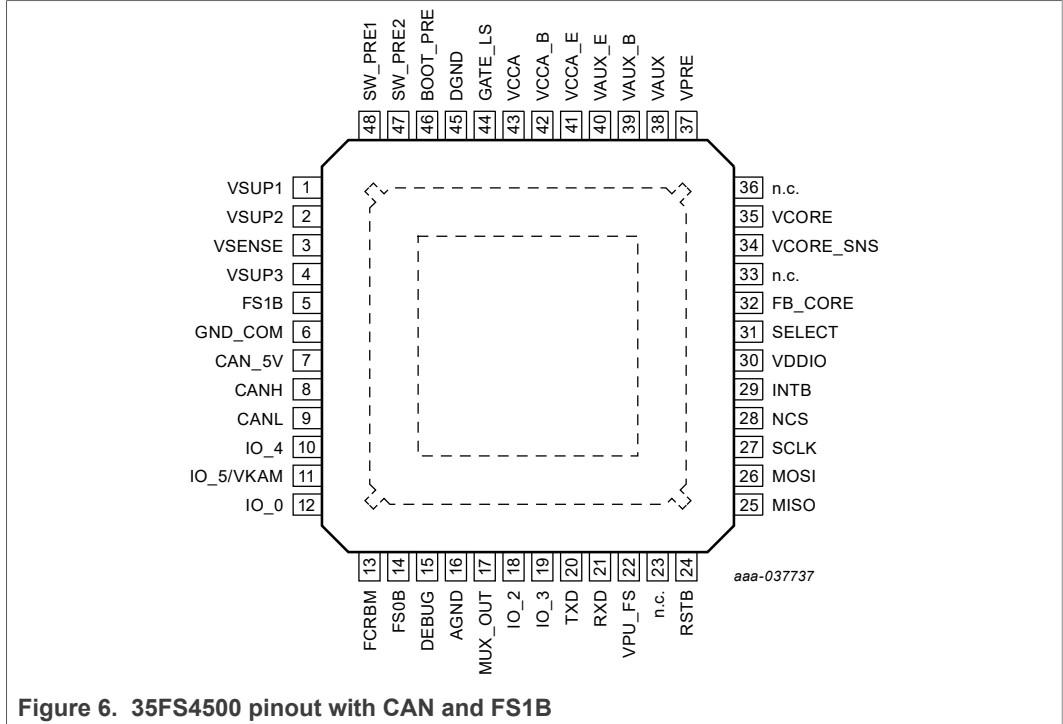


Figure 6. 35FS4500 pinout with CAN and FS1B

7.2 Pin description

A functional description of each pin can be found in the full data sheet.

Table 3. 35FS4500/35FS6500 pin definition

Pin number	Pin name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5	FS1B	D_OUT	Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure.
6	GND_COM	GROUND	Dedicated ground for physical layers
7	CAN_5V	A_OUT	Output voltage for the embedded CAN FD interface
8	CANH	A_IN/OUT	CAN output high. If CAN function is not used, this pin must be left open.
9	CANL	A_IN/OUT	CAN output low. If CAN function is not used, this pin must be left open.
10	IO_4	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver Digital input: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_5). Wake-up capability: Can be selectable to wake-up on edges or levels. Output gate driver: Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
11	IO_5/VKAM	A_IN D_IN A_OUT	Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. Analog input: Pin status can be read through the MUX output terminal Digital input: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_4). Wake-up capability: Can be selectable to wake-up on edges or levels. Supply output: Provide keep alive memory supply in low-power mode
12	IO_0	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) Analog input: Pin status can be read through the MUX output terminal Digital input: Pin status can be read through the SPI. Wake-up capability: Can be selectable to wake-up on edges or levels.
13	FCRBM	A_IN	Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V _{CORE} (in parallel to the one used to set the V _{CORE} voltage). If not used, this pin must be connected directly to FB_CORE.
14	FS0B	D_OUT	First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.

Table 3. 35FS4500/35FS6500 pin definition...continued

Pin number	Pin name	Type	Definition
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) Digital input: Pin status can be read through the SPI. Wake-up capability: Can be selectable to wake-up on edges or levels.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the CAN-bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open.
21	RXD	D_OUT	Receiver output which reports the state of the CAN-bus to the MCU If CAN function is not used, this pin must be left open.
22	VPU_FS	A_OUT	Pull-up output for FS1B function. If FS1B function is not used, this pin must be left open.
23	NC	N/A	Not connected. Pin must be left open.
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master input slave output
26	MOSI	D_IN	SPI bus. Master output slave input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	Not chip select (active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_OUT	Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC).
34	VCORE_SNS	A_IN	VCORE input voltage sense
35	SW_CORE	A_OUT	VCORE output switching point for FS6500 series
	or VCORE	A_OUT	VCORE output voltage for FS4500 series
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive For FS4500 series, this pin must be left open (NC).
37	VPRE	A_IN	VPRE input voltage sense
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection

Table 3. 35FS4500/35FS6500 pin definition...continued

Pin number	Pin name	Type	Definition
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for non-inverting buck-boost configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRES internal NMOS gate drive
47	SW_PRE2	A_OUT	Second pre-regulator output switching point
48	SW_PRE1	A_OUT	First pre-regulator output switching point

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V _{SUP1/2/3}	DC voltage at power supply pins	-1.0 to 40	V	[1]
V _{SENSE}	DC voltage at battery sense pin (with ext R in series mandatory)	-14 to 40	V	
V _{SW1,2}	DC voltage at SW_PRE1 and SW_PRE2 Pins	-1.0 to 40	V	
V _{PRE}	DC voltage at VPRES Pin	-0.3 to 8	V	
V _{GATE_LS}	DC voltage at Gate_LS pin	-0.3 to 8	V	
V _{BOOT_PRE}	DC voltage at BOOT_PRE pin	-1.0 to 50	V	
V _{SW_CORE}	DC voltage at SW_CORE pin	-1.0 to 8	V	
V _{CORE_SNS}	DC voltage at VCORE_SNS pin	0.0 to 8	V	
V _{BOOT_CORE}	DC voltage at BOOT_CORE pin	0.0 to 15	V	
V _{FB_CORE}	DC voltage at FB_CORE pin	-0.3 to 2.5	V	
V _{COMP_CORE}	DC voltage at COMP_CORE pin	-0.3 to 2.5	V	
V _{FCRBM}	DC voltage at FCRBM pin	-0.3 to 8	V	
V _{AUX_B,E}	DC voltage at VAUX_B, VAUX_E pins	-0.3 to 40	V	
V _{AUX}	DC voltage at VAUX pin	-2.0 to 40	V	
V _{VCCA_B,E}	DC voltage at VCCA_B, VCCA_E pins	-0.3 to 8	V	
V _{VCCA}	DC voltage at VCCA pin	-0.3 to 8	V	
V _{VDDIO}	DC voltage at VDDIO pin	-0.3 to 8	V	
V _{CAN_5V}	DC voltage on CAN_5V pin	-0.3 to 8	V	
V _{VPU_FS}	DC voltage at VPU_FS pin	-0.3 to 8	V	
V _{FSxB}	DC voltage at FS0B, FS1B pins (with ext R in series mandatory)	-0.3 to 40	V	
V _{DEBUG}	DC voltage at DEBUG pin	-0.3 to 40	V	
V _{IO_0,4}	DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)	-0.3 to 40	V	
V _{IO_5}	DC voltage at IO_5 pin	-0.3 to 20	V	
V _{VKAM}	DC voltage at VKAM pin	-0.3 to 8	V	

Table 4. Maximum ratings ...continued

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
V _{DIG}	DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3 pins	-0.3 to 8	V	
V _{SELECT}	DC voltage at SELECT pin	-0.3 to 8	V	
V _{BUS_CAN}	DC voltage on CANL, CANH pins	-27 to 40	V	
I _{Isense}	V _{SENSE} maximum current capability	-5.0 to 5.0	mA	
I _{IO_{0, 4, 5}}	IOs maximum current capability (IO_0, IO_4, IO_5)	-5.0 to 5.0	mA	
ESD voltage				
Human body model (JESD22/A114)⁽¹⁸⁾ – 100 pF, 1.5 kΩ				
V _{ESD-HBM1}	• All pins	±2.0	kV	[2]
V _{ESD-HBM2}	• VSUP1, 2, 3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG	±4.0	kV	
V _{ESD-HBM3}	• CANH, CANL	±6.0	kV	
Charge device model (JESD22/C101)⁽¹⁹⁾:				
V _{ESD-CDM1}	• All pins	±500	V	
V _{ESD-CDM2}	• Corner pins	±750	V	
System level ESD (gun test)				
	• VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B			
V _{ESD-GUN1}	330 Ω/150 pF unpowered according to IEC 61000-4-2: ⁽¹⁵⁾	±8.0	kV	
V _{ESD-GUN2}	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±8.0	kV	
V _{ESD-GUN3}	2.0 kΩ/150 pF unpowered according to ISO 10605 ⁽¹⁴⁾	±8.0	kV	
V _{ESD-GUN4}	2.0 kΩ/330 pF powered according to ISO 10605 ⁽¹⁴⁾	±8.0	kV	
	• CANH, CANL			
V _{ESD-GUN5}	330 Ω/150 pF unpowered according to IEC 61000-4-2: ⁽¹⁵⁾	±15.0	kV	
V _{ESD-GUN6}	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±12.0	kV	
V _{ESD-GUN7}	2.0 kΩ/150 pF unpowered according to ISO 10605 ⁽¹⁴⁾	±15.0	kV	
V _{ESD-GUN8}	2.0 kΩ/330 pF powered according to ISO 10605 ⁽¹⁴⁾	±12.0	kV	
Thermal ratings				
T _A	Ambient temperature	-40 to 150	°C	
T _J	Junction temperature	-40 to 175	°C	
T _{STG}	Storage temperature	-55 to 150	°C	
Thermal resistance				
R _{θJA}	Thermal resistance junction to ambient	30	°C/W	[3]
R _{θJCTOP}	Thermal resistance junction to case top	23.8	°C/W	[4]
R _{θJCBOTTOM}	Thermal resistance junction to case bottom	0.9	°C/W	[5]

[1] All V_{SUPS} (V_{SUP1/2/3}) must be connected to the same supply (Figure 1).

[2] Compared to AGND.

[3] Per JEDEC JESD51-6⁽¹⁶⁾ with the board (JESD51-7)⁽¹⁷⁾ horizontal.

[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1)⁽²⁰⁾.

[5] Thermal resistance between the die and the solder pad on the bottom of the packaged based on simulation without any interface resistance.

9 Packaging

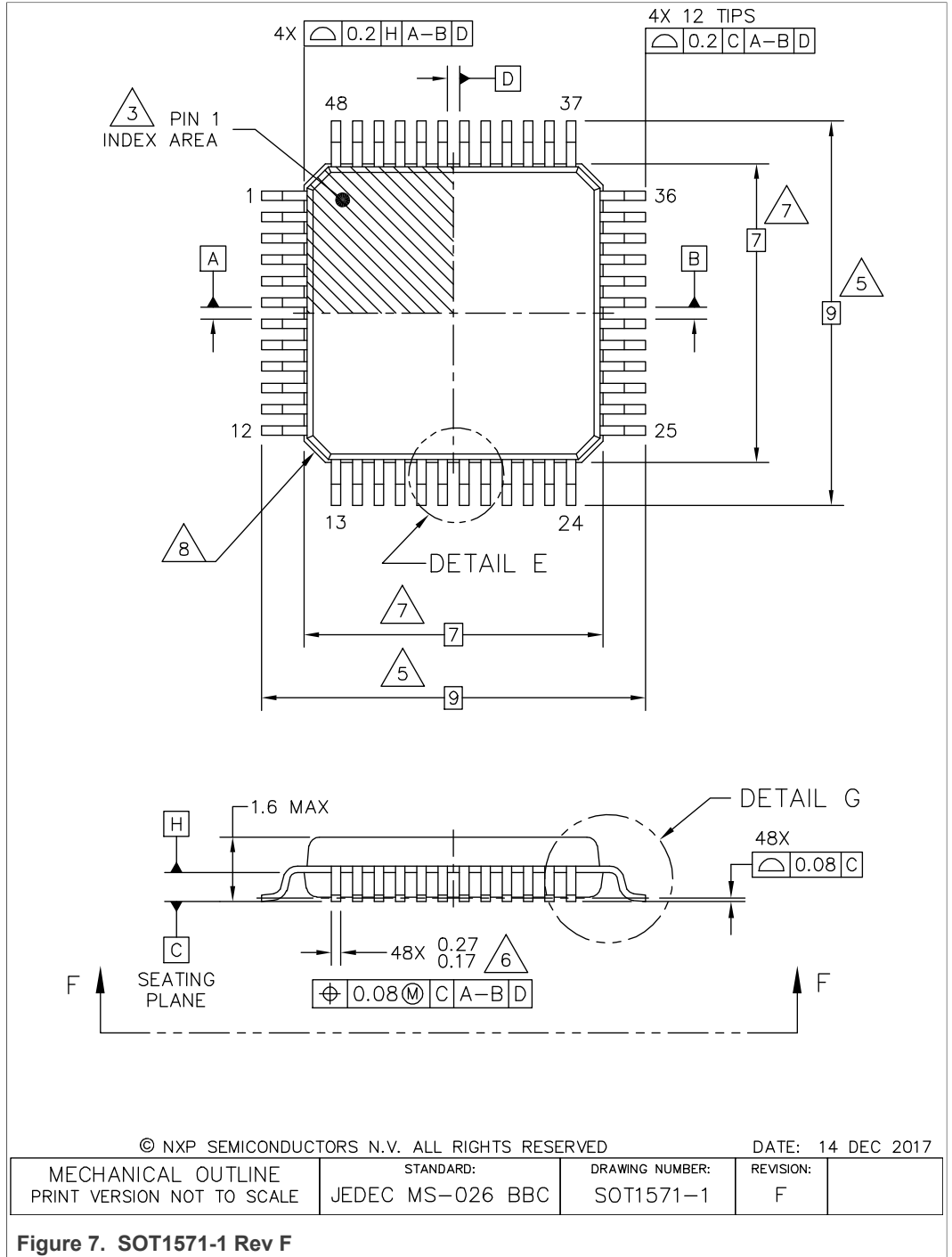
9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 5. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48-Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00173D

9.2 Package outline



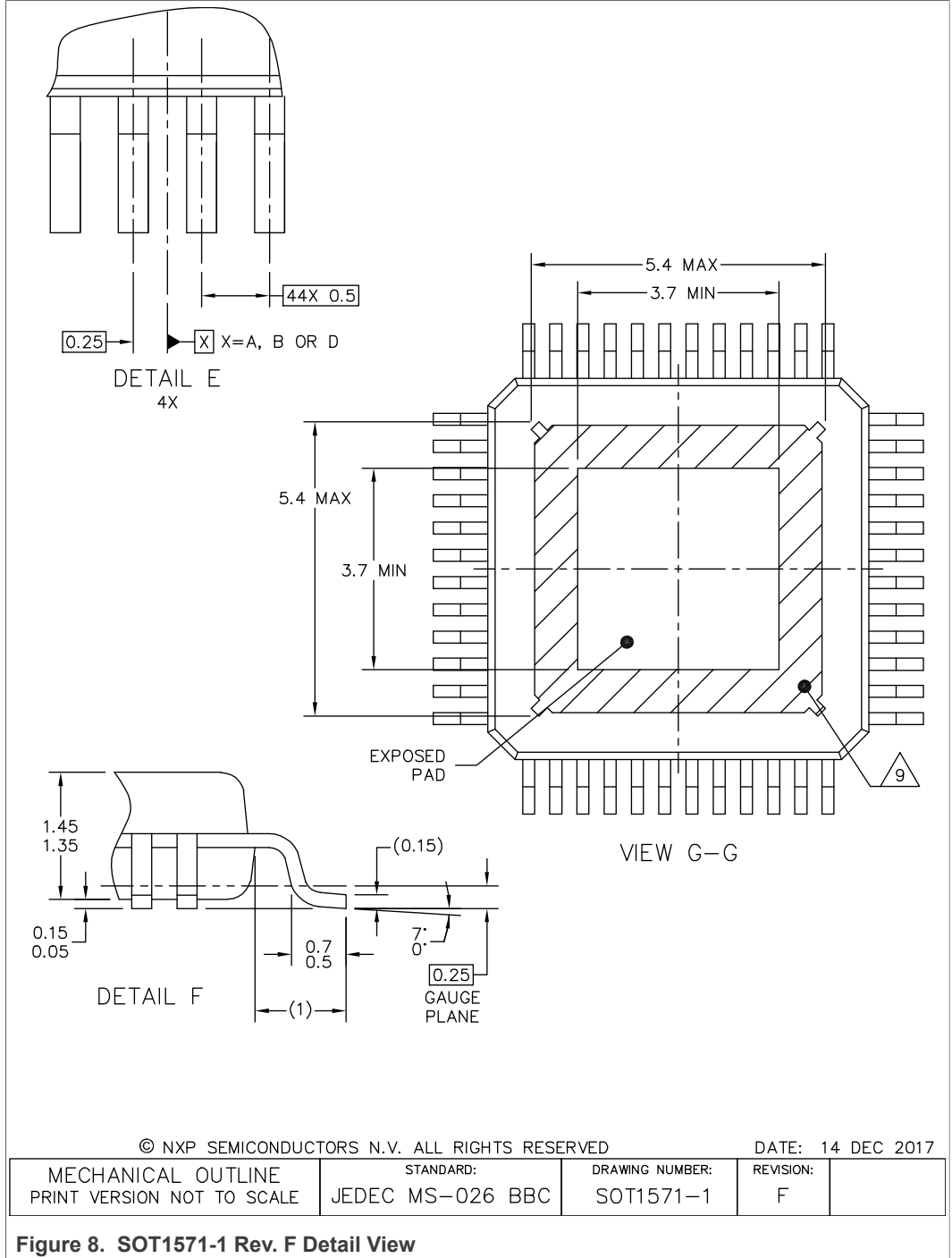
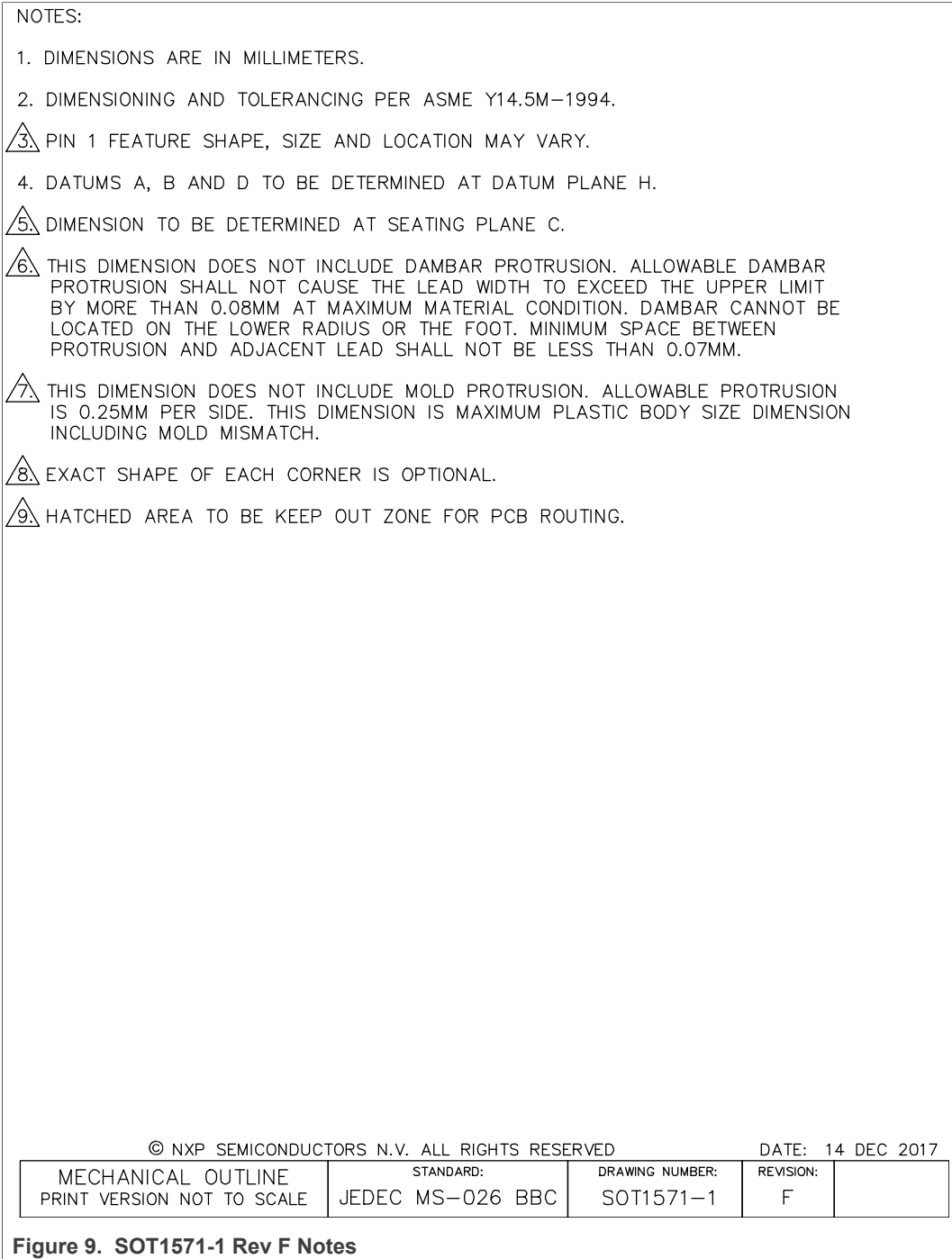
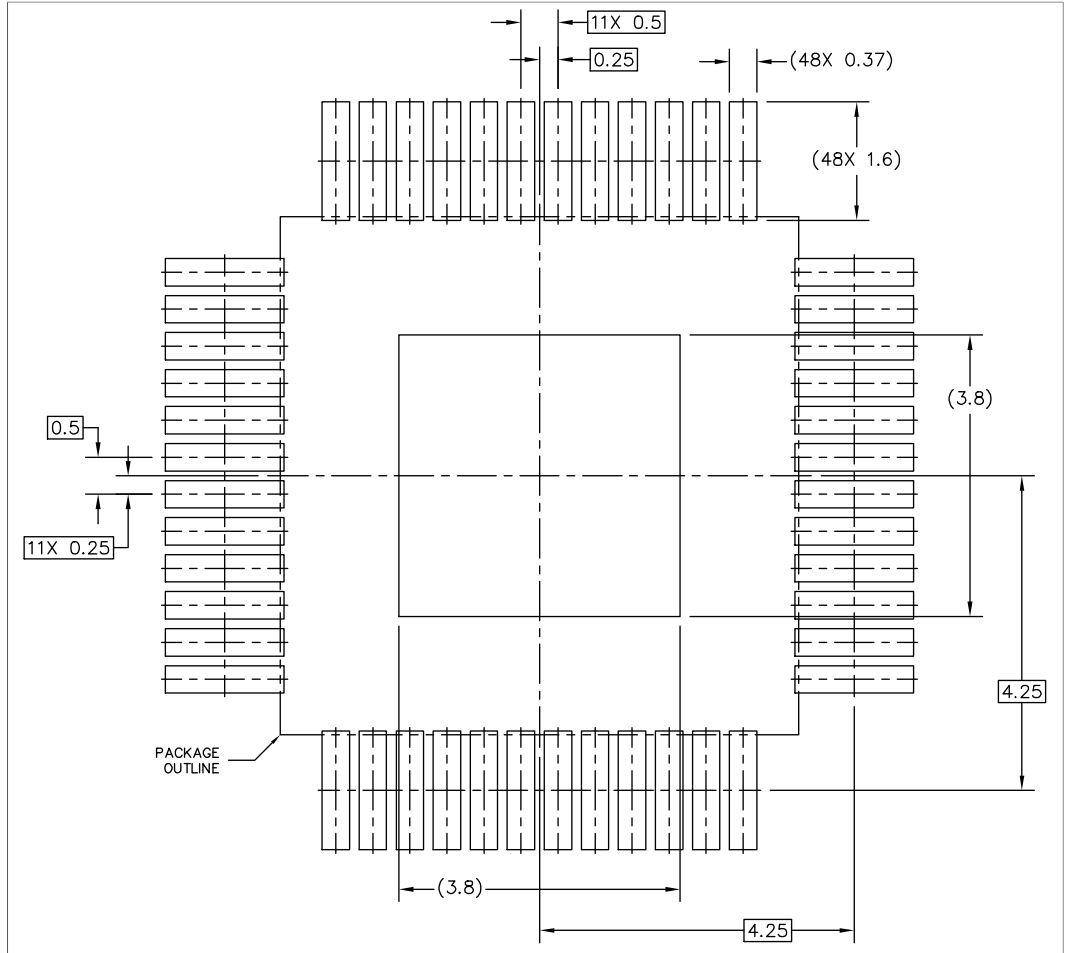


Figure 8. SOT1571-1 Rev. F Detail View



10 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

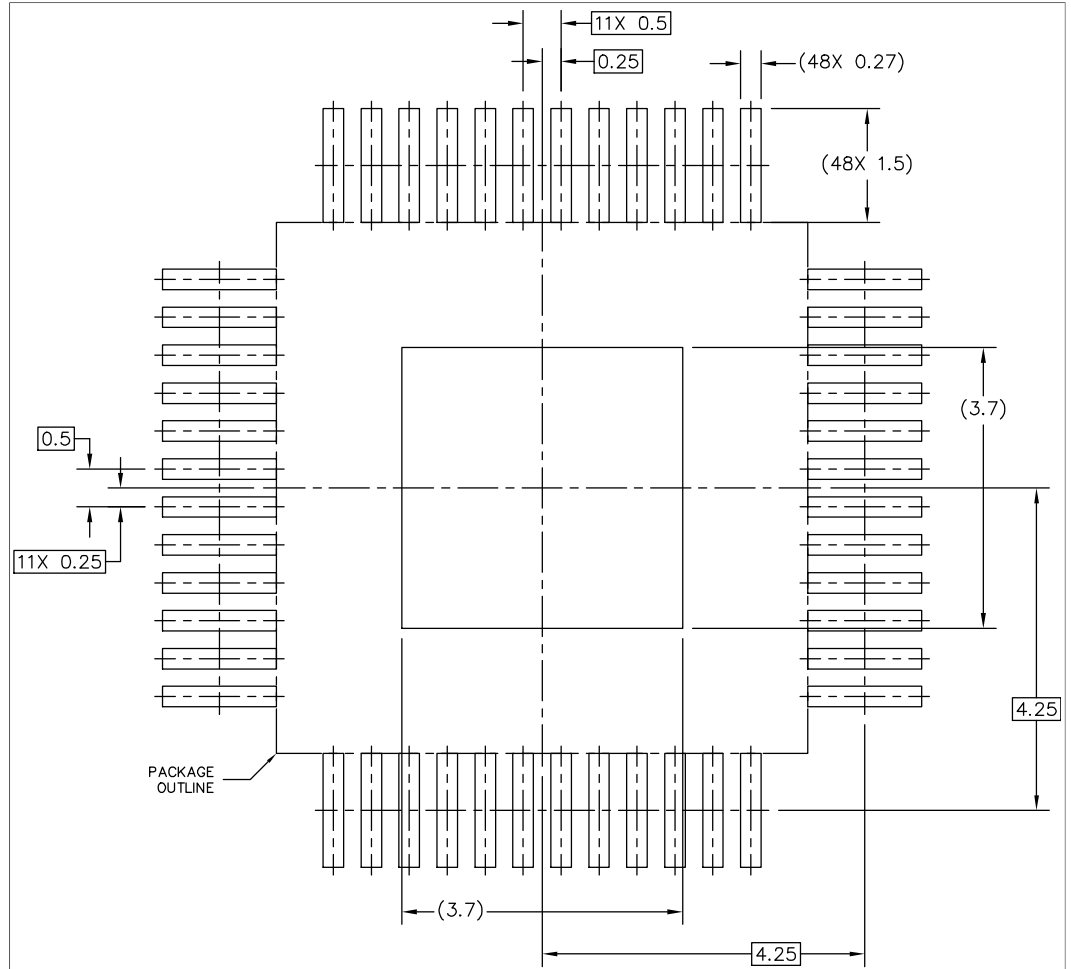
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F
--	-------------------------------	------------------------------	----------------

Figure 10. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

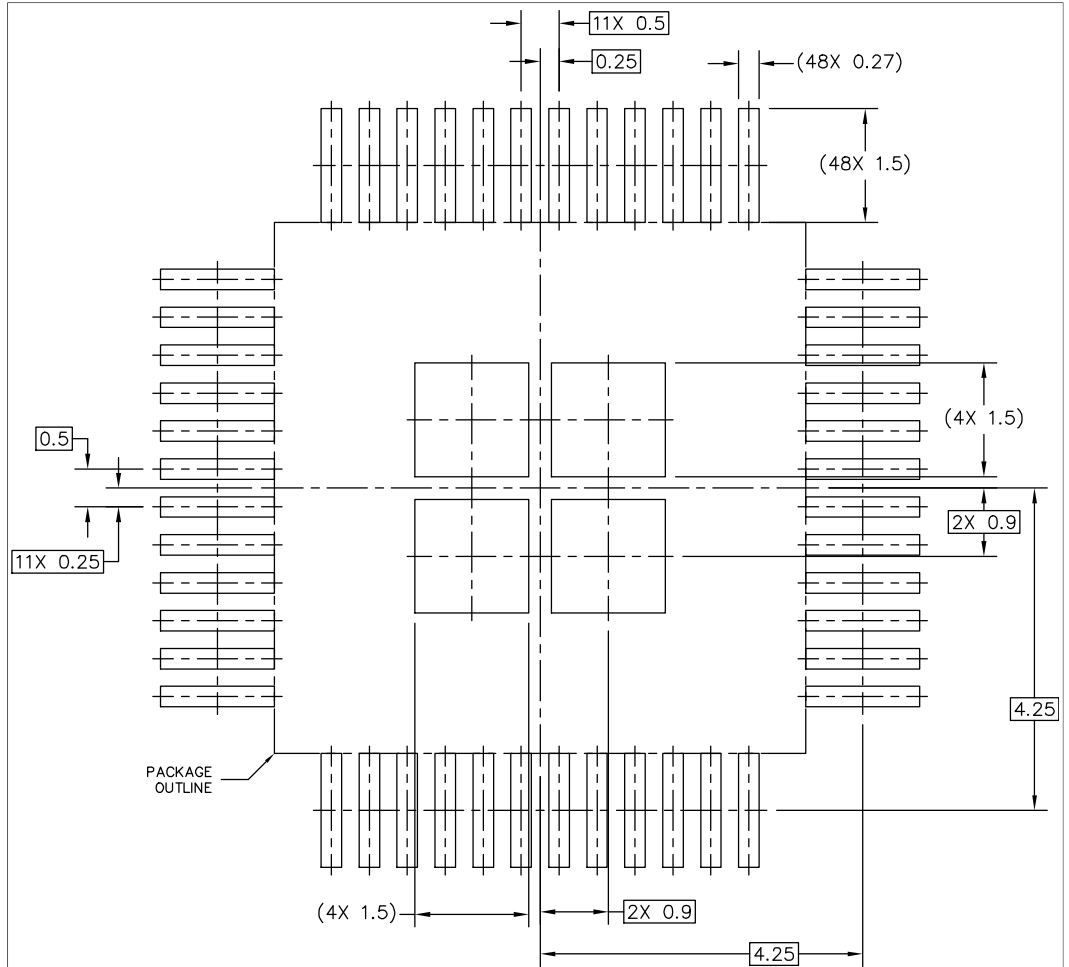
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
--	-------------------------------	------------------------------	----------------	--

Figure 11. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-1	REVISION: F	
--	-------------------------------	------------------------------	----------------	--

Figure 12. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil

11 References

Obtain additional information on related NXP products and application solutions through the documents and URLs listed below.

- (1) **AN5238** - FS6500 and FS4500 Safe System Basis Chip Hardware Design and Product Guidelines - Application Note
<https://www.nxp.com/AN5238-DOWNLOAD>
- (2) **AN4388** - Quad Flat Package (QFP)
https://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
- (3) **FS6500-FS4500PDTCALC** - Power dissipation tool (Excel File)
https://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx
- (4) **V_{CORE} compensation network simulation tool (CNC)**^[1]
- (5) **FMEDA** - FS6500/FS4500 ASILB Grade 0 FMEDA^[1]
- (6) **UM11548** - 35FS4500/35FS6500 functional safety manual – ASIL B – Safety manual
- (7) **KITFS4508CAEEVM** - FS4508, System Basis Chip, ASIL B, Linear 0.5 A Vcore, FS1b, LDT, CAN
<https://www.nxp.com/KITFS4508CAEEVM>
- (8) **FS6500 product summary page** - <https://www.nxp.com/FS6500>
- (9) **FS4500 product summary page** - <https://www.nxp.com/FS4500>
- (10) **Analog power management homepage** - <https://www.nxp.com/products/power-management>
- (11) **ISO 11898-2:2003** - Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit
<https://www.iso.org/standard/33423.html>
- (12) **ISO 11898-5:2007** - Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode
<https://www.iso.org/contents/data/standard/04/12/41284.html>
- (13) **ISO 7637-2:2011** - Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only
<https://www.iso.org/standard/50925.html>
- (14) **ISO 10605:2008** - Road vehicles — Test methods for electrical disturbances from electrostatic discharge
<https://www.iso.org/standard/41937.html>
- (15) **IEC 61000-4-2:2008** - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
<https://webstore.iec.ch/publication/4189>
- (16) **JESD51- 6** - INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR)
- (17) **JESD51-7** - HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES
- (18) **JESD22-A114F** - ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)
- (19) **JESD22-C101F** - FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS
- (20) **MIL-STD-883-1, Method 1012.1** - TEST METHOD STANDARD MICROCIRCUITS

[1] Available upon request.

12 Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Supersedes
35FS4500-35FS6500SDS-ASILB v.2.0	20210414	Product	35FS4500-35FS6500SDS-ASILB v.1.0
Modifications	<ul style="list-style-type: none"> • Section 1: replaced "0.8 A" by "1.5 A" • Section 2: replaced "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A) or LDO (0.5 A)" to "Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A to 1.5 A) or LDO (0.5 A)" • Section 5: updated Table 1 and Table 2 (added new part numbers) 		
35FS4500-35FS6500SDS-ASILB v.1.0	20210105	Product	—
Modifications	<ul style="list-style-type: none"> • Initial release 		

13 Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

13.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL-classified accordingly. If

this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

SafeAssure — is a trademark of NXP B.V.

Tables

Tab. 1.	Part number breakdown	3	Tab. 4.	Maximum ratings	10
Tab. 2.	Orderable part variations	4	Tab. 5.	Package mechanical dimensions	12
Tab. 3.	35FS4500/35FS6500 pin definition	8	Tab. 6.	Revision history	20

Figures

Fig. 1.	35FS6500C simplified application diagram - buck boost configuration - FS1B	2	Fig. 7.	SOT1571-1 Rev F	13
Fig. 2.	35FS4500C simplified application diagram - buck boost configuration - FS1B	3	Fig. 8.	SOT1571-1 Rev. F Detail View	14
Fig. 3.	35FS4500/35FS6500 with CAN simplified internal block diagram	5	Fig. 9.	SOT1571-1 Rev F Notes	15
Fig. 4.	35FS6500 pinout with CAN and FS1B	6	Fig. 10.	SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern	16
Fig. 5.	35FS6500 pinout without CAN	6	Fig. 11.	SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area	17
Fig. 6.	35FS4500 pinout with CAN and FS1B	7	Fig. 12.	SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil	18