MC56F836XXDS

MC56F836xx

Supports MC56F836xx

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. On a single chip, each device combines the processing power of a DSP and the functionality of an MCU, with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - General-purpose inverters
  - Smart sensors, fire and security systems
  - Switched-mode power supply and power management
  - Power distribution systems
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Uninterruptible power supplies (UPS)
  - Solar inverter
  - Medical monitoring applications
- DSC based on 32-bit 56800EX core
  - Up to 100 MIPS at 100 MHz core frequency
  - DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - Up to 2×128 KB dual partition flash memory with ECC protection
  - Up to 64 KB data/program RAM
  - Both on-chip flash memory and RAM can be mapped into both program and data memory spaces
  - 32 KB boot ROM supports boot from SCI, I2C and CAN
- Analog
  - Two high-speed, 8-ch external and 2-ch internal, 12-bit ADCs with dynamic x1, x2, and x4 programmable amplifier
  - Four analog comparators with integrated 8-bit DAC references
- Two standard FlexPWM modules with up to 2x8 PWM outputs
- Communication interfaces
  - Up to three high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to two queued SPI (QSPI) modules
  - Two I2C/SMBus ports
  - One FlexCAN module, with Flexible Data-rate (CAN-FD) supported
  - One USB2.0 controller with integrated PHY
- Timers
  - Two 16-bit quad timer (2 x 4 16-bit timer)
  - Two Periodic Interval Timers (PITs)
- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Windowed Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)
- Clocks
  - On-chip relaxation oscillators: 200 kHz, and 48 MHz IRC
  - Crystal / resonator oscillator
- System
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-Module Crossbar and Event Generator
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging
- Operating characteristics
  - Single supply: 2.7 V to 3.6 V
  - 5 V–tolerant I/O (except for 3.3 V RESETB and USB_DP/USB_DM pins)
  - Operation ambient temperature: V temperature option: -40°C to 105°C
- 100-pin LQFP, 80-pin LQFP, and 64-pin LQFP packages

Table of Contents

1 Overview

1.1 Product Family

The following table lists major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. MC56F836xx Family

Feature	MC56F83			
	689	686	683	663
Core frequency (MHz)	100			
Flash memory (KB)	256	256	256	128
RAM (KB)	64	64	64	48
ROM (KB)	32			
Inter-module Xbar	Yes			
Event Generator	4			
Windowed Watchdog	1			
External Watchdog Monitor	1			
eDMA	4-Ch			
Internal OSC	200 kHz / 48 MHz			
External Crystal Oscillator	Yes (4 MHz ~ 16 MHz)			
Comparator	4			
Cyclic ADC channels (External + Internal)	2 x (8+2)			
Standard PWM	2 x 8	2 x 8 [1]	1 x 8 + 1 x 6 [2]	
Timers	2 x 4			
Periodic Interval Timers	2			
CAN-FD	1			
I2C/SMBus	2			
QSCI	3	3	2	
QSPI	2	2	1	
USB 2.0 FS/LS	1	—		
GPIO	82	68	54	
Operating Temperature	105℃			
LQFP package pin count	100 LQFP	80 LQFP	64 LQFP	

1. The outputs of PWMB_3A and PWMB_3B are available through the on-chip inter-module crossbar (XBAR).
2. The outputs of PWMB are available through XBAR. PWMA_3A/PWMB_3B coupled with XB_OUT10/XB_OUT11.

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 100 MHz operation mode
- Operation ambient temperature:

-40 ºC to 105ºC
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.5 Peripheral highlights

1.5.1 Flex Pulse Width Modulator (FlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWMA with accumulative fractional clock calculation
  - Arbitrary PWM edge placement
- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:

    - Channels not used for PWM generation can be used for buffered output compare functions.
    - Channels not used for PWM generation can be used for input capture functions.
    - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers
- Direct phase shift controls among each submodule
- Trigger signal can share the same load frequency as reload signal in each submodule

1.5.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
    - 2 x 8-channel external inputs
    - Built-in x1, x2, x4 programmable gain pre-amplifier
    - Maximum ADC clock frequency up to 25 MHz, having period as low as 40 ns
    - Single conversion time of 10 ADC clock cycles
    - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential (including unipolar differential) conversions
- Sequential and parallel scan modes. Parallel mode includes simultaneous and independent scan modes.
- Samples of each ADC have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for hardware-triggering and software-triggering conversions

- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.5.3 Periodic Interrupt Timer (PIT) Modules

- 16-bit counter with programmable count modulo
- PIT0 is master and PIT1 is slave (if synchronizing both PITs)
- The output signals of both PIT0 and PIT1 are internally connected to a peripheral crossbar module
- Can run when the CPU is in Wait/Stop modes. Can also wake up the CPU from Wait/Stop modes.
- In addition to its existing bus clock (up to 100 MHz), 3 alternate clock sources for the counter clock are available:
  - Crystal oscillator output
  - 48 MHz/6
  - On-chip low-power 200 kHz oscillator

1.5.4 Inter-Module Crossbar and Event Generator (EVTG) logic

- Provides generalized connections between and among on-chip peripherals: ADCs, comparators, quad-timers, FlexPWMs, EWM, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- The EVTG module mainly includes two parts: Two AND/OR/INVERT (known simply as the AOI) modules and one configurable Flip-Flop. It supports the generation of a configurable number of EVENT signals. The inputs are from crossbar (XBAR) outputs, and the outputs feed to XBAR inputs.

1.5.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 8-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.5.6 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.5.7 Queued Serial Communications Interface (QSCI) modules with LIN Slave Functionality

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Support for Local Interconnect Network (LIN) slave operation

1.5.8 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 25 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as the maximum Baud rate / 4096
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB or LSB as first bit transmitted)

1.5.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard

- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter

1.5.10 Flexiable Controller Area Network (FlexCAN) module

This device utilizes the FlexCAN which is configured with 32 message buffers and DMA support as well as CAN-FD (Flexible Data-rate). The FlexCAN module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The interface between CAN engine and CPU is done via a mailbox system (Message Buffers) stored in embedded RAM.

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B
- Supports DMA request
- Flexible message buffers (MBs), totaling 32 message buffers of 8 bytes data length each, configurable as Rx or Tx
- SRAM array for 32 message buffer and individual mask registers.

1.5.11 Universal Serial Bus (USB) 2.0 controller

- Low Speed (1.5 Mbit/s) / Full Speed (12 Mbit/s)
- Device mode only in this device
- IRC48M with clock recovery block to eliminate the on-board crystal
- USB1.1 PHY included

1.5.12 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator
  - On-chip low-power 200 kHz oscillator

    - System bus (IPBus up to 100 MHz)
    - 48 MHz/6
- Support for interrupt generation

1.5.13 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
    - External crystal oscillator
    - On-chip low-power 200 kHz oscillator
    - System bus (IPBus up to 100 MHz)
    - 48 MHz/6

1.5.14 Power supervisor

- Power-on reset (POR) is released after VDD > 2.7 V during supply is ramped up; CPU, peripherals, and JTAG/EOnCE controllers exit RESET state
- Brownout reset (V_{DD} < 2.0 V)
- Critical warn low-voltage interrupt (LVI 2.2 V)
- Peripheral low-voltage warning interrupt (LVI 2.7 V)

1.5.15 Phase-locked loop

- Output frequency range is optimized from 150 MHz to 450 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.5.16 Clock sources

1.5.16.1 On-chip oscillators

- IRC48M
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.5.16.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.5.17 Cyclic Redundancy Check (CRC) generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.5.18 General Purpose I/O (GPIO)

- 5 V tolerance (except RESETB and USB_DP/USB_DM pins)
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG, RESETB and USB_DP/USB_DM pins) default to be GPIO inputs
- 2 mA / 9 mA capability
- Controllable output slew rate

1.6 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

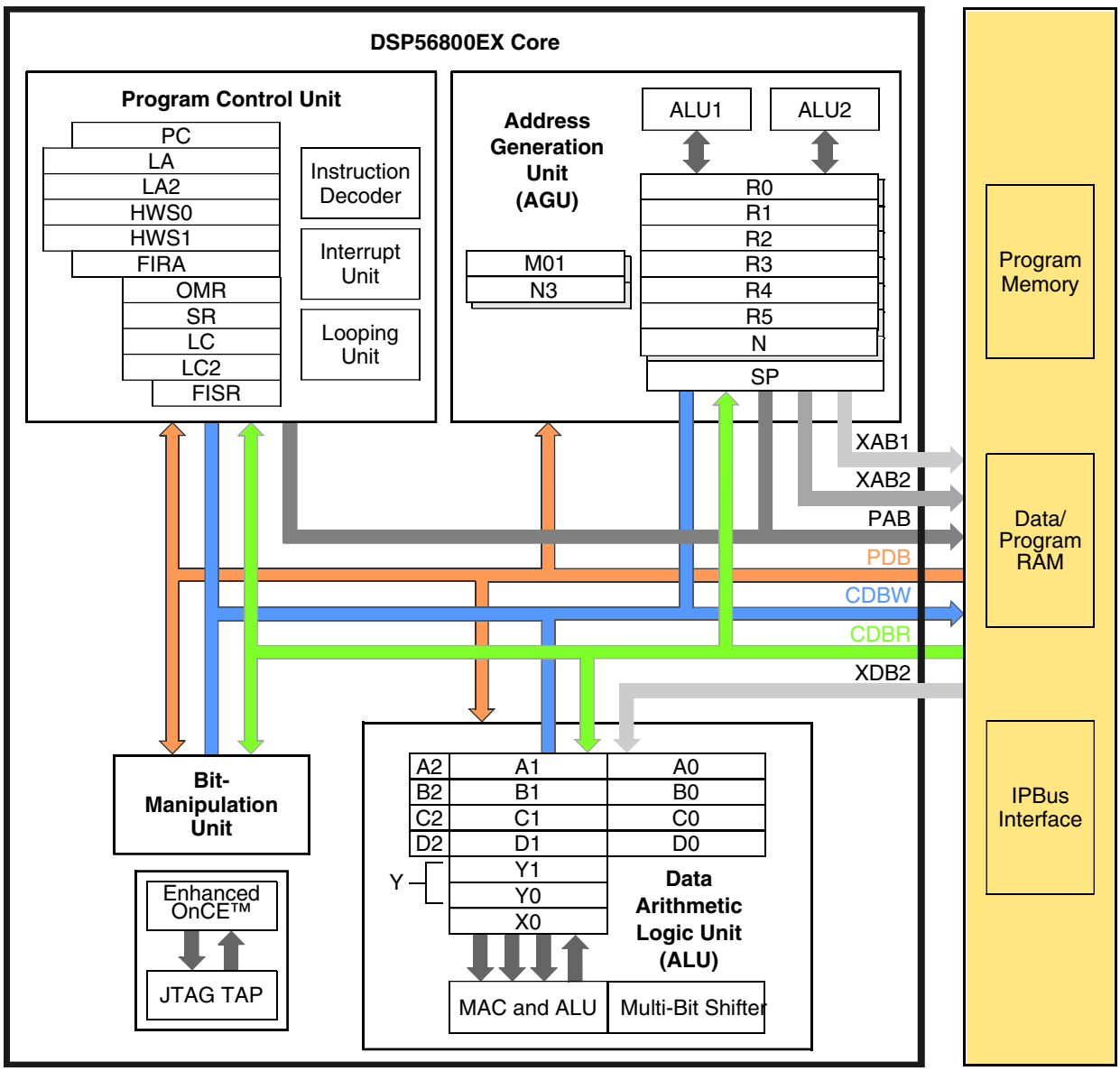


Figure 1. 56800EX basic block diagram

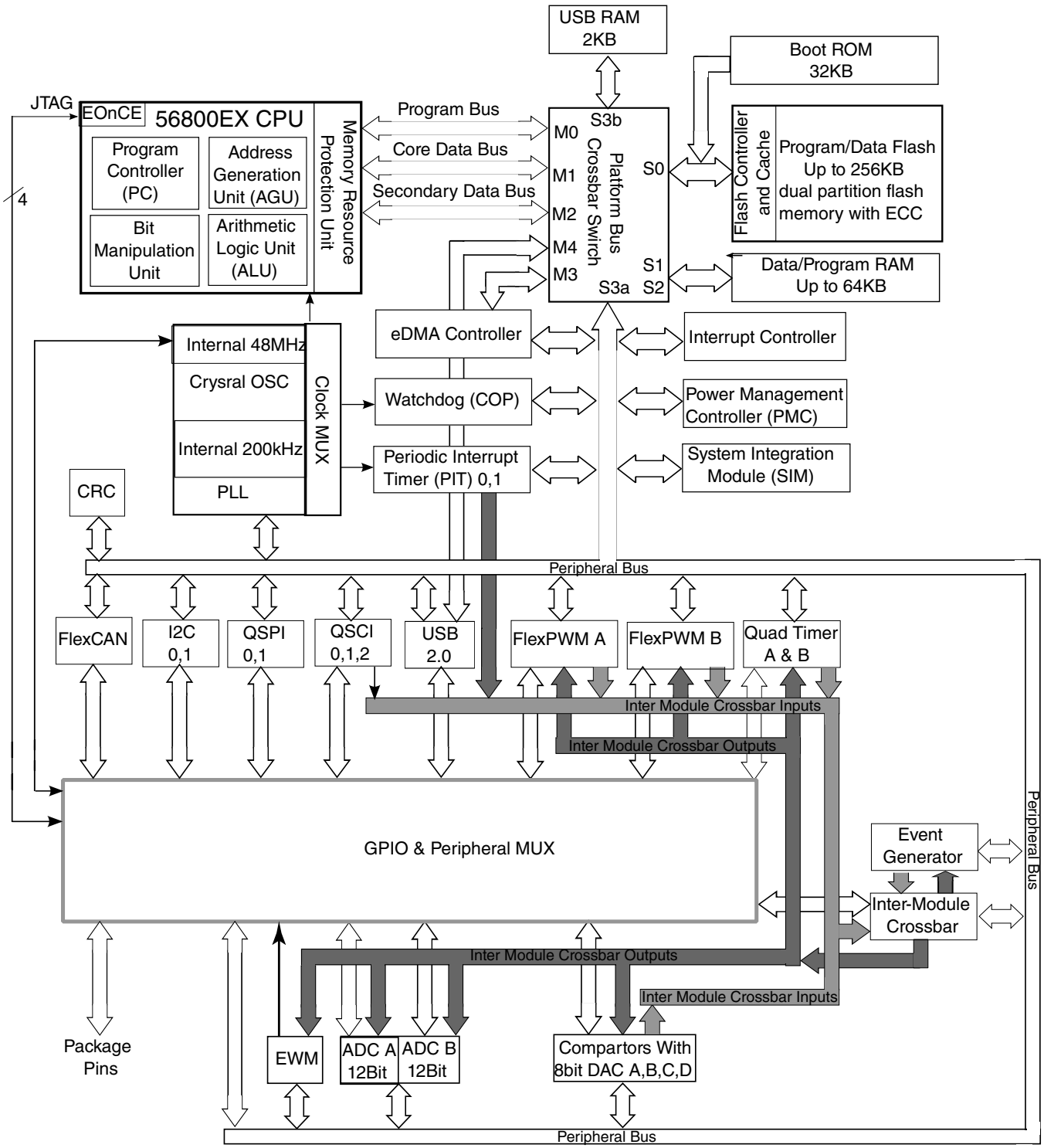


Figure 2. System diagram

2 Ordering parts

2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **nxp.com** and perform a part number search for the following device numbers: MC56F83

2.2 Part number list

The following table shows a part number list for this device.

Table 2. Part numbers

Part Number	Flash Size	Temperature	Package
MC56F83689VLL	256 KB	105°C	100 LQFP
MC56F83686VLK	256 KB	105°C	80 LQFP
MC56F83683VLH	256 KB	105°C	64 LQFP
MC56F83663VLH	128 KB	105°C	64 LQFP

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format: Q 56F8 3 C F P T PP N

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
3	DSC subfamily	• 3
C	Maximum CPU frequency (MHz)	• 6 = 100 MHz
F	Primary program flash memory size	• 6 = 128 KB • 8 = 256 KB
P	Pin count	• 3 = 64 • 6 = 80 • 9 = 100
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64LQFP • LK = 80LQFP • LL = 100LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

3.4 Example

This is an example part number: MC56F83689VLL

4 Terminology and guidelines

4.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

4.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

4.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

4.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

4.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

4.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

4.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

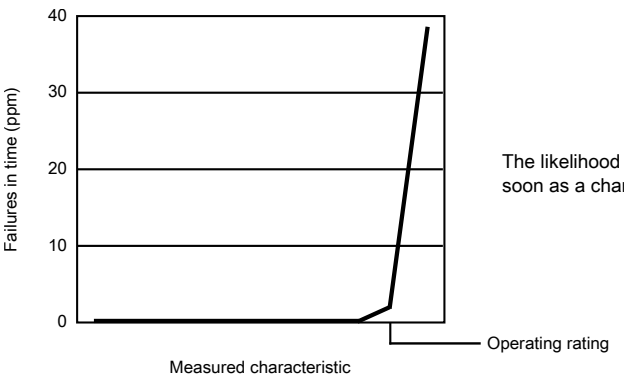
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

4.4.1 Example

This is an example of an operating rating:

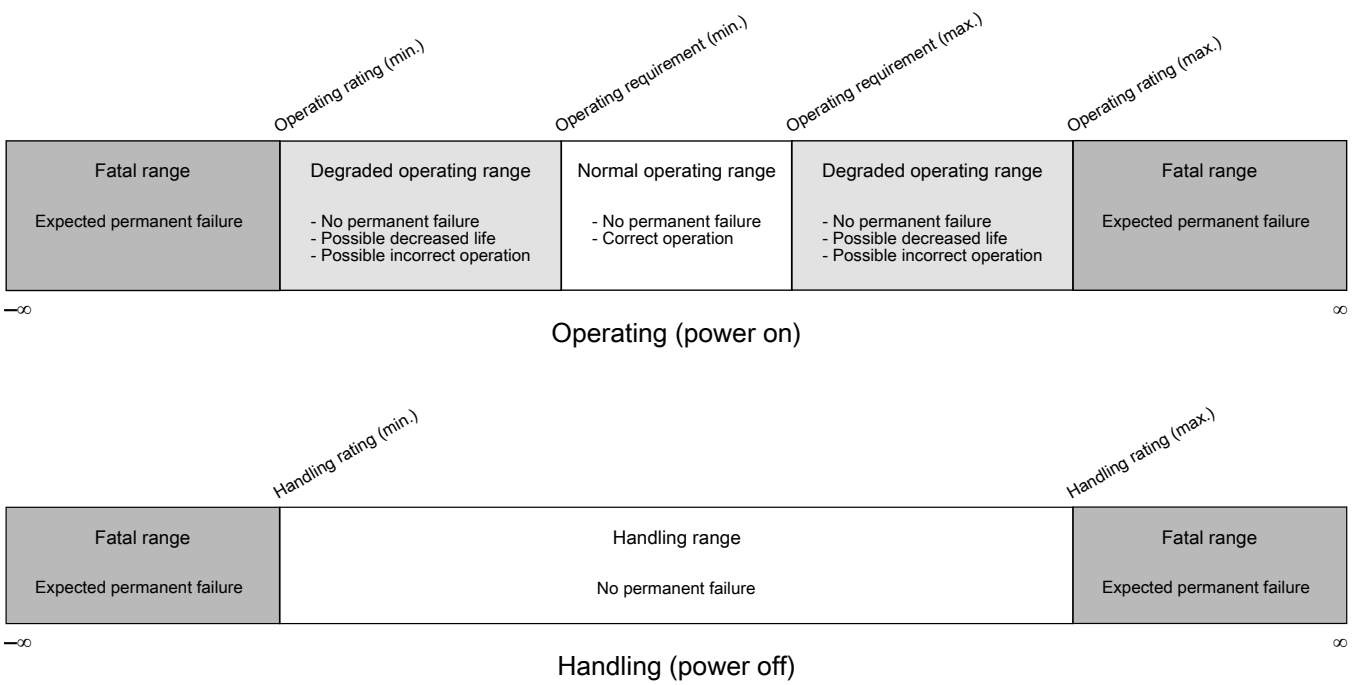
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

4.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

4.6 Relationship between ratings and operating requirements



4.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

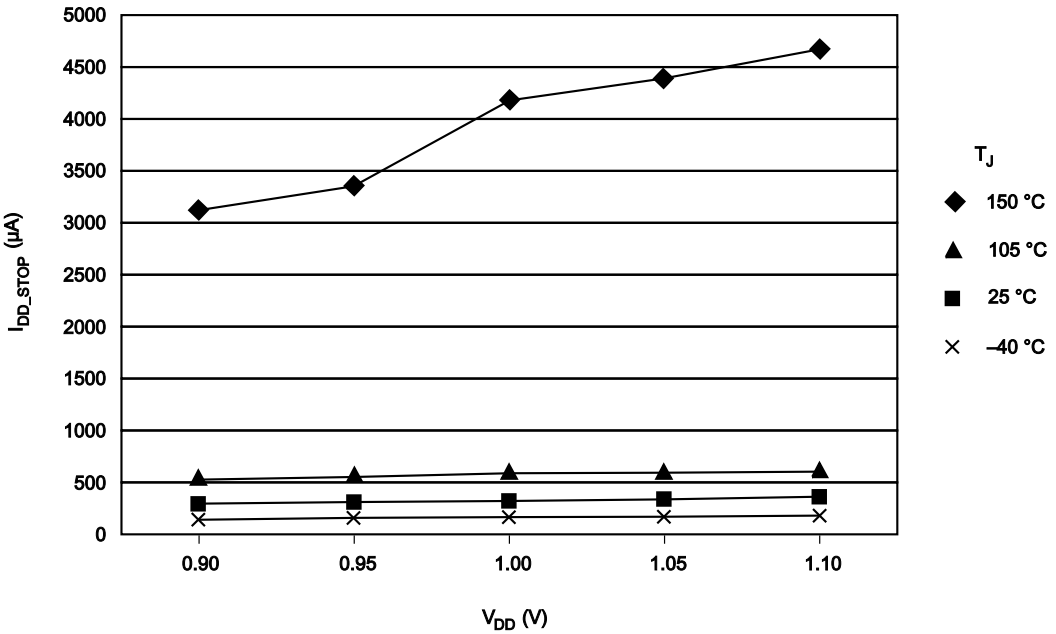
4.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

4.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



4.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

5 Ratings

5.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit	Notes
ESD for Human Body Model (V_{HBM})	–2000	+2000	V	2
ESD for Charge Device Model (V_{CDM})	–500 –750	+500 [3] +750 [4]	V	5
Latch-up current at T_A= 85°C (I_{LAT}) (V part)	–100	+100	mA	6

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.
2. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
3. All pins except the corner pins
4. Corner pins only
5. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
6. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

NOTE

If the voltage difference between VDD and VDDA or VSS and VSSA is too large, then the device can malfunction or be permanently damaged. The restrictions are:

- **At all times, it is recommended that the voltage difference of VDD - VSS be within +/-200 mV of the voltage difference of VDDA - VSSA**, including power ramp up and ramp down; see additional requirements in Table 5. Failure to do this recommendation may result in a harmful leakage current through the substrate, between the VDD/VSS and VDDA/VSSA pad cells. This harmful leakage current could prevent the device from operating after power up.
- **At all times, to avoid permanent damage to the part, the voltage difference between VDD and VDDA must absolutely be limited to 0.3 V**; see Table 4.
- **At all times, to avoid permanent damage to the part, the voltage difference between VSS and VSSA must absolutely be limited to 0.3 V**; see Table 4.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V

Table continues on the next page...

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
Ambient Temperature	T_A	V temperature	-40	105	°C
Junction Temperature	T_j	V temperature	-40	125	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than VDIO_MIN (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

6 General

6.1 General characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except 3.3 V for $\overline{\text{RESET}}$, USB_DP/USB_DM pins. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels . This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply to the temperature range specified in Table 4 over the following supply ranges: V_{SS}=V_{SSA}=0V, V_{DD}=V_{DDA}=3.0V to 3.6V, CL≤50 pF, f_{OP}=100MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

6.2 AC electrical characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

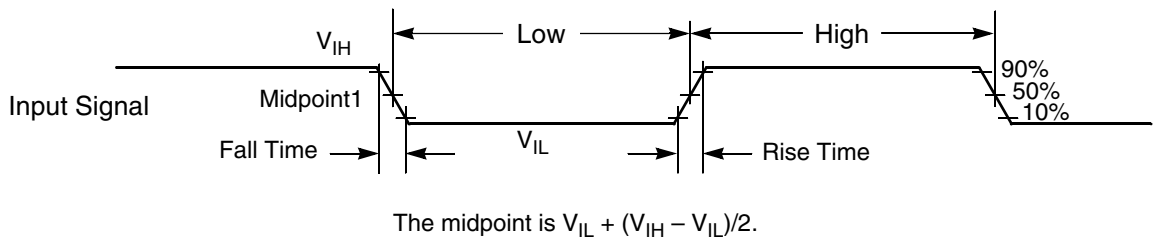


Figure 3. Input signal measurement references

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

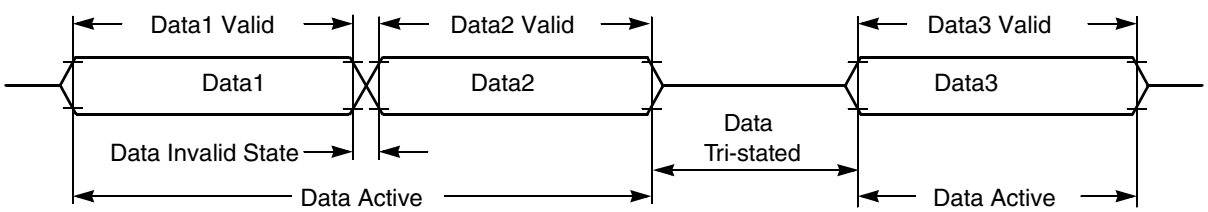


Figure 4. Signal states

6.3 Nonswitching electrical specifications

6.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is monotonically and greater than 100 µs.

Table 5. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}				V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.2	0	0.2	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.2	0	0.2	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Input Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.3 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.) • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	Pin Group 1 Pin Group 1	— —		-2 -9	mA
Output Source Current Low (at V_{OL} max.)[2, 3] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	Pin Groups 1, 2 Pin Groups 1, 2	— —		2 9	mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
2. Total IO sink current and total IO source current are limited to 75 mA each
3. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

6.3.2 LVD and POR operating requirements

Table 6. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73 [3]		V

Table continues on the next page...

Table 6. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
LVI_2p2 Threshold Voltage			2.23 [3]		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)
3. Value is based on the fact that the bandgap is trimmed.

6.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 7. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes [1]	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
pull-up enabled or disabled		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low [2, 3] pull-up disabled	I_{IL}	Pin Groups 1, 2	—	0	+/- 0.5	µA	V_{IN} = 0V
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Output Current [2, 3] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 × V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$

- Pin Group 3: ADC and Comparator Analog Inputs
- Pin Group 4: XTAL, EXTAL

2. See the following figure "I_{IN}/I_{OZ} vs. V_{IN} (typical; pull-up & pull-down disabled) (design simulation)" .
3. To minimize the excessive leakage (> 1 µA) current from digital pin, input signal should **NOT** stay between 1.1 V and 0.9 × V_{DD} for prolonged time.

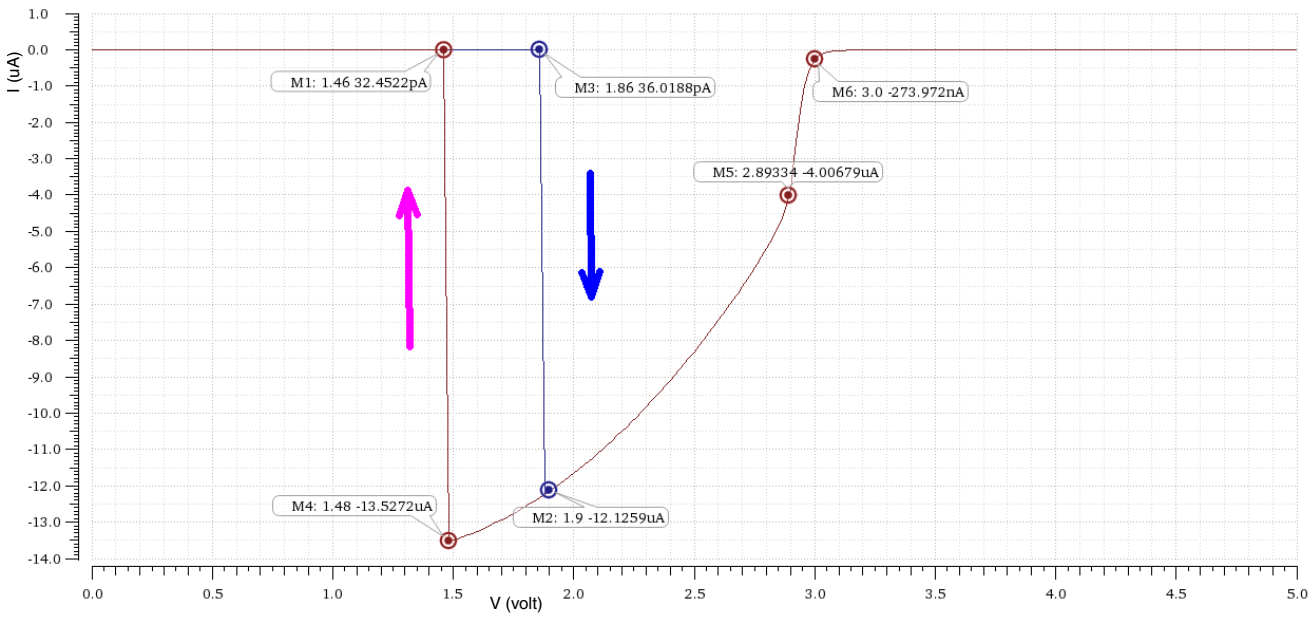


Figure 5. I_{IN}/I_{OZ} vs. V_{IN} (typical; pull-up & pull-down disabled) (design simulation)

6.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 8. Reset, stop, wait, and interrupt timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16 [1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 × T_{OSC} + 8 × T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 µF on $\overline{\text{RESET}}$.

NOTE

In Table 8, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 100MHz, T=10 ns. At 4 MHz (used coming out of reset and stop modes), T=250 ns.

Table 9. Power mode transition behavior

Symbol	Description	Typical	Max	Unit	Notes[1]
T_{POR}	After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range).	430	495	µs	
	STOP mode to RUN mode	8.61	9.90	µs	2
	LPS mode to LPRUN mode	358	411	µs	3
	VLPS mode to VLPRUN mode	1090	1254	µs	4
	WAIT mode to RUN mode	0.347	0.399	µs	5
	LPWAIT mode to LPRUN mode	351	404	µs	3
	VLPWAIT mode to VLPRUN mode	1070	1231	µs	4

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is from 48 MHz/6 in normal mode.
3. CPU clock = 100 kHz . Exit by an interrupt on PORTA GPIO.
4. Using 64 kHz external clock; CPU Clock = 32 kHz. Exit by an interrupt on PORTA GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 100 MHz. Exit by interrupt on PORTA GPIO

6.3.5 Power consumption operating behaviors

Table 10. Current Consumption (mA)

Mode	Maximum Frequency	Conditions[1]	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 105 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	100 MHz	• 100 MHz Core and Peripheral clock • Regulators are in full regulation • Internal Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. • ADC/DAC (all 8-bit DACs) powered on and clocked • Comparator powered on	46.7	6.1	65.6	8.8
WAIT	100 MHz	• 100 MHz Core and Peripheral clock • Regulators are in full regulation • Internal Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • ADC/Comparator powered off	21.8	—	37.5	—

Table continues on the next page...

Table 10. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions[1]	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 105 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
STOP	4 MHz	• 4 MHz Core and Peripheral clock • Regulators are in full regulation • Internal Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/Comparator powered off	5.2	—	20.0	—
LPRUN	2 MHz	• 100 kHz Core and Peripheral clock from Relaxation Oscillator's (ROSC) low speed clock • 48 MHz Internal Oscillator disabled • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except cyclic ADCs. all 8-bit DACs enabled. • Simple loop with running from platform instruction buffer	1.1	—	15.0	—
LPWAIT	2 MHz	• 100 kHz Core and Peripheral clock from Relaxation Oscillator's (ROSC) low speed clock • 48 MHz Internal Oscillator disabled • Regulators are in standby • PLL disabled • All peripheral modules enabled, except cyclic ADCs. all 8-bit DACs enabled. • Processor core in wait mode	1.1	—	15.0	—
LPSTOP	2 MHz	• 100 kHz Core and Peripheral clock from Relaxation Oscillator's (ROSC) low speed clock • 48 MHz Internal Oscillator disabled • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off • Processor core in stop mode	1.0	—	14.0	—
VLPRUN	200 kHz	• 32 kHz Core and Peripheral clock from a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	0.6	—	12.0	—
VLPWAIT	200 kHz	• 32 kHz Core and Peripheral clock from a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled	0.6	—	12.0	—

Table continues on the next page...

Table 10. Current Consumption (mA) (continued)

Mode	Maximum Frequency	Conditions[1]	Typical at 3.3 V, 25 °C		Maximum at 3.6 V, 105 °C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode				
VLPSTOP	200 kHz	• 32 kHz Core and Peripheral clock from a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby. • Small regulator is disabled. • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	0.6	—	12.0	—

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.

6.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

6.3.7 Capacitance attributes

Table 11. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

6.4 Switching specifications

6.4.1 Device clock specifications

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{BUS}	Bus clock	—	100	MHz	

6.4.2 General switching timing

Table 13. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), slew disabled, 2.7V ≤ V_{DD} ≤ 3.6V	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), slew enabled, 2.7V ≤ V_{DD} ≤ 3.6V	1.5	6.8	ns	4
	Port rise and fall time (low drive strength), slew disabled, 2.7V ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	3
	Port rise and fall time (low drive strength), slew enabled, 2.7V ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

6.5 Thermal specifications

6.5.1 Thermal operating requirements

Table 14. Thermal operating requirements

Symbol	Description	Grade	Min	Max	Unit
T_J	Die junction temperature	V	–40	125	°C
T_A	Ambient temperature	V	–40	105	°C

6.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal design considerations for more detail on thermal design considerations.

Board type [1]	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	44	42	46	°C/W	2
Single-layer (1s)	$R_{\theta JC}$	Thermal resistance, junction to case	14	13	16	°C/W	2
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	1.2	1.0	1.4	°C/W	

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 JTAG timing

Table 15. JTAG timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 6
TCK clock pulse width	t_{PW}	50	—	ns	Figure 6
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 7
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 7
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 7
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 7

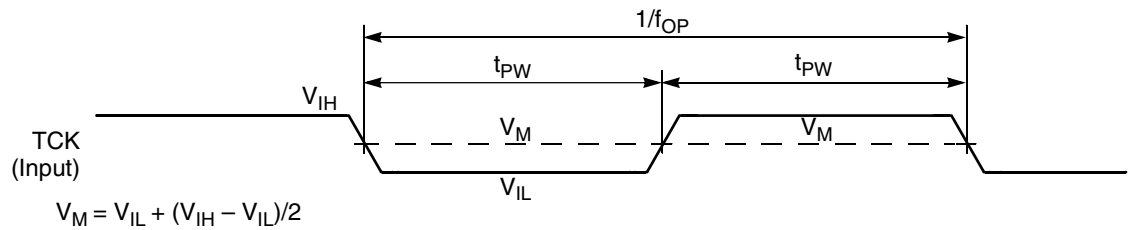


Figure 6. Test clock input timing diagram

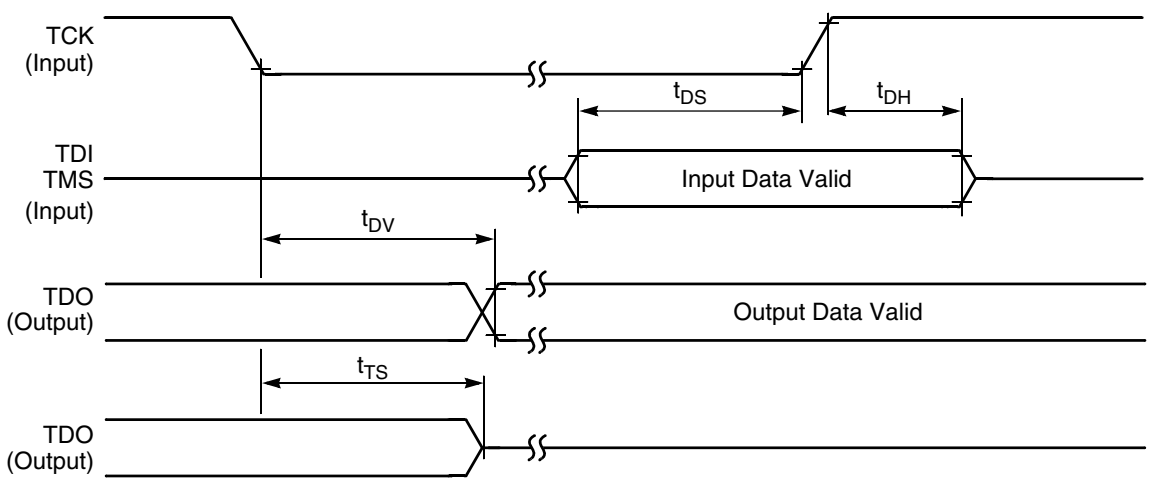


Figure 7. Test access port timing diagram

7.2 System modules

7.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the device's core logic. For proper operations, the voltage regulator requires using at minimum 4.4 µF capacitors in total on each V_{CAP} pin. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 16.

Table 16. Regulator 1.2 V parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage [1]	V_{CAP}	1.08	1.22	1.32	V
Short Circuit Current [2]	I_{SS}	—	600	—	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	1	minute

1. Value is after trim
2. Guaranteed by design

Table 17. Bandgap electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.22[1]	—	V

1. Typical value is trimmed at 25°C. There could be ±50 mV variation due to temperature change.

7.3 Clock modules

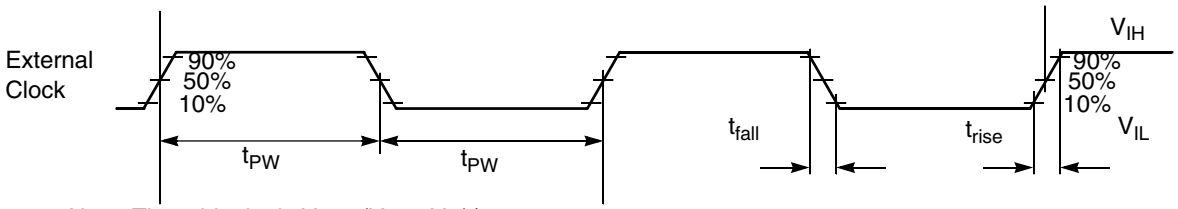
7.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 18. External clock operation timing requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.7 \times V_{DD}$	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3 \times V_{DD}$	V

1. See the "External clock timing" figure for details on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 8. External clock timing

7.3.2 Phase-Locked Loop timing

Table 19. Phase-Locked Loop timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	8	8	16	MHz
PLL output frequency[2]	f_{op}	150	—	450	MHz
PLL lock time[3]	t_{plls}	30		81	µs
Allowed Duty Cycle of input reference	t_{dc}	40	50	60	%

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 100 MHz.
3. This is the time required *after the PLL is enabled* to ensure reliable operation.

7.3.3 External crystal or resonator requirement

Table 20. Crystal or resonator requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

7.3.4 200 kHz RC Oscillator Timing

Table 21. 200 kHz RC Oscillator Oscillator Electrical Specifications

Characteristic		Symbol	Min	Typ	Max	Unit
200 kHz Output Frequency[1]						
	T_A: -40°C to 105°C		193	200	206	kHz
Stabilization Time	200 kHz output	t_{stab}		10		µs
Output Duty Cycle			48	50	52	%

1. Frequency after factory trim

7.3.5 IRC48M specifications

Table 22. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency over temperature • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	2

1. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1). Only applicable to devices/packages that contain USB.
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1

7.4 Memories and memory interfaces

7.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

7.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Flash Block high-voltage time for 128 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

7.4.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk1k}$	Read 1s Block execution time • 256 KB program flash	—	—	1.0	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
$t_{ersblk128k}$	Erase Flash Block execution time • 128 KB program flash	—	110	925	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.6	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	225	1850	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	225	1850	ms	2

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

7.4.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

7.4.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

7.5 Analog

7.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 27. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	VDDA	3	3.3	3.6	V
VREFH (in external reference mode)	Vrefhx	VDDA-0.6		VDDA	V
ADC Conversion Clock[2]	f_{ADCCLK}	0.6		25	MHz
Conversion Range[3] Fully Differential Single Ended/Unipolar	R_{AD}	 $-(V_{REFH} - V_{REFL})$ V_{REFL}		$V_{REFH} - V_{REFL}$ V_{REFH}	V
Input Voltage Range (per input)[4] External Reference Internal Reference	V_{ADIN}	V_{REFL} V_{SSA}		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time[5]	t_{ADC}		8		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		60		ADC Clock Cycles
ADC RUN Current (per ADC block)	I_{ADRUN}		2.45		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.1		µA
V_{REFH} Current (in external mode)	I_{VREFH}		190	225	µA
Accuracy (DC or Absolute)					
Integral non-Linearity[6]	INL		± 1.5	± 2.2	LSB[7]
Differential non-Linearity[6]	DNL		± 0.6	± 0.8	LSB[7]
Monotonicity		GUARANTEED			
Offset[8] Fully Differential Single Ended/Unipolar	V_{OFFSET}		± 5 ± 5		mV
Gain Error	E_{GAIN}		0.996 to 1.004	0.990 to 1.010	
AC Specifications[9]					
Signal to Noise Ratio	SNR		68		dB

Table continues on the next page...

Table 27. 12-bit ADC Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Total Harmonic Distortion	THD		71		dB
Spurious Free Dynamic Range	SFDR		72		dB
Signal to Noise plus Distortion	SINAD		66		dB
Effective Number of Bits	ENOB		—		bits
Gain = 1x (Fully Differential)			10.7		
Gain = 2x (Fully Differential)			10.3		
Gain = 4x (Fully Differential)			9.9		
Gain = 1x (Single Ended/Unipolar)			10.2		
Gain = 2x (Single Ended/Unipolar)			10.0		
Gain = 4x (Single Ended/Unipolar)			9.7		
Variation across channels[10]			0.1		
ADC Inputs					
Input Leakage Current	I_{IN}		1		nA
Temperature sensor slope	T_{SLOPE}		-2.96		mV/°C
Temperature sensor voltage at 25 °C	V_{TEMP25}		1.59		V
Disturbance					
Input Injection Current [11]	I_{INJ}			±3	mA
Channel to Channel Crosstalk[12]	ISOXTLK		-82		dB
Memory Crosstalk[13]	MEMXTLK		-71		dB
Input Capacitance	C_{ADI}				pF
Sampling Capacitor			1.2		
• 1x mode			2.4		
• 2x mode			4.8		
• 4x mode					

1. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA}, x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave; the measurement mode is Gain = 1x (Fully Differential).
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

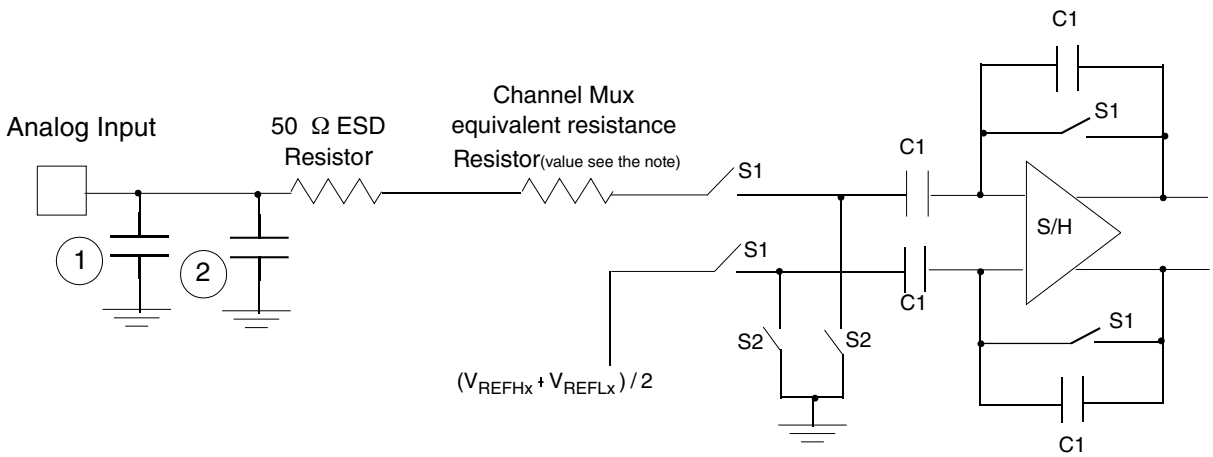
7.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times C_{ADI}} + 50\,ohm + \textbf{Resistor}$$

NOTE

Resistor=1200 ohm@gain1×, or 730 ohm@gain2×, or 500 ohm@gain4×



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

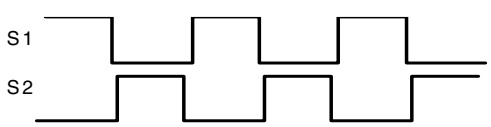


Figure 9. Equivalent circuit for A/D loading

7.5.2 CMP and 8-bit DAC electrical specifications

Table 28. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	3.0	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	—	300	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	36	—	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis				
	• CR0[HYSTCTR] = 00[1]	—	5	13	mV
	• CR0[HYSTCTR] = 01[2]	—	25	48	mV
	• CR0[HYSTCTR] = 10[2]	—	55	105	mV
	• CR0[HYSTCTR] = 11[2]	—	80	148	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)[3]	—	25	70	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)[3]	—	60	200	ns
	Analog comparator initialization delay[4]	—	40	—	µs
I_{DAC8b}	8-bit DAC current adder (enabled)	—	7	—	µA
$V_{reference}$	8-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	—	V_{DD}	—	V
INL	8-bit DAC integral non-linearity	–1	—	1	LSB[5]
DNL	8-bit DAC differential non-linearity	–1	—	1	LSB

1. Measured with input voltage range limited to 0 to V_{DD}
2. Measured with input voltage range limited to $0.7 \le Vin \le V_{DD}-0.8$
3. Input voltage range: $0.1V_{DD} \le Vin \le 0.9V_{DD}$, step = ±100mV, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/256$

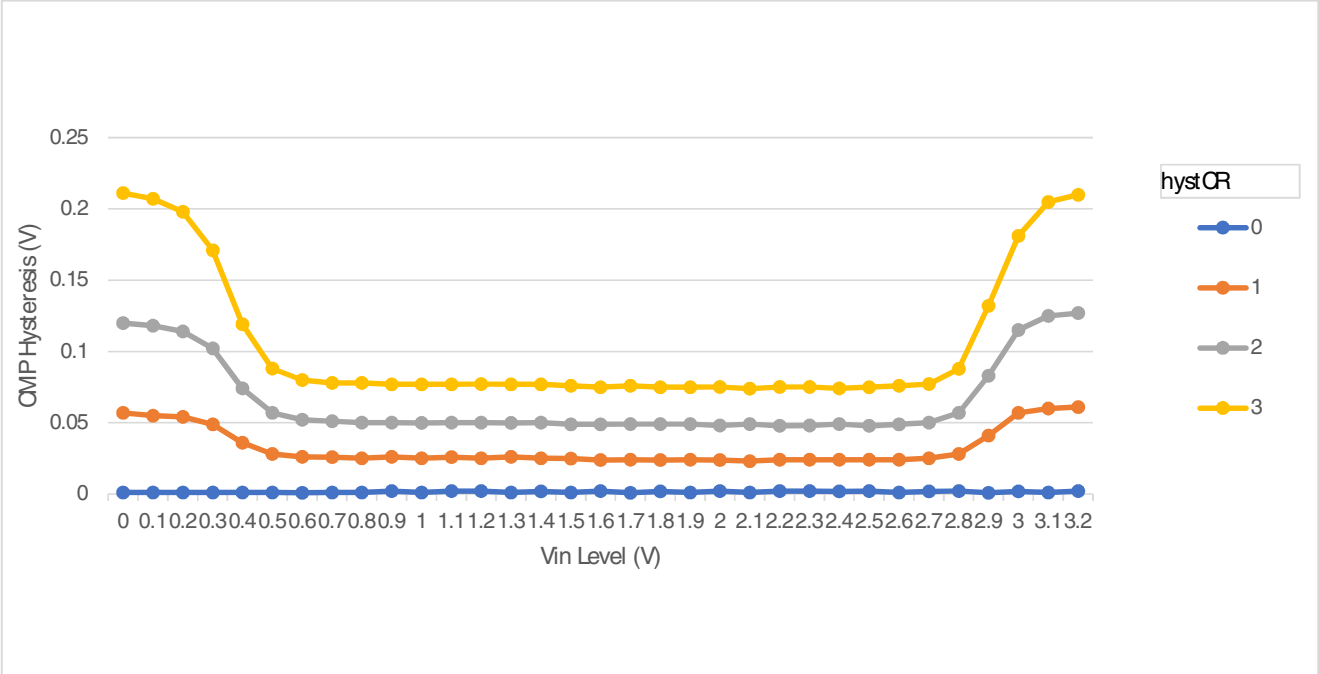


Figure 10. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

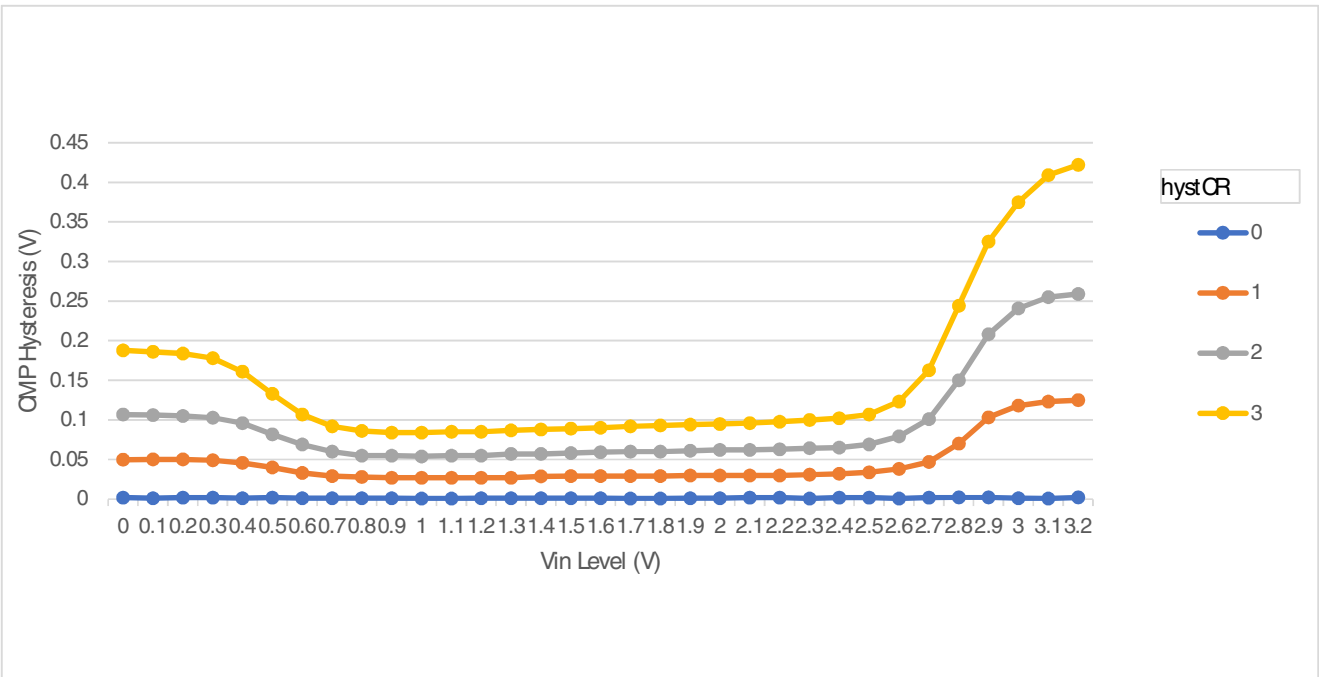


Figure 11. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

7.6 PWMs and timers

7.6.1 PWM characteristics

Table 29. PWM timing parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency			100		MHz
Delay for fault input activating to PWM output deactivated		1		33	ns

7.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

Table 30. Timer timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 12
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 12
Timer output period	P_{OUT}	20	—	ns	Figure 12
Timer output high/low period	P_{OUTHL}	10	—	ns	Figure 12

1. T = clock cycle. For 100 MHz operation, T = 10 ns.

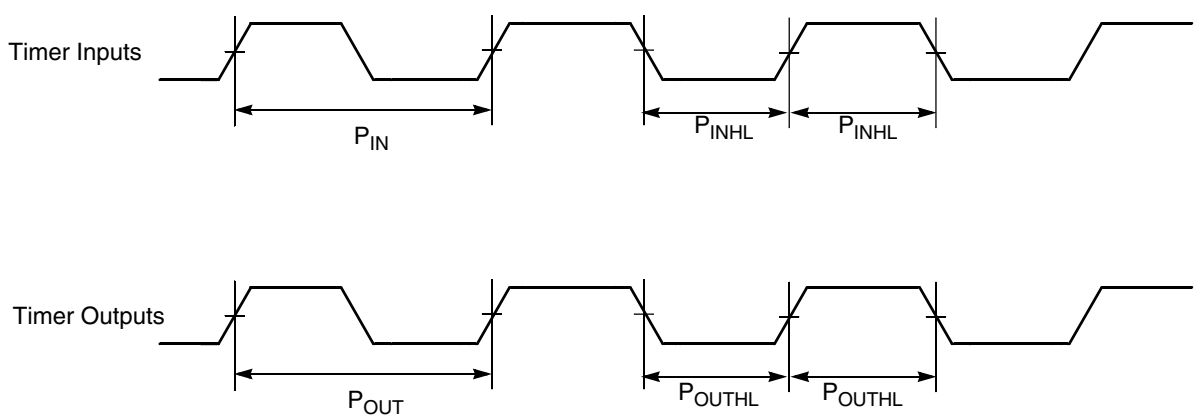


Figure 12. Timer timing

7.7 Communication interfaces

7.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 31. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	35 35	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Enable lead time Master Slave	t_{ELD}	— 17.5	— —	ns ns	Figure 16
Enable lag time Master Slave	t_{ELG}	— 17.5	— —	ns ns	Figure 16
Clock (SCK) high time Master Slave	t_{CH}	16.6 16.6	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Clock (SCK) low time Master Slave	t_{CL}	16.6 16.6	— —	ns ns	Figure 16
Data set-up time required for inputs Master Slave	t_{DS}	16.5 1	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Data hold time required for inputs Master Slave	t_{DH}	1 3	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Access time (time to data active from high-impedance state) Slave	t_A	5	—	ns	Figure 16
Disable time (hold time to high-impedance state) Slave	t_D	5	—	ns	Figure 16
Data valid for outputs Master Slave (after enable edge)	t_{DV}	— —	5 15	ns ns	Figure 13 Figure 14 Figure 15 Figure 16

Table continues on the next page...

Table 31. SPI timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Data invalid	t_{DI}	0	—	ns	Figure 13
Master		0	—	ns	Figure 14
Slave					Figure 15
					Figure 16
Rise time	t_R	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16
Fall time	t_F	—	1	ns	Figure 13
Master		—	1	ns	Figure 14
Slave					Figure 15
					Figure 16

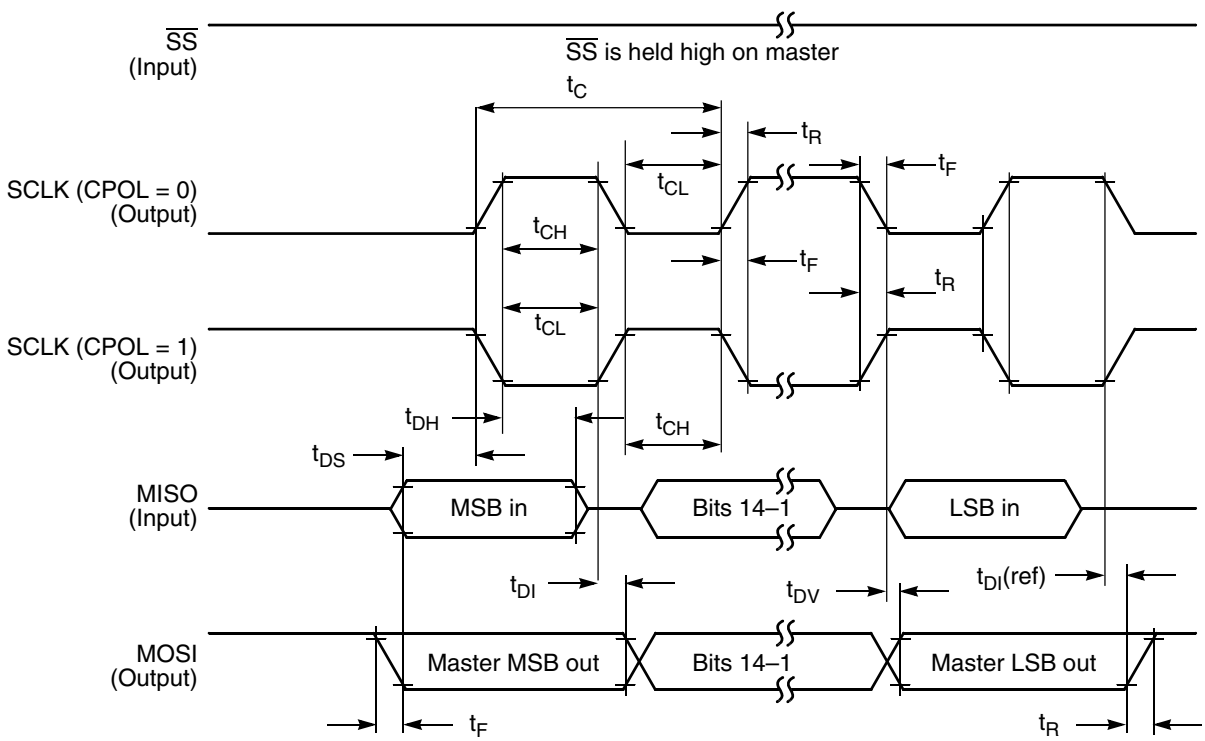


Figure 13. SPI master timing (CPHA = 0)

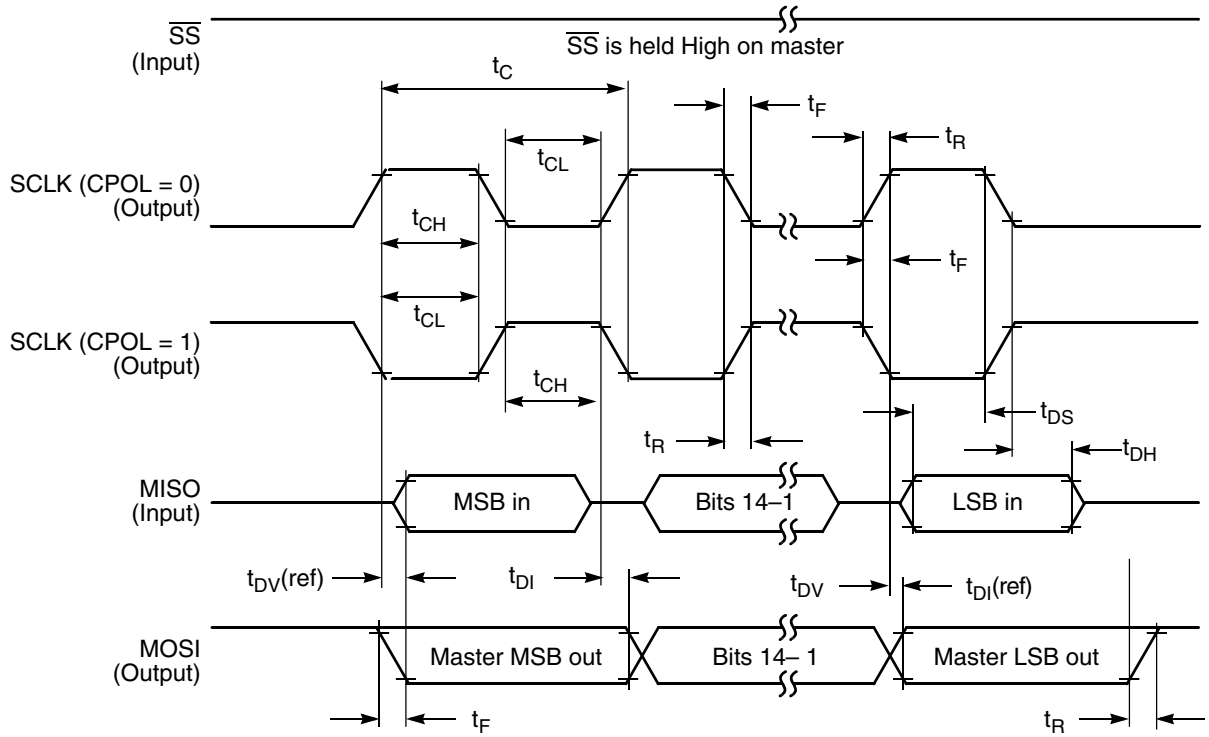


Figure 14. SPI master timing (CPHA = 1)

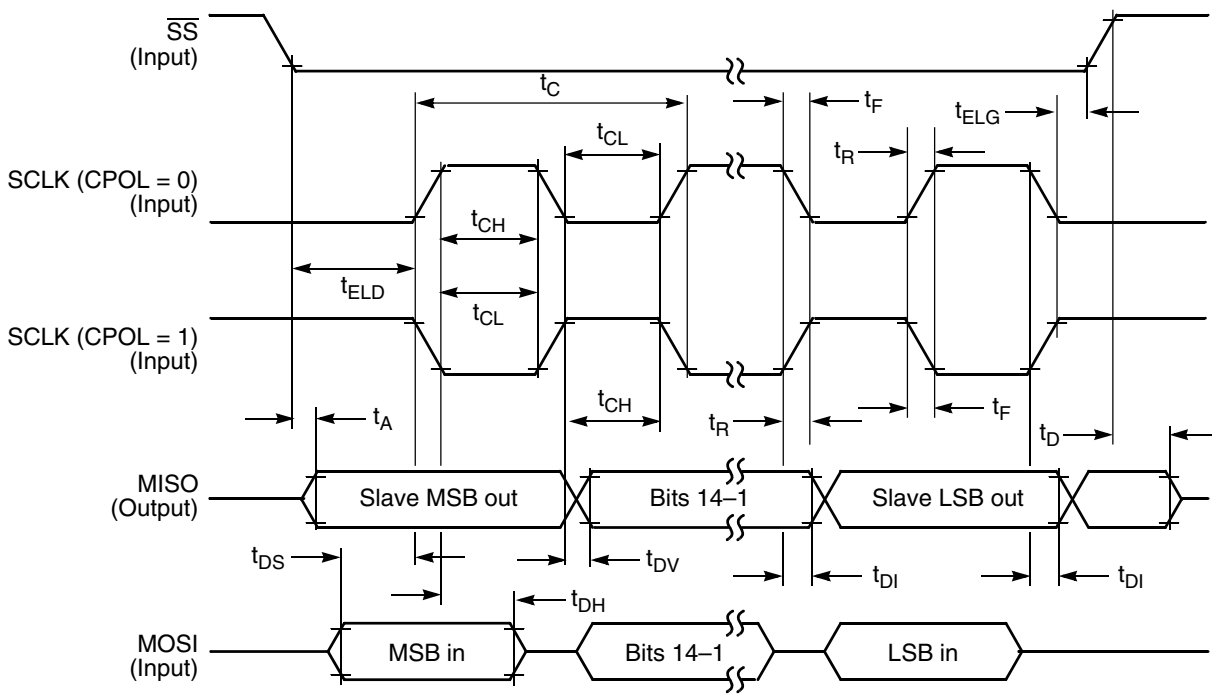


Figure 15. SPI slave timing (CPHA = 0)

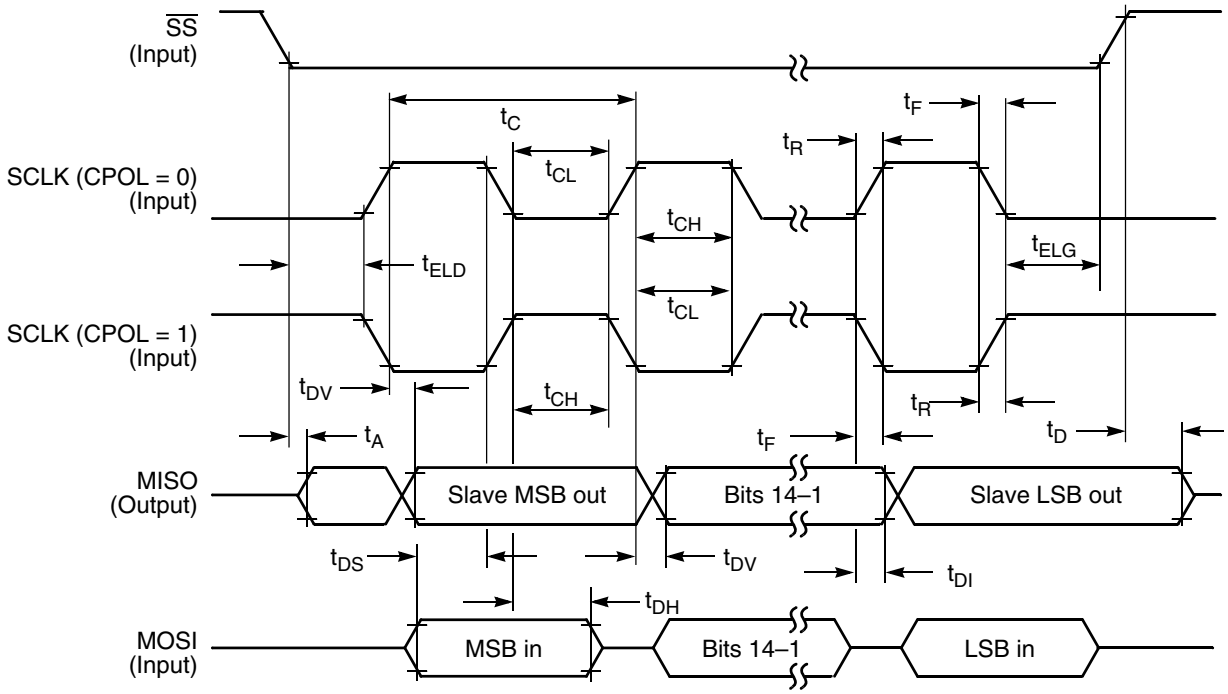


Figure 16. SPI slave timing (CPHA = 1)

7.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 32. SCI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbit/s	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	µs	Figure 17
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	µs	Figure 18
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.200 MHz depending on part number) or 2x bus clock (max. 200 MHz) for the devices.

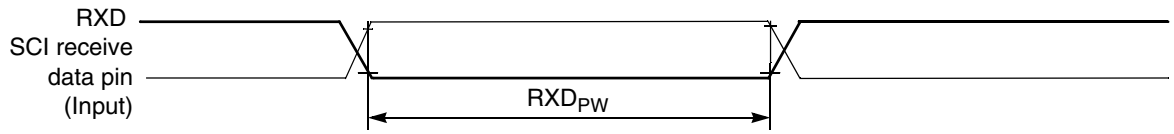


Figure 17. RXD pulse width

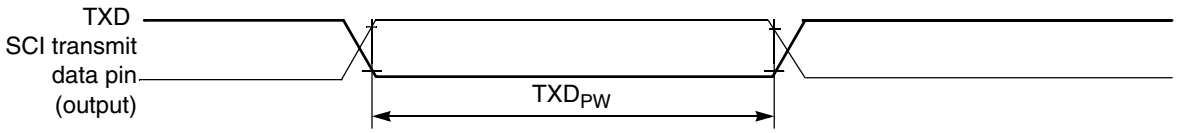


Figure 18. TXD pulse width

7.7.3 Inter-Integrated Circuit Interface (I^2C) timing

Table 33. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[5, 6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5, 6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF.
4. Set-up time in slave-transmitter mode is 1 IP Bus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

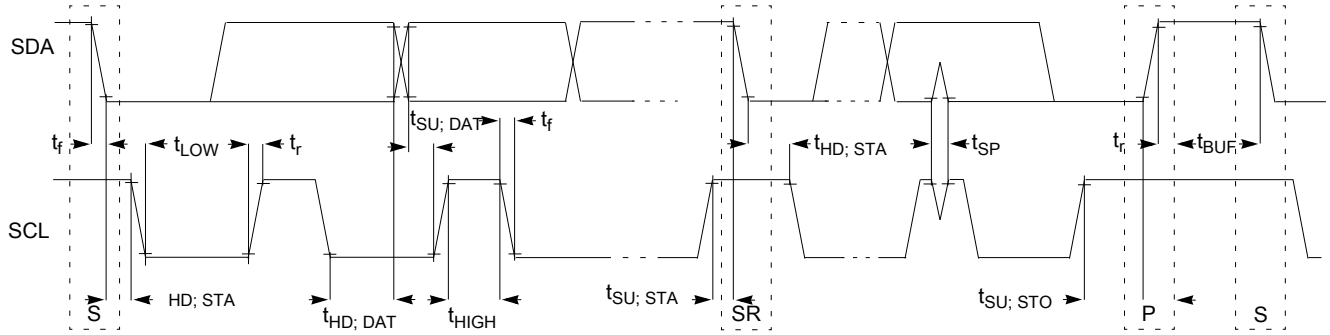


Figure 19. Timing definition for fast and standard mode devices on the I^2C bus

7.7.4 FlexCAN switching specifications

See the "General switching timing" section.

8 Design Considerations

8.1 Thermal design considerations

An estimate of the chip junction temperature (T_J) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

where

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W).

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which T_J value is closer to the application depends on the power dissipated by other components on the board.

- The T_J value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The T_J value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

where

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W).

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W).

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the

case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.

- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.1 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a reset state during normal operation if JTAG converter is not present. Furthermore, configure TMS, TDI, TDO and TCK to GPIO if operation environment is very noisy.
- During reset and after reset but before I/O initialization, all the GPIO pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

8.3 Power-on Reset design considerations

8.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDD within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells. This leakage current could prevent operation of the device after it powers up. The voltage difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See Table 4). Also see Table 5.

8.3.2 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.7V. However, the device might exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 20). This can cause the DSC fail to start up.

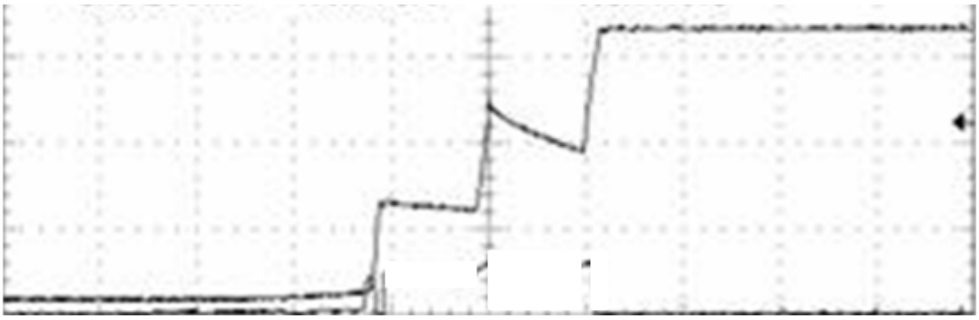


Figure 20. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

9 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23174W
100-pin LQFP	98ASS23308W

10 Pinout

10.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM module is responsible for selecting which ALT functionality is available on each pin.

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
—	33	—	GPIOB8	GPIOB8	CMPD_O	XB_IN8	XB_OUT11	
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	3	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	4	GPIOC1	GPIOC1	XTAL			
5	5	5	GPIOC2	GPIOC2	TXD0	TB0	XB_IN2	CLKO0
6	6	6	GPIOF8	GPIOF8	RXD0	TB1	CMPD_O	PWMA_2X
7	—	—	VDD	VDD				
8	—	—	VSS	VSS				
9	7	—	GPIOD6	GPIOD6	TXD2	XB_IN4	XB_OUT8	
10	8	—	GPIOD5	GPIOD5	RXD2	XB_IN5	XB_OUT9	
11	9	7	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
12	10	8	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN8	EWM_OUT_B
13	—	—	GPIOA10	GPIOA10	CMPD_IN3			
14	—	—	GPIOA9	GPIOA9	CMPD_IN2			
15	11	—	VSS	VSS				
16	12	—	VCAP	VCAP				
17	13	9	GPIOA7	GPIOA7	ANA7			
18	—	—	GPIOA8	GPIOA8	CMPD_IN1			
19	14	10	GPIOA6	GPIOA6	ANA6			
20	15	11	GPIOA5	GPIOA5	ANA5			
21	16	12	GPIOA4	GPIOA4	ANA4+CMPD_IN0			
22	17	13	GPIOA0	GPIOA0	ANA0+CMPA_IN3	CMPC_O		
23	18	14	GPIOA1	GPIOA1	ANA1+CMPA_IN0			
24	19	15	GPIOA2	GPIOA2	ANA2+VREFHA+CMPA_IN1			
25	20	16	GPIOA3	GPIOA3	ANA3+VREFLA+CMPA_IN2			
26	21	17	GPIOB7	GPIOB7	ANB7+CMPB_IN2			
27	22	18	GPIOC5	GPIOC5		XB_IN7		
28	23	19	GPIOB6	GPIOB6	ANB6+CMPB_IN1			
29	24	20	GPIOB5	GPIOB5	ANB5+CMPC_IN2			
30	25	21	GPIOB4	GPIOB4	ANB4+CMPC_IN1			
31	26	22	VDDA	VDDA				
32	27	23	VSSA	VSSA				
33	28	24	GPIOB0	GPIOB0	ANB0+CMPB_IN3			

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
34	29	25	GPIOB1	GPIOB1	ANB1+CMPB_IN0			
35	30	26	VCAP	VCAP				
36	31	27	GPIOB2	GPIOB2	ANB2+VERFHB+CMPC_IN3			
37	32	—	GPIOA11	GPIOA11	CMPC_O	XB_IN9	XB_OUT10	USB_SOFOUT
38	—	—	VSS_USB	VSS_USB				
39	—	—	USB_DP	USB_DP				
40	—	—	USB_DM	USB_DM				
41	—	—	VDD_USB	VDD_USB				
42	34	28	GPIOB3	GPIOB3	ANB3+VREFLB+CMPC_IN0			
43	35	29	VDD	VDD				
44	36	30	VSS	VSS				
45	—	—	GPIOF11	GPIOF11	TXD0	XB_IN11		
46	—	—	GPIOF15	GPIOF15	RXD0	XB_IN10		
47	37	—	GPIOD7	GPIOD7	XB_OUT11	XB_IN7	MISO1	
48	38	—	GPIOG11	GPIOG11	TB3	CLKO0	MOSI1	
49	39	31	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	SS0_B
50	40	32	GPIOC7	GPIOC7	SS0_B	TXD0	XB_IN8	XB_OUT6
51	—	—	GPIOG10	GPIOG10	PWMB_2X	PWMA_2X	XB_IN8	
52	41	33	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
53	42	34	GPIOC9	GPIOC9	SCLK0	XB_IN4	TXD0	XB_OUT8
54	43	35	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	XB_OUT9
55	44	36	GPIOF0	GPIOF0	XB_IN6	TB2	SCLK1	
56	45	—	GPIOF10	GPIOF10	TXD2	PWMA_FAULT6	PWMB_FAULT6	XB_OUT10
57	46	—	GPIOF9	GPIOF9	RXD2	PWMA_FAULT7	PWMB_FAULT7	XB_OUT11
58	47	37	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
59	48	38	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	
60	49	39	GPIOF2	GPIOF2	SCL1	XB_OUT6	MISO1	
61	50	40	GPIOF3	GPIOF3	SDA1	XB_OUT7	MOSI1	
62	51	41	GPIOF4	GPIOF4	TXD1	XB_OUT8	PWMA_0X	PWMA_FAULT6
63	52	42	GPIOF5	GPIOF5	RXD1	XB_OUT9	PWMA_1X	PWMA_FAULT7
64	—	—	GPIOG8	GPIOG8	PWMB_0X	PWMA_0X	TA2	XB_OUT10
65	—	—	GPIOG9	GPIOG9	PWMB_1X	PWMA_1X	TA3	XB_OUT11
66	53	43	VSS	VSS				
67	54	44	VDD	VDD				
68	55	45	GPIOE0	GPIOE0	PWMA_0B			XB_OUT4
69	56	46	GPIOE1	GPIOE1	PWMA_0A			XB_OUT5
70	57	—	GPIOG2	GPIOG2	PWMB_0B	XB_OUT4		
71	58	—	GPIOG3	GPIOG3	PWMB_0A	XB_OUT5		
72	—	—	GPIOE8	GPIOE8	PWMB_2B	PWMA_FAULT0		XB_OUT8
73	—	—	GPIOE9	GPIOE9	PWMB_2A	PWMA_FAULT1		XB_OUT9

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
74	59	47	GPIOE2	GPIOE2	PWMA_1B			XB_OUT6
75	60	48	GPIOE3	GPIOE3	PWMA_1A			XB_OUT7
76	61	49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
77	62	50	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
78	63	—	GPIOG0	GPIOG0	PWMB_1B	XB_OUT6		
79	64	—	GPIOG1	GPIOG1	PWMB_1A	XB_OUT7		
80	—	—	GPIOG4	GPIOG4	PWMB_3B	PWMA_FAULT2		XB_OUT10
81	—	—	GPIOG5	GPIOG5	PWMB_3A	PWMA_FAULT3		XB_OUT11
82	65	51	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		XB_OUT8
83	66	52	GPIOE5	GPIOE5	PWMA_2A	XB_IN3		XB_OUT9
84	67	53	GPIOE6	GPIOE6	PWMA_3B	XB_IN4	PWMB_2B	XB_OUT10
85	68	54	GPIOE7	GPIOE7	PWMA_3A	XB_IN5	PWMB_2A	XB_OUT11
86	69	—	GPIOG6	GPIOG6	PWMA_FAULT4	PWMB_FAULT4	TB2	XB_OUT8
87	70	55	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWMA_FAULT4	
88	71	56	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWMA_FAULT5	
89	—	—	GPIOF12	GPIOF12	MISO1	PWMB_FAULT2		
90	—	—	GPIOF13	GPIOF13	MOSI1	PWMB_FAULT1		
91	—	—	GPIOF14	GPIOF14	SCLK1	PWMB_FAULT0		
92	72	—	GPIOG7	GPIOG7	PWMA_FAULT5	PWMB_FAULT5	XB_OUT9	CLKIN2 (USB optional)
93	73	57	VCAP	VCAP				
94	74	58	GPIOF6	GPIOF6	TB2	PWMA_3X	PWMB_3X	XB_IN2
95	75	59	GPIOF7	GPIOF7	TB3	CMPC_O	SS1_B	XB_IN3
96	76	60	VDD	VDD				
97	77	61	VSS	VSS				
98	78	62	TDO	TDO	GPIOD1			
99	79	63	TMS	TMS	GPIOD3			
100	80	64	TDI	TDI	GPIOD0			

10.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

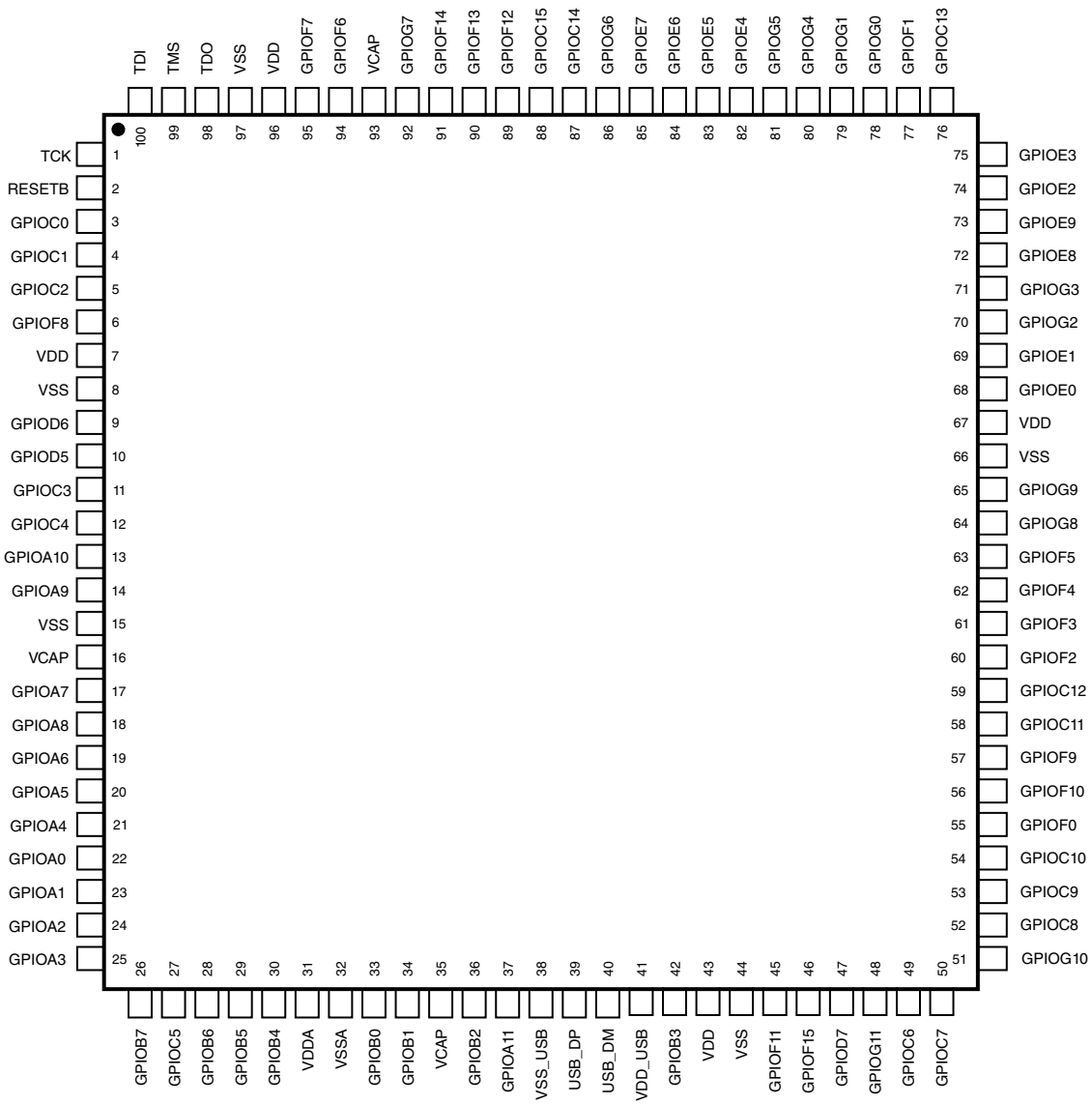


Figure 21. 100-pin LQFP

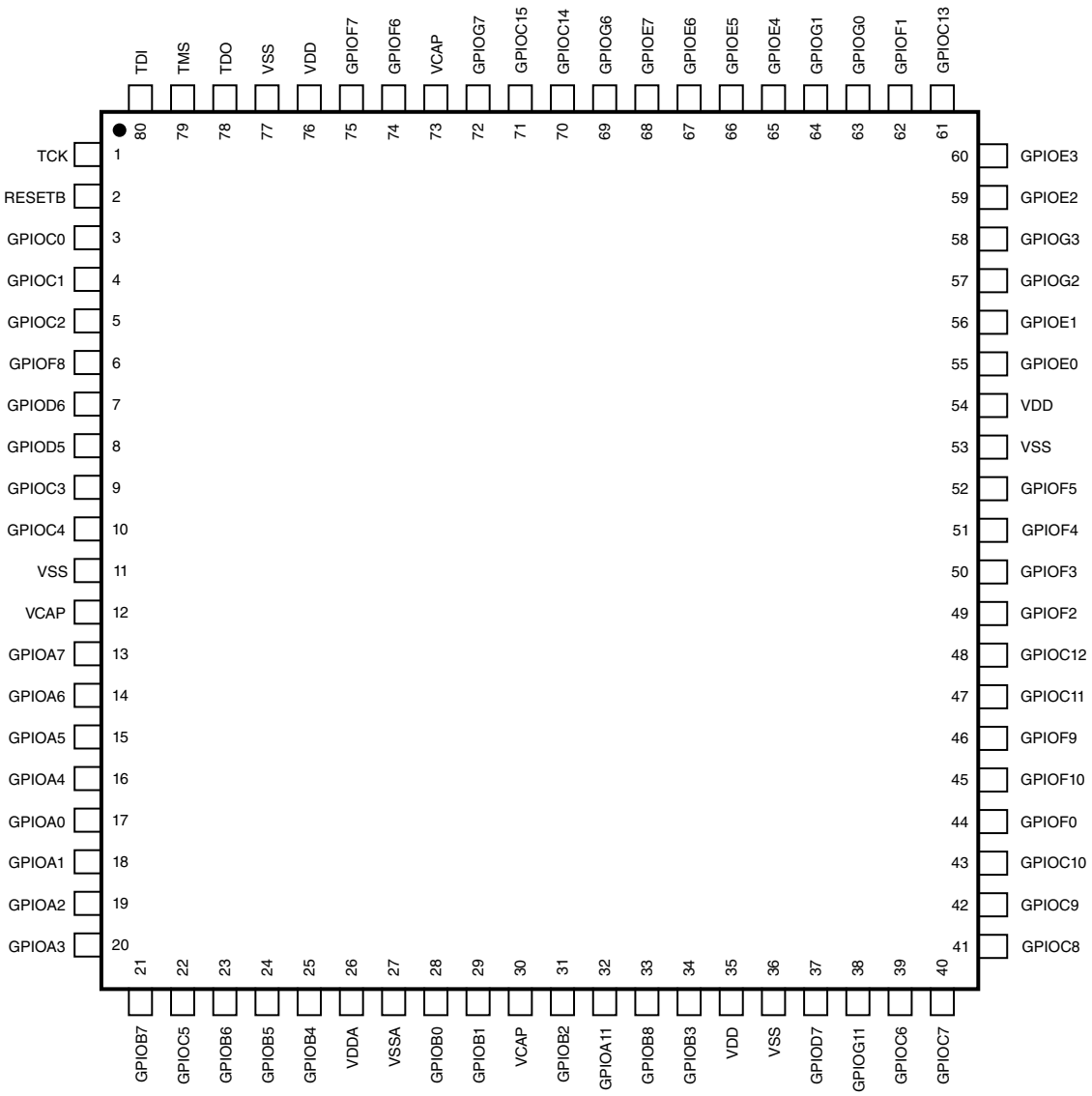


Figure 22. 80-pin LQFP

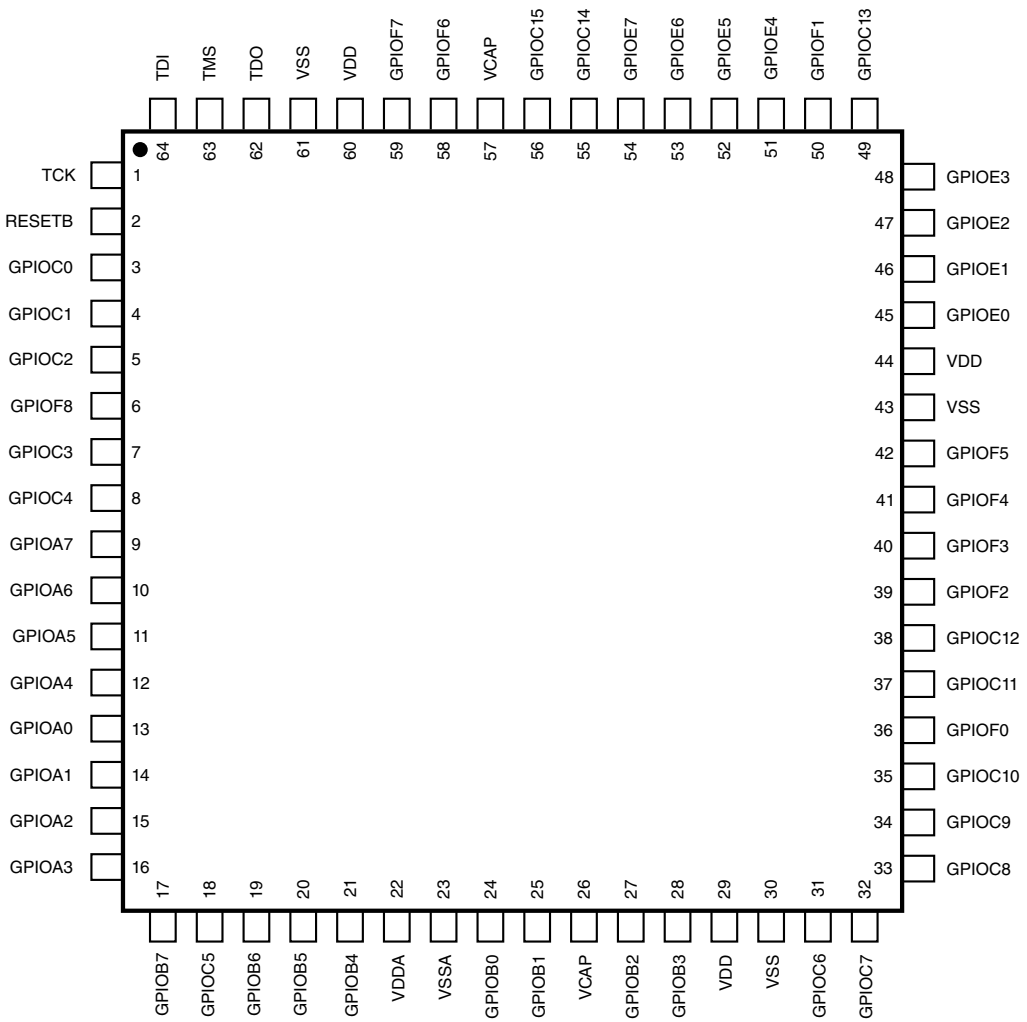


Figure 23. 64-pin LQFP

11 Product documentation

The documents listed in Table 34 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 34. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F83xxx Reference Manual	Detailed functional description and programming model	MC56F83XXXRM
MC56F836xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F836XXDS
MC56F83xxx Errata	Details any chip issues that might be present	MC56F83XXX_0N64Y

12 Revision history

The following table summarizes changes to this document since the release of the previous version.

Table 35. Revision history

Rev.	Date	Substantial Changes
1.6	09/2019	Initial public release