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# 1-of-8 Decoder/ Demultiplexer

## **High-Performance Silicon-Gate CMOS**

The MC74HC138A is identical in pinout to the LS138. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC138A decodes a three-bit Address to one-of-eight active-low outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

#### **Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 100 FETs or 29 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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#### MARKING DIAGRAMS

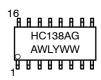


PDIP-16 N SUFFIX CASE 648





SOIC-16 D SUFFIX CASE 751B





1

TSSOP-16 DT SUFFIX CASE 948F



A = Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

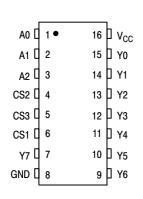


Figure 1. Pin Assignment

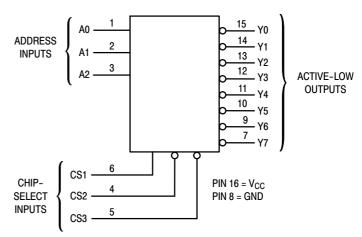


Figure 2. Logic Diagram

#### **FUNCTION TABLE**

		Inp	uts						Out	tput	s		
CS-	1CS2	CS3	A2	<b>A</b> 1	Α0	Y0	<b>Y</b> 1	Y2	<b>Y3</b>	<b>Y4</b>	Y5	Y6	<b>Y</b> 7
X	Х	Н	Х	Х	Χ	Н	Н	Н	Н	Н	Н	Н	Н
X	Н	Χ	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
L	Χ	Χ	Х	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
H	L	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
H	L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Η	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
H	L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
H	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
Н	L	L	Ι	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

H = high level (steady state); L = low level (steady state); X = don't care

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74HC138ANG	PDIP-16 (Pb-Free)	500 Units / Rail
MC74HC138ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC138ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74HC138ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLV74HC138ADR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV74HC138ADTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

#### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
l <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C SOIC Package: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 .W/°C from 65° to 125°C

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)			6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Re	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 2)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

			V <sub>CC</sub>	Guara	nteed Limit	!	
Symbol	Parameter	Test Conditions	V	-55°C to 25°C	≤ 85°C	≤ 125°C	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0 3.0	1.5 2.1	1.5 2.1	1.5 2.1	V
	voltage	$ I_{out}  \le 20 \mu A$	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2	
V <sub>IL</sub>	Maximum Low-Level Input	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	2.0	0.5	0.5	0.5	V
, IL	Voltage	$ I_{\text{out}}  \le 20 \mu\text{A}$	3.0 4.5	0.9 1.35	0.9 1.35	0.9 1.35	•
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in}$ = $V_{IH}$ or $V_{IL}$ $\left I_{out}\right  \le 2.4$ mA $\left I_{out}\right  \le 4.0$ mA $\left I_{out}\right  \le 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out}  \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$\begin{aligned} V_{in} = V_{IH} \text{ or } V_{IL} & \left  I_{out} \right  \leq 2.4 \text{ mA} \\ \left  I_{out} \right  \leq 4.0 \text{ mA} \\ \left  I_{out} \right  \leq 5.2 \text{ mA} \end{aligned}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4	40	160	μΑ

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \ pF$ , Input $t_r = t_f = 6.0 \ ns$ )

		V <sub>CC</sub>	Guara	nteed Limit	i	
Symbol	Parameter	V	–55°C to 25°C	≤ <b>85</b> °C	≤ 125°C	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 4)	2.0 3.0 4.5 6.0	135 90 27 23	170 125 34 29	205 165 41 35	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS1 to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 85 22 19	140 100 28 24	165 125 33 28	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, CS2 or CS3 to Output Y (Figures 3 and 4)	2.0 3.0 4.5 6.0	120 90 24 20	150 120 30 26	180 150 36 31	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	-	10	10	10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Per Package)*	55	pF

<sup>\*</sup>Used to determine the no–load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

#### **SWITCHING WAVEFORMS**

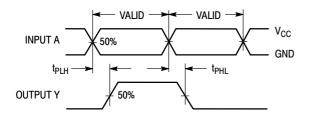


Figure 1.

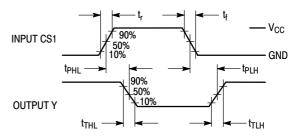


Figure 2.

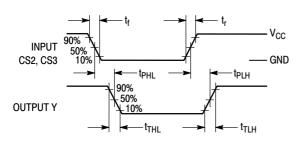
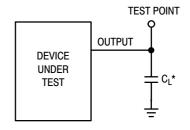


Figure 3.



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

#### **PIN DESCRIPTIONS**

#### ADDRESS INPUTS A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active—low.

### CONTROL INPUTS CS1, CS2, CS3 (Pins 6, 4, 5)

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the

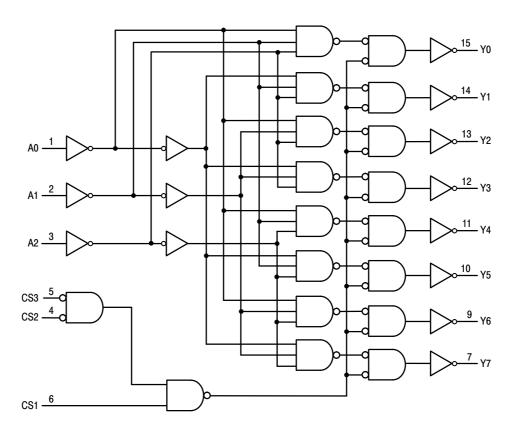
Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

#### **OUTPUTS**

Y0 - Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

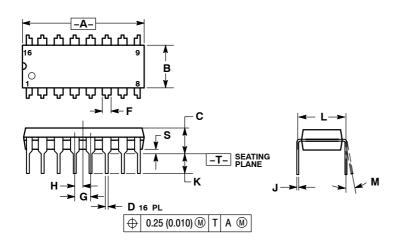
Active-low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

### **EXPANDED LOGIC DIAGRAM**



### **PACKAGE DIMENSIONS**

PDIP-16 CASE 648-08 **ISSUE T** 

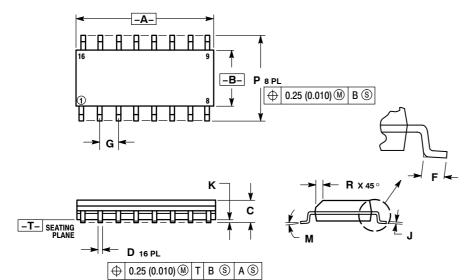


- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
М	0°	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

#### PACKAGE DIMENSIONS

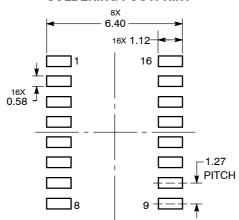
SOIC-16 CASE 751B-05 ISSUE K



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
7	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

#### **SOLDERING FOOTPRINT\***

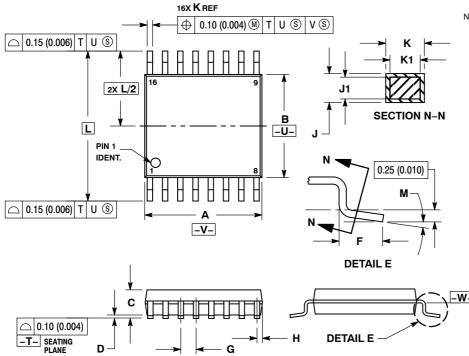


**DIMENSIONS: MILLIMETERS** 

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

#### TSSOP-16 CASE 948F-01 **ISSUE B**



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS.
- FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

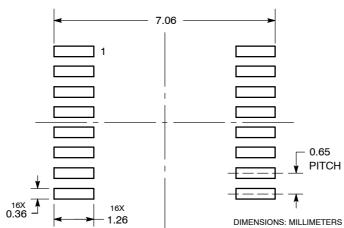
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K
- (0.003) TOTAL IN EXCESS OF THE K
  DIMENSION AT MAXIMUM MATERIAL
  CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.18	0.28	0.007	0.011	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
Κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
Ĺ	6.40 BSC		0.252 BSC		
М	0°	8°	0°	8°	

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.