

MC74LCX373

Low-Voltage CMOS Octal Transparent Latch

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX373 is a high performance, non-inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX373 inputs to be safely driven from 5 V devices.

The MC74LCX373 contains 8 D-type latches with 3-state outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are enabled. When \overline{OE} is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

Features

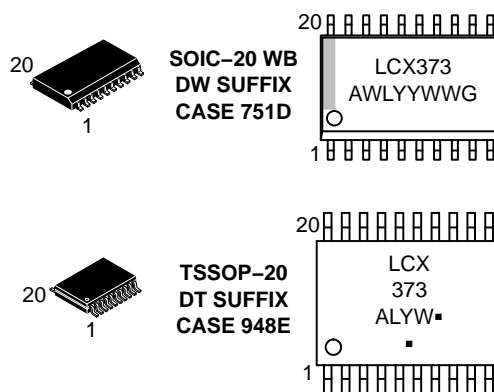
- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in all Three Logic States (10 μ A)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAMS



LCX373 = Specific Device Code
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74LCX373

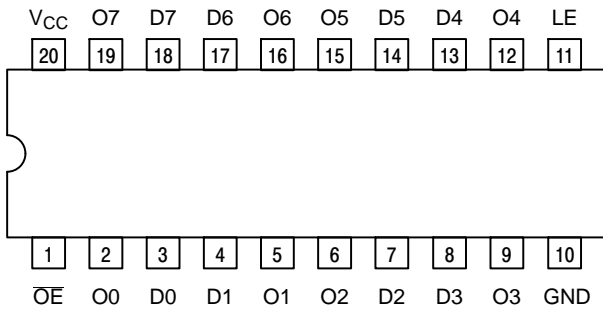


Figure 1. Pinout (Top View)

PIN NAMES

PINS	FUNCTION
OE	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

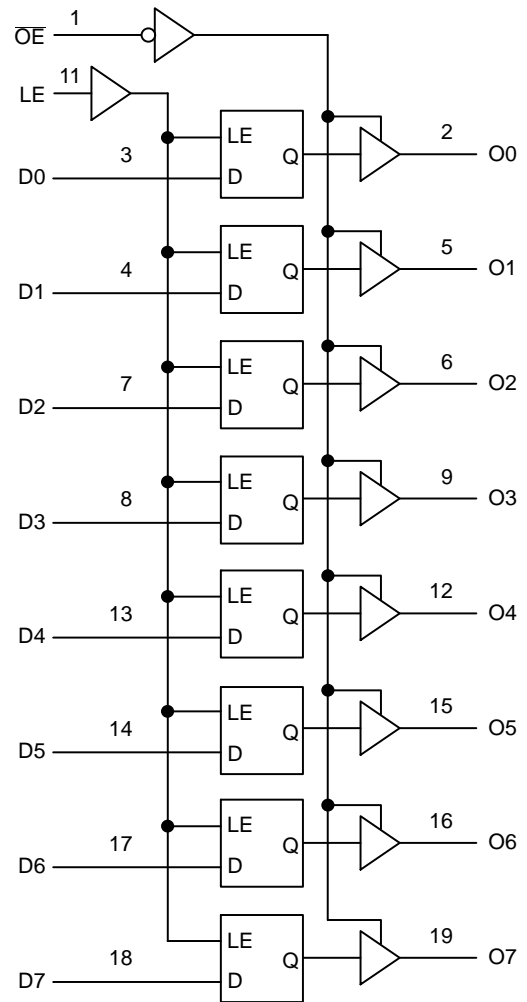


Figure 2. Logic Diagram

TRUTH TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition

NC = No Change, State Prior to the Latch Enable High-to-Low Transition

X = High or Low Voltage Level or Transitions are Acceptable

Z = High Impedance State

For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	2.0	2.5, 3.3	3.6	V
		1.5	2.5, 3.3	3.6	
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3-State)	0		V_{CC}	V
		0		5.5	
I_{OH}	HIGH Level Output Current $V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			-24	mA
				-12	
				-8	
I_{OL}	LOW Level Output Current $V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			+24	mA
				+12	
				+8	
T_A	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0 \text{ V}$	0		10	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Units
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _{OZ}	3-State Output Current	V _{CC} = 3.6 V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 0 to 5.5 V		±5	μA
I _{OFF}	Power Off Leakage Current	V _{CC} = 0, V _{IN} = 5.5 V or V _{OUT} = 5.5 V		10	μA
I _{IN}	Input Leakage Current	V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND		±5	μA
I _{CC}	Quiescent Supply Current	V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND		10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; R_L = 500 Ω)

Symbol	Parameter	Waveform	Limits						Units
			T _A = -40°C to +85°C						
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.5 V ± 0.2 V		
			C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	1	1.5 8.0	1.5 8.0	1.5 9.0	1.5 9.0	1.5 9.6	ns	
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	3	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	1.5 10.5		
t _{PZH} t _{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 8.5	1.5 8.5	1.5 9.5	1.5 9.5	1.5 10.5	ns	
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 7.5	1.5 7.5	1.5 8.5	1.5 8.5	1.5 9.0		
t _s	Setup Time, HIGH or LOW D _n to LE	3	2.5		2.5		4.0		
t _h	Hold Time, HIGH or LOW D _n to LE	3	1.5		1.5		2.0		
t _w	LE Pulse Width, HIGH	3	3.3		3.3		4.0		
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0				ns	

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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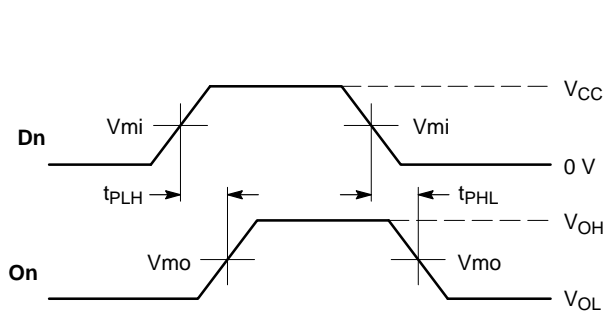
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Units
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.8 0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		-0.8 -0.6		V

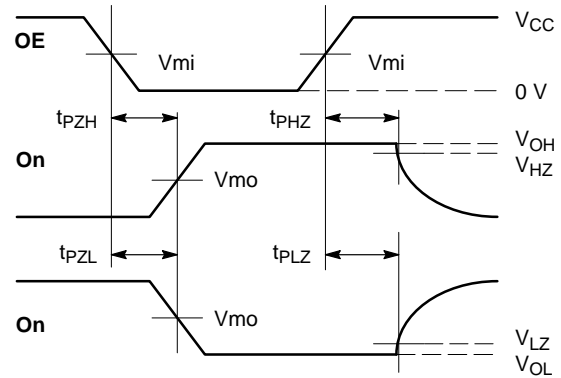
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

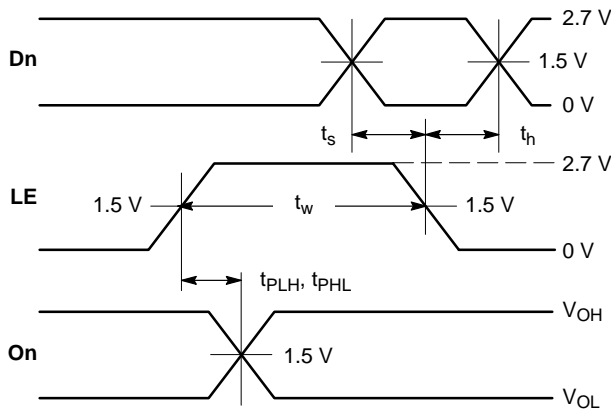
Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF



WAVEFORM 1 – PROPAGATION DELAYS
t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

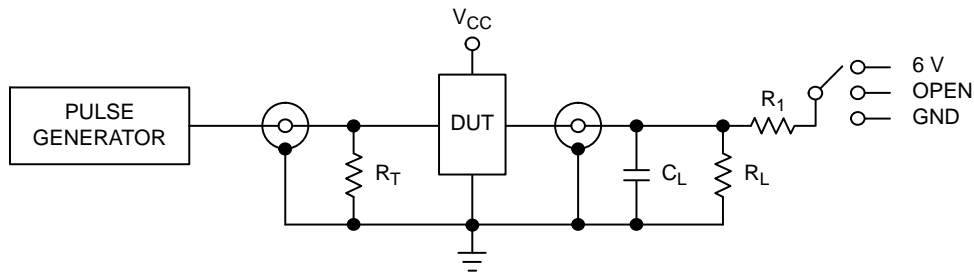


WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns except when noted

Symbol	V _{CC}		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
V _{mi}	1.5 V	1.5 V	V _{CC} /2
V _{mo}	1.5 V	1.5 V	V _{CC} /2
V _{HZ}	V _{OL} + 0.3 V	V _{OL} + 0.3 V	V _{OL} + 0.15 V
V _{LZ}	V _{OH} - 0.3 V	V _{OH} - 0.3 V	V _{OH} - 0.15 V

Figure 3. AC Waveforms

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TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3$ V 6 V at $V_{CC} = 2.5 \pm 0.2$ V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH} , t_{PHZ}	GND

$C_L = 50$ pF at $V_{CC} = 3.3 \pm 0.3$ V or equivalent (includes jig and probe capacitance)

$C_L = 30$ pF at $V_{CC} = 2.5 \pm 0.2$ V or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX373DWR2G	SOIC-20 WB (Pb-Free)	1000 Tape & Reel
MC74LCX373DTG	TSSOP-20 (Pb-Free)	75 Units / Rail
MC74LCX373DTR2G	TSSOP-20 (Pb-Free)	2500 Tape & Reel
NLV74LCX373DTR2G*	TSSOP-20 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

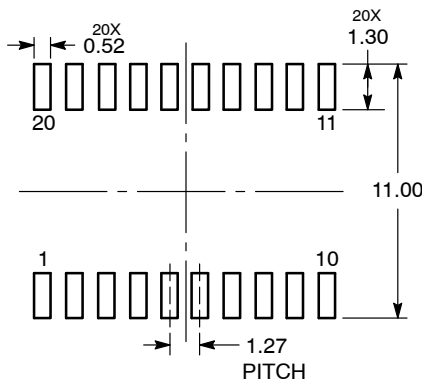


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

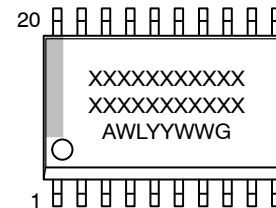
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

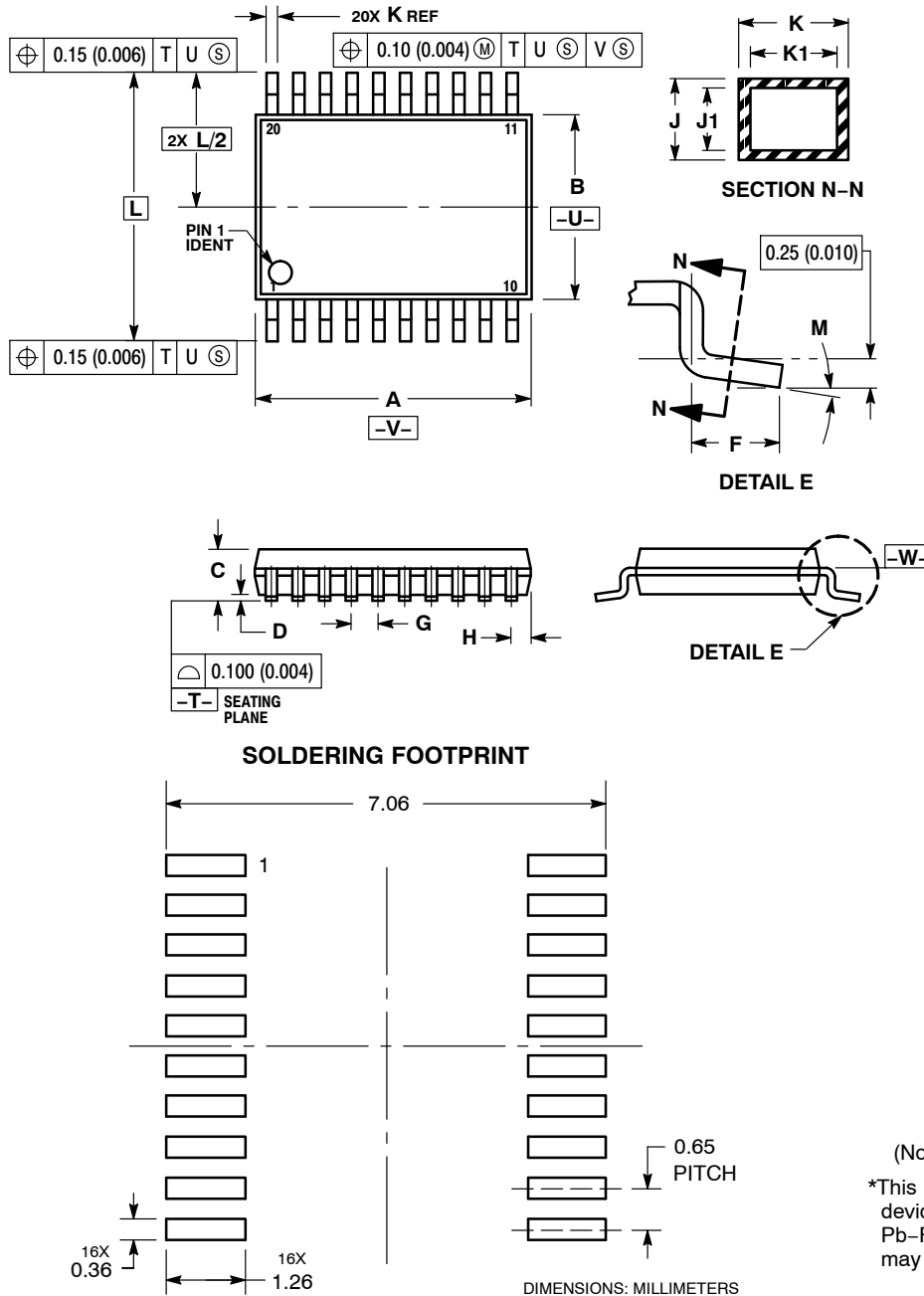
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TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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