

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# MC74LVX257

## Quad 2-Channel Multiplexer with 3-State Outputs

The MC74LVX257 is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology.

It consists of four 2-input digital multiplexers with common select (S) and enable ( $\overline{OE}$ ) inputs. When ( $\overline{OE}$ ) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 4.5$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant



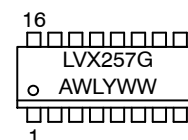
ON Semiconductor®

<http://onsemi.com>

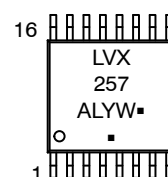
### MARKING DIAGRAMS



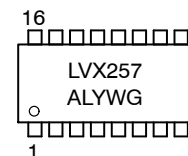
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
M SUFFIX  
CASE 966



LVX257 = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74LVX257

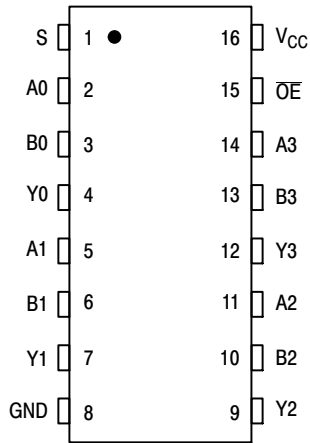


Figure 1. Pin Assignment

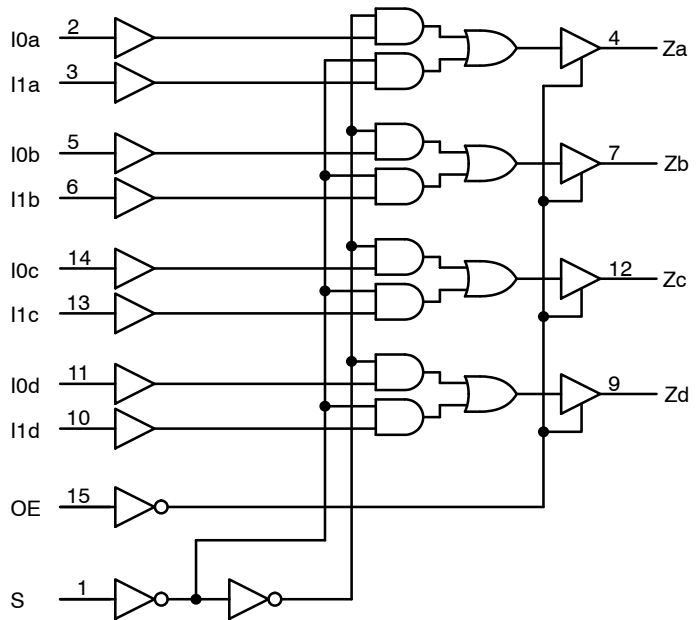


Figure 2. Expanded Logic Diagram

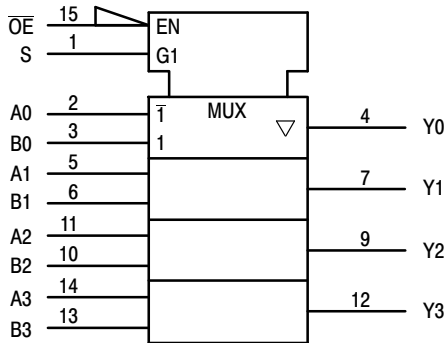


Figure 3. IEC Logic Symbol

## FUNCTION TABLE

Inputs		Outputs Y0 – Y3
OE	S	
H	X	Z
L	L	A0 – A3
L	H	B0 – B3

A0 – A3, B0 – B3 = the levels of the respective Data-Word Inputs.

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX257DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74LVX257DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX257DTG	TSSOP-16*	96 Units / Rail
MC74LVX257DTR2G	TSSOP-16*	2500 Tape & Reel
MC74LVX257MG	SOEIAJ-16	50 Units / Rail
MC74LVX257MELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74LVX257

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +7.0	V	
$V_{IN}$	Digital Input Voltage	-0.5 to +7.0	V	
$V_{OUT}$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V	
$I_{IK}$	Input Diode Current	-20	mA	
$I_{OK}$	Output Diode Current	$\pm 20$	mA	
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA	
$P_D$	Power Dissipation in Still Air	SOIC Package	200	mW
		TSSOP	180	
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$	
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 1)	>2000	V
		Machine Model (Note 2)	>200	
		Charged Device Model (Note 3)	>2000	
$I_{LATCHUP}$	Latchup Performance	Above $V_{CC}$ and Below GND at 125 $^{\circ}C$ (Note 4)	$\pm 300$	mA
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient	SOIC Package	143	$^{\circ}C/W$
		TSSOP	164	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, all Package Types	-40	85	$^{\circ}C$
$t_r, t_f$	Input Rise or Fall Time $V_{CC} = 3.3 V \pm 0.3 V$	0	100	ns/V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

# MC74LVX257

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 3.6	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>			0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 3.6			0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>		0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	3.6			±0.1		±1.0	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	1.0	1.0	2.0		40	μA

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.5 9.5	10.0 14.0	1.0 1.0	15.0 18.5	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		4.5 7.5	8.0 12.0	1.0 1.0	10.0 13.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, S to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		8.0 10.5	12.0 15.5	1.0 1.0	17.0 20.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.0 8.5	10.0 13.5	1.0 1.0	12.0 15.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Output Enable, Time, OE to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF R <sub>L</sub> = 1 kΩ    C <sub>L</sub> = 50pF		7.5 10.5	11.5 15.0	1.0 1.0	16.5 18.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF R <sub>L</sub> = 1 kΩ    C <sub>L</sub> = 50pF		5.5 8.5	9.5 13.0	1.0 1.0	11.5 15.0	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Output Disable, Time, OE to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 50pF R <sub>L</sub> = 1 kΩ		13.0	17.0	1.0	18.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 50pF R <sub>L</sub> = 1 kΩ		12	17.0	1.0	18.0	
C <sub>IN</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	<b>Typical @ 25°C, V<sub>CC</sub> = 3.3 V</b>						pF
		20						

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# MC74LVX257

**NOISE CHARACTERISTICS** Input  $t_r = t_f = 3.0$  ns,  $C_L = 50$  pF,  $V_{CC} = 3.3$  V

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.5	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

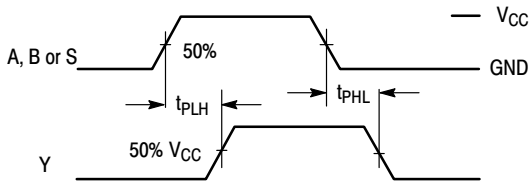


Figure 4. Switching Waveform

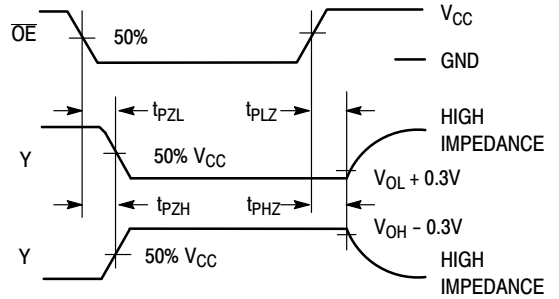
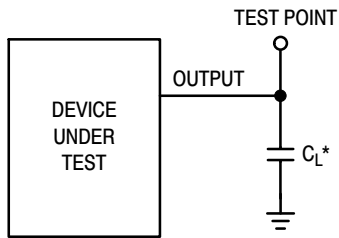
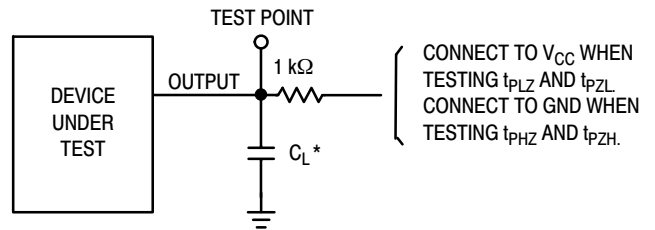


Figure 5. Switching Waveform



\*Includes all probe and jig capacitance

Figure 6. Test Circuit



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

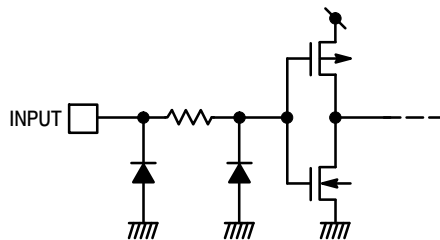
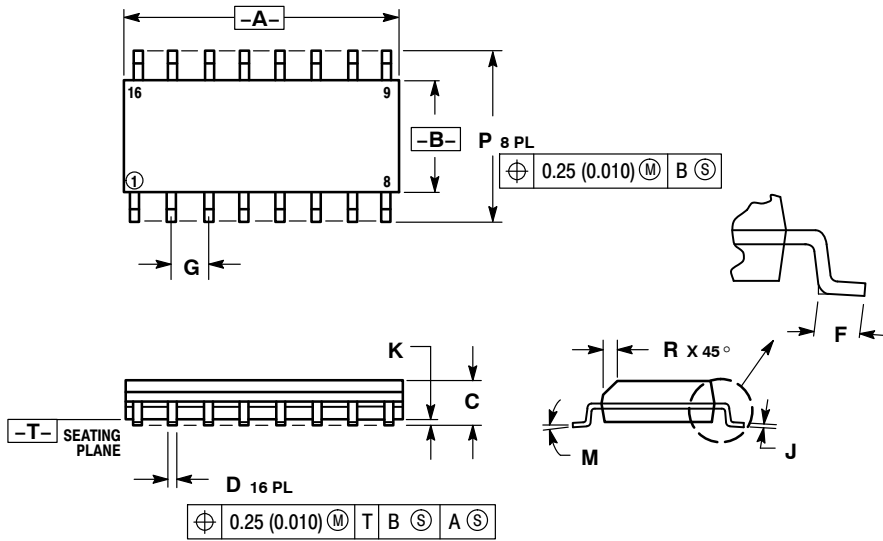


Figure 8. Input Equivalent Circuit

# MC74LVX257

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

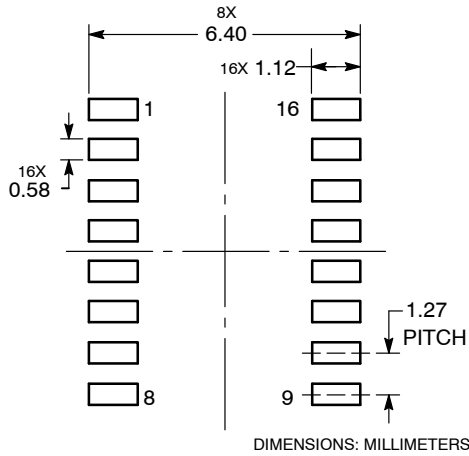


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

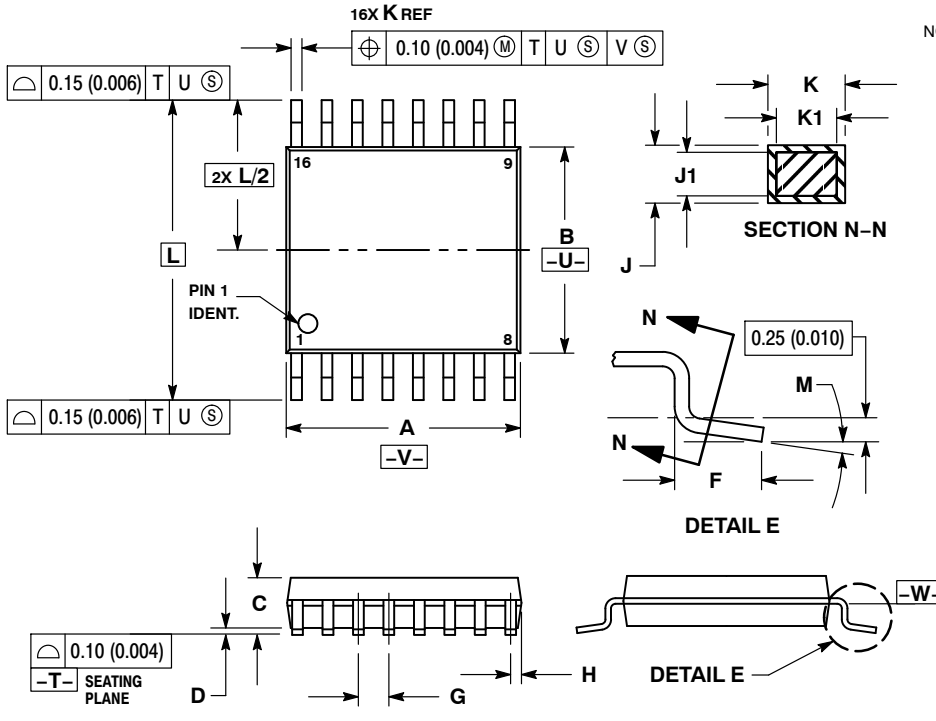
### SOLDERING FOOTPRINT



# MC74LVX257

## PACKAGE DIMENSIONS

TSSOP-16  
CASE 948F-01  
ISSUE B



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT

