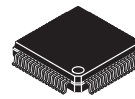


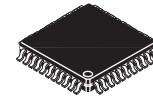


MC9S08GW64 Series

Covers: MC9S08GW64 and MC9S08GW32



80-LQFP
Case 917A
14 × 14



64-LQFP
Case 840F
10 × 10

comparator can be used as hardware breakpoint. Full mode, Comparator A compares address and Comparator B compares data. Supports both tag and force breakpoints

8-Bit HCS08 Central Processor Unit (CPU)

- New version of S08 core with same performance as traditional S08 and lower power
- Up to 20 MHz CPU at 3.6 V to 2.15 V and up to 10 MHz CPU at 3.6 V to 1.8 V, across temperature range of –40 °C to 85 °C
- HC08 instruction set with added BGND instruction
- Support for up to 48 interrupt/reset sources

On-Chip Memory

- Flash read/program/erase over full operating voltage and temperature
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and flash contents

Power-Saving Modes

- Two low power stop modes and reduced power wait mode
- Low power run and wait modes allow peripherals to run while voltage regulator is in standby
- Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
- Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
- 6 μs typical wakeup time from stop3 mode

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; Crystal or ceramic resonator of 32.768 kHz; Clock source for iRTC or ICS
- Oscillator (XOSC2) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz; optional clock source for ICS
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1, XOSC2); precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting CPU/bus frequencies from 1 MHz to 20 MHz

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage warning with interrupt
- Low-voltage detection with reset or interrupt
- Illegal opcode and illegal address detection with reset
- Flash block protection

Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus 3 more breakpoints in breakpoint unit)
- Breakpoint (BKPT) debug module containing three comparators (A, B, and C) with ability to match addresses in 64 KB space. Each

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Peripherals

- **LCD** — up to 4×40 or 8×36 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control
- **ADC16** — two analog-to-digital converters; 16-bit resolution; one dedicated differential per ADC; up to 16-ch; up to 2.5 μs conversion time for 12-bit mode; automatic compare function; hardware averaging; calibration registers; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
- **PRACMP** — three rail to rail programmable reference analog comparator; up to 8 inputs; on-chip programmable reference generator output; selectable interrupt on rising, falling, or either edge of comparator output; operation in stop3
- **SCI** — four full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge; SCI0 designed for AMR operation; TxD of SCI1 and SCI2 can be modulated with timers and RxD can be received through PRACMP;
- **SPI** — three full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting; SPI0 designed for AMR operation
- **IIC** — up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supporting broadcast mode and 10-bit addressing; supporting SM BUS functionality; can wake from stop3
- **FTM** — 2-channel flextimer module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **IRTC** — independent real-time clock, independent power domain, 32 bytes RAM, 32.768 kHz input clock optional output to ICS, hardware calendar, hardware compensation due to crystal or temperature characteristics, tamper detection and indicator
- **PCRC** — 16/32 bit programmable cyclic redundancy check for high-speed CRC calculation
- **MTIM** — two 8-bit and one 16-bit timers; configurable clock inputs and interrupt generation on overflow
- **PDB** — programmable delay block; optimized for scheduling ADC conversions
- **PCNT** — position counter; working in stop3 mode without waking CPU; can be used to generate waveforms like timer

Input/Output

- 57 GPIOs including one output-only pin
- Eight KBI interrupts with selectable polarity
- Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.

Package Options

- 80-pin LQFP, 64-pin LQFP

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Rev | Date | Description of Changes |
|-----|------------|---|
| 1 | 5/26/2010 | Initial public release |
| 2 | 10/29/2010 | Completed all the TBDs. Updated the voltage output data in the Table 20 . Changed the classification marking of I_{INT} to C in the Table 8 . |
| 3 | 1/28/2011 | Updated Table 7 . |

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08GW64RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 Devices in the MC9S08GW64 Series

Table 1 summarizes the feature set available in the MC9S08GW64 series of MCUs.

Table 1. MC9S08GW64 Series Features by MCU and Package

| Feature | MC9S08GW64 | | MC9S08GW32 | |
|---|--------------|--------------|--------------|--------------|
| | 80-pin LQFP | 64-pin LQFP | 80-pin LQFP | 64-pin LQFP |
| FLASH | 65,536 Bytes | | 32,768 Bytes | |
| RAM | 4,032 Bytes | | 2,048 Bytes | |
| ADC0 ¹ Single-ended Channels | 7-ch | 7-ch | 7-ch | 7-ch |
| ADC0 Differential Channels ² | 1 | 0 | 1 | 0 |
| ADC1 Single-ended Channels | 7-ch | 7-ch | 7-ch | 7-ch |
| ADC1 Differential Channels | 1 | 1 | 1 | 1 |
| BKPT | yes | | yes | |
| ICS | yes | | yes | |
| IIC | yes | | yes | |
| IRQ | yes | | yes | |
| IRTC | yes | | yes | |
| KBI | 8-ch | | 8-ch | |
| MTIM8 | 2 | | 2 | |
| MTIM16 | yes | | yes | |
| PCNT | yes | | yes | |
| PCRC | yes | | yes | |
| PDB | yes | | yes | |
| PRACMP | 3 | | 3 | |
| SCI | 4 | | 4 | |
| SPI | 3 | | 3 | |
| FTM | 2-ch | | 2-ch | |
| LCD | 8×36 4×40 | 8×24 4×28 | 8×36 4×40 | 8×24 4×28 |
| VREFO | yes | yes | yes | yes |
| XOSC | 2 | | 2 | |
| I/O pins ³ | 57 | 45 | 57 | 45 |

Devices in the MC9S08GW64 Series

- ¹ There are two 16-bit ADC modules, so two parallel conversions at two channels can be made simultaneously.
- ² Each differential channel consists of two pins (DADPx and DADMx).
- ³ The I/O pins include one output-only pin.

The block diagram in [Figure 1](#) shows the structure of the MC9S08GW64 series MCUs.

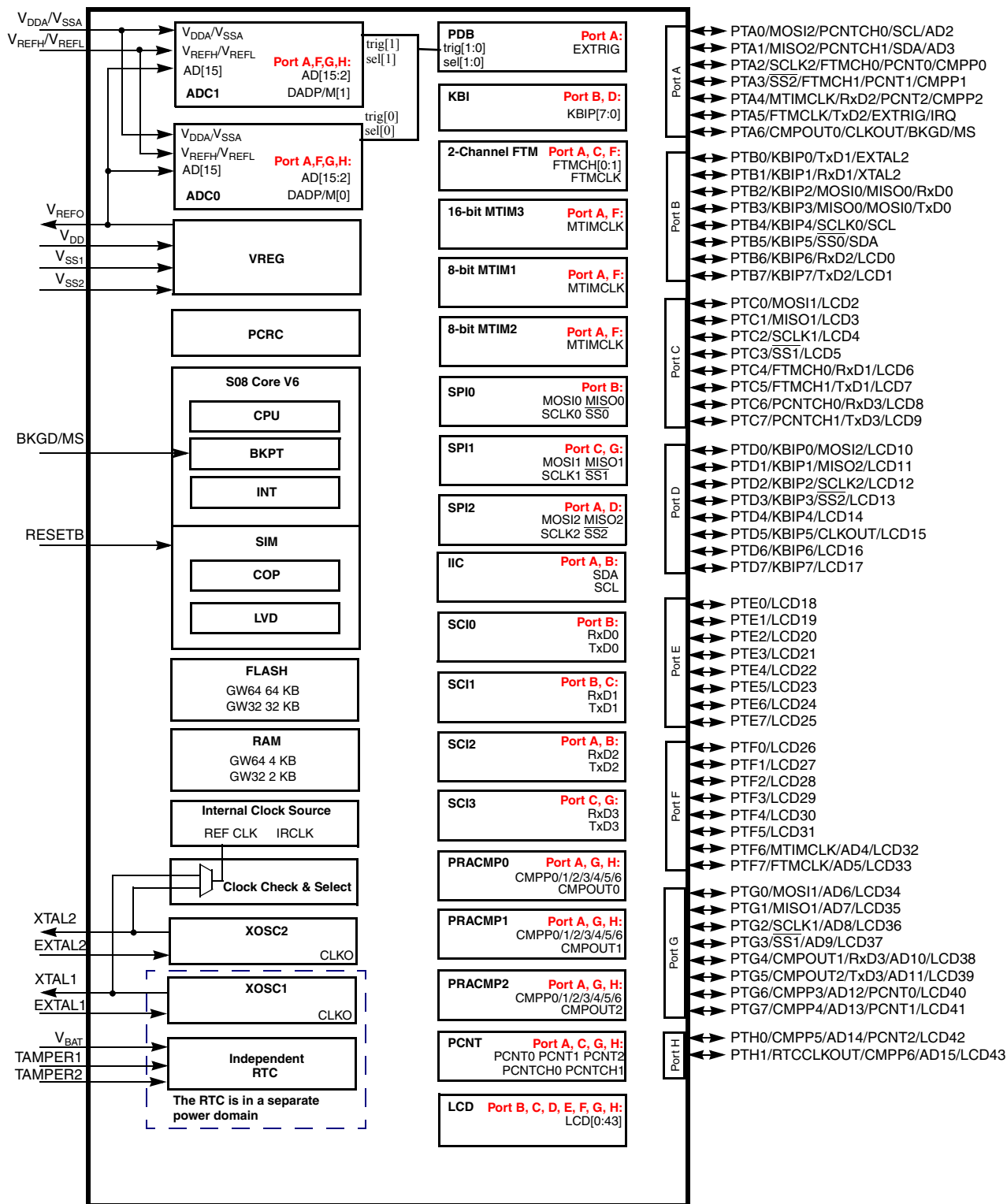


Figure 1. MC9S08GW64 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08GW64 series devices.

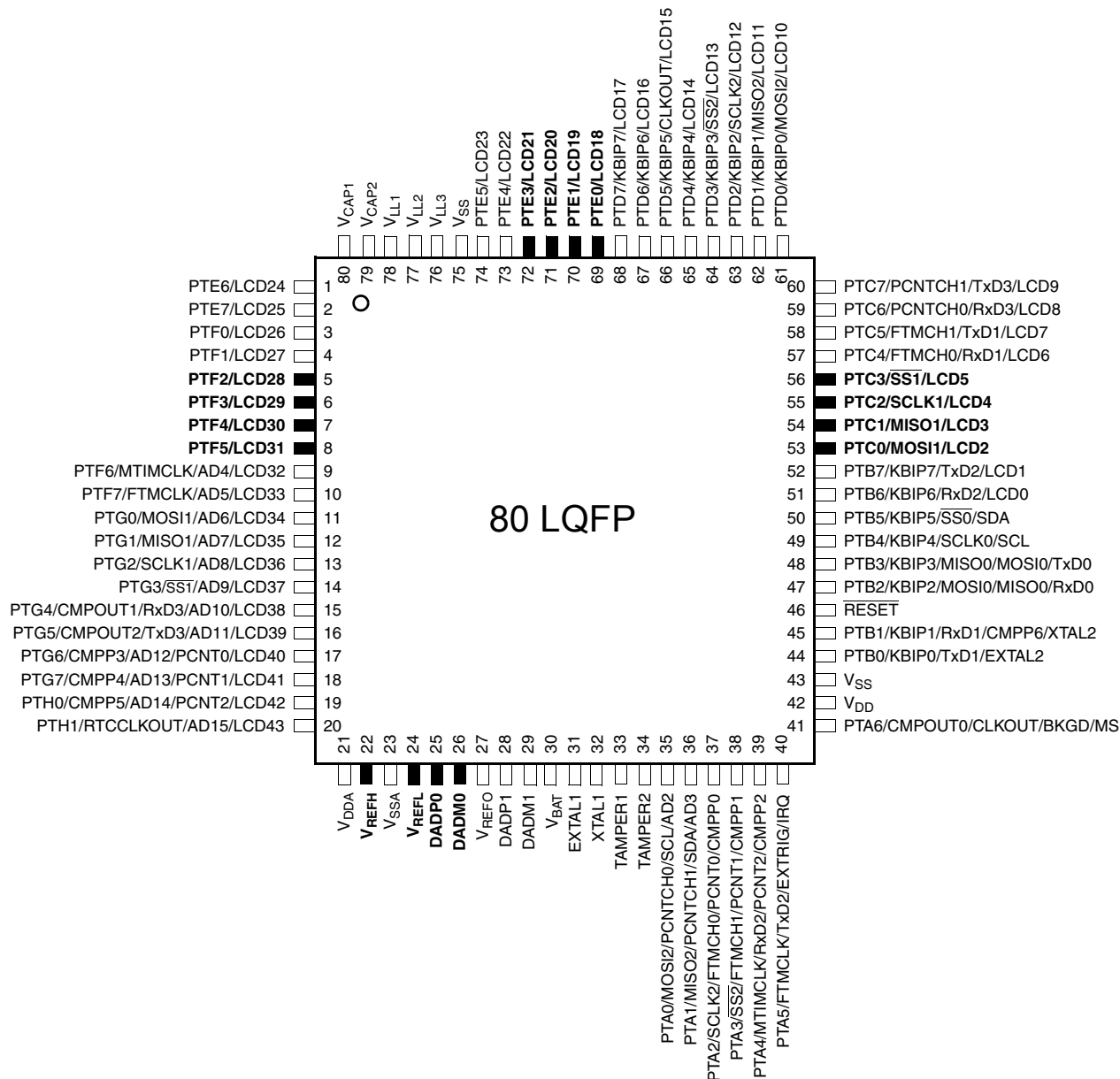


Figure 2. MC9S08GW64 Series in 80-Pin LQFP Package

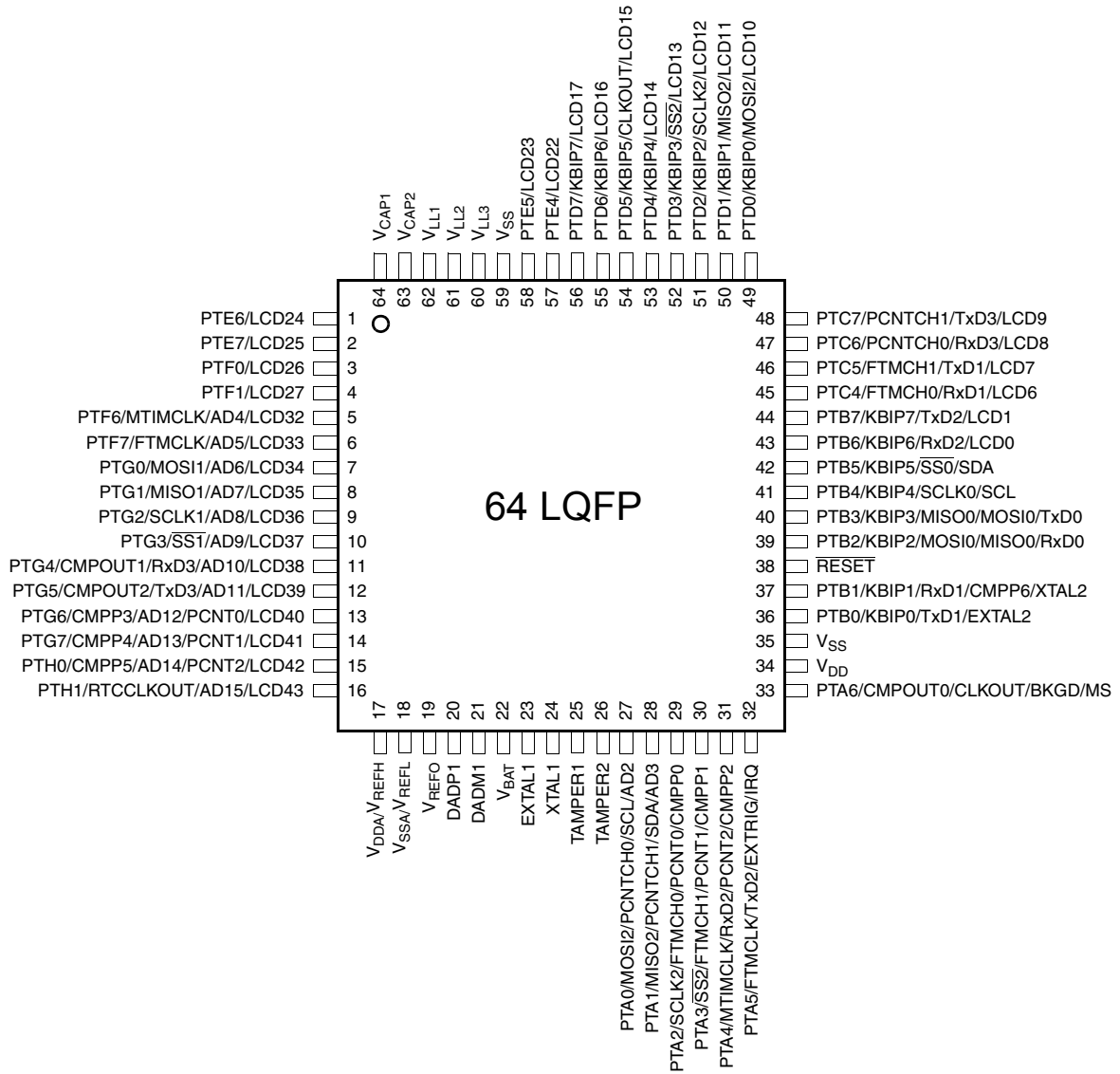


Figure 3. MC9S08GW64 Series in 64-Pin LQFP Package

Table 2. Pin Availability by Package Pin-Count

| 80 | 64 | Port Pin | Default func | Alt 1 | Alt 2 | Alt3 | Alt4 |
|----|----|----------|--------------|-------|-------|------|------|
| 1 | 1 | PTE6 | PTE6 | | LCD24 | | |
| 2 | 2 | PTE7 | PTE7 | | LCD25 | | |
| 3 | 3 | PTF0 | PTF0 | LCD26 | | | |
| 4 | 4 | PTF1 | PTF1 | LCD27 | | | |
| 5 | | PTF2 | PTF2 | LCD28 | | | |
| 6 | | PTF3 | PTF3 | LCD29 | | | |

Table 2. Pin Availability by Package Pin-Count (continued)

| 80 | 64 | Port Pin | Default func | Alt 1 | Alt 2 | Alt3 | Alt4 |
|----|----|----------------------|-------------------|------------------|---------|---------|-------|
| 7 | | PTF4 | PTF4 | LCD30 | | | |
| 8 | | PTF5 | PTF5 | LCD31 | | | |
| 9 | 5 | PTF6 | PTF6 | MTIMCLK | AD4 | LCD32 | |
| 10 | 6 | PTF7 | PTF7 | FTMCLK | AD5 | LCD33 | |
| 11 | 7 | PTG0 | PTG0 | MOSI1 | AD6 | LCD34 | |
| 12 | 8 | PTG1 | PTG1 | MISO1 | AD7 | LCD35 | |
| 13 | 9 | PTG2 | PTG2 | SCLK1 | AD8 | LCD36 | |
| 14 | 10 | PTG3 | PTG3 | $\overline{SS1}$ | AD9 | LCD37 | |
| 15 | 11 | PTG4 | PTG4 | CMPOUT1 | RxD3 | AD10 | LCD38 |
| 16 | 12 | PTG5 | PTG5 | CMPOUT2 | TxD3 | AD11 | LCD39 |
| 17 | 13 | PTG6 | PTG6 | CMPP3 | AD12 | PCNT0 | LCD40 |
| 18 | 14 | PTG7 | PTG7 | CMPP4 | AD13 | PCNT1 | LCD41 |
| 19 | 15 | PTH0 | PTH0 | CMPP5 | AD14 | PCNT2 | LCD42 |
| 20 | 16 | PTH1 | PTH1 | RTCCLKOUT | AD15 | LCD43 | |
| 21 | 17 | V _{DDA} | V _{DDA} | | | | |
| 22 | | V _{REFH} | V _{REFH} | | | | |
| 23 | 18 | V _{SSA} | V _{SSA} | | | | |
| 24 | | V _{REFL} | V _{REFL} | | | | |
| 25 | | DADP0 | DADP0 | | | | |
| 26 | | DADM0 | DADM0 | | | | |
| 27 | 19 | V _{REFO} | V _{REFO} | | | | |
| 28 | 20 | DADP1 | DADP1 | | | | |
| 29 | 21 | DADM1 | DADM1 | | | | |
| 30 | 22 | V _{BAT} | V _{BAT} | | | | |
| 31 | 23 | EXTAL1 | EXTAL1 | | | | |
| 32 | 24 | XTAL1 | XTAL1 | | | | |
| 33 | 25 | TAMPER1 ¹ | TAMPER1 | | | | |
| 34 | 26 | TAMPER2 | TAMPER2 | | | | |
| 35 | 27 | PTA0 | PTA0 | MOSI2 | PCNTCH0 | SCL | AD2 |
| 36 | 28 | PTA1 | PTA1 | MISO2 | PCNTCH1 | SDA | AD3 |
| 37 | 29 | PTA2 | PTA2 | SCLK2 | FTMCH0 | PCNT0 | CMPP0 |
| 38 | 30 | PTA3 | PTA3 | $\overline{SS2}$ | FTMCH1 | PCNT1 | CMPP1 |
| 39 | 31 | PTA4 | PTA4 | MTIMCLK | RxD2 | PCNT2 | CMPP2 |
| 40 | 32 | PTA5 ² | PTA5 | FTMCLK | TxD2 | EXTRIG | IRQ |
| 41 | 33 | PTA6 ³ | BKGD/MS | CMPOUT0 | CLKOUT | BKGD/MS | |

Table 2. Pin Availability by Package Pin-Count (continued)

| 80 | 64 | Port Pin | Default func | Alt 1 | Alt 2 | Alt3 | Alt4 |
|----|----|---------------------------|---------------------------|-------------------------|-------------------------|--------|-------|
| 42 | 34 | V _{DD} | V _{DD} | | | | |
| 43 | 35 | V _{SS} | V _{SS} | | | | |
| 44 | 36 | PTB0 | PTB0 | KBIP0 | TxD1 | EXTAL2 | |
| 45 | 37 | PTB1 ¹ | PTB1 | KBIP1 | RxD1 | CMPP6 | XTAL2 |
| 46 | 38 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ | | | | |
| 47 | 39 | PTB2 | PTB2 | KBIP2 | MOSI0 | MISO0 | RxD0 |
| 48 | 40 | PTB3 ⁴ | PTB3 | KBIP3 | MISO0 | MOSI0 | TxD0 |
| 49 | 41 | PTB4 ³ | PTB4 | KBIP4 | SCLK0 | SCL | |
| 50 | 42 | PTB5 ³ | PTB5 | KBIP5 | $\overline{\text{SS0}}$ | SDA | |
| 51 | 43 | PTB6 | PTB6 | KBIP6 | RxD2 | LCD0 | |
| 52 | 44 | PTB7 | PTB7 | KBIP7 | TxD2 | LCD1 | |
| 53 | | PTC0 | PTC0 | MOSI1 | LCD2 | | |
| 54 | | PTC1 | PTC1 | MISO1 | LCD3 | | |
| 55 | | PTC2 | PTC2 | SCLK1 | LCD4 | | |
| 56 | | PTC3 | PTC3 | $\overline{\text{SS1}}$ | LCD5 | | |
| 57 | 45 | PTC4 | PTC4 | FTMCH0 | RxD1 | LCD6 | |
| 58 | 46 | PTC5 | PTC5 | FTMCH1 | TxD1 | LCD7 | |
| 59 | 47 | PTC6 | PTC6 | PCNTCH0 | RxD3 | LCD8 | |
| 60 | 48 | PTC7 | PTC7 | PCNTCH1 | TxD3 | LCD9 | |
| 61 | 49 | PTD0 | PTD0 | KBIP0 | MOSI2 | LCD10 | |
| 62 | 50 | PTD1 | PTD1 | KBIP1 | MISO2 | LCD11 | |
| 63 | 51 | PTD2 | PTD2 | KBIP2 | SCLK2 | LCD12 | |
| 64 | 52 | PTD3 | PTD3 | KBIP3 | $\overline{\text{SS2}}$ | LCD13 | |
| 65 | 53 | PTD4 | PTD4 | KBIP4 | LCD14 | | |
| 66 | 54 | PTD5 | PTD5 | KBIP5 | CLKOUT | LCD15 | |
| 67 | 55 | PTD6 | PTD6 | KBIP6 | LCD16 | | |
| 68 | 56 | PTD7 | PTD7 | KBIP7 | LCD17 | | |
| 69 | | PTE0 | PTE0 | LCD18 | | | |
| 70 | | PTE1 | PTE1 | LCD19 | | | |
| 71 | | PTE2 | PTE2 | LCD20 | | | |
| 72 | | PTE3 | PTE3 | LCD21 | | | |
| 73 | 57 | PTE4 | PTE4 | | LCD22 | | |
| 74 | 58 | PTE5 | PTE5 | | LCD23 | | |
| 75 | 59 | V _{SS} | V _{SS} | | | | |
| 76 | 60 | V _{LL3} | V _{LL3} | | | | |

Table 2. Pin Availability by Package Pin-Count (continued)

| 80 | 64 | Port Pin | Default func | Alt 1 | Alt 2 | Alt3 | Alt4 |
|----|----|-------------------|-------------------|-------|-------|------|------|
| 77 | 61 | V _{LL2} | V _{LL2} | | | | |
| 78 | 62 | V _{LL1} | V _{LL1} | | | | |
| 79 | 63 | V _{CAP2} | V _{CAP2} | | | | |
| 80 | 64 | V _{CAP1} | V _{CAP1} | | | | |

¹ TAMPER0 pin is dedicatedly used for Battery Removal Tamper and not exposed on any SoC pins.

² PTA5 is with double drive strength.

³ PTA6 is an output-only pin when it is configured as GPIO.

⁴ PTB2, PTB3 and PTB4 are compatible with 5 V devices with a pullup device.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08GW64 sries of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

| | |
|----------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 4](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this

high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|--|-----------|------------------------|------|
| Supply voltage | V_{DD} | -0.3 to +3.8 | V |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Digital input voltage | V_{In} | -0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins except PTA5 and PTB1) ^{1, 2, 3} | I_D | ± 25 | mA |
| Instantaneous maximum current Single pin limit (applies to PTA5 and PTB1) ^{1, 2, 3} | I_D | ± 50 | mA |
| Storage temperature range | T_{stg} | -55 to 150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

| Rating | Symbol | Value | Unit |
|--|---------------|-----------------------------|------|
| Operating temperature range (packaged) | T_A | T_L to T_H -40 to 85 | °C |
| Maximum junction temperature | T_J | 95 | °C |
| Thermal resistance Single-layer board | | | |
| 80-pin LQFP | θ_{JA} | 61 | °C/W |
| 64-pin LQFP | | 70 | |
| Thermal resistance Four-layer board | | | |
| 80-pin LQFP | θ_{JA} | 48 | °C/W |
| 64-pin LQFP | | 52 | |

Electrical Characteristics

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|---------------------|-----------------------------|--------|-------|------|
| Human Body Model | Series resistance | R1 | 1500 | Ω |
| | Storage capacitance | C | 100 | pF |
| | Number of pulses per pin | — | 3 | |
| Charge Device Model | Series resistance | R1 | 0 | Ω |
| | Storage capacitance | C | 200 | pF |
| | Number of pulses per pin | — | 3 | |
| Latch-up | Minimum input voltage limit | | -2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

Table 7. ESD and Latch-Up Protection Characteristics

| No. | Rating ¹ | Symbol | Min | Max | Unit |
|-----|---|-----------|-------------|-----|------|
| 1 | Human body model (HBM) | V_{HBM} | ± 2000 | — | V |
| 2 | Machine Model (MM) | V_{MM} | ± 200 | — | V |
| 3 | Charge device model (CDM) | V_{CDM} | ± 500 | — | V |
| 4 | Latch-up current at $T_A = 85^\circ\text{C}$ (applies to all pins except pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to all pins except pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package) | I_{LAT} | $\pm 100^2$ | — | mA |
| | Latch-up current at $T_A = 85^\circ\text{C}$ (applies to pin 31EXTAL1 and pin 30 XTAL1 in 80-pin package, applies to pin 23 EXTAL1 and pin 24 XTAL1 in 64-pin package) | I_{LAT} | $\pm 62^3$ | — | mA |

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

² These pins meet JESD78A Class II (section 1.2) Level A (section 1.3) requirement of $\pm 100\text{mA}$.

³ This pin meets JESD78A Class II (section 1.2) Level B (section 1.3) characterization to $\pm 62\text{mA}$.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

| Num | C | Characteristic | Symbol | Condition | Min | Typ ¹ | Max | Unit |
|-----|---|--|-----------|--|----------------|------------------|-----|------|
| 1 | | Operating Voltage | | | 1.8 | | 3.6 | V |
| 2 | C | Output high voltage All non-LCD pins low-drive strength | V_{OH} | $V_{DD} > 1.8\text{ V}$ $I_{Load} = -0.6\text{ mA}$ | $V_{DD} - 0.5$ | — | — | V |
| | P | All non-LCD pins high-drive strength | | $V_{DD} > 2.7\text{ V}$ $I_{Load} = -10\text{ mA}$ | $V_{DD} - 0.5$ | — | — | |
| | C | | | $V_{DD} > 1.8\text{ V}$ $I_{Load} = -3\text{ mA}$ | $V_{DD} - 0.5$ | — | — | |
| 3 | C | Output high voltage All LCD/GPIO pins low-drive strength | V_{OH} | $V_{DD} > 1.8\text{ V}$ $I_{Load} = -0.5\text{ mA}$ | $V_{DD} - 0.5$ | — | — | V |
| | P | All LCD/GPIO pins high-drive strength | | $V_{DD} > 2.7\text{ V}$ $I_{Load} = -2.5\text{ mA}$ | $V_{DD} - 0.5$ | — | — | |
| | C | | | $V_{DD} > 1.8\text{ V}$ $I_{Load} = -1\text{ mA}$ | $V_{DD} - 0.5$ | — | — | |
| 4 | D | Output high current Max total I_{OH} for all ports | I_{OHT} | | — | — | 100 | mA |

Table 8. DC Characteristics (continued)

| Num | C | Characteristic | Symbol | Condition | Min | Typ ¹ | Max | Unit |
|-----|---|--|------------------------|---|----------------------|------------------|----------------------|------------------|
| 5 | C | Output low voltage All non-LCD pins low-drive strength | V_{OL} | $V_{DD} > 1.8\text{ V}$ $I_{Load} = 0.6\text{ mA}$ | — | — | 0.5 | V |
| | P | All non-LCD pins high-drive strength | | $V_{DD} > 2.7\text{ V}$ $I_{Load} = 10\text{ mA}$ | — | — | 0.5 | |
| | C | | | $V_{DD} > 1.8\text{ V}$ $I_{Load} = 3\text{ mA}$ | — | — | 0.5 | |
| 6 | C | Output low voltage All LCD/GPIO pins low-drive strength | V_{OL} | $V_{DD} > 1.8\text{ V}$ $I_{Load} = 0.5\text{ mA}$ | — | — | 0.5 | V |
| | P | All LCD/GPIO pins high-drive strength | | $V_{DD} > 2.7\text{ V}$ $I_{Load} = 3\text{ mA}$ | — | — | 0.5 | |
| | C | | | $V_{DD} > 1.8\text{ V}$ $I_{Load} = 1\text{ mA}$ | — | — | 0.5 | |
| 7 | D | Output low current Max total I_{OL} for all ports | I_{OLT} | | — | — | 100 | mA |
| 8 | P | Input high voltage all digital inputs | V_{IH} | $V_{DD} > 2.7\text{ V}$ | $0.70 \times V_{DD}$ | — | — | V |
| | C | | | $V_{DD} > 1.8\text{ V}$ | $0.85 \times V_{DD}$ | — | — | |
| 9 | P | Input low voltage all digital inputs | V_{IL} | $V_{DD} > 2.7\text{ V}$ | — | — | $0.35 \times V_{DD}$ | |
| | C | | | $V_{DD} > 1.8\text{ V}$ | — | — | $0.30 \times V_{DD}$ | |
| 10 | C | Input hysteresis all digital inputs | V_{hys} | | $0.06 \times V_{DD}$ | — | — | mV |
| 11 | P | Input leakage current all input only pins (per pin) | $ I_{in} $ | $V_{in} = V_{DD}$ or V_{SS} | — | 0.025 | 1 | μA |
| 12 | P | Hi-Z (off-state) leakage current all input/output (per pin) | $ I_{OZ} $ | $V_{in} = V_{DD}$ or V_{SS} | — | 0.025 | 1 | μA |
| 13 | C | Total leakage current ² Total leakage current for all pins | $ I_{inT} $ | $V_{in} = V_{DD}$ or V_{SS} | — | — | 2 | μA |
| 14 | P | Pullup, Pulldown resistors all digital inputs, when enabled | R_{PU} , R_{PD} | | 17.5 | — | 52.5 | $\text{k}\Omega$ |
| 15 | P | Pullup, Pulldown resistors all digital inputs, when enabled | R_{PU} , R_{PD} | | 17.5 | — | 52.5 | $\text{k}\Omega$ |
| 16 | D | DC injection current ^{3, 4, 5} Single pin limit Total MCU limit, includes sum of all stressed pins | I_{IC} | $V_{in} < V_{SS}$, $V_{in} > V_{DD}$ | -0.2 | — | 0.2 | mA |
| | | | | | -5 | — | 5 | mA |
| 17 | C | Input Capacitance, all pins | C_{in} | | — | — | 8 | pF |
| 18 | C | RAM retention voltage | V_{RAM} | | — | 0.6 | 1.0 | V |
| 19 | C | iRTC RAM retention voltage | V_{iRAM} | | — | 1.05 | — | V |
| 20 | C | POR re-arm voltage ⁶ | V_{POR} | | 0.9 | 1.4 | 2.0 | V |
| 21 | D | POR re-arm time | t_{POR} | | 10 | — | — | μs |

Table 8. DC Characteristics (continued)

| Num | C | Characteristic | Symbol | Condition | Min | Typ ¹ | Max | Unit |
|-----|---|--|------------|-------------------------------|------|------------------|------|------|
| 22 | C | Low-voltage detection threshold | V_{LVDH} | High range — V_{DD} falling | 2.11 | 2.16 | 2.22 | V |
| | | High range — V_{DD} rising | | 2.16 | 2.23 | 2.27 | | |
| 23 | C | Low-voltage detection threshold | V_{LVDL} | Low range — V_{DD} falling | 1.80 | 1.85 | 1.91 | V |
| | | Low range — V_{DD} rising | | 1.86 | 1.92 | 1.99 | | |
| 24 | C | Low-voltage warning threshold | V_{LVWH} | V_{DD} falling, LVWV = 1 | 2.36 | 2.46 | 2.56 | V |
| | | V_{DD} rising, LVWV = 1 | | 2.52 | 2.49 | 2.71 | | |
| 25 | C | Low-voltage warning | V_{LVWL} | V_{DD} falling, LVWV = 0 | 2.10 | 2.16 | 2.23 | V |
| | | V_{DD} rising, LVWV = 0 | | 2.15 | 2.23 | 2.26 | | |
| 26 | C | Low-voltage inhibit reset/recover hysteresis | V_{hys} | | — | 80 | — | mV |
| 27 | P | Bandgap Voltage Reference ⁷ | V_{BG} | | 1.15 | 1.17 | 1.19 | V |

¹ Typical values are measured at 25°C. Characterized, not tested

² Total leakage current is the sum value for all GPIO pins. This leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250nA.

³ All functional non-supply pins, except for PTB2 are internally clamped to V_{SS} and V_{DD} .

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ POR will occur below the minimum voltage.

⁷ Factory trimmed at $V_{DD} = 3.0$ V, Temp = 25°C

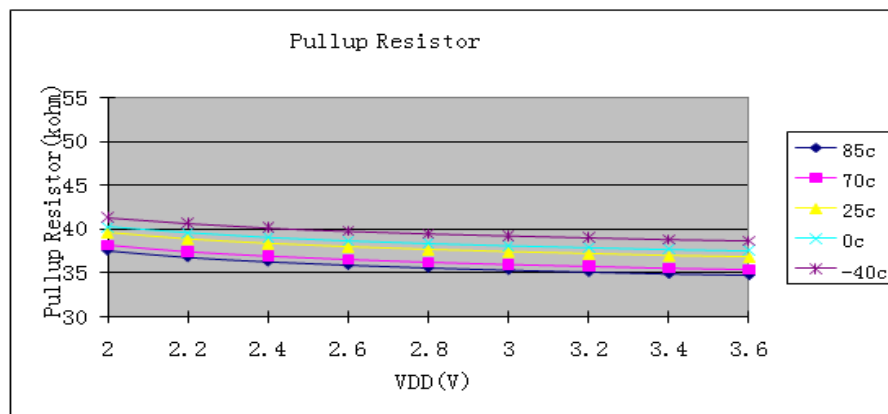


Figure 4. Non LCD pins I/O Pullup Typical Resistor Values

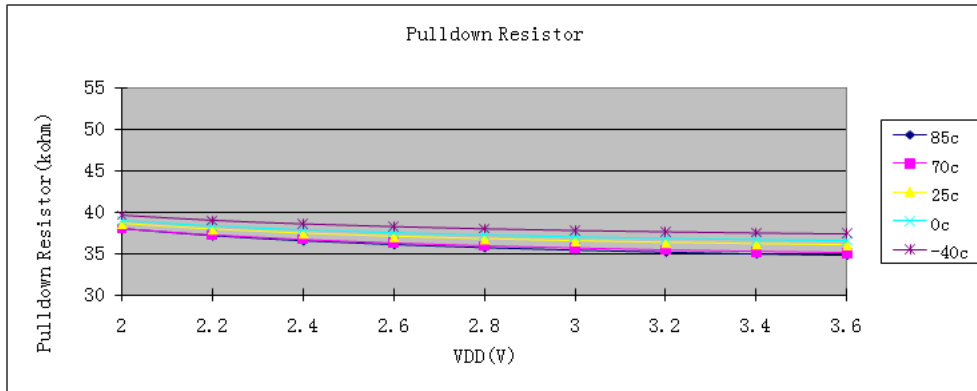


Figure 5. Non LCD pins I/O Pull-down Typical Resistor Values

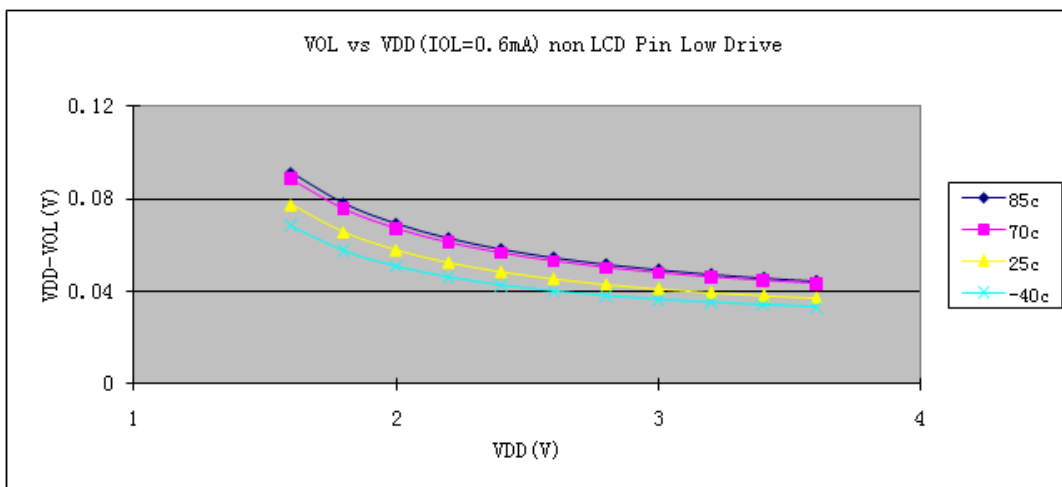
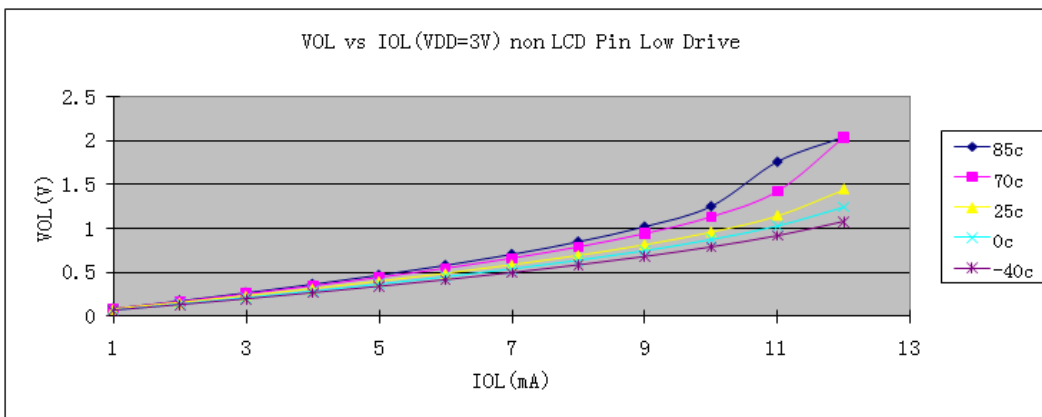


Figure 6. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — Low Drive (PTxDSn = 0)

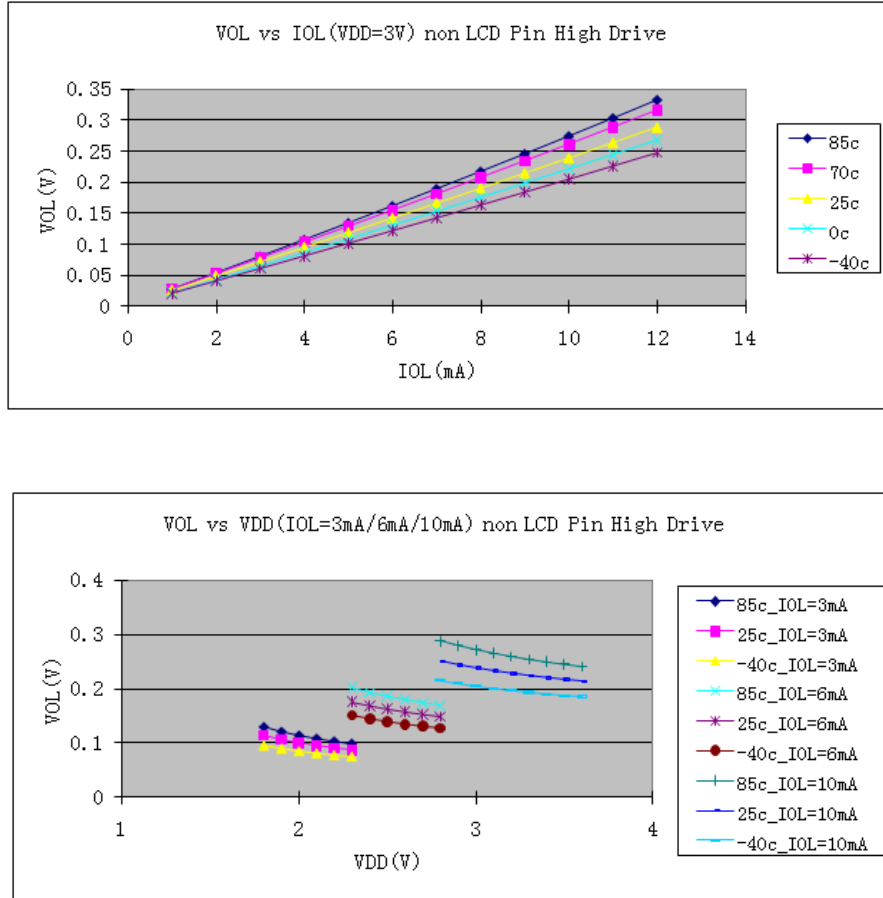


Figure 7. Typical Low-Side Driver (Sink) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

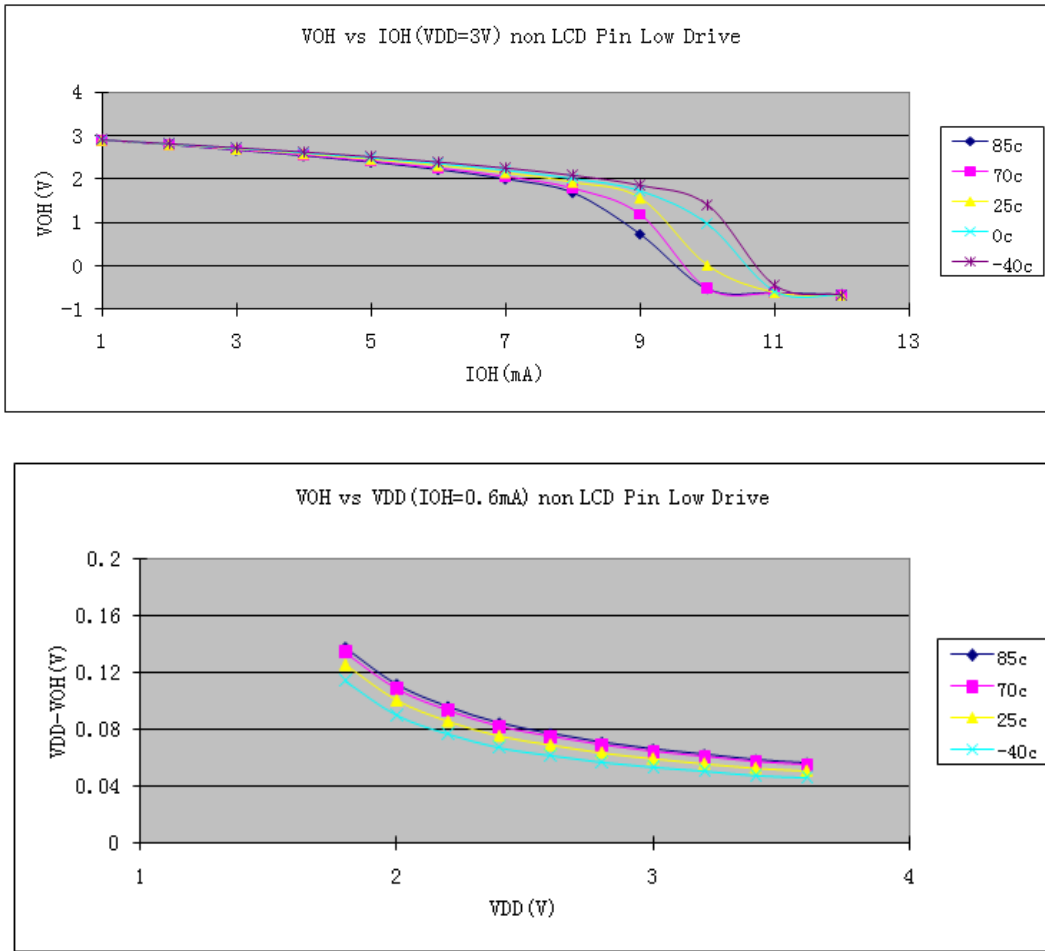


Figure 8. Typical High-Side (Source) Characteristics (Non LCD pins)— Low Drive (PTxDSn = 0)

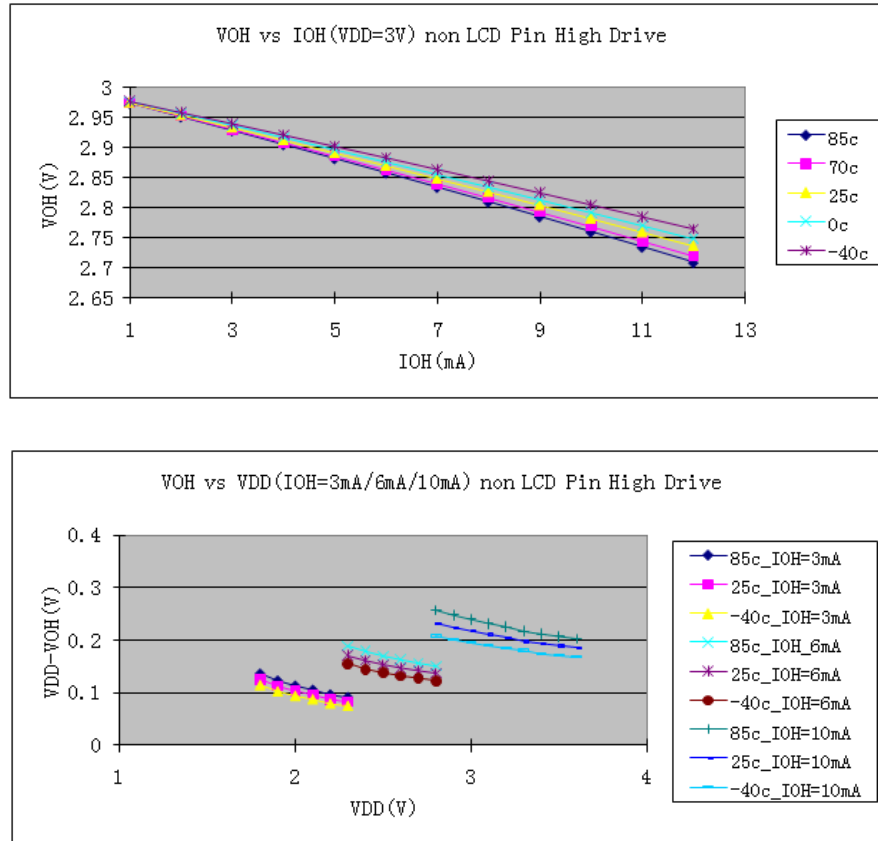


Figure 9. Typical High-Side (Source) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

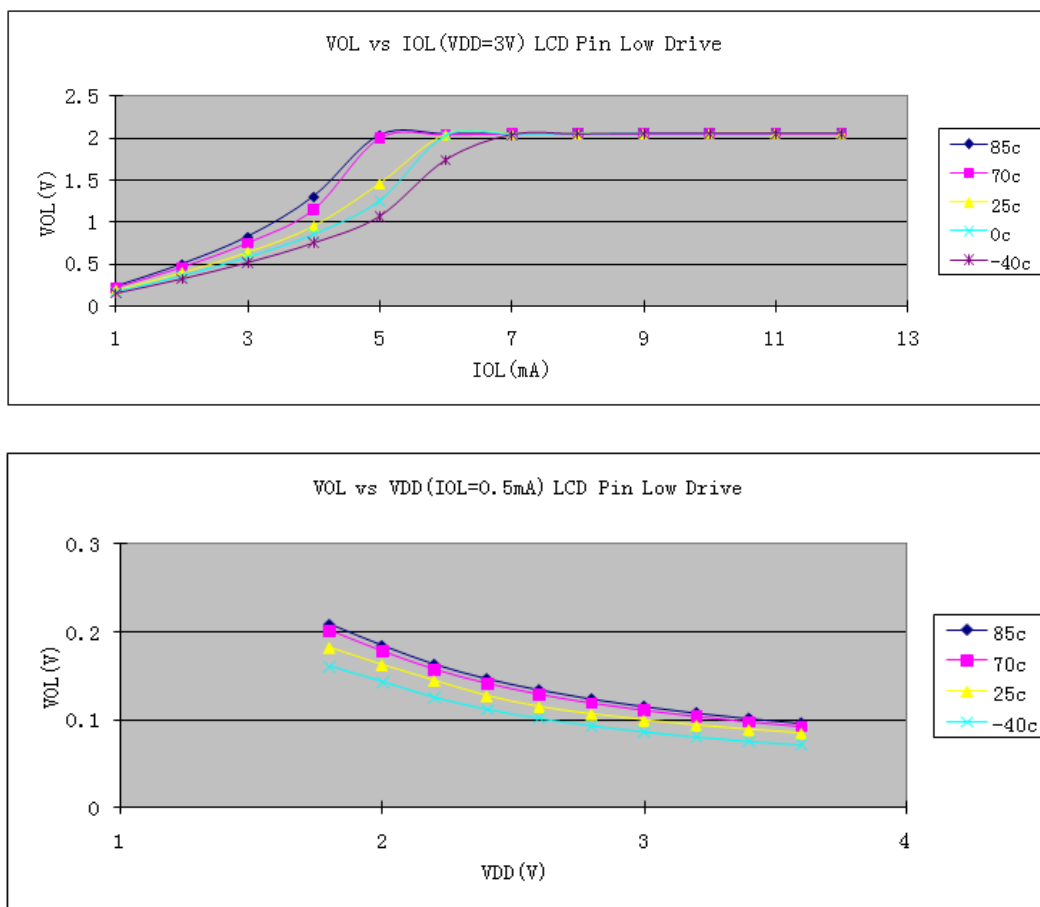


Figure 10. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — Low Drive (PTxDSn = 0)

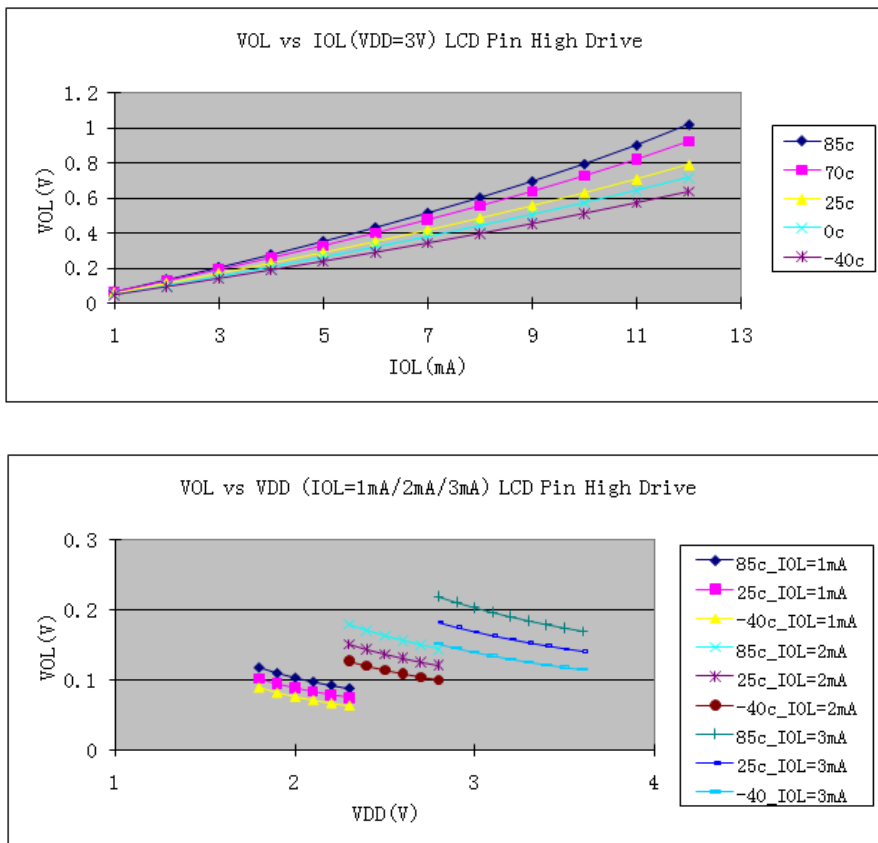


Figure 11. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

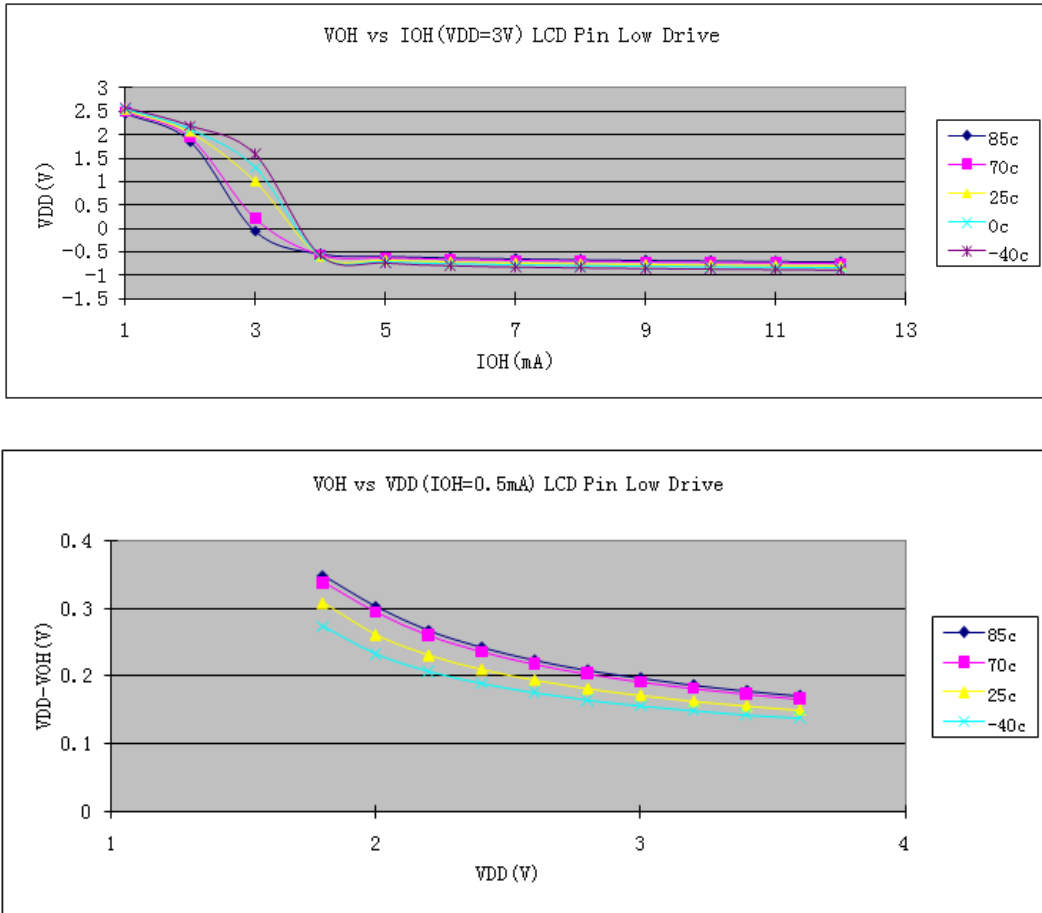


Figure 12. Typical High-Side (Source) Characteristics (LCD/GPIO pins)— Low Drive (PTxDSn = 0)

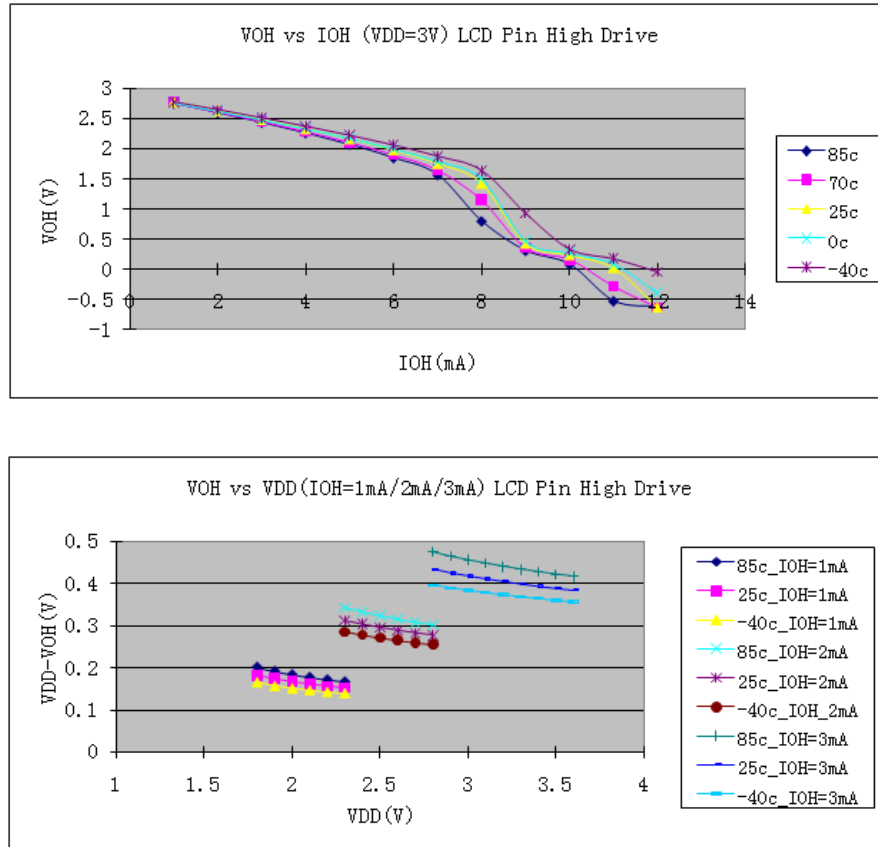


Figure 13. Typical High-Side (Source) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

| Num | C | Parameter | Symbol | Bus Freq | V _{DD} (V) | Typ ¹ | Max | Unit | Temp (°C) |
|-----|---|--|------------------|-----------------|---------------------|------------------|------|------|-------------|
| 1 | C | Run supply current FEI mode, all modules on, running from Flash | R _{IDD} | 20 MHz | 3 | 17.4 | 20.5 | mA | -40 to 85°C |
| | T | | | 2 MHz | | 2.6 | — | | |
| 2 | C | Run supply current FEI mode, all modules off, running from Flash | R _{IDD} | 20 MHz | 3 | 10.5 | — | mA | -40 to 85°C |
| | T | | | 2 MHz | | 1.6 | — | | |
| 3 | T | Run supply current LPRS=0, all modules off, running from Flash | R _{IDD} | 16 kHz FBILP | 3 | 158 | — | μA | -40 to 85°C |
| | T | | | 16 kHz FBELP | | 148 | — | | |
| 4 | T | Run supply current LPRS=1, all modules off; running from Flash | R _{IDD} | 16 kHz FBILP | 3 | 160 | — | μA | -40 to 85°C |
| | T | | | 16 kHz FBELP | | 23 | — | | |

Table 9. Supply Current Characteristics

| Num | C | Parameter | Symbol | Bus Freq | V _{DD} (V) | Typ ¹ | Max | Unit | Temp (°C) |
|-----|---|---|--------------------|--------------|---------------------|------------------|------|------|-------------|
| 5 | T | Run supply current LPRS=1, all modules off; running from RAM | R _I DD | 16 kHz FBILP | 3 | 137 | — | μA | -40 to 85°C |
| | T | | | 16 kHz FBELP | | 8 | — | | |
| 6 | C | Wait mode supply current, all modules off | W _I DD | 20 MHz | 3 | 5.4 | 7.5 | mA | -40 to 85°C |
| | C | | | 2 MHz | | 1.1 | — | | |
| 7 | T | Wait mode supply current LPRS = 0, all modules off | W _I DD | 16 kHz FBILP | 3 | 131 | — | μA | -40 to 85°C |
| | T | | | 16 kHz FBELP | 3 | 123 | — | | |
| 8 | T | Wait mode supply current LPRS = 1, all modules off | W _I DD | 16 kHz FBILP | 3 | 159 | — | μA | -40 to 85°C |
| | T | | | 16 kHz FBELP | 3 | 5.6 | — | | |
| 9 | C | Stop2 mode supply current | S2 _I DD | N/A | 3 | 330 | 1000 | nA | -40 to 25°C |
| | | | | | | 1622 | — | | 70°C |
| | | | | | | 6000 | — | | 85°C |
| | C | | | N/A | 2 | — | — | | -40 to 25°C |
| | | | | | | — | — | | 70°C |
| | | | | | | — | — | | 85°C |
| 10 | C | Stop3 mode supply current No clocks active | S3 _I DD | N/A | 3 | 474 | 1100 | nA | -40 to 25°C |
| | | | | | | 2608 | — | | 70°C |
| | | | | | | 9000 | — | | 85°C |
| | C | | | N/A | 2 | — | — | | -40 to 25°C |
| | | | | | | — | — | | 70°C |
| | | | | | | — | — | | 85°C |

¹ Typical values are measured at 25°C. Characterized, not tested.

Table 10. Stop Mode Adders (V_{DD}=3V, V_{DDA}=V_{DD})

| Num | C | Parameter | Condition | Temperature (°C) | | | | Units |
|-----|---|-----------------------|---|------------------|-----|-----|-----|-------|
| | | | | -40 | 25 | 70 | 85 | |
| 1 | C | LPO | | 100 | 100 | 150 | 175 | nA |
| 2 | C | ERREFSTEN | RANGE = HGO = 0 | 600 | 737 | 830 | 863 | nA |
| 3 | C | IREFSTEN ¹ | | — | 73 | 80 | 92 | μA |
| 4 | C | LVD ¹ | LVDSE = 1 | 110 | 112 | 112 | 113 | μA |
| 5 | C | PRACMP ¹ | Not using the bandgap (BGBE = 0), PRG enabled | 30 | 35 | 40 | 55 | μA |

Table 10. Stop Mode Adders (continued)($V_{DD}=3V$, $V_{DDA}=V_{DD}$)

| Num | C | Parameter | Condition | Temperature (°C) | | | | Units |
|-----|---|-------------------|---|------------------|------|------|------|-------|
| | | | | -40 | 25 | 70 | 85 | |
| 6 | C | VREFO | Not using the bandgap (BGBE = 0), in tight regulation mode | 264 | 286 | 296 | 298 | μA |
| 7 | C | IRTC | | 1.4 | 1.65 | 2.01 | 2.27 | μA |
| 8 | C | ADC ¹ | ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0), single conversion | 78.1 | 88.5 | 92.6 | 93.6 | μA |
| 9 | C | LCD | VIREG enabled for Contrast control, 1/8 Duty cycle, 8x24 configuration for driving 192 Segments, 32Hz frame rate, No LCD glass connected. | 0.67 | 0.88 | 3.74 | 7.16 | μA |
| 10 | C | PCNT ¹ | 32KHz clock, without PWM output | 33 | 47 | 67 | 77 | nA |
| 11 | C | PCNT ¹ | 32KHz clock, with PWM output | 40 | 50 | 63 | 77 | nA |

¹ Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference [Figure 14](#) and [Figure 15](#) for crystal or resonator circuits.

Table 11. XOSCVLP and ICS Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|---|----------------------------------|--|------------------------------|------------------------------|-------------------|
| 1 | C | Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0) | f_{lo} f_{hi} f_{hi} | 32 1 1 | — — — | 38.4 16 8 | kHz MHz MHz |
| 2 | D | Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings | C_1, C_2 | See Note ² See Note ³ | | | |
| 3 | D | Feedback resistor Low range, low power (RANGE=0, HGO=0) ² Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X) | R_F | — — — | — 10 1 | — — — | MΩ |
| 4 | D | Series resistor — Low range, low power (RANGE = 0, HGO = 0) ² Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz | R_S | — — — — — — | — 100 0 0 0 0 | — — — 0 10 20 | kΩ |
| 5 | C | Crystal start-up time ⁴ Low range, low power Low range, high gain High range, low power High range, high gain | t_{CSTL} t_{CSTH} | — — — — | 600 400 5 15 | — — — — | ms |
| 6 | D | Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode | f_{extal} | 0.03125 0 | — — | 20 20 | MHz MHz |

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

³ See crystal or resonator manufacturer's recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

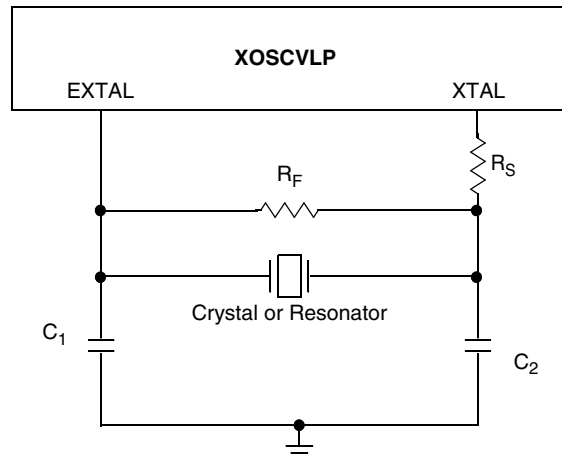


Figure 14. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

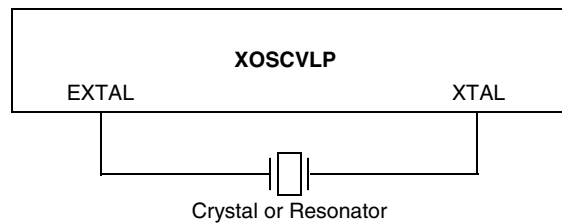


Figure 15. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|---|--------------------------|-------|------------------|--------|-------------|
| 1 | P | Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C | f_{int_ft} | — | 32.768 | — | kHz |
| 2 | P | Average internal reference frequency - trimmed | f_{int_t} | 31.25 | — | 39.063 | kHz |
| 3 | T | Internal reference start-up time | t_{IRST} | — | — | 6 | μs |
| 4 | P | DCO output frequency range - untrimmed | f_{dco_ut} | 12.8 | 16.8 | 21.33 | MHz |
| 5 | P | DCO output frequency range - trimmed | f_{dco_t} | 16 | — | 20 | MHz |
| 6 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) | $\Delta f_{dco_res_t}$ | — | ± 0.1 | ± 0.2 | % f_{dco} |
| 7 | C | Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) | $\Delta f_{dco_res_t}$ | — | ± 0.2 | ± 0.4 | % f_{dco} |
| 8 | C | Total deviation from trimmed DCO output frequency over voltage and temperature | Δf_{dco_t} | — | + 0.5 - 1.0 | ± 2 | % f_{dco} |

Table 12. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient) (continued)

| Num | C | Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|--|---------------------|-----|------------------|-----|-------------|
| 9 | C | Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C | Δf_{dco_t} | — | ± 0.5 | ± 1 | % f_{dco} |
| 10 | C | FLL acquisition time ² | $t_{Acquire}$ | — | — | 1 | ms |
| 11 | C | Long term jitter of DCO output clock (averaged over 2-ms interval) ³ | C_{Jitter} | — | 0.02 | 0.2 | % f_{dco} |

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

³ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

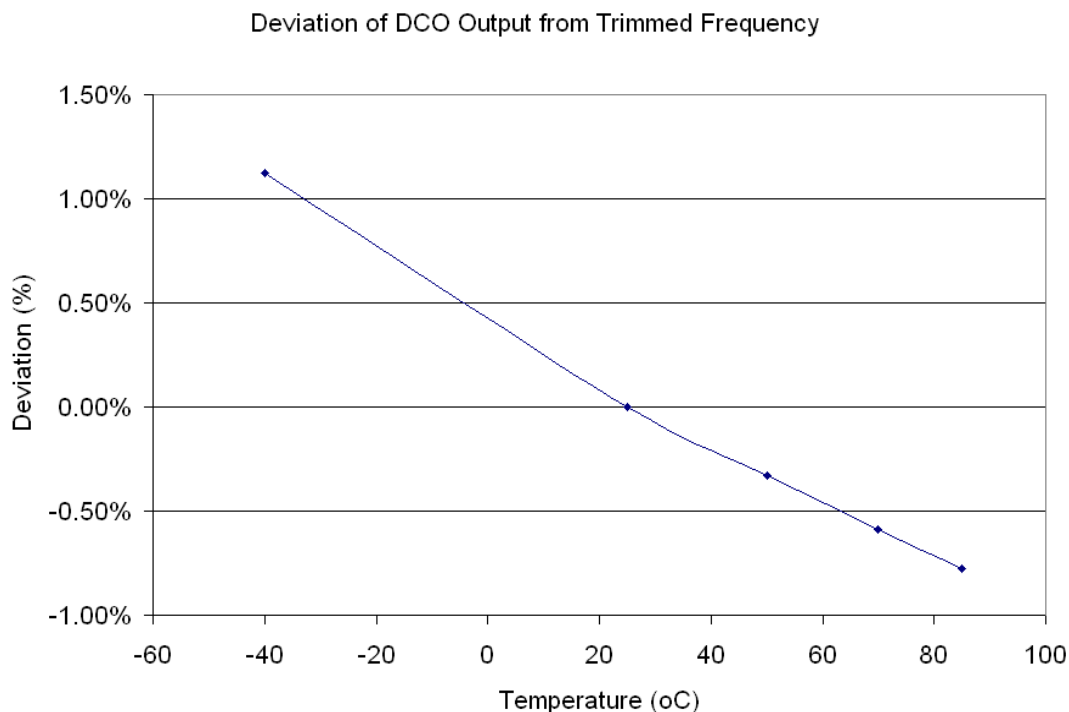


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

| Num | C | Rating | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|---|----------------------|-----------------------------|------------------|--------|---------|
| 1 | D | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | f_{Bus} | dc | — | 20 | MHz |
| 2 | D | Internal low power oscillator period | t_{LPO} | 700 | — | 1300 | μs |
| 3 | D | External reset pulse width ² | t_{extrst} | 100 | — | — | ns |
| 4 | D | Reset low drive | t_{rstdrv} | $34 \times t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | t_{MSSU} | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³ | t_{MSH} | 100 | — | — | μs |
| 7 | D | IRQ pulse width Asynchronous path ² Synchronous path ⁴ | t_{ILIH}, t_{IHIL} | 100 $1.5 \times t_{cyc}$ | — — | — — | ns |
| 8 | D | Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁴ | t_{ILIH}, t_{IHIL} | 100 $1.5 \times t_{cyc}$ | — — | — — | ns |
| 9 | C | Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF) ^{5, 6} Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise}, t_{Fall} | — — | 16 23 | — — | ns |
| | | Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF) ^{5, 6} Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise}, t_{Fall} | — — | 5 9 | — — | ns |
| 10 | C | Voltage Regulator Recovery time | t_{VRR} | — | 6 | 10 | μs |

¹ Typical values are based on characterization data at $V_{DD} = 3.0$ V, 25°C unless otherwise stated.

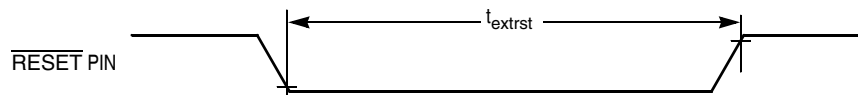
² This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

³ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

⁶ Except for LCD pins in Open Drain mode.


Figure 17. Reset Timing

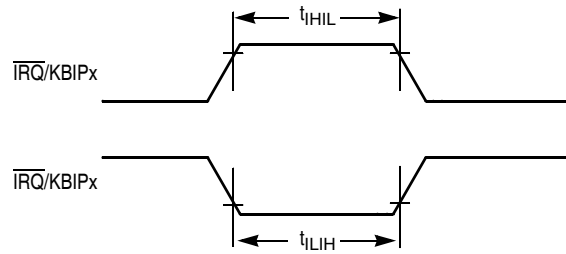


Figure 18. $\overline{\text{IRQ}}/\text{KBIPx}$ Timing

3.10.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|---------------------------|-------------------|-----|--------------------|------------------|
| 1 | D | External clock frequency | f_{TCLK} | 0 | $f_{\text{Bus}}/4$ | Hz |
| 2 | D | External clock period | t_{TCLK} | 4 | — | t_{cyc} |
| 3 | D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| 4 | D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| 5 | D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

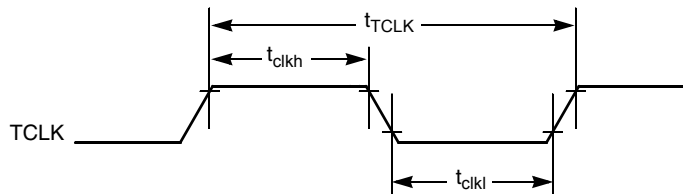
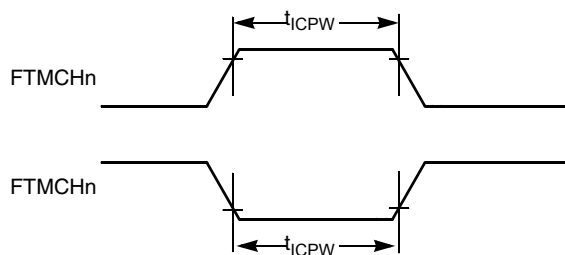


Figure 19. Timer External Clock



3.10.3 SPI Timing

Table 15 and Figure 20 through Figure 23 describe the timing requirements for the SPI system^{1,2}.

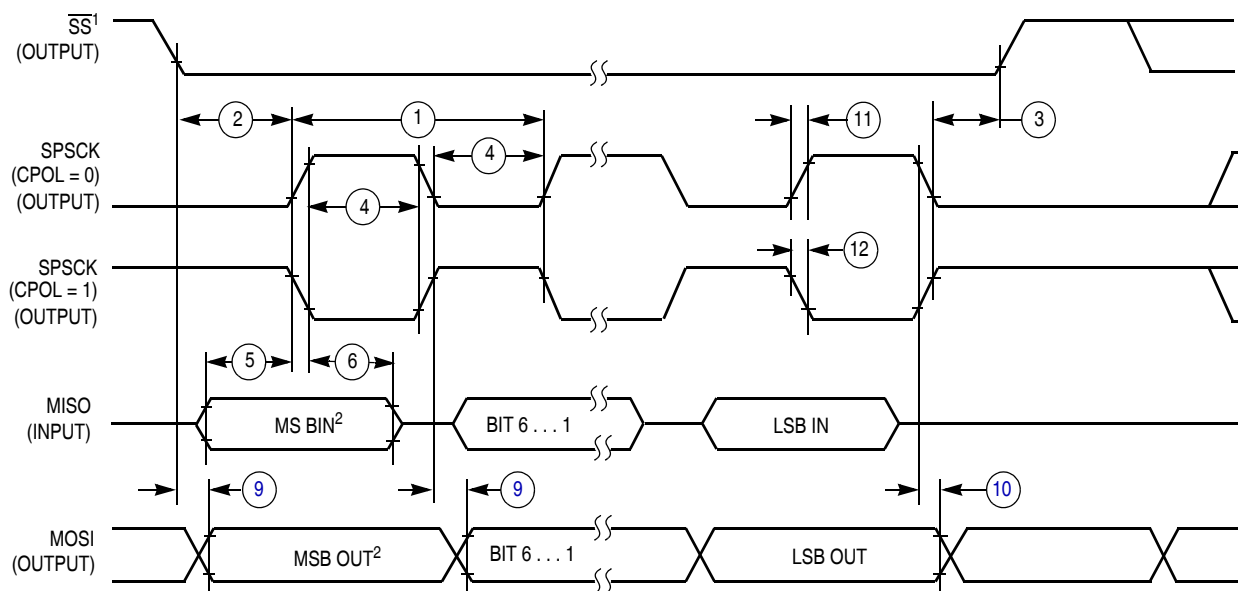
Table 15. SPI Timing

| No. | C | Function | Symbol | Min | Max | Unit |
|-----|---|---|----------------------|----------------------------------|----------------------------|--------------------------|
| — | D | Operating frequency Master Slave | f_{op} | $f_{Bus}/2048$ 0 | $f_{Bus}/2$ $f_{Bus}/4$ | Hz |
| ① | D | SPSCK period Master Slave | t_{SPSCK} | 2 4 | 2048 — | t_{cyc} t_{cyc} |
| ② | D | Enable lead time Master Slave | t_{Lead} | 1/2 1 | — — | t_{SPSCK} t_{cyc} |
| ③ | D | Enable lag time Master Slave | t_{Lag} | 1/2 1 | — — | t_{SPSCK} t_{cyc} |
| ④ | D | Clock (SPSCK) high or low time Master Slave | t_{WSPSCK} | $t_{cyc} - 30$ $t_{cyc} - 30$ | $1024 t_{cyc}$ — | ns ns |
| ⑤ | D | Data setup time (inputs) Master Slave | t_{SU} | 30 30 | — — | ns ns |
| ⑥ | D | Data hold time (inputs) Master Slave | t_{HI} | 0 25 | — — | ns ns |
| ⑦ | D | Slave access time | t_a | — | 1 | t_{cyc} |
| ⑧ | D | Slave MISO disable time | t_{dis} | — | 1 | t_{cyc} |
| ⑨ | D | Data valid (after SPSCK edge) Master Slave | t_v | — — | 60 60 | ns ns |
| ⑩ | D | Data hold time (outputs) Master Slave | t_{HO} | 0 0 | — — | ns ns |
| ⑪ | D | Rise time Input Output | t_{RI} t_{RO} | — — | $t_{cyc} - 25$ 25 | ns ns |
| ⑫ | D | Fall time Input Output | t_{FI} t_{FO} | — — | $t_{cyc} - 25$ 25 | ns ns |

1. There is 20 pF load on the SPI ports.

2. There are three types of SPI ports in MC9S08GW64 Series. They are ports for AMR, ports shared with LCD pads and normal ports. This timing is for normal ports condition.

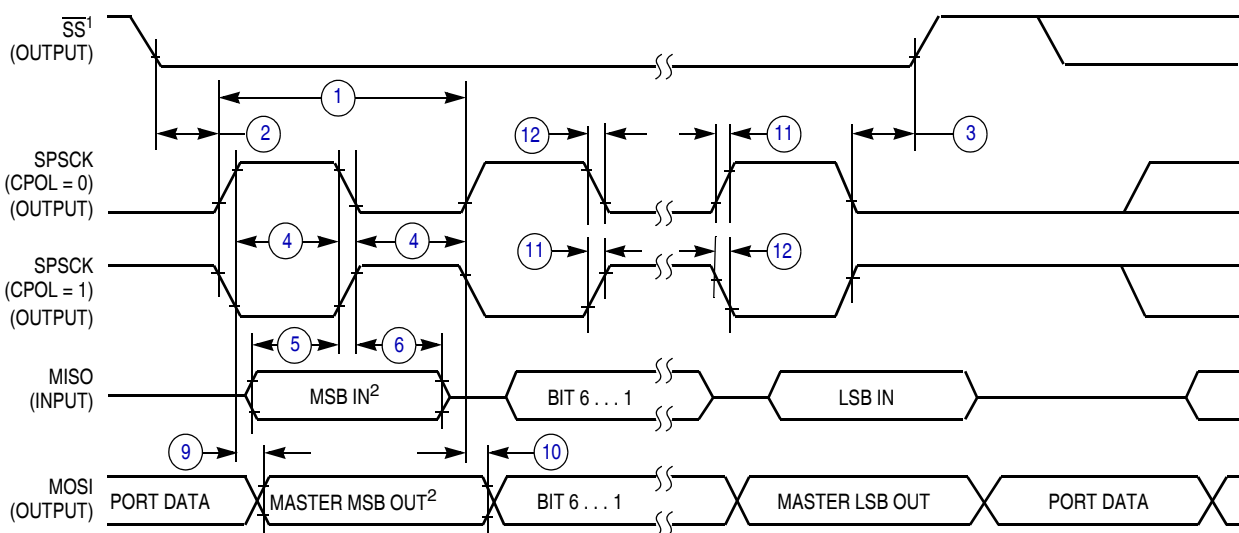
Electrical Characteristics



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

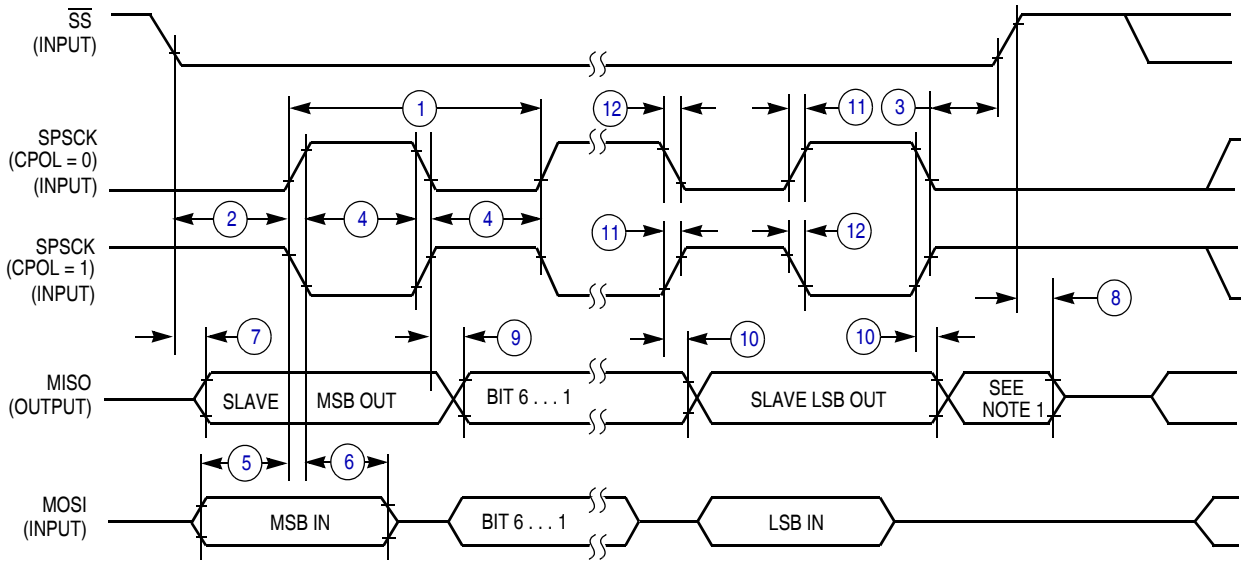
Figure 20. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

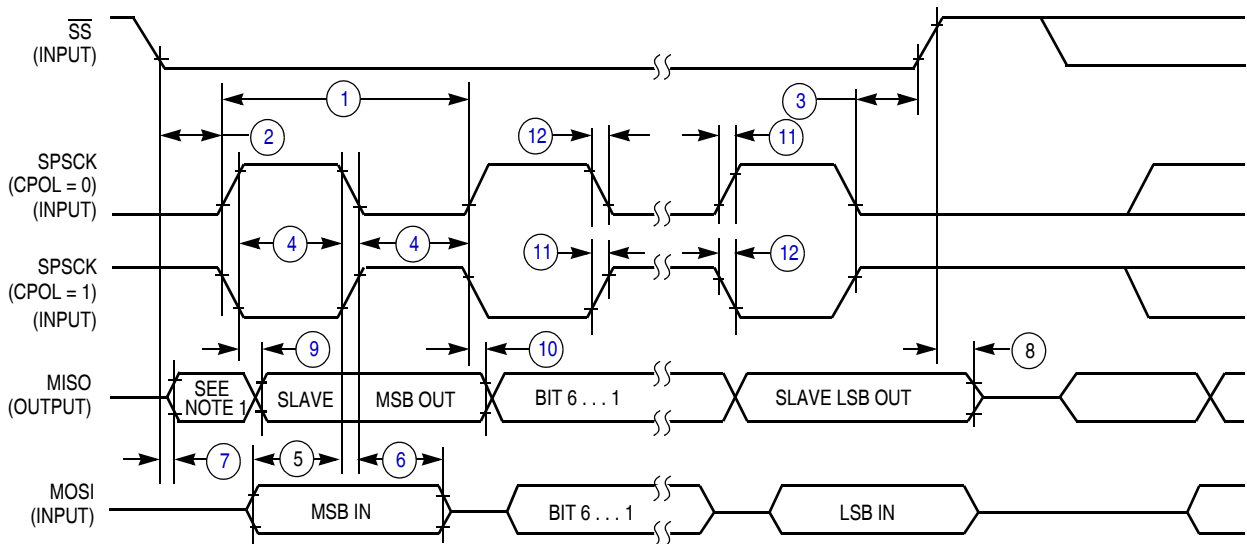
Figure 21. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received.

Figure 22. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received.

Figure 23. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (PRACMP) Electricals

Table 16. PRACMP Electrical Specifications

| N | C | Characteristic | Symbol | Min | Typical | Max | Unit |
|----|---|--|---------------------|----------------|---------|----------|---------|
| 1 | D | Supply voltage | V_{PWR} | 1.8 | — | 3.6 | V |
| 2 | C | Supply current (active) (PRG enabled) | I_{DDACT1} | — | — | 60 | μA |
| 3 | C | Supply current (active) (PRG disabled) | I_{DDACT2} | — | — | 40 | μA |
| 4 | C | Supply current (ACMP and PRG all disabled) | I_{DDDIS} | — | — | 2 | nA |
| 5 | D | Analog input voltage | V_{AIN} | $V_{SS} - 0.3$ | — | V_{DD} | V |
| 6 | C | Analog input offset voltage | V_{AIO} | — | 5 | 40 | mV |
| 7 | C | Analog comparator hysteresis | V_H | 3.0 | — | 20.0 | mV |
| 8 | P | Analog input leakage current | I_{ALKG} | — | — | 1 | nA |
| 9 | C | Analog comparator initialization delay | t_{AINIT} | — | — | 1.0 | μs |
| 10 | C | Programmable reference generator inputs | $V_{In1}(V_{DD})$ | 1.8 | — | V_{DD} | V |
| 11 | C | Programmable reference generator inputs | $V_{In2}(V_{DD25})$ | 1.8 | — | 2.75 | V |
| 12 | C | Programmable reference generator setup delay | t_{PRGST} | — | — | — | ns |
| 13 | C | Programmable reference generator step size | V_{step} | -0.25 | 1 | 0.25 | LSB |
| 14 | C | Programmable reference generator voltage range | V_{prgout} | $V_{In}/32$ | — | V_{in} | V |

3.12 ADC Characteristics

These specs all assume separate V_{DDAD} supply for ADC and isolated pad segment for ADC supplies and differential inputs.. Spec's should be de-rated for $V_{REFH} = V_{bg}$ condition.

Table 17. 16-bit ADC Operating Conditions

| Num | Charact eristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|-----|------------------|---|------------------|------|------------------|-----------|------|---------|
| 1 | Supply voltage | Absolute | V_{DDA} | 1.8 | — | 3.6 | V | |
| 2 | | Delta to V_{DD} ($V_{DD} - V_{DDA}$) ² | ΔV_{DDA} | -100 | 0 | 100 | mV | |
| 3 | Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSA}$) ² | ΔV_{SSA} | -100 | 0 | 100 | mV | |
| 4 | Ref Voltage High | | V_{REFH} | 1.15 | V_{DDA} | V_{DDA} | V | |

Table 17. 16-bit ADC Operating Conditions

| Num | Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit | Comment |
|-----|----------------------------|---|------------|------------|------------------|---------------|------------|--|
| 5 | Ref Voltage Low | | V_{REFL} | V_{SSA} | V_{SSA} | V_{SSA} | V | |
| 6 | Input Voltage | | V_{ADIN} | V_{REFL} | — | V_{REFH} | V | |
| 7 | Input Capacitance | 16-bit modes 8/10/12-bit modes | C_{ADIN} | — | 8 4 | 10 5 | pF | |
| 8 | Input Resistance | | R_{ADIN} | — | 2 | 5 | k Ω | |
| 9 | Analog Source Resistance | 16 bit modes $f_{ADCK} > 8\text{MHz}$ $4\text{MHz} < f_{ADCK} < 8\text{MHz}$ $f_{ADCK} < 4\text{MHz}$ | R_{AS} | — | — | 0.5 1 2 | k Ω | External to MCU Assumes ADLSMP=0 |
| 10 | | 13/12 bit modes $f_{ADCK} > 8\text{MHz}$ $4\text{MHz} < f_{ADCK} < 8\text{MHz}$ $f_{ADCK} < 4\text{MHz}$ | | — | — | 1 2 5 | | |
| 11 | | 11/10 bit modes $f_{ADCK} > 8\text{MHz}$ $4\text{MHz} < f_{ADCK} < 8\text{MHz}$ $f_{ADCK} < 4\text{MHz}$ | | — | — | 2 5 10 | | |
| 12 | | 9/8 bit modes $f_{ADCK} > 8\text{MHz}$ $f_{ADCK} < 8\text{MHz}$ | | — | — | 5 10 | | |
| 13 | ADC Conversion Clock Freq. | ADLPC = 0, ADHSC = 1 | f_{ADCK} | 1.0 | — | 10 | MHz | |
| 14 | | ADLPC = 0, ADHSC = 0 | | 1.0 | — | 5 | | |
| 15 | | ADLPC = 1, ADHSC = 0 | | 1.0 | — | 2.5 | | |

¹ Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

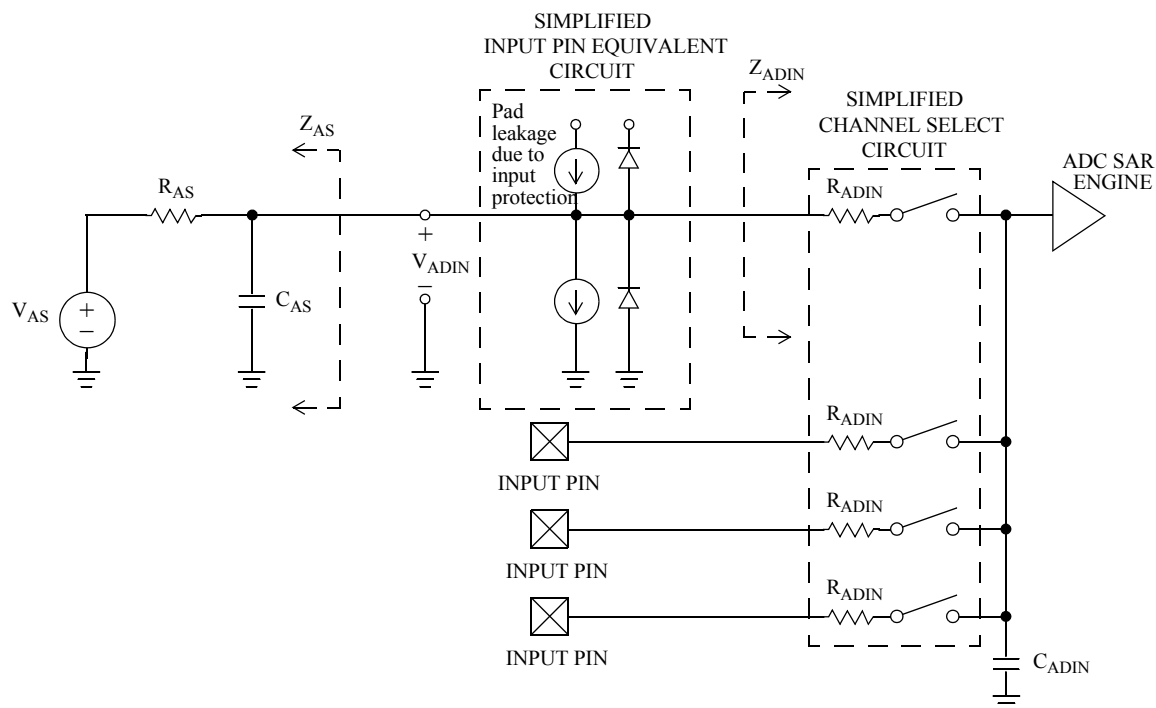


Figure 24. ADC Input Impedance Equivalency Diagram

Table 18. 16-bit ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 10\text{MHz}$)

| Characteristic | Conditions ¹ | C | Symb | Min | Typ ² | Max | Unit | Comment |
|-------------------------------|---|---|-------------|-----|------------------|-----|---------------|---------------------------|
| Supply Current | ADLPC = 1, ADHSC = 0 | T | I_{DDA} | — | 215 | — | μA | ADLSMP = 0 ADCO = 1 |
| | ADLPC = 0, ADHSC = 0 | | | — | 540 | — | | |
| | ADLPC=0, ADHSC=1 | | | — | 610 | — | | |
| Supply Current | Stop, Reset, Module Off | C | I_{DDA} | — | 0.072 | — | μA | |
| ADC Asynchronous Clock Source | ADLPC = 1, ADHSC = 0 | P | f_{ADACK} | — | 2.4 | — | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | ADLPC = 0, ADHSC = 0 | | | — | 5.2 | — | | |
| | ADLPC = 0, ADHSC = 1 | | | — | 6.2 | — | | |
| Sample Time | See reference manual for sample times | | | | | | | |
| Conversion Time | See reference manual for conversion times | | | | | | | |

¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

² Typical values assume $V_{DDAD} = 3.0\text{V}$, Temp = 25°C, $f_{ADCK} = 2.0\text{MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, $ADHSC=1$)

| Characteristic | Conditions ¹ | C | Symb | Min | Typ ² | Max | Unit | Comment |
|----------------------------|--|---|-----------------|--------|-------------------------|--------------------------|------------------|---|
| Total Unadjusted Error | 16-bit differential mode 16-bit single-ended mode | T | TUE | — — | ± 16 ± 20 | $+24/-24$ $+32/-20$ | LSB ³ | 32x Hardware Averaging (AVGE = %1 AVGS = %11) |
| | 13-bit differential mode 12-bit single-ended mode | T | | — — | ± 1.5 ± 1.75 | ± 2.0 ± 2.5 | | |
| | 11-bit differential mode 10-bit single-ended mode | T | | — — | ± 0.7 ± 0.8 | ± 1.0 ± 1.25 | | |
| | 9-bit differential mode 8-bit single-ended mode | T | | — — | ± 0.5 ± 0.5 | ± 1.0 ± 1.0 | | |
| Differential Non-Linearity | 16-bit differential mode 16-bit single-ended mode | T | DNL | — — | ± 2.5 ± 2.5 | ± 3 ± 3 | LSB ² | |
| | 13-bit differential mode 12-bit single-ended mode | T | | — — | ± 0.7 ± 0.7 | ± 1 ± 1 | | |
| | 11-bit differential mode 10-bit single-ended mode | T | | — — | ± 0.5 ± 0.5 | ± 0.75 ± 0.75 | | |
| | 9-bit differential mode 8-bit single-ended mode | T | | — — | ± 0.2 ± 0.2 | ± 0.5 ± 0.5 | | |
| Integral Non-Linearity | 16-bit differential mode 16-bit single-ended mode | T | INL | — — | ± 6.0 ± 10.0 | ± 12.0 ± 16.0 | LSB ² | |
| | 13-bit differential mode 12-bit single-ended mode | T | | — — | ± 1.0 ± 1.0 | ± 2.0 ± 2.0 | | |
| | 11-bit differential mode 10-bit single-ended mode | T | | — — | ± 0.5 ± 0.5 | ± 1.0 ± 1.0 | | |
| | 9-bit differential mode 8-bit single-ended mode | T | | — — | ± 0.3 ± 0.3 | ± 0.5 ± 0.5 | | |
| Zero-Scale Error | 16-bit differential mode 16-bit single-ended mode | T | E _{ZS} | — — | ± 4.0 ± 4.0 | $+16/0$ $+16/-38$ | LSB ² | $V_{ADIN} = V_{SSAD}$ |
| | 13-bit differential mode 12-bit single-ended mode | T | | — — | ± 0.7 ± 0.7 | ± 2.0 ± 2.0 | | |
| | 11-bit differential mode 10-bit single-ended mode | T | | — — | ± 0.4 ± 0.4 | ± 1.0 ± 1.0 | | |
| | 9-bit differential mode 8-bit single-ended mode | T | | — — | ± 0.2 ± 0.2 | ± 0.5 ± 0.5 | | |

Electrical Characteristics

Table 19. 16-bit ADC Characteristics($V_{REFH} = V_{DDAD} \geq 2.7V$, $V_{REFL} = V_{SSAD}$, $F_{ADCK} \leq 4MHz$, $ADHSC=1$)

| Characteristic | Conditions ¹ | C | Symb | Min | Typ ² | Max | Unit | Comment |
|---------------------------------|---|---|--------------|----------------------------------|--|-----------------------|------------------|---|
| Full-Scale Error | 16-bit differential mode 16-bit single-ended mode | T | E_{FS} | — — | +8/0 +12/0 | +24/0 +24/0 | LSB ² | $V_{ADIN} = V_{DDAD}$ |
| | 13-bit differential mode 12-bit single-ended mode | T | | — — | ±0.7 ±0.7 | ±2.0 ±2.5 | | |
| | 11-bit differential mode 10-bit single-ended mode | T | | — — | ±0.4 ±0.4 | ±1.0 ±1.0 | | |
| | 9-bit differential mode 8-bit single-ended mode | T | | — — | ±0.2 ±0.2 | ±0.5 ±0.5 | | |
| Quantization Error | 16 bit modes | D | E_Q | — | -1 to 0 | — | LSB ² | |
| | ≤13 bit modes | | | — | — | ±0.5 | | |
| Effective Number of Bits | 16 bit differential mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1 | C | ENOB | — — — — — | 13.5 13.4 13.2 13 12.6 | — — — — — | Bits | For ADC_DIV=1, ADC_CLK=10 MHz. |
| | 16 bit single-ended mode Avg = 32 Avg = 16 Avg = 8 Avg = 4 Avg = 1 | | | — — — — — | 12.39 12.34 12.13 11.94 11.4 | — — — — — | | |
| Signal to Noise plus Distortion | See ENOB | | SINAD | $SINAD = 6.02 \cdot ENOB + 1.76$ | | | dB | |
| Total Harmonic Distortion | 16-bit differential mode Avg = 32 | C | THD | — | — | — | dB | |
| | 16-bit single-ended mode Avg = 32 | D | | — | — | — | | |
| Spurious Free Dynamic Range | 16-bit differential mode Avg = 32 | C | SFDR | 91.0 | 96.5 | — | dB | |
| | 16-bit single-ended mode Avg = 32 | D | | — | — | — | | |
| Input Leakage Error | all modes | D | E_{IL} | $I_{in} \cdot R_{AS}$ | | | mV | I_{in} = leakage current (refer to DC characteristics) |
| Temp Sensor Slope | -40°C–25°C | D | m | — | 1.646 | — | mV/°C | |
| | 25°C–125°C | | | — | 1.769 | — | | |
| Temp Sensor Voltage | 25°C | D | V_{TEMP25} | — | 966 | — | mV | |

- ¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDAD}$
- ² Typical values assume $V_{DDAD} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK}=2.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
- ³ $1\text{ LSB} = (V_{REFH}-V_{REFL})/2^N$

3.13 VREF Characteristics

Table 20. Electrical specifications

| Num | C | Characteristic | Symbol | Min | Max | Unit |
|------------------------------|---|--|------------------------------|----------------------------------|------|-------------------------|
| 1 | P | Supply voltage | V_{DD} | 1.80 | 3.60 | V |
| 2 | P | Operating temperature range | T_{op} | -40 | 85 | C |
| 3 | C | Maximum Load | | | 10 | mA |
| Operation across Temperature | | | | | | |
| 4 | P | Voltage output room temperature | Untrimmed | 1.070–1.3 | | V |
| 5 | P | Voltage output room temperature | Factory trimmed ¹ | 1.180–1.22 | | V |
| 6 | C | -40 °C | Factory trimmed | 1.19–1.200 | | V |
| 7 | C | 85 °C | Factory trimmed | 1.185–1.200 | | V |
| Load Bandwidth | | | | | | |
| 8 | C | Load Regulation Mode = 10 at 1mA load | Mode = 10 | 20 | 100 | $\mu\text{V}/\text{mA}$ |
| 9 | C | Line Regulation (Power Supply Rejection) | DC | ± 0.1 from room temp voltage | | mV |
| | | | AC | -60 | | dB |
| Power Consumption | | | | | | |
| 10 | C | Powered down Current (Stop Mode, $V_{REFEN} = 0$, $V_{RSTEN} = 0$) | I | | 100 | μA |
| 11 | C | Bandgap only (Mode[1:0] 00) | I | | 75 | μA |
| 12 | C | Low Power buffer (Mode[1:0] 01) | I | | 125 | μA |
| 13 | C | Tight Regulation buffer (Mode[1:0] 10) | I | | 1.1 | mA |
| 14 | C | Low Power and Tight Regulation (Mode[1:0] 11) | I | | 1.15 | mA |

¹ Factory trim is performed at the room temperature.

3.14 LCD Specifications

Table 21. LCD Electricals, 3-V Glass

| C | Characteristic | Symbol | Min | Typ | Max | Unit | |
|---|-----------------------------------|----------------------------|-------------------|-------------|--------------|---------------------------|---|
| D | LCD Frame Frequency | f_{Frame} | 28 | 30 | 58 | Hz | |
| D | LCD Charge Pump Capacitance | C_{LCD} | | 100 | 100 | nF | |
| D | LCD Bypass Capacitance | C_{BYLCD} | | 100 | 100 | nF | |
| D | LCD Glass Capacitance | C_{glass} | | 2000 | 8000 | pF | |
| D | V_{IREG} | HRefSel = 0 HRefSel = 1 | V_{IREG} | .89 1.49 | 1.00 1.67 | 1.15 1.85 ¹ | V |
| D | V_{IREG} TRIM Resolution | Δ_{RTRIM} | 1.5 | | | % V_{IREG} | |
| D | V_{IREG} Ripple | HRefSel = 0 HRefSel = 1 | | | .1 .15 | V | |

¹ V_{IREG} Max can not exceed $V_{\text{DD}} - 0.15$ V

3.15 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 22. FLASH Characteristics

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|-------------------------|--------|--------------|--------|-------------------|
| D | Supply voltage for program/erase -40°C to 85°C | $V_{\text{prog/erase}}$ | 1.8 | | 3.6 | V |
| D | Supply voltage for read operation | V_{Read} | 1.8 | | 3.6 | V |
| D | Internal FCLK frequency ¹ | f_{FCLK} | 150 | | 200 | kHz |
| D | Internal FCLK period (1/FCLK) | t_{FcyC} | 5 | | 6.67 | μs |
| P | Byte program time (random location) ² | t_{prog} | | 9 | | t_{FcyC} |
| P | Byte program time (burst mode) ² | t_{Burst} | | 4 | | t_{FcyC} |
| P | Page erase time ² | t_{Page} | | 4000 | | t_{FcyC} |
| P | Mass erase time ² | t_{Mass} | | 20,000 | | t_{FcyC} |
| D | Byte program current ³ | R_{IDDBP} | — | 4 | — | mA |
| D | Page erase current ³ | R_{IDDEPE} | — | 6 | — | mA |
| C | Program/erase endurance ⁴ T_{L} to $T_{\text{H}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $T = 25^{\circ}\text{C}$ | | 10,000 | — 100,000 | — — | cycles |
| C | Data retention ⁵ | $t_{\text{D-ret}}$ | 15 | 100 | — | years |

¹ The frequency of this clock is controlled by a software setting.

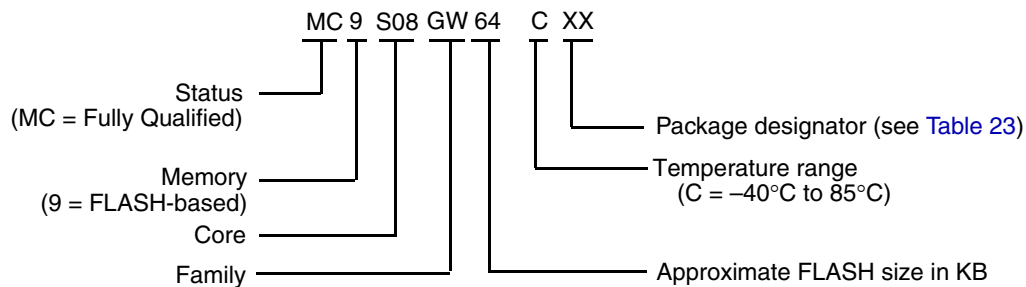
- ² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.
- ³ The program and erase currents are additional to the standard run I_{DD} . These values are measured at room temperatures with $V_{DD} = 3.0$ V, bus frequency = 4.0 MHz.
- ⁴ Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.
- ⁵ Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08GW64 Series.

4.1 Device Numbering System

Example of the device numbering system:



5 Package Information and Mechanical Drawings

Table 23 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08GW64 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 23, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 23) in the “Enter Keyword” search box at the top of the page.

Table 23. Package Descriptions

| Pin Count | Package Type | Abbreviation | Designator | Case No. | Document No. |
|-----------|-----------------------|--------------|------------|----------|-----------------------------|
| 80 | Low Quad Flat Package | LQFP | LK | 917A | 98ASS23237W |
| 64 | Low Quad Flat Package | LQFP | LH | 840F | 98ASS23234W |