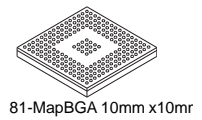
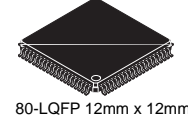
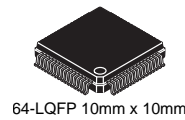


MC9S08JE128 series

Covers: MC9S08JE128 and MC9S08JE64



8-Bit HCS08 Central Processor Unit (CPU)

- Up to 48-MHz CPU above 2.4 V, 40 MHz CPU above 2.1 V, and 20 MHz CPU above 1.8 V across temperature of -40°C to 105°C
- HCS08 instruction set with added BGRND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- 128 K Dual Array Flash read/program/erase over full operating voltage and temperature
- 12 KB Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and Flash

Power-Saving Modes

- Two ultra-low power stop modes. Peripheral clock enable register can disable clocks to unused modules to reduce currents
- Time of Day (TOD) — Ultra-low power 1/4 sec counter with up to 64s timeout.
- Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to the TOD. 6 usec typical wake up time from stop3 mode

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator dedicated for TOD operation.
- Oscillator (XOSC2) — for high frequency crystal input for MCG reference to be used for system clock and USB operations.
- Multipurpose Clock Generator (MCG) — PLL and FLL; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 48 MHz.

System Protection

- Watchdog computer operating properly (COP) reset Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points; separate low-voltage warning with optional interrupt; selectable trip points
- Illegal opcode and illegal address detection with reset
- Flash block protection for each array to prevent accidental write/erasure
- Hardware CRC to support fast cyclic redundancy checks

Development Support

- Single-wire background debug interface
- Real-time debug with 6 hardware breakpoints (4 PC, 1 address and 1 data) Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- On-chip in-circuit emulator (ICE) debug module containing 3 comparators and 9 trigger modes

Peripherals

- **CMT**— Carrier Modulator timer for remote control communications. Carrier generator, modulator and driver for dedicated infrared out. Can be used as an output compare timer.
- **IIC**— Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven

- byte-by-byte data transfer; supports broadcast mode and 11-bit addressing
- **PRACMP** — Analog comparator with selectable interrupt; compare option to programmable internal reference voltage; operation in stop3
- **SCI** — Two serial communications interfaces with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; High current drive on Tx on SCI1 and SCI2; wake-up from stop3 on Rx edge
- **SPI1**— Serial peripheral interface (SPI) with 64-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI2**— Serial peripheral interface with full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **TPM** — Two 4-channel Timer/PWM Module; Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator
- **USB** — Supports USB in full-speed device configuration. On-chip transceiver and 3.3V regulator help save system cost, fully compliant with USB Specification 2.0. Allows control, bulk, interrupt and isochronous transfers.
- **ADC12** — 12-bit Successive approximation ADC with up to 4 dedicated differential channels and 8 single-ended channels; range compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V, Configurable hardware trigger for 8 Channel select and result registers
- **PDB** — Programmable delay block with 16-bit counter and modulus and prescale to set reference clock to bus divided by 1 to bus divided by 2048; 8 trigger outputs for ADC12 module provides periodic coordination of ADC sampling sequence with sequence completion interrupt; Back-to-Back mode and Timed mode
- **DAC** — 12-bit resolution; 16-word data buffers with configurable watermark.

Input/Output

- Up to 47 GPIOs and 2 output-only pin and 1 input-only pin.
- Voltage Reference output (VREF0).
- Dedicated infrared output pin (IRO) with high current sink capability.
- Up to 16 KBI pins with selectable polarity.

Package Options

- 81-MBGA 10x10 mm
- 80-LQFP 12x12 mm
- 64-LQFP 10x10 mm



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Contents

1 Devices in the MC9S08JE128 series.....	3	2.15 VREF Specifications.....	35
2 Preliminary Electrical Characteristics	12	3 Ordering Information.....	41
2.1 Parameter Classification	12	3.1 Device Numbering System.....	42
2.2 Absolute Maximum Ratings	13	3.2 Package Information.....	42
2.3 Thermal Characteristics	14	3.3 Mechanical Drawings	42
2.4 Electrostatic Discharge (ESD) Protection Characteristics	15	4 Revision History	43
2.5 DC Characteristics	16		
2.6 Supply Current Characteristics	19		
2.7 Comparator (PRACMP) Electricals.....	21		
2.8 12-Bit Digital-to-Analog Converter (DAC12LV) Electricals	22		
2.9 ADC Characteristics.....	23		
2.10 MCG and External Oscillator (XOSC) Characteristics	28		
2.11 AC Characteristics	31		
2.12 SPI Characteristics	32		
2.13 Flash Specifications	35		
2.14 USB Electricals	36		

Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>.

Reference Manual —MC9S08JE128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preliminary — Subject to Change

1 Devices in the MC9S08JE128 series

The following table summarizes the feature set available in the MC9S08JE128 series of MCUs.

Table 1. MC9S08JE128 series Features by MCU and Package

Feature	MC9S08JE128			MC9S08JE64
Pin quantity	81	80	64	64
FLASH size (bytes)	131072			65535
RAM size (bytes)	12K			12K
Programmable Analog Comparator (PRACMP)	yes			yes
Debug Module (DBG)	yes			yes
Multipurpose Clock Generator (MCG)	yes			yes
Inter-Integrated Communication (IIC)	yes			yes
Interrupt Request Pin (IRQ)	yes			yes
Keyboard Interrupt (KBI)	16	16	7	7
Port I/O ¹	47	46	33	33
Dedicated Analog Input Pins	12			12
Power and Ground Pins	8			8
Time Of Day (TOD)	yes			yes
Serial Communications (SCI1)	yes			yes
Serial Communications (SCI2)	yes			yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes
Serial Peripheral Interface 2 (SPI2)	yes			yes
Carrier Modulator Timer pin (IRO)	yes			yes
TPM input clock pin (TPMCLK)	yes			yes
TPM1 channels	4			4
TPM2 channels	4	4	2	2
XOSC1	yes			yes
XOSC2	yes			yes
USB	yes			yes
Programmable Delay Block (PDB)	yes			yes
SAR ADC differential channels ²	4	4	3	3
SAR ADC single-ended channels	8	8	6	6
Voltage reference output pin (VREFO)	yes			yes

¹ Port I/O count does not include two (2) output-only and one (1) input-only pins.

² Each differential channel is comprised of 2 pin inputs.

Devices in the MC9S08JE128 series

A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC12)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programmable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

The block diagram in [Figure 1](#) shows the structure of the MC9S08JE128 series MCU.

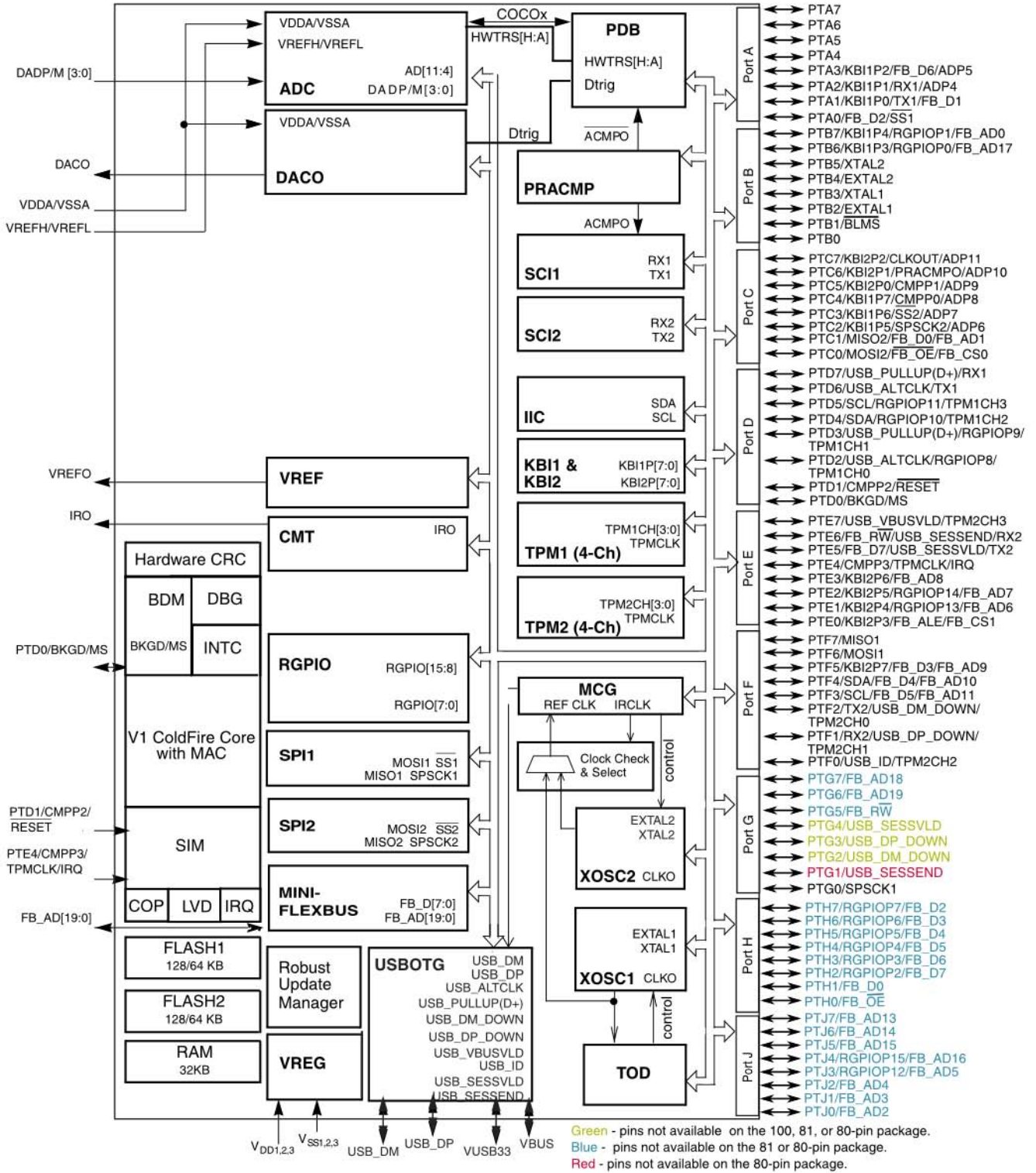


Figure 1. MC9S08JE128 series Block Diagram

1.1.2 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

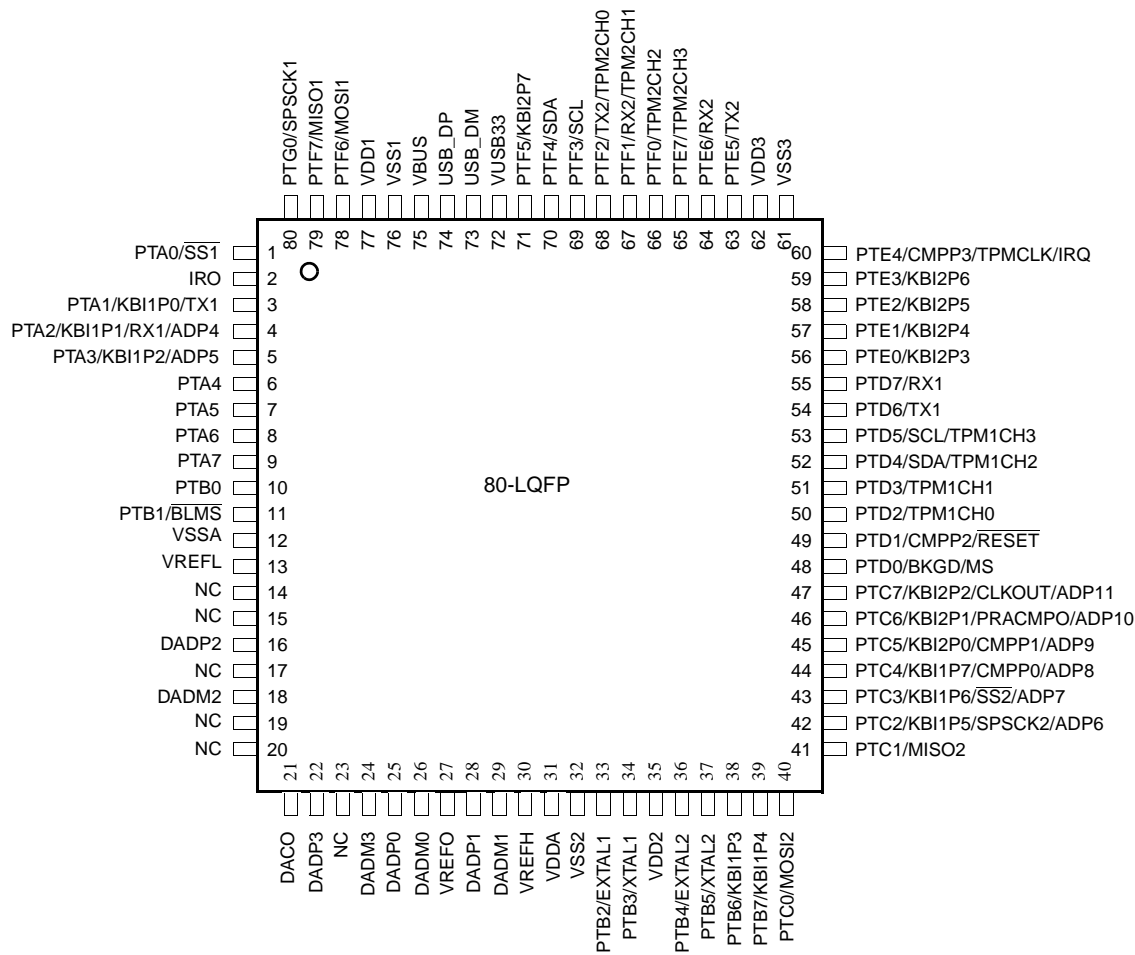


Figure 3. 80-Pin LQFP

1.1.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0
E		DADM2		VDD2	VDD3	VDD1	PTD2	PTD3	PTD6
F		DADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4
G	DADP0	DACO	DADP3	DADM3	VREFO	PTB6	PTC0	PTC1	PTC2
H	DADM0	DADM1	DADP1		PTC3	PTC4	PTD0	PTC5	PTC6
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5

Figure 4. 81-Pin MAPBGA

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/ $\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	—	—	—	PTA4
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	—	—	—	PTA7
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	\overline{BLMS}	—	—	PTB1/ \overline{BLMS}
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	NC	—	—	—	NC
E1	15	12	NC	—	—	—	NC
F2	16	13	DADP2	—	—	—	DADP2
F1	17	14	NC	—	—	—	NC
E2	18	15	DADM2	—	—	—	DADM2
F3	19	16	NC	—	—	—	NC
E3	20	17	NC	—	—	—	NC
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	—	—	—	DADP3
H4	23	20	NC	—	—	—	NC
G4	24	21	DADM3	—	—	—	DADM3
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
J3	30	25	VREFH	—	—	—	VREFH
J4	31	26	VDDA	—	—	—	VDDA
F4	32	27	VSS2	—	—	—	VSS2
J5	33	28	PTB2	EXTAL1	—	—	PTB2/EXTAL1
J6	34	29	PTB3	XTAL1	—	—	PTB3/XTAL1
E4	35	30	VDD2	—	—	—	VDD2
J8	36	31	PTB4	EXTAL2	—	—	PTB4/EXTAL2
J9	37	32	PTB5	XTAL2	—	—	PTB5/XTAL2
G6	38	—	PTB6	KBI1P3	—	—	PTB6/KBI1P3
F7	39	—	PTB7	KBI1P4	—	—	PTB7/KBI1P4
G7	40	33	PTC0	MOSI2	—	—	PTC0/MOSI2
G8	41	34	PTC1	MISO2	—	—	PTC1/MISO2
G9	42	35	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
H5	43	36	PTC3	KBI1P6	$\overline{SS2}$	ADP7	PTC3/KBI1P6/ $\overline{SS2}$ /ADP7
H6	44	37	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
H8	45	38	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
H9	46	39	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	47	40	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
H7	48	41	PTD0	BKGD	MS	—	PTD0/BKGD/MS
J7	49	42	PTD1	CMPP2	\overline{RESET}	—	PTD1/CMPP2/ \overline{RESET}
E7	50	43	PTD2	TPM1CH0	—	—	PTD2/TPM1CH0
E8	51	44	PTD3	TPM1CH1	—	—	PTD3/TPM1CH1
F9	52	45	PTD4	SDA	TPM1CH2	—	PTD4/SDA/TPM1CH2
D7	53	46	PTD5	SCL	TPM1CH3	—	PTD5/SCL/TPM1CH3
E9	54	47	PTD6	TX1	—	—	PTD6/TX1
D8	55	48	PTD7	RX1	—	—	PTD7/RX1
D9	56	—	PTE0	KBI2P3	—	—	PTE0/KBI2P3
C9	57	—	PTE1	KBI2P4	—	—	PTE1/KBI2P4
C8	58	—	PTE2	KBI2P5	—	—	PTE2/KBI2P5
B9	59	—	PTE3	KBI2P6	—	—	PTE3/KBI2P6
A9	60	49	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33	—	—	—	VUSB33
B4	73	57	USB_DM	—	—	—	USB_DM
A4	74	58	USB_DP	—	—	—	USB_DP
A5	75	59	VBUS	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08JE128/64 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	-0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	-0.3 to $V_{DD} + 0.3$	V
4	Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	± 25	mA
5	Storage temperature range	T_{stg}	-55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MC9S08JE128	-40 to 105	
		MC9S08JE64	-40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance ^{1,2,3,4} Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	θ_{JA}	Thermal resistance ^{1, 2, 3, 4} Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Junction to Ambient Natural Convection

³ 1s — Single layer board, one signal layer

⁴ 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \tag{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at $T_A = 125^\circ\text{C}$	I_{LAT}	±100	—	mA	T

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ ¹	Max	Unit	C
1	V _{DD}	Operating Voltage	—	1.8 ²	—	3.6	V	—
2	V _{OH}	Output high voltage	All I/O pins, low-drive strength					
			1.8 V, I _{Load} = -600 μA	V _{DD} - 0.5	—	—	V	C
			All I/O pins, high-drive strength					
			2.7 V, I _{Load} = -10 mA	V _{DD} - 0.5	—	—	V	P
			1.8 V, I _{Load} = -3 mA	V _{DD} - 0.5	—	—	V	C
3	I _{OHT}	Output high current	Max total I _{OH} for all ports					
			—	—	—	100	mA	D
4	V _{OL}	Output low voltage	All I/O pins, low-drive strength					
			1.8 V, I _{Load} = 600 μA	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			2.7 V, I _{Load} = 10 mA	—	—	0.5	V	P
			1.8 V, I _{Load} = 3 mA	—	—	0.5	V	C
5	I _{OLT}	Output low current	Max total I _{OL} for all ports	—	—	100	mA	D
6	V _{IH}	Input high voltage all digital inputs						
			all digital inputs, 2.7 V > V _{DD} ≥ 1.8 V	0.85 x V _{DD}	—	—	V	P

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ ¹	Max	Unit	C	
7	V _{IL}	Input low voltage all digital inputs	all digital inputs, V _{DD} > 2.7 V	—	—	0.35 x V _{DD}	V	P	
			all digital inputs, 2.7 > V _{DD} ≥ 1.8 V	—	—	0.30 x V _{DD}	V	P	
8	V _{hys}	Input hysteresis all digital inputs	—	0.06 x V _{DD}	—	—	mV	C	
9	I _{In}	Input leakage current all input only pins (Per pin)	V _{In} = V _{DD} or V _{SS}	—	—	0.25 (TBD)	μA	P	
10	I _{OZ}	Hi-Z (off-state) leakage current all input/output (per pin)	V _{In} = V _{DD} or V _{SS}	—	—	1(TBD)	μA	P	
11	I _{OZ}	Leakage current for analog output pins (DACO, VREFO) all input/output (per pin)	V _{In} = V _{DD} or V _{SS}	—	—	(TBD)	μA	P	
12	I _{InT}	Total Leakage Current ³ For all pins	—	—	—	2	μA	D	
13	R _{PU}	Pull-up resistors	—	17.5	—	52.5	kΩ	P	
14	R _{PD}	Internal pull-down resistors ⁴	—	17.5	—	52.5	kΩ	P	
15	I _{IC}	DC injection current ^{5, 6, 7} Single pin limit	V _{SS} > V _{IN} > V _{DD}	-0.2	—	0.2	mA	D	
			Total MCU limit, includes sum of all stressed pins						
			V _{SS} > V _{IN} > V _{DD}	-5	—	5	mA	D	
16	C _{In}	Input Capacitance, all pins	—	—	—	8	pF	C	
17	V _{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C	
18	V _{POR}	POR re-arm voltage ⁸	—	0.9	1.4	1.79	V	C	
19	t _{POR}	POR re-arm time	—	10	—	—	μs	D	

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ ¹	Max	Unit	C	
20	V _{LVDH} ⁹	Low-voltage detection threshold — high range	V _{DD} falling	—	2.11	2.16	2.22	V	P
			V _{DD} rising	—	2.16	2.23	2.27	V	P
21	V _{LVDL}	Low-voltage detection threshold — low range ⁹	V _{DD} falling	—	1.80	1.84	1.88	V	P
			V _{DD} rising	—	1.88	1.93	1.96	V	P
22	V _{LVWH}	Low-voltage warning threshold — high range ⁹	V _{DD} falling	—	2.36	2.46	2.56	V	P
			V _{DD} rising	—	2.36	2.46	2.56	V	P
23	V _{LVWL}	Low-voltage warning threshold — low range ⁹	V _{DD} falling	—	2.11	2.16	2.22	V	P
			V _{DD} rising	—	2.16	2.23	2.27	V	P
24	V _{hys}	Low-voltage inhibit reset/recover hysteresis ¹⁰	—	—	50	—	mV	C	
25	V _{BG}	Bandgap Voltage Reference ¹¹	—	1.15	1.17	1.18	V	P	

¹ Typical values are measured at 25°C. Characterized, not tested

² As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

³ Total Leakage current is the sum value for all GPIO pins; this leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

⁴ Measured with V_{In} = V_{DD}.

⁵ All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

⁶ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

- ⁷ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- ⁸ Maximum is highest voltage that POR is guaranteed.
- ⁹ Run at 1 MHz bus frequency
- ¹⁰ Low voltage detection and warning limits measured at 1 MHz bus frequency.
- ¹¹ Factory trimmed at $V_{DD} = 3.0$ V, Temp = 25°C

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	C
1	R _I DD	Run supply current FEI mode All modules ON	24 MHz	3	20	24	mA	-40 to 25	P
			24 MHz	3	20	TBD	mA	105	P
			20 MHz	3	18	—	mA	-40 to 105	T
			8 MHz	3	8	—	mA	-40 to 105	T
			1 MHz	3	1.8	—	mA	-40 to 105	T
2	R _I DD	Run supply current FEI mode; All modules OFF	24 MHz	3	12.3	TBD	mA	-40 to 105	C
			20 MHz	3	10.5	—	mA	-40 to 105	T
			8 MHz	3	4.8	—	mA	-40 to 105	T
			1 MHz	3	1.3	—	mA	-40 to 105	T
3	R _I DD	Run supply current LPS=0; All modules OFF	16 kHz FBILP	3	TBD	—	μA	-40 to 105	T
			16 kHz FBELP	3	TBD	—	μA	-40 to 105	T
4	R _I DD	Run supply current LPS=1, all modules OFF	16 kHz FBELP	3	TBD	—	μA	0 to 70	T
			16 kHz FBELP	3	TBD	—	μA	-40 to 105	T

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	C
5	W _I DD	Wait mode supply current FEI mode, all modules OFF	24 MHz	3	TBD	6	mA	-40 to 105	C
			20 MHz	3	TBD	—	mA	-40 to 105	T
			8 MHz	3	TBD	—	mA	-40 to 105	T
			1 MHz	3	TBD	—	mA	-40 to 105	T
6	S ₂ I _{DD}	Stop2 mode supply current	N/A	3	0.39	0.6	μA	-40 to 25	P
			N/A	3	TBD	TBD	μA	70	C
			N/A	3	7	TBD	μA	85	C
			N/A	3	16	TBD	μA	105	P
			N/A	2	TBD	TBD	μA	-40 to 25	C
			N/A	2	TBD	TBD	μA	70	C
			N/A	2	TBD	TBD	μA	85	C
			N/A	2	TBD	TBD	μA	105	C
7	S ₃ I _{DD}	Stop3 mode supply current No clocks active	N/A	3	0.55	0.9	μA	-40 to 25	P
			N/A	3	TBD	TBD	μA	70	C
			N/A	3	14	TBD	μA	85	C
			N/A	3	37	TBD	μA	105	P
			N/A	2	TBD	TBD	μA	-40 to 25	C
			N/A	2	TBD	TBD	μA	70	C
			N/A	2	14	TBD	μA	85	C
			N/A	2	TBD	TBD	μA	105	C

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600 (TBD)	650 (TBD)	750 (TBD)	850 (TBD)	1000 (TBD)	nA	D
3	IREFSTEN ¹	—	68	70	77	86	120	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD ¹	LVDSE = 1	114	115	123	135	170	μA	T
6	ACMP ¹	Not using the bandgap (BGBE = 0)	18	20	23	33	65	μA	T
7	ADC ¹	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	μA	T
8	DAC ¹	High power mode; no load on DACO	500	500	500	500	500	μA	T

¹ Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V _{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I _{DDACT1}	—	—	60	μA	C
3	Supply current (active) (PRG disabled)	I _{DDACT2}	—	—	40	μA	C
4	Supply current (ACMP and PRG all disabled)	I _{DDDIS}	—	—	2	nA	D
5	Analog input voltage	V _{AIN}	V _{SS} - 0.3	—	V _{DD}	V	—
6	Analog input offset voltage	V _{AIO}	—	5	40	mV	T
7	Analog comparator hysteresis	V _H	3.0	—	20.0	mV	T
8	Analog input leakage current	I _{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	t _{AINIT}	—	—	1.0	μs	T

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	μs	D
12	Programmable reference generator step size	V_{step}	-0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	V_{prgout}	$V_{In}/32$	—	V_{in}	V	P

2.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	-40	105	$^{\circ}\text{C}$	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Resolution	N	12	12	bit	C	
2	Supply current low-power mode	I_{DDA_DACLP}	50	100	μA	C	
3	Supply current high-power mode	I_{DDA_DACHP}	120	500 (TBD)	μA	C	
4	Full-scale Settling time (± 0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	T_{SFSLP}	—	200 (TBD)	μs	C	
5	Full-scale Settling time (± 0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	T_{SFSHP}	—	30	μs	C	
6	Code-to-code Settling time (± 0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	T_{SCCLP}	—	5	μs	C	
7	Code-to-code Settling time (± 0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	T_{SCCHP}	—	1(TBD)	μs	C	
8	DAC output voltage range low (high-power mode, no load, DAC set to 0)	$V_{dacoutl}$	—	100 (TBD)	mV	C	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0xFFFF)	$V_{dacouth}$	$V_{DACR} - 100$	—	mV	C	
10	Integral non-linearity error	INL	—	± 8	LSB	C	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	± 1	LSB	C	
12	Offset error	E_O	—	± 0.5	%FSR	C	
13	Gain error	E_G	—	± 0.5 (TBD)	%FSR	C	
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	dB	C	
15	Temperature drift of offset voltage (DAC set to 0x0800)	T_{co}	—	2 (TBD)	mV	C	See Typical Drift figure that follows.
16	Offset aging coefficient	A_c	—	TBD	$\mu V/yr$	C	

Figure 5. Offset at Half Scale vs Temperature

2.9 ADC Characteristics

Table 15. 12-bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ ¹	Max	Unit	C	Comment
1	V _{DDAD}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV _{DDAD}		Delta to V _{DD} (V _{DD} -V _{DDAD}) ²	-100	0	+100	mV	D	
3	ΔV _{SSAD}	Ground voltage	Delta to V _{SS} (V _{SS} -V _{SSAD}) ²	-100	0	+100	mV	D	
4	V _{REFH}		Ref Voltage High	1.13	V _{DDAD}	V _{DDAD}	V	D	
5	V _{REFL}	Ref Voltage Low	V _{SSAD}	V _{SSAD}	V _{SSAD}	V	D		
6	V _{ADIN}	Input Voltage	V _{REFL}	—	V _{REFH}	V	D		
7	C _{ADIN}	Input Capacitance		—	4	5	pF	C	
8	R _{ADIN}	Input Resistance		—	2	5	kΩ	C	
9	R _{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
			12-bit mode f _{ADCK} > 4 MHz	—	—	2	kΩ	C	
			f _{ADCK} < 4 MHz	—	—	5	kΩ	C	
			11/10-bit mode f _{ADCK} > 8 MHz	—	—	2	kΩ	C	
			4 MHz < f _{ADCK} < 8 MHz	—	—	5	kΩ	C	
			f _{ADCK} < 4 MHz	—	—	10	kΩ	C	
			9/8-bit mode f _{ADCK} > 4 MHz	—	—	5	kΩ	C	
			f _{ADCK} < 4 MHz	—	—	10	kΩ	C	
10	f _{ADCK}	ADC Conversion Clock Freq.	High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D	
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D	
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D	

¹ Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

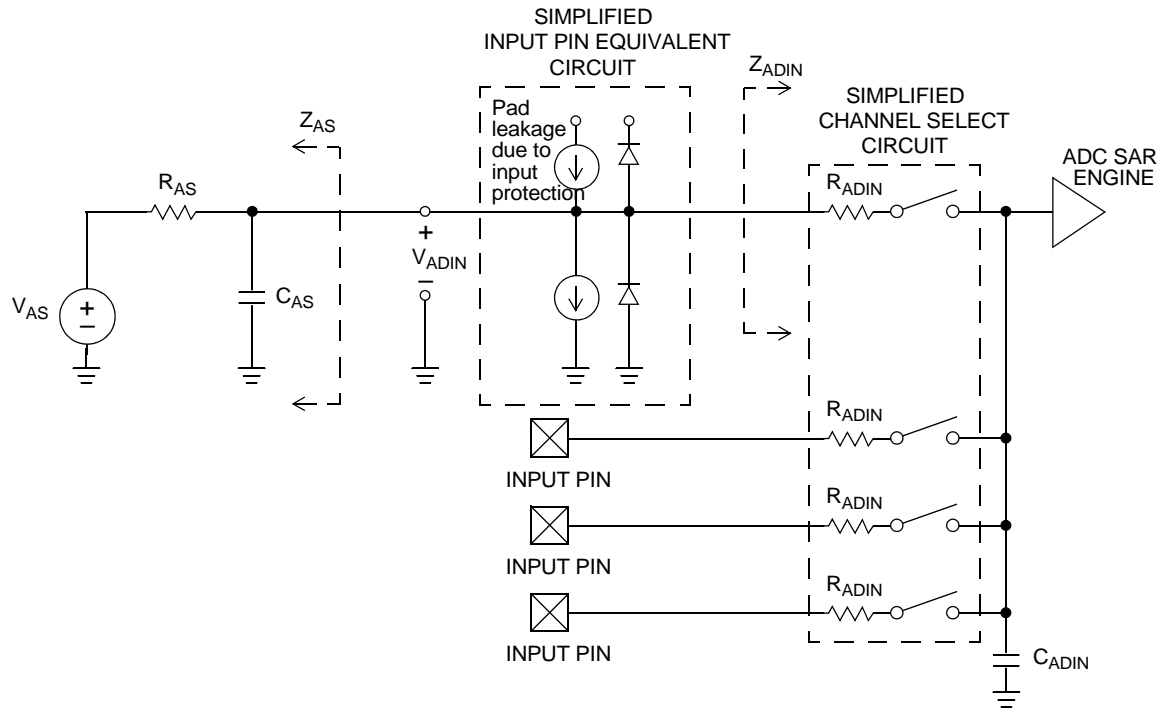


Figure 6. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range
 ($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD} \leq 8$ MHz)

Characteristic	Conditions ¹	Symb	Min	Typ ²	Max	Unit	C	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μ A	T	ADLSMP=0 ADCO=1
	ADLPC=0, ADHSC=0		—	470	—			
	ADLPC=0, ADHSC=1		—	610	—			
Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μ A	C	
ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	P	$t_{ADACK} = 1/f_{ADACK}$
	ADLPC=0, ADHSC=0		—	5.2	—			
	ADLPC=0, ADHSC=1		—	6.2	—			
Sample Time	See Block Guide for sample times							
Conversion Time	See Block Guide for conversion times							
Total Unadjusted Error	12-bit single-ended mode	TUE	—	± 1.75	± 3.5	LSB ³	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	11-bit differential mode 10-bit single-ended mode		—	± 0.7	± 1.5		T	
	9-bit differential mode 8-bit single-ended mode		—	± 0.5	± 1.0		T	
Differential Non-Linearity	12-bit single-ended mode	DNL	—	± 0.7	± 1	LSB ²	T	
	11-bit differential mode 10-bit single-ended mode		—	± 0.5	± 0.75		T	
	9-bit differential mode 8-bit single-ended mode		—	± 0.2	± 0.5		T	
Integral Non-Linearity	12-bit single-ended mode	INL	—	± 1.0	± 2.5	LSB ²	T	
	11-bit differential mode 10-bit single-ended mode		—	± 0.5	± 1.0		T	
	9-bit differential mode 8-bit single-ended mode		—	± 0.3	± 0.5		T	

Table 16. 12-bit SAR ADC Characteristics full operating range
($V_{REFH} = V_{DDAD} > 1.8$, $V_{REFL} = V_{SSAD} \leq 8$ MHz) (Continued)

Characteristic	Conditions ¹	Symb	Min	Typ ²	Max	Unit	C	Comment
Zero-Scale Error	12-bit single-ended mode	E_{ZS}	—	± 0.7	± 2.0	LSB ²	T	$V_{ADIN} = V_{SSAD}$
	11-bit differential mode 10-bit single-ended mode		— —	± 0.4 ± 0.4	± 1.0 ± 1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	± 0.2 ± 0.2	± 0.5 ± 0.5		T	
Full-Scale Error	12-bit single-ended mode	E_{FS}	—	± 1.0	± 3.5	LSB ²	T	$V_{ADIN} = V_{DDAD}$
	11-bit differential mode 10-bit single-ended mode		— —	± 0.4 ± 0.4	± 1.5 ± 1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	± 0.2 ± 0.2	± 0.5 ± 0.5		T	
Quantization Error	All modes	E_Q	—	—	± 0.5	LSB ²	D	
Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	-40°C – 25°C	m	—	1.646	—	mV/x C	C	
	25°C – 125°C		—	1.769	—			
Temp Sensor Voltage	25°C	V_{TEMP25}	—	701.2	—	mV	C	

¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDAD}$

² Typical values assume $V_{DDAD} = 3.0V$, Temp = 25°C, $f_{ADCK} = 2.0MHz$ unless otherwise stated. Typical values are for reference only and are not tested in production.

³ $1 \text{ LSB} = (V_{REFH} - V_{REFL}) / 2^N$

2.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = -40 to 105°C Ambient)

#	Rating	Symbol	Min	Typical	Max	Unit	C	
1	Internal reference startup time	t_{irefst}	—	55	100	μs	D	
2	Average internal reference frequency	f_{int_ft}	—	factory trimmed at VDD=3.0 V and temp=25°C	31.25	—	C	
				user trimmed	31.25	—	39.0625	C
3	DCO output frequency range - trimmed	f_{dco_t}	—	Low range (DRS=00)	—	20	MHz	C
				Mid range (DRS=01)	32	—	40	C
				High range ¹ (DRS=10)	40	—	60	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco_res_t}$	—	with FTRIM	± 0.1	± 0.2	% f_{dco}	C
				without FTRIM	± 0.2	± 0.4	C	
5	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	over voltage and temperature	± 1.0	± 2	% f_{dco}	P
				over fixed voltage and temp range of 0 - 70 °C	± 0.5	± 1	C	
6	Acquisition time	FLL ²	$t_{fll_acquire}$	—	—	1	ms	C
		PLL ³	$t_{pll_acquire}$	—	—	1		D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) ⁴	C_{jitter}	—	0.02	0.2	% f_{dco}	C	
8	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz	D	
9	PLL reference frequency range	f_{pll_ref}	1.0	—	2.0	MHz	D	
10	Jitter of PLL output clock measured over 625ns ⁵	Long term	$f_{pll_jitter_625ns}$	—	0.566 ⁴	—	% f_{pll}	D
11	Lock frequency tolerance	Entry ⁶	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit ⁷	D_{unl}	± 4.47	—	± 5.97		D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll_acquire} + 1075(1/f_{int_t})$	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll_acquire} + 1075(1/f_{pll_ref})$		D
13	Loss of external clock minimum frequency - RANGE = 0	f_{loc_low}	$(3/5) \times f_{int_t}$	—	—	kHz	D	
14	Loss of external clock minimum frequency - RANGE = 1	f_{loc_high}	$(16/5) \times f_{int_t}$	—	—	kHz	D	

¹ This should not exceed the maximum CPU frequency for this device.

² This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

Preliminary Electrical Characteristics

- ³ This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- ⁴ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
- ⁵ 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.
- ⁶ Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.
- ⁷ Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 18. XOSC (Temperature Range = -40 to 105°C Ambient)

#	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) <ul style="list-style-type: none"> • Low range (RANGE = 0) • High range (RANGE = 1), FEE or FBE mode² • High range (RANGE = 1), High gain (HGO = 1), FBELP mode • High range (RANGE = 1), Low power (HGO = 0), FBELP mode 	f_{lo}	32	—	38.4	kHz	
		f_{hi}	1	—	5	MHz	
		f_{hi}	1	—	16	MHz	
		f_{hi}	1	—	8	MHz	
2	Load capacitors	C_1 C_2	See Note ³				
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_{F}	—	10	—	M Ω
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_{S}	—	0	—	k Ω
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range <ul style="list-style-type: none"> • Low Gain (HGO = 0) • High Gain (HGO = 1) 	≥ 8 MHz	R_{S}	—	0	0	k Ω
		4 MHz		—	0	10	
		1 MHz		—	0	20	

Table 18. XOSC (Temperature Range = -40 to 105°C Ambient)

#	Characteristic	Symbol	Min	Typ ¹	Max	Unit
6	Crystal start-up time ^{4, 5}	t _{CSTL}	—	200	—	ms
			—	400	—	
		t _{CSTH}	—	5	—	
			—	15	—	

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ See crystal or resonator manufacturer's recommendation.

⁴ This parameter is characterized and not tested on each device.

⁵ Proper PC board layout procedures must be followed to achieve specifications.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 19. Control Timing

#	Symbol	Parameter	Min	Typical ¹	Max	C	Unit	
1	f_{Bus}	Bus frequency ($t_{\text{cyc}} = 1/f_{\text{Bus}}$)					MHz	
			$V_{\text{DD}} \geq 1.8 \text{ V}$	dc	—	10		D
			$V_{\text{DD}} > 2.1 \text{ V}$	dc	—	20		D
			$V_{\text{DD}} > 2.4 \text{ V}$	dc	—	24		D
2	t_{LPO}	Internal low-power oscillator period	800	990 (TBD)	1500	D	μs	
3	t_{extrst}	External reset pulse width ² ($t_{\text{cyc}} = 1/f_{\text{Self_reset}}$)	100	—	—	D	ns	
4	t_{rstdrv}	Reset low drive	$66 \times t_{\text{cyc}}$	—	—	D	ns	
5	t_{MSSU}	Active background debug mode latch setup time	500	—	—	D	ns	
6	t_{MSH}	Active background debug mode latch hold time	100	—	—	D	ns	
7	$t_{\text{ILIH}}, t_{\text{IHIL}}$	IRQ pulse width • Asynchronous path ² • Synchronous path ³	100 $1.5 \times t_{\text{cyc}}$	—	—	D	ns	
8	$t_{\text{ILIH}}, t_{\text{IHIL}}$	KBIPx pulse width • Asynchronous path ² • Synchronous path ³	100 $1.5 \times t_{\text{cyc}}$	—	—	D	ns	

Table 19. Control Timing

#	Symbol	Parameter	Min	Typical ¹	Max	C	Unit
9	$t_{\text{Rise}}, t_{\text{Fall}}$	Port rise and fall time (load = 50 pF) ⁴ , Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

- ¹ Typical values are based on characterization data at $V_{\text{DD}} = 5.0 \text{ V}$, $25 \text{ }^\circ\text{C}$ unless otherwise stated.
- ² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.
- ³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- ⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40 \text{ }^\circ\text{C}$ to $105 \text{ }^\circ\text{C}$.

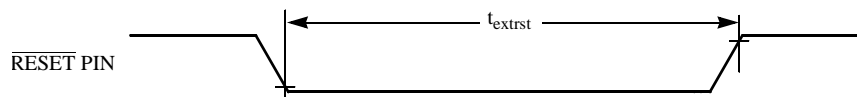


Figure 7. Reset Timing

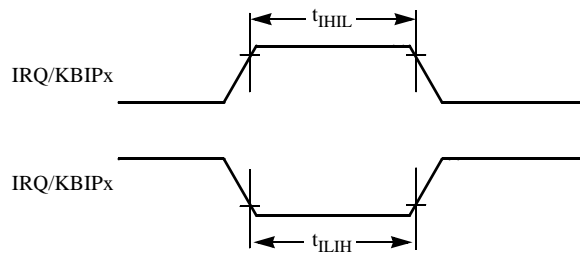


Figure 8. IRQ/KBIPx Timing

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 20. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{\text{Bus}}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{ckl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

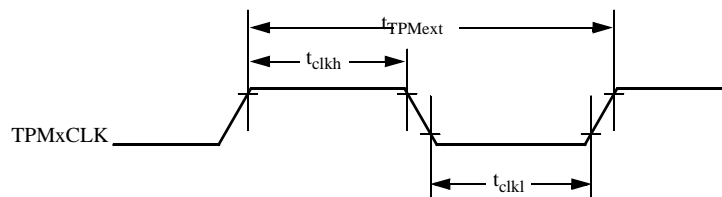


Figure 9. Timer External Clock

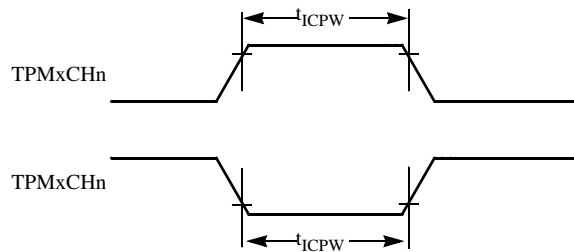


Figure 10. Timer Input Capture Pulse

2.12 SPI Characteristics

Table 21 and Figure 11 through Figure 14 describe the timing requirements for the SPI system.

Table 21. SPI Timing

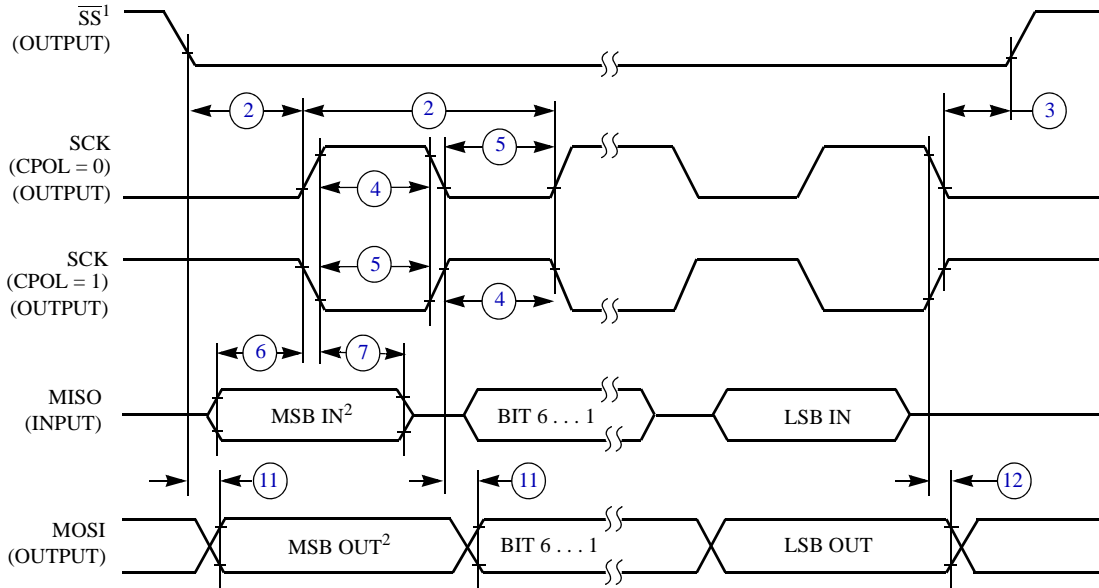
No. ¹	Characteristic ²	Symbol	Min	Max	Unit	C
1	Operating frequency	Master	$f_{\text{Bus}}/2048$	$f_{\text{Bus}}/2$	Hz	D
		Slave	0	$f_{\text{Bus}}/4$	Hz	
2	SPSCK period	Master	2	2048	t_{cyc}	D
		Slave	4	—	t_{cyc}	
3	Enable lead time	Master	1/2	—	t_{SPSCK}	D
		Slave	1	—	t_{cyc}	
4	Enable lag time	Master	1/2	—	t_{SPSCK}	D
		Slave	1	—	t_{cyc}	
5	Clock (SPSCK) high or low time	Master	$t_{\text{cyc}} - 30$	$1024 t_{\text{cyc}}$	ns	D
		Slave	$t_{\text{cyc}} - 30$	—	ns	
6	Data setup time (inputs)	Master	15	—	ns	D
		Slave	15	—	ns	
7	Data hold time (inputs)	Master	0	—	ns	D
		Slave	25	—	ns	
8	Slave access time ³	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time ⁴	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge)	Master	—	25	ns	D
		Slave	—	25	ns	
11	Data hold time (outputs)	Master	0	—	ns	D
		Slave	0	—	ns	
12	Rise time	Input	—	$t_{\text{cyc}} - 25$	ns	D
		Output	—	25	ns	
13	Fall time	Input	—	$t_{\text{cyc}} - 25$	ns	D
		Output	—	25	ns	

¹ Numbers in this column identify elements in Figure 11 through Figure 14.

² All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

³ Time to data active from high-impedance state.

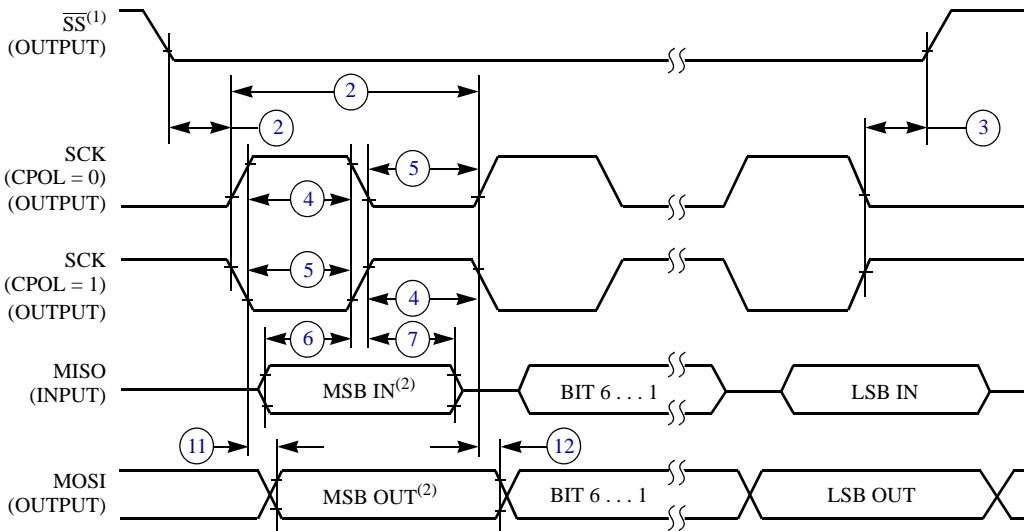
⁴ Hold time to high-impedance state.



NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

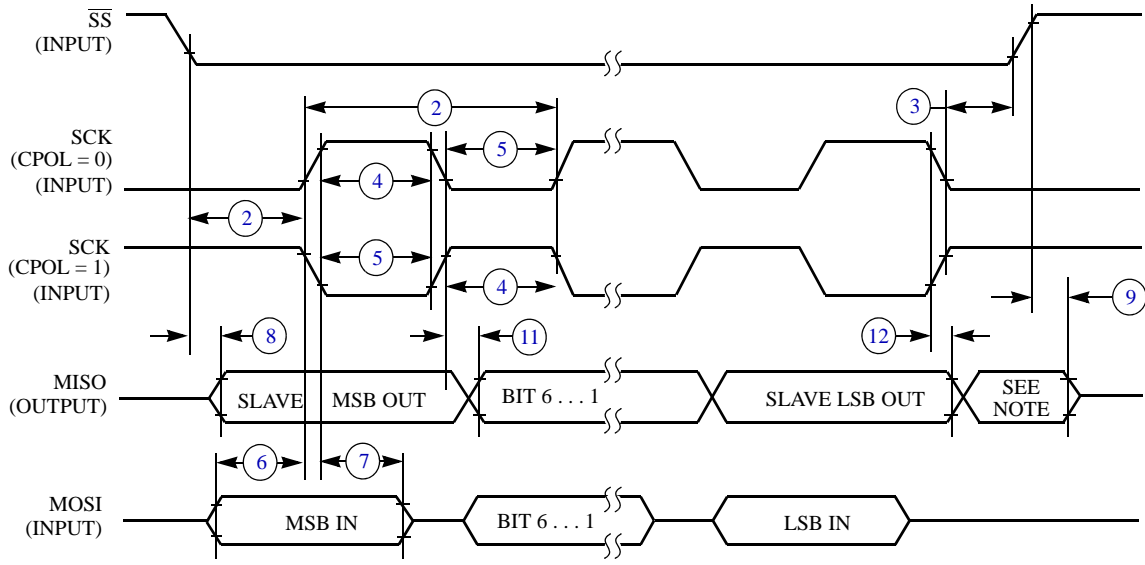
Figure 11. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

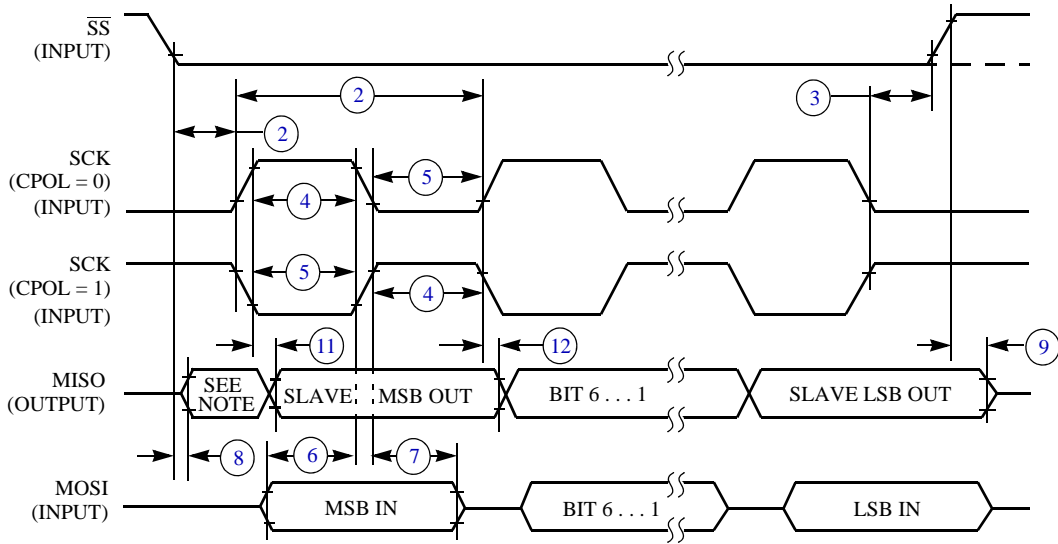
Figure 12. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 13. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 14. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MC9S08JE128RM).

Table 22. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{\text{prog/erase}}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency ¹	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{FcyC}	5	—	6.67	μs	D
5	Byte program time (random location) ²	t_{prog}	9			t_{FcyC}	P
6	Byte program time (burst mode) ²	t_{Burst}	4			t_{FcyC}	P
7	Page erase time ²	t_{Page}	4000			t_{FcyC}	P
8	Mass erase time ²	t_{Mass}	20,000			t_{FcyC}	P
9	Program/erase endurance ³ T_L to $T_H = -40^\circ\text{C}$ to $+105^\circ\text{C}$ $T = 25^\circ\text{C}$		10,000 —	— 100,000	— —	cycles	C
10	Data retention ⁴	$t_{\text{D_ret}}$	15	100	—	years	C

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

³ **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

⁴ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 23. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.6	V	P
3	V_{USB33} input with internal VREG disabled	V_{usb33in}	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

2.15 VREF Electrical Specifications

Table 24. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V _{DDA}	1.80	3.6	V	C
2	Temperature	T _A	-40	105	°C	C
3	Output Load Capacitance	C _L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V _{DD} = 3 V.	V _{out}	1.140	1.160	V	P
6	Temperature Drift (V _{min} - V _{max} across the full temperature range)	T _{drift}	—	10 (TBD)	mV ¹	T
7	Aging Coefficient	A _c	—	TBD	ppm/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	μA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	μA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	μA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	μV/mA	C
13	Line Regulation (Power Supply Rejection)	DC	—	TBD	mV	C
14		AC	TBD	—	dB	

¹ See typical chart below.

Table 25. VREF Limited Range Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Temperature	T _A	0	50	°C	C	

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim	V _{out}	TBD	TBD	μA	C	

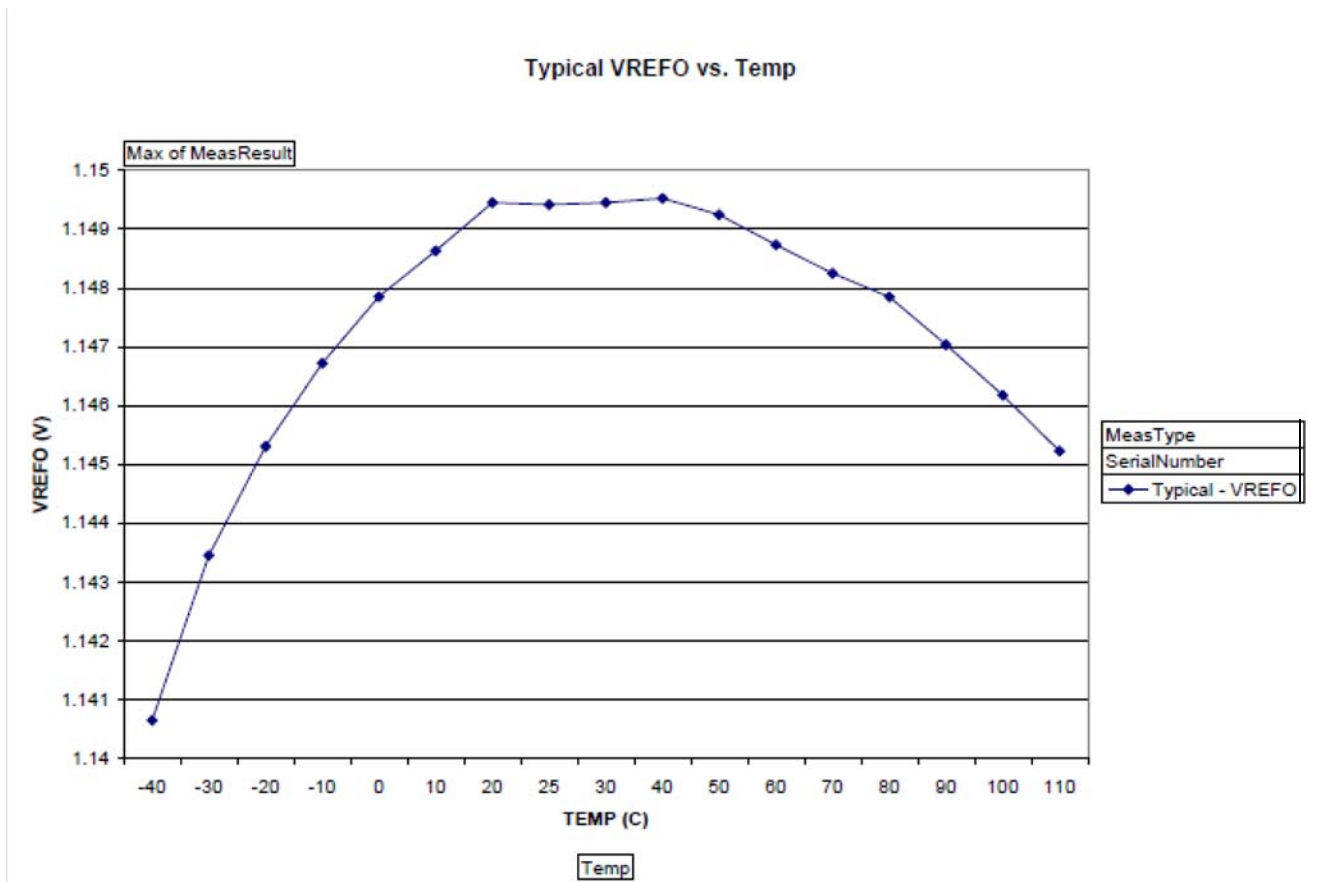


Figure 15. Typical Output vs. Temperature

TBD

Figure 16. Typical Output vs. V_{DD}

3 Ordering Information

This appendix contains ordering information for the device numbering system. MC9S08JE128 and MC9S08JE64 devices.

3.1 Device Numbering System

Example of the device numbering system:

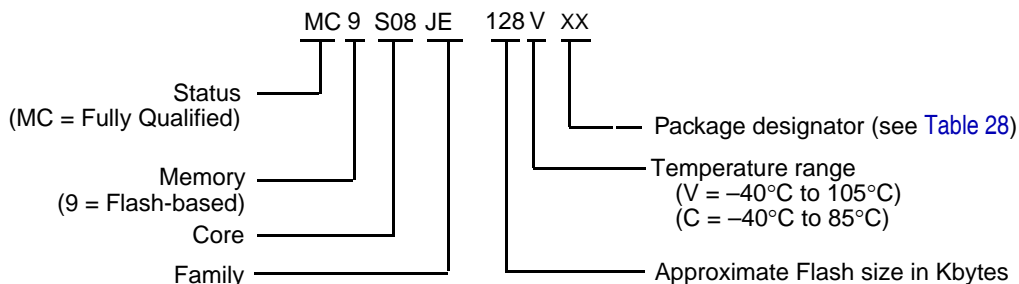


Table 27. Device Numbering System

Device Number ¹	Memory		Available Packages ²
	Flash	RAM	
MC9S08JE128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08JE64	65,536	12,288	64 LQFP

¹ See Table 2 for a complete description of modules included on each device.

² See Table 28 for package information.

3.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F-02	98ASS23234W
80	Low Quad Flat Package	LQFP	LK	917-01	98ASS23174W
81	MAPBGA Package	Map PBGA	MB	1662-01	98ASA10670D

3.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08JE128 series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

4 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
0	6/2009	Initial release of the Data Sheet.
1	7/2009	Updated MCG and XOSC Average internal reference frequency.
2	04/2010	Updated electrical characteristic data.