Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

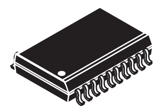
For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

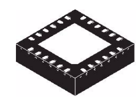
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08JS16
Rev. 4, 4/2009

MC9S08JS16



20 W-SOIC
Case 751D



24 QFN
Case 1982-01

MC9S08JS16 Series

Covers:
MC9S08JS16
MC9S08JS8
MC9S08JS16L
MC9S08JS8L

Features:

- 8-Bit HCS08 Central Processor Unit (CPU)
  - 48 MHz HCS08 CPU (central processor unit)
  - 24 MHz internal bus frequency
  - Support for up to 32 interrupt/reset sources
- Memory Options
  - Up to 16 KB of on-chip in-circuit programmable flash memory with block protection and security options
  - Up to 512 bytes of on-chip RAM
  - 256 bytes of USB RAM
- Clock Source Options
  - Clock source options include crystal, resonator, external clock
  - MCG (multi-purpose clock generator) — PLL and FLL; internal reference clock with trim adjustment
- System Protection
  - Optional computer operating properly (COP) reset with option to run from independent 1 kHz internal clock source or the bus clock
  - Low-voltage detection
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Power-Saving Modes
  - Wait plus two stops
- USB Bootload
  - Mass erase entire flash array
  - Partial erase flash array — erase all flash blocks except for the first 1 KB of flash
  - Program flash
- Peripherals
  - **USB —** USB 2.0 full-speed (12 Mbps) with dedicated on-chip 3.3 V regulator and transceiver; supports endpoint 0 and up to 6 additional endpoints
  - **SPI** — One 8- or 16-bit selectable serial peripheral interface module with a receive data buffer hardware match function
  - **SCI** — One serial communications interface module with optional 13 bit break. Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - **MTIM** — One 8-bit modulo counter with 8-bit prescaler and overflow interrupt
  - **TPM** — One 2-channel 16-bit timer/pulse-width modulator (TPM) module; selectable input capture, output compare, and edge-aligned PWM capability on each channel; timer module may be configured for buffered, centered PWM (CPWM) on all channels
  - **KBI** — 8-pin keyboard interrupt module
  - **RTC** — Real-time counter with binary- or decimal-based prescaler
  - **CRC** — Hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16}+x^{12}+x^5+1$ polynomial
- Input/Output
  - Software selectable pullups on ports when used as inputs
  - Software selectable slew rate control on ports when used as outputs
  - Software selectable drive strength on ports when used as outputs
  - Master reset pin and power-on reset (POR)
  - Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost
- Package Options
  - 24-pin quad flat no-lead (QFN)
  - 20-pin small outline IC package (SOIC)

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision	Date	Description of Changes
1	9/1/2008	Initial public released
2	1/8/2009	In Table 7, changed the parameter description of RI_{DD} and $S3I_{DD}$, the typicals of RI_{DD} were changed as well.
3	3/9/2009	Corrected the 24-pin QFN case number and doc. number information.
4	4/24/2009	Added new parts information about MC9S08JS16L and MC9S08JS8L.

Related Documentation

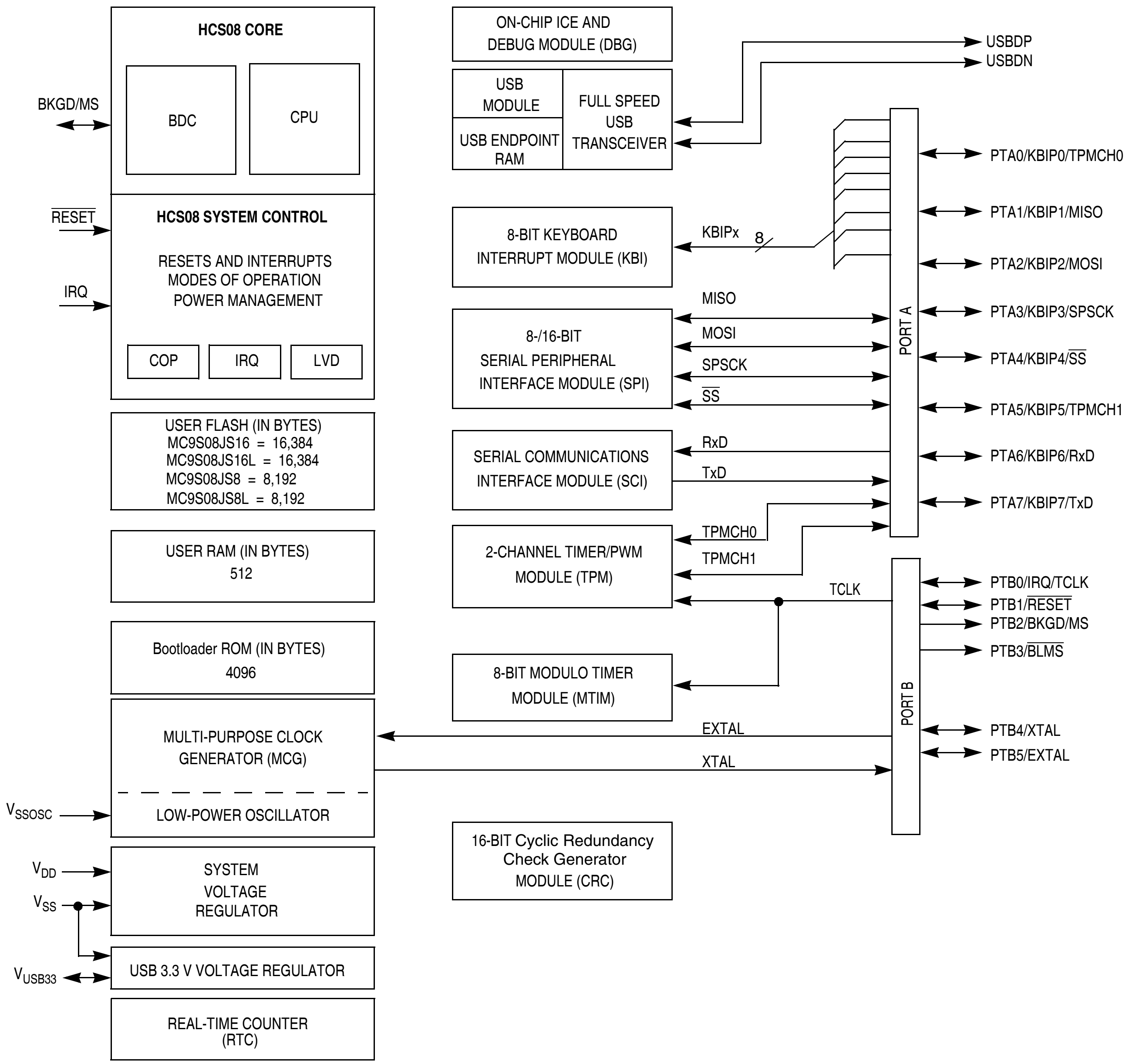
Find the most current versions of all documents at: http://www.freescale.com

Reference Manual **(MC9S08JS16RM)**

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of the MC9S08JS16 series MCU.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ is enabled (IRQPE = 1). Pulldown is enabled if rising edge detect is selected (IRQEDG = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ must not be driven above V_{DD}.
4. RESET contains integrated pullup device if PTB1 enabled as reset pin function (RSTPE = 1).
5. Pin contains integrated pullup device.
6. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 1. MC9S08JS16 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9S08JS16 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number (Package)		<-- Lowest	Priority	--> Highest
24 (QFN)	**20 (SOIC)**	**Port Pin**	**Alt 1**	**Alt 2**
1	4	PTB0	IRQ	TCLK
2	5	PTB1		$\overline{\text{RESET}}$
3	6	PTB2	BKGD	MS
4	7	PTB3		$\overline{\text{BLMS}}$
5	8	PTA0	KBIP0	TPMCH0
6	—	NC		
7	9	PTA1	KBIP1	MISO
8	10	PTA2	KBIP2	MOSI
9	11	PTA3	KBIP3	SPSCK
10	12	PTA4	KBIP4	$\overline{\text{SS}}$
11	13			V_{DD}
12	—	NC		
13	14			V_{SS}
14	15			USBDN
15	16			USBDP
16	17			V_{USB33}
17	18	PTA5	KBIP5	TPMCH1
18	—	NC		
19	19	PTA6	KBIP6	RxD
20	20	PTA7	KBIP7	TxD
21	1	PTB4	XTAL	
22	2	PTB5	EXTAL	
23	3			V_{SSOSC}
24	—	NC		

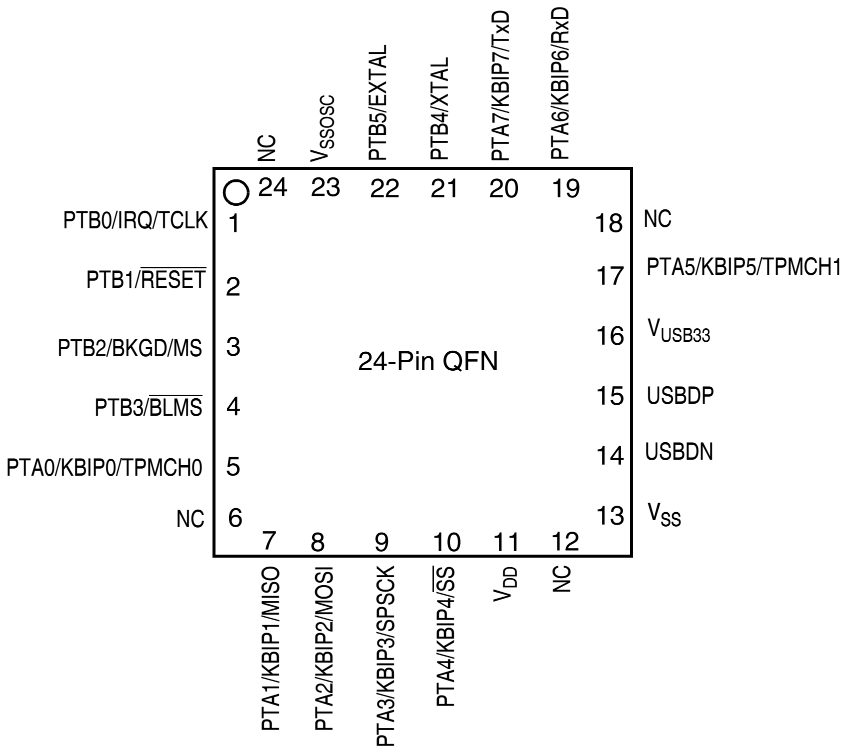


Figure 2. MC9S08JS16 Series in 24-QFN Package

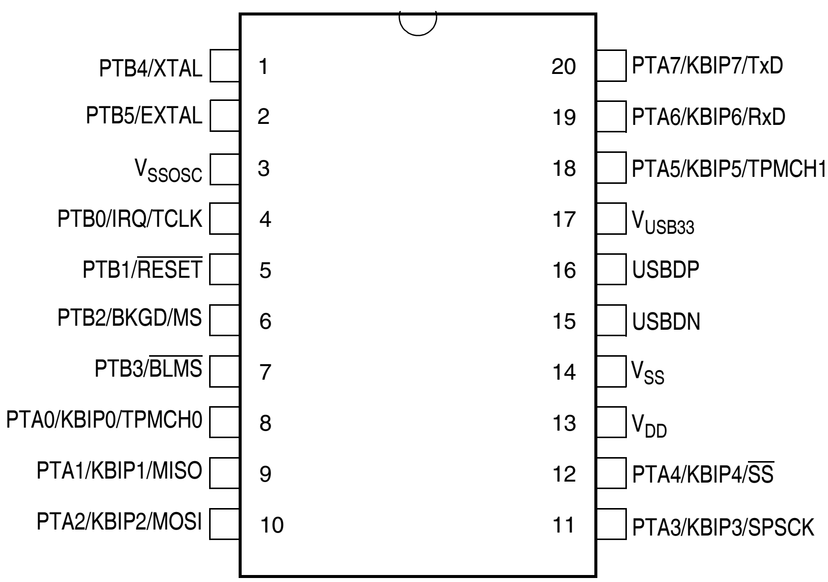


Figure 3. MC9S08JS16 Series in 20-pin SOIC Package

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The above classifications are used in the column labeled “C” in applicable tables of this data sheet.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current (applies to all port pins)[1, 2, 3] Single pin limit	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C
Maximum junction temperature	T_J	150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.
2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 85	°C
Thermal resistance [1,2,3,4] 24-pin QFN 1s 2s2p 20-pin SOIC 1s 2s2p	θ_{JA}	 92 33 86 58	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage. This device was qualified to AEC-Q100 Rev E. A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD Protection Characteristics

Parameter	Symbol	Value	Unit
ESD Target for Machine Model (MM) — MM circuit description	V_{THMM}	200	V
ESD Target for Human Body Model (HBM) — HBM circuit description	V_{THHBM}	2000	V

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1		Operating voltage[2]	—	2.7	—	5.5	V

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
2	P	Output high voltage — Low drive (PTxDSn = 0)	V_{OH}				V
		5 V, I_{Load} = –2 mA		V_{DD} – 1.5	—	—	
		3 V, I_{Load} = –0.6 mA		V_{DD} – 1.5	—	—	
		5 V, I_{Load} = –0.4 mA		V_{DD} – 0.8	—	—	
		3 V, I_{Load} = –0.24 mA		V_{DD} – 0.8	—	—	
		Output high voltage — High drive (PTxDSn = 1)					
		5 V, I_{Load} = –10 mA		V_{DD} – 1.5	—	—	
		3 V, I_{Load} = –3 mA		V_{DD} – 1.5	—	—	
		5 V, I_{Load} = –2 mA		V_{DD} – 0.8	—	—	
		3 V, I_{Load} = –0.4 mA		V_{DD} – 0.8	—	—	
3	P	Output low voltage — Low drive (PTxDSn = 0)	V_{OL}				V
		5 V, I_{Load} = 2 mA		1.5	—	—	
		3 V, I_{Load} = 0.6 mA		1.5	—	—	
		5 V, I_{Load} = 0.4 mA		0.8	—	—	
		3 V, I_{Load} = 0.24 mA		0.8	—	—	
		Output low voltage — High drive (PTxDSn = 1)					
		5 V, I_{Load} = 10 mA		1.5	—	—	
		3 V, I_{Load} = 3 mA		1.5	—	—	
		5 V, I_{Load} = 2 mA		0.8	—	—	
		3 V, I_{Load} = 0.4 mA		0.8	—	—	
4	P	Output high current — Max total I_{OH} for all ports	I_{OHT}				mA
		5 V		—	—	100	
		3 V		—	—	60	
5	P	Output low current — Max total I_{OL} for all ports	I_{OLT}				mA
		5 V		—	—	100	
		3 V		—	—	60	
6	P	Input high voltage; all digital inputs	V_{IH}	0.65 × V_{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 × V_{DD}	V
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current; input only pins[3]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[3]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[4]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[5]	R_{PD}	20	45	65	kΩ
13	C	Internal pullup resistor to USBDP (to V_{USB33})	R_{PUPD}				kΩ
		Idle		900	—	1575	
		Transmit		1425	—	3090	
14	C	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	C	RAM retention voltage	V_{RAM}	0.6	1.0	—	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	μs

Table 6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
18	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
19	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
20	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
21	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
22	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
23	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
24	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV

1 Typical values are based on characterization data at 25 °C unless otherwise stated.

2 Operating voltage with USB enabled can be found in Section 3.11, "USB Electricals."

3 Measured with $V_{In} = V_{DD}$ or V_{SS}.

4 Measured with $V_{In} = V_{SS}$.

5 Measured with $V_{In} = V_{DD}$.

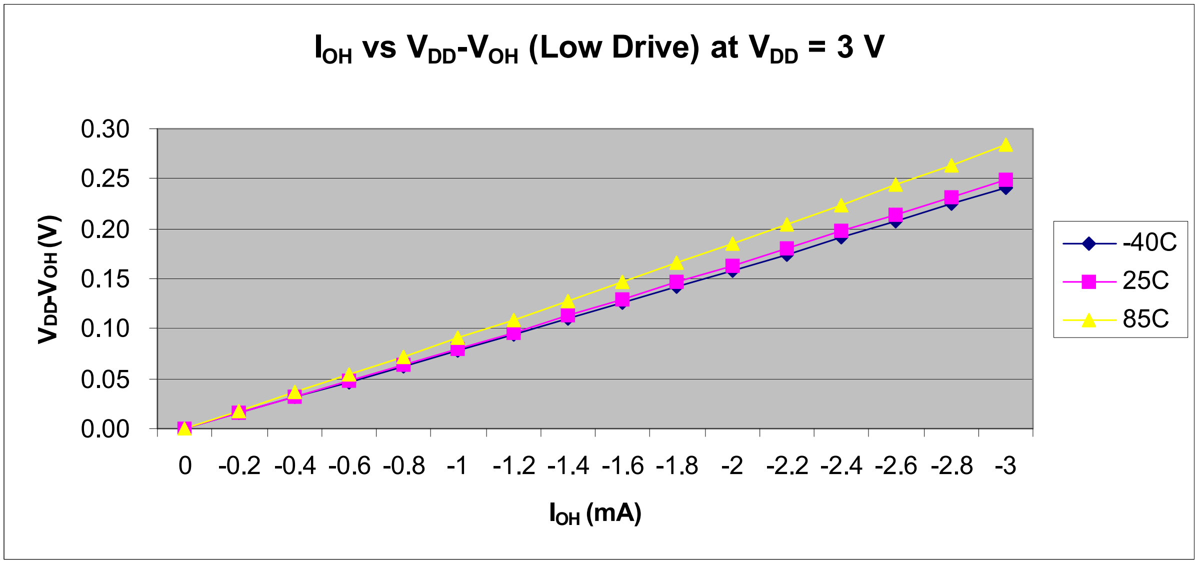


Figure 4. Typical I_{OH} (Low Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 3 V

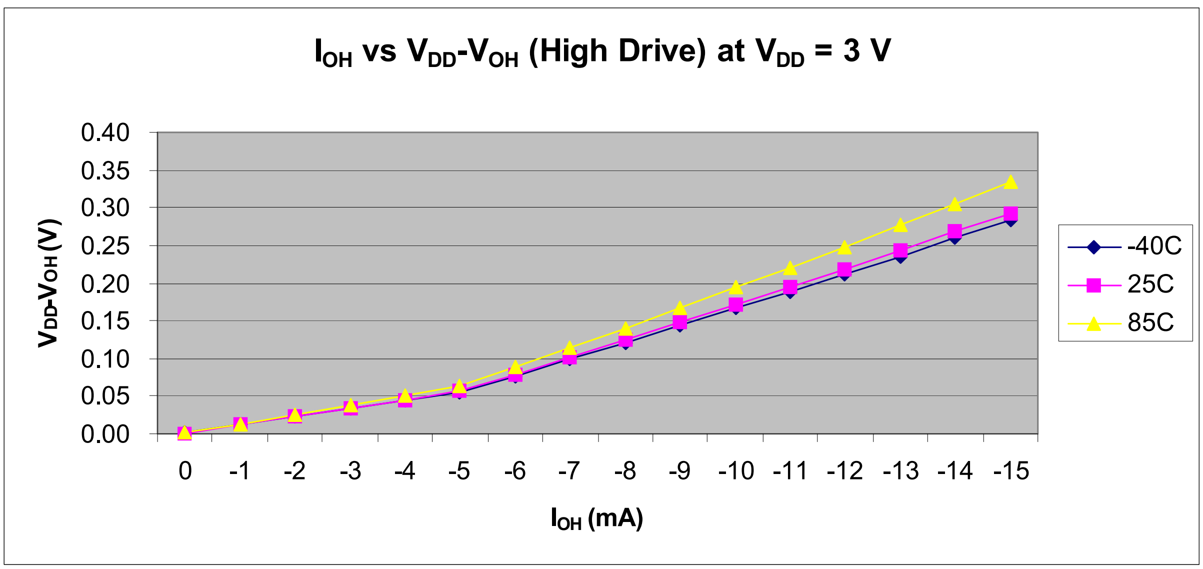


Figure 5. Typical I_{OH} (High Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 3 V

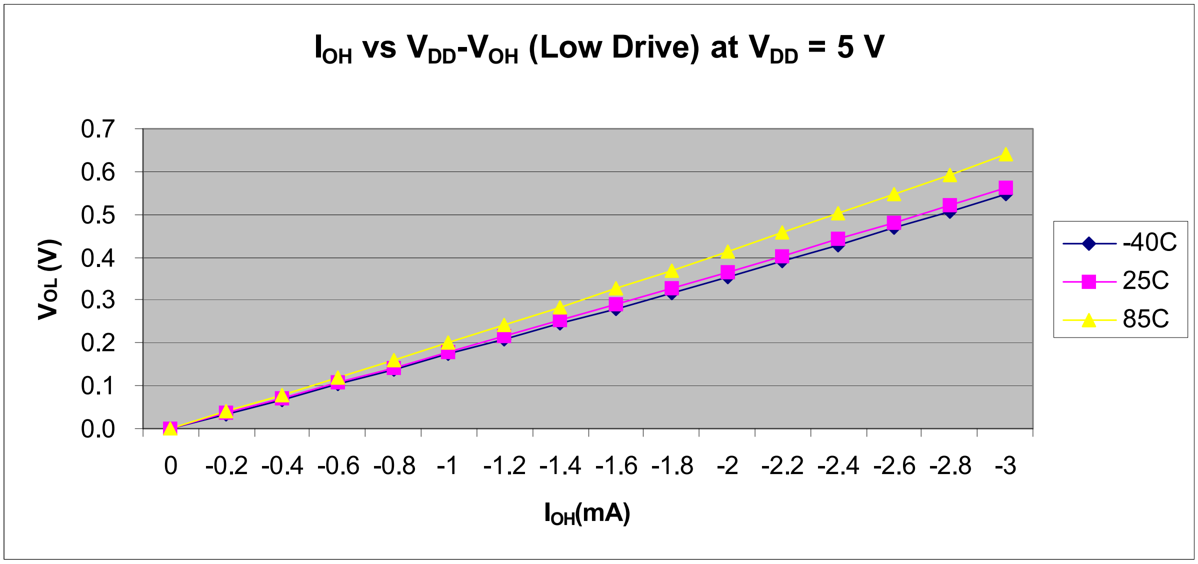


Figure 6. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 5 V

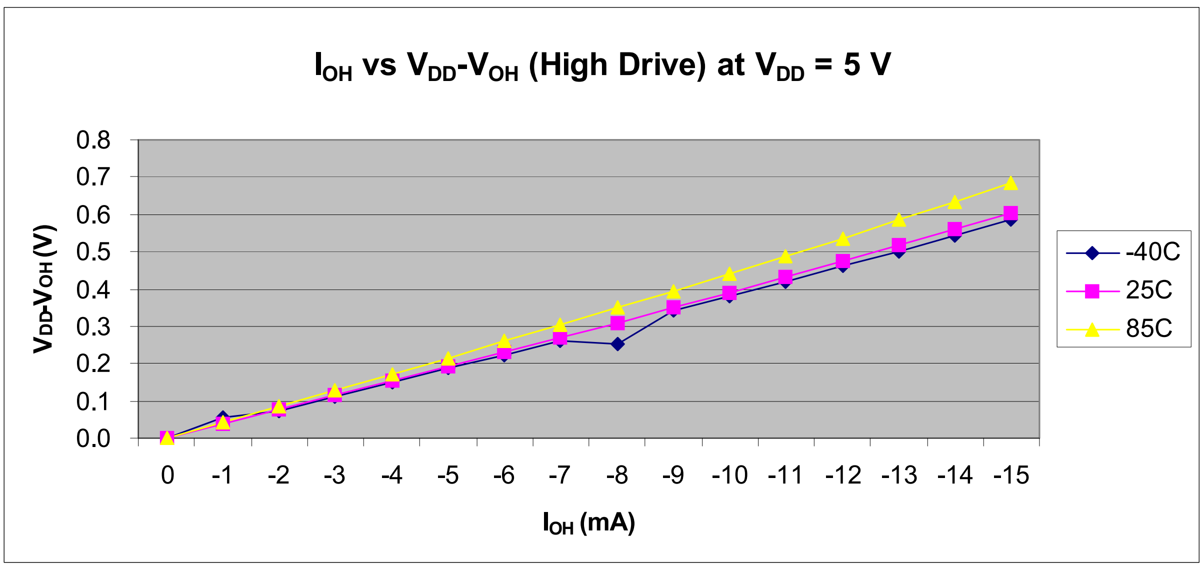


Figure 7. Typical I_{OH} (High Drive) vs V_{DD}–V_{OH} at V_{DD} = 5 V

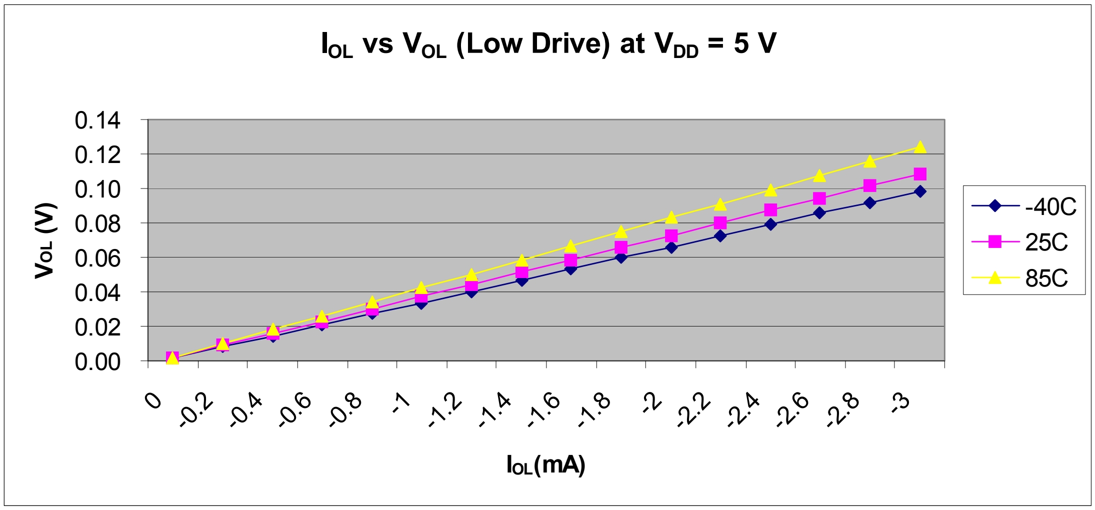


Figure 8. I_{OL} vs V_{OL} (Low Drive) at V_{DD} = 5 V

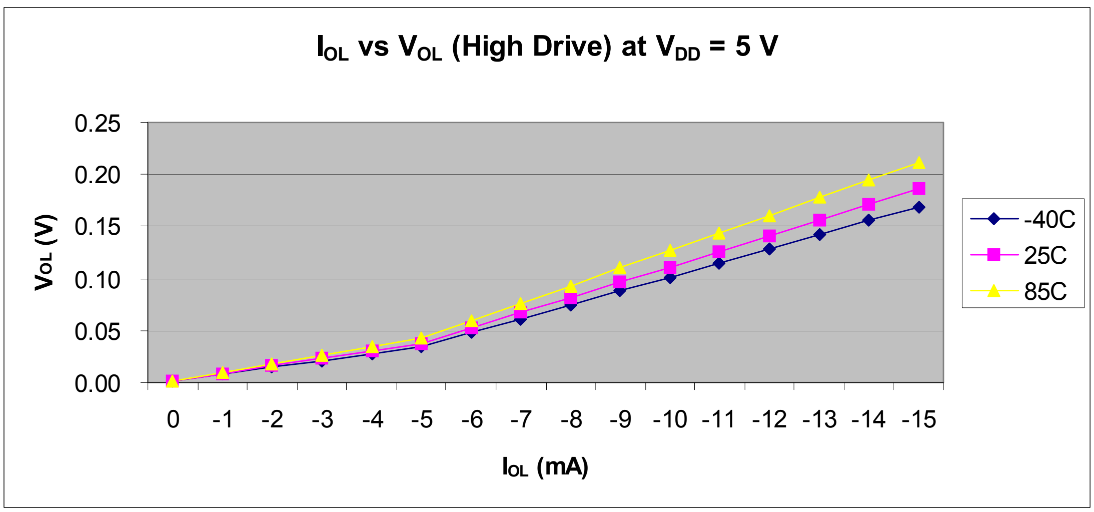


Figure 9. I_{OL} vs V_{OL} (High Drive) at V_{DD} = 5 V

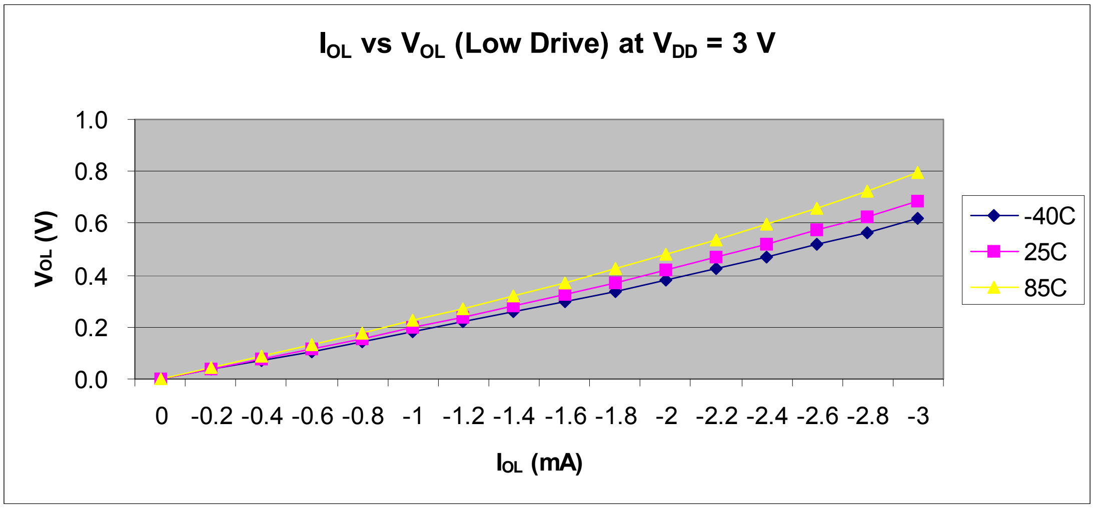


Figure 10. I_{OL} vs V_{OL} (Low Drive) at V_{DD} = 3 V

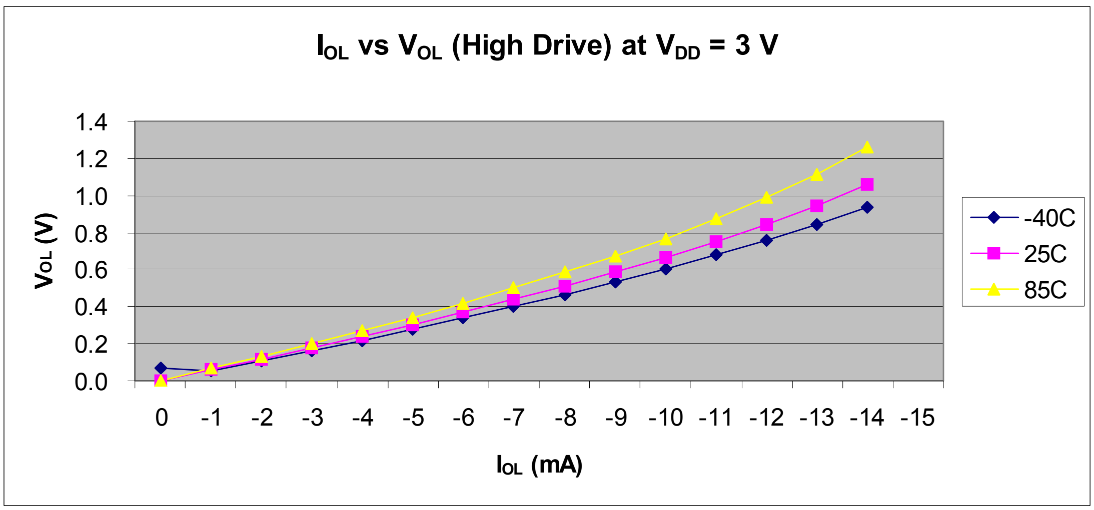


Figure 11. I_{OL} vs V_{OL} (High Drive) at V_{DD} = 3 V

3.6 Supply Current Characteristics

Table 7. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz, BLPE mode)	RI_{DD}	5	1.03	—	mA
				3	0.83	—	
2	P	Run supply current[3] measured at (CPU clock = 48 MHz, f_{Bus} = 24 MHz, PEE mode, all module on)	RI_{DD}	5	19.93	—	mA
				3	18.74	—	
3	P	Stop2 mode supply current	$S2I_{DD}$	5	1.36	—	μA
				3	1.18	—	μA
4	P	Stop3 mode supply current, all module off	$S3I_{DD}$	5	1.50	—	μA
				3	1.31	—	μA
5	P	RTC adder to stop2 or stop3[3], 25 °C	ΔI_{SRTC}	5	300	—	nA
				3	300	—	nA
6	P	LVD adder to stop3 (LVDE = LVDSE = 1)	ΔI_{SLVD}	5	106.7	—	μA
				3	95.6	—	μA
7	P	Adder to stop3 for oscillator enabled[4] (ERCLKEN =1 and EREFSTEN = 1)	ΔI_{SOSC}	5	5.6	—	μA
				3	5.3	—	μA
8	T	USB module enable current[5]	ΔI_{USBE}	5	1.5	—	mA
9	T	USB suspend current[6]	I_{SUSP}	5	273.3	—	μA

1 Typicals are measured at 25 °C. See Figure 12 through Figure 10 for typical curves across voltage/temperature.

2 Values given here are preliminary estimates prior to completing characterization.

3 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 μA at 5 V and 422 μA at 3 V with f_{Bus} = 1 MHz.

4 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

5 Here USB module is enabled and clocked at 48 MHz (USBEN = 1, USBVREN =1, USBPHYEN = 1 and USBPU = 1), and D+ and D– pulled down by two 15.1 kΩ resisters independently. The current consumption may be much higher when the packets are being transmitted through the attached cable.

6 MCU enters stop3 mode, USB bus in idle state. The USB suspend current will be dominated by the D+ pullup resister.

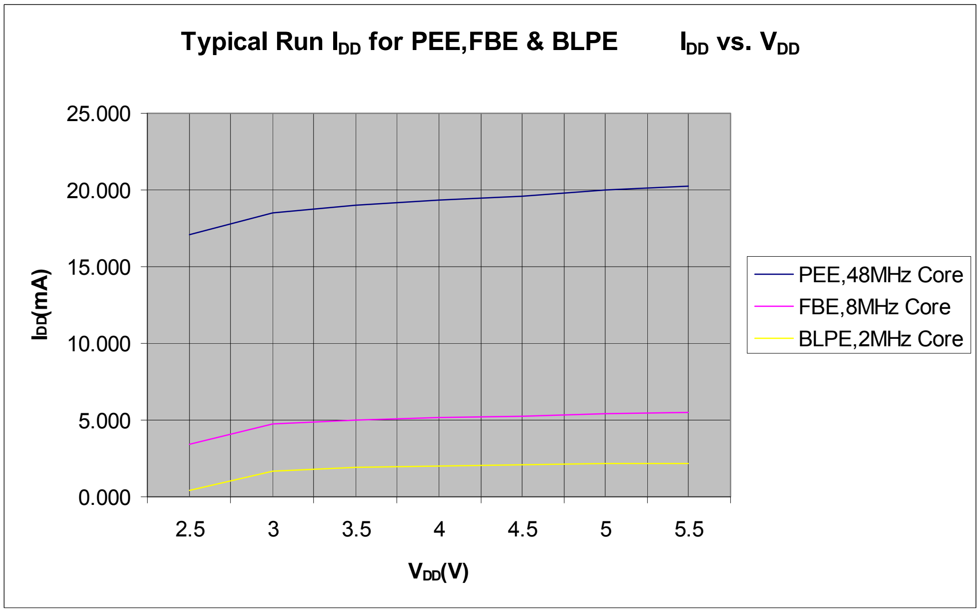


Figure 12. Typical Run I_{DD} for PEE, FBE and BLPE Modes (I_{DD} vs. V_{DD})

3.7 External Oscillator (XOSC) Characteristics

Table 8. Oscillator Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1) PEE or PBE mode[3] High range (RANGE = 1, HGO = 1) BLPE mode High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	 32 1 1 1 1	 — — — — —	 38.4 5 16 16 8	 kHz MHz MHz MHz MHz
2	—	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time[4] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[5] High range, high gain (RANGE = 1, HGO = 1)[5]	 $t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] PEE or PBE mode[3] BLPE mode	f_{extal}	 0.03125 1 0	 — — —	 5 16 40	MHz

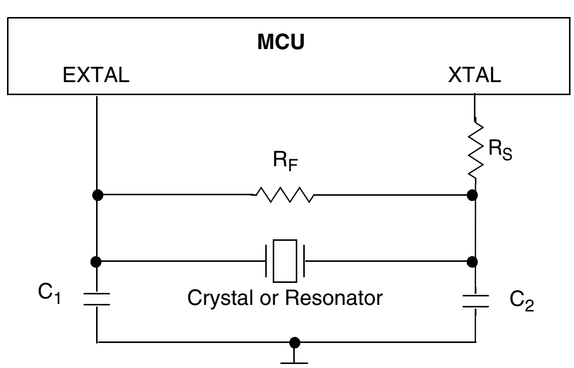
1 Typical data was characterized at 3.0 V, 25 °C or is recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divided using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

5 4 MHz crystal.



3.8 MCG Specifications

Table 9. MCG Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	C	Average internal reference frequency — untrimmed	f_{int_ut}	25	32.7	41.66	kHz
2	P	Average internal reference frequency — trimmed	f_{int_t}	31.25	—	39.0625	kHz
3	T	Internal reference startup time	t_{irefst}	—	60	100	μs
4	C	DCO output frequency range — untrimmed	f_{dco_ut}	25.6	33.48	42.66	MHz
5	P	DCO output frequency range — trimmed	f_{dco_t}	32	—	40	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[1]	$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[2]	$t_{pll\_acquire}$	—	—	1	ms
12	C	Long term Jitter of DCO output clock (averaged over 2ms interval)[3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
14	D	PLL reference frequency range	f_{pll_ref}	1.0	—	2.0	MHz
15	T	Long term accuracy of PLL output clock (averaged over 2 ms)	$f_{pll\_jitter\_2ms}$	—	0.590[4]	—	%
16	T	Jitter of PLL output clock measured over 625 ns[5]	$f_{pll\_jitter\_625ns}$	—	0.566[4]	—	%
17	D	Lock entry frequency tolerance[6]	D_{lock}	±1.49	—	±2.98	%
18	D	Lock exit frequency tolerance[7]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ $1075(1/f_{int\_t})$	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ $1075(1/f_{pll\_ref})$	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz
22	D	Loss of external clock minimum frequency — RANGE = 1	f_{loc_high}	(16/5) x f_{int}	—	—	kHz

1 This specification applies any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

2 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[3] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

[4] Jitter measurements are based upon a 48 MHz clock frequency.

[5] 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

[6] Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

[7] Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.9 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.9.1 Control Timing

Figure 13. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	$1.5 \times t_{Self\_reset}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	25	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	25	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	C	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	3 30	— —	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

[3] This is the minimum pulse width guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

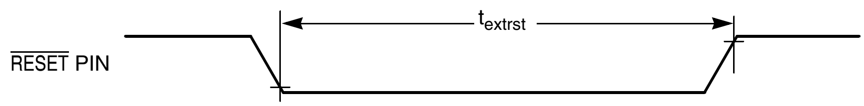


Figure 14. Reset Timing

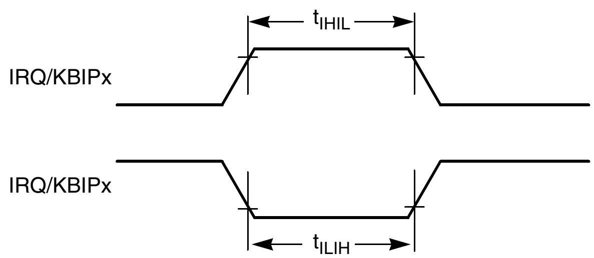


Figure 15. IRQ/KBIPx Timing

3.9.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 10. TPM Input Timing

Num	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	D	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

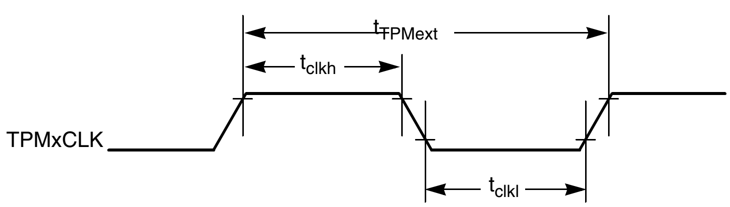


Figure 16. Timer External Clock

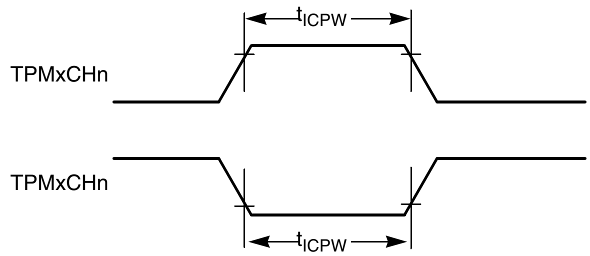


Figure 17. Timer Input Capture Pulse

3.10 SPI Characteristics

Table 11 and Figure 18 through Figure 21 describe the timing requirements for the SPI system.

Table 11. SPI Electrical Characteristic

Num[1]	C	Characteristic[2]	Symbol	Min	Typical	Max	Unit
1	D	Operating frequency[3] Master Slave	f_{op} f_{op}	f_{Bus}/2048DC	— —	f_{Bus}/2 f_{Bus}/4	Hz
2	D	Cycle time Master Slave	t_{SCK} t_{SCK}	2 4	— —	2048 —	t_{cyc}
3	D	Enable lead time Master Slave	t_{Lead} t_{Lead}	— —	1/2 1/2	— —	t_{SCK}
4	D	Enable lag time Master Slave	t_{Lag} t_{Lag}	— —	1/2 1/2	— —	t_{SCK}
5	D	Clock (SPSCK) high time Master Slave	t_{SCKH}	— 1/2 t_{SCK} – 25	1/2 t_{SCK} 1/2 t_{SCK}	— —	ns
6	D	Clock (SPSCK) low time Master Slave	t_{SCKL}	— 1/2 t_{SCK} – 25	1/2 t_{SCK} 1/2 t_{SCK}	— —	ns
7	D	Data setup time (inputs) Master Slave	$t_{SI(M)}$ $t_{SI(S)}$	30 30	— —	— —	ns
8	D	Data hold time (inputs) Master Slave	$t_{HI(M)}$ $t_{HI(S)}$	30 30	— —	— —	ns
9	D	Access time, slave[4]	t_A	—	—	40	ns
10	D	Disable time, slave[5]	t_{dis}	—	—	40	ns
11	D	Data setup time (outputs) Master Slave	t_{SO} t_{SO}	— —	— —	25 25	ns
12	D	Data hold time (outputs) Master Slave	t_{HO} t_{HO}	–10 –10	— —	— —	ns

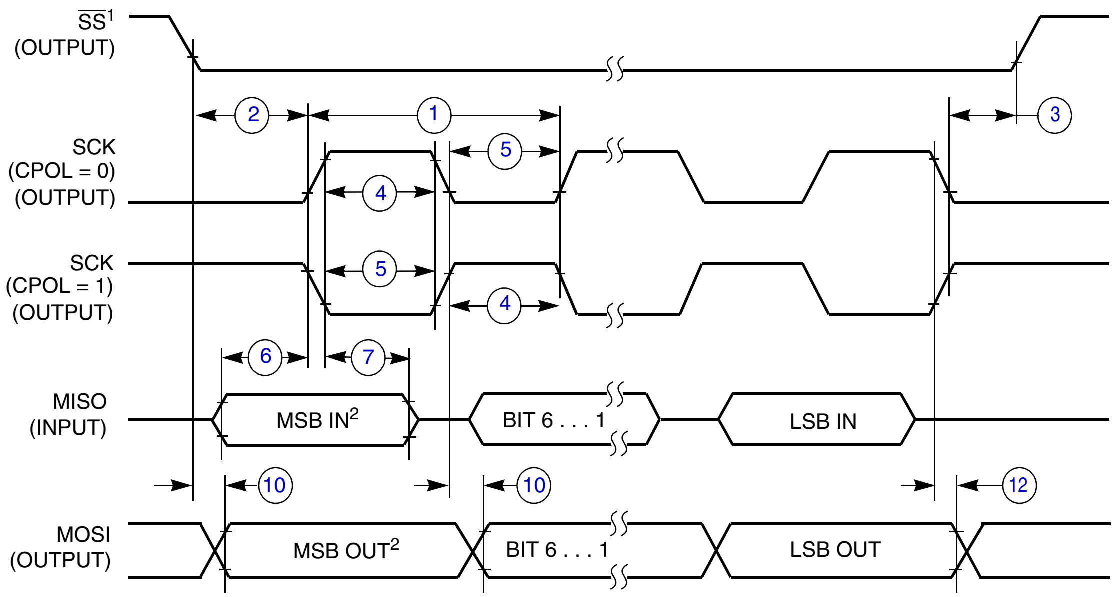
1 Refer to Figure 18 through Figure 21.

2 All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted; 50 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 The maximum frequency is 8 MHz when input filter on SPI pins is disabled.

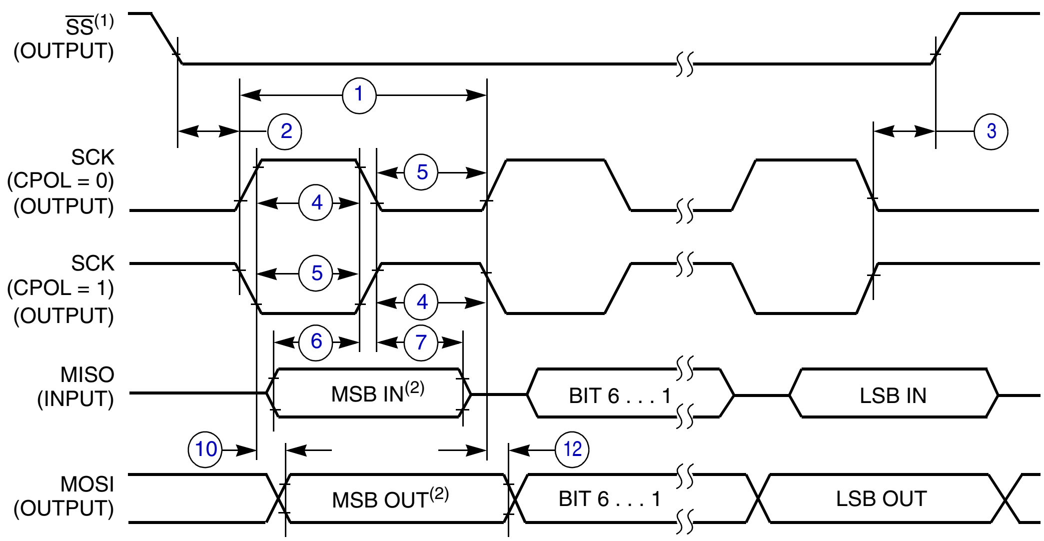
4 Time to data active from high-impedance state.

5 Hold time to high-impedance state.



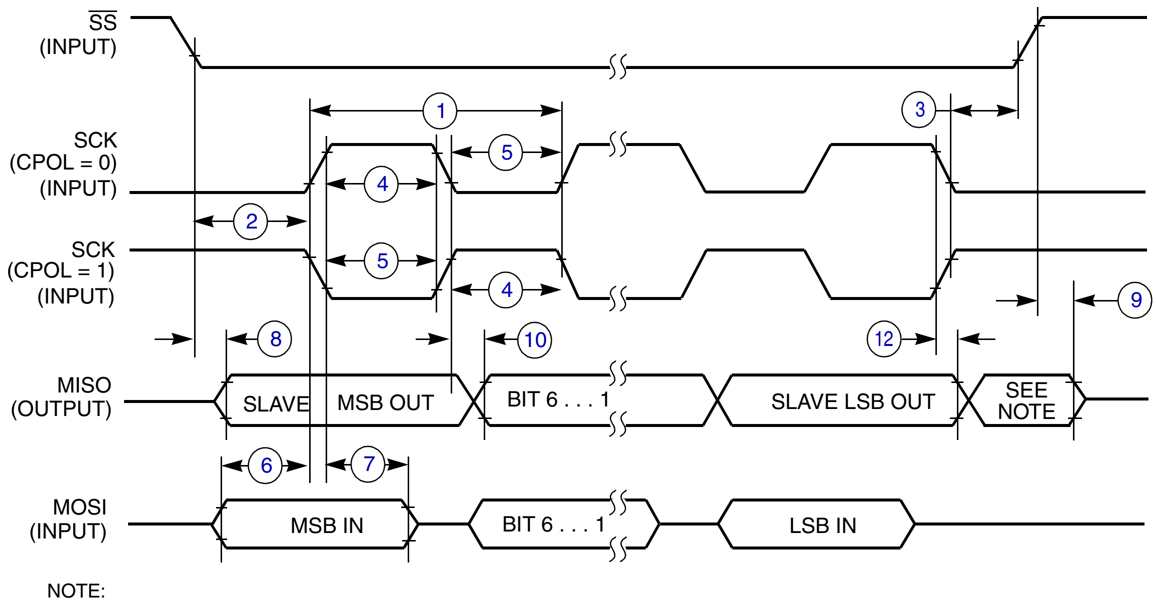
NOTES:
1. SS output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

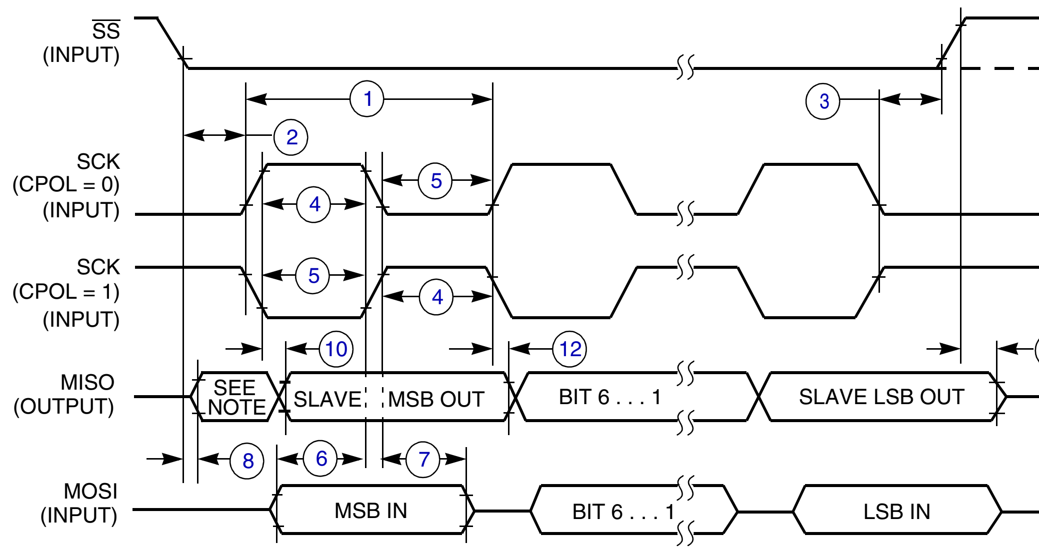
Figure 19. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 20. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 21. SPI Slave Timing (CPHA = 1)

3.11 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 12. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	D	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	D	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	P	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
6	P	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
7	P	Page erase time[3]	t_{Page}		4000		t_{Fcyc}
8	P	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to 85 °C T = 25 °C	—	10,000 —	— 100,000	— —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 The frequency of this clock is controlled by a software setting.

3 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

4 Typical endurance for flash was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory.*

5 Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

3.12 USB Electricals

The USB electricals for the S08USBV1 module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale S08USBV1 implementation requires additional or deviant electrical characteristics, this space would be used to communicate that information.

Table 13. Internal USB 3.3 V Voltage Regulator Characteristics

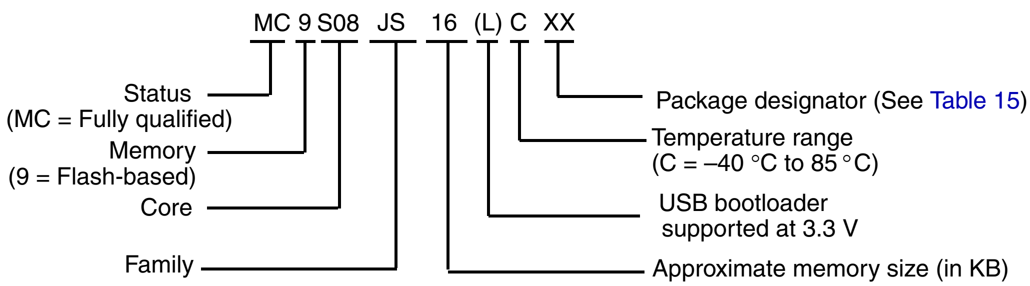
	Symbol	Min	Typical	Max	Unit
Regulator operating voltage	V_{regin}	3.9	—	5.5	V
V_{reg} output	V_{regout}	3	3.3	3.6	V
V_{reg} filter capacitor	C_{usbreg}	—	100	—	pF
V_{usb33} input with internal V_{reg} disabled	$V_{usb33in}$	3	3.3	3.6	V

Table 14. External 3.3 V Voltage Regulator Supply for V_{usb33} Pin

	Symbol	Min	Typical	Max	Unit
External 3.3 V regulator output current	—	39	—	—	mA

4 Ordering Information

This section contains ordering information for Device Numbering System. See below for an example of the device numbering system.



4.1 Package Information

Table 15. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
24	Quad Flat No-Leads	QFN	FK	1982-01	98ARL10608D
20	Wide Body Small Outline Integrated Circuit	W-SOIC	WJ	751D	98ASB42343B

4.2 Mechanical Drawings

This following pages contain mechanical specifications for MC9S08JS16 series package options.

- 24-pin QFN (quad flat no-lead)
- 20-pin W-SOIC (wide body small outline integrated circuit)

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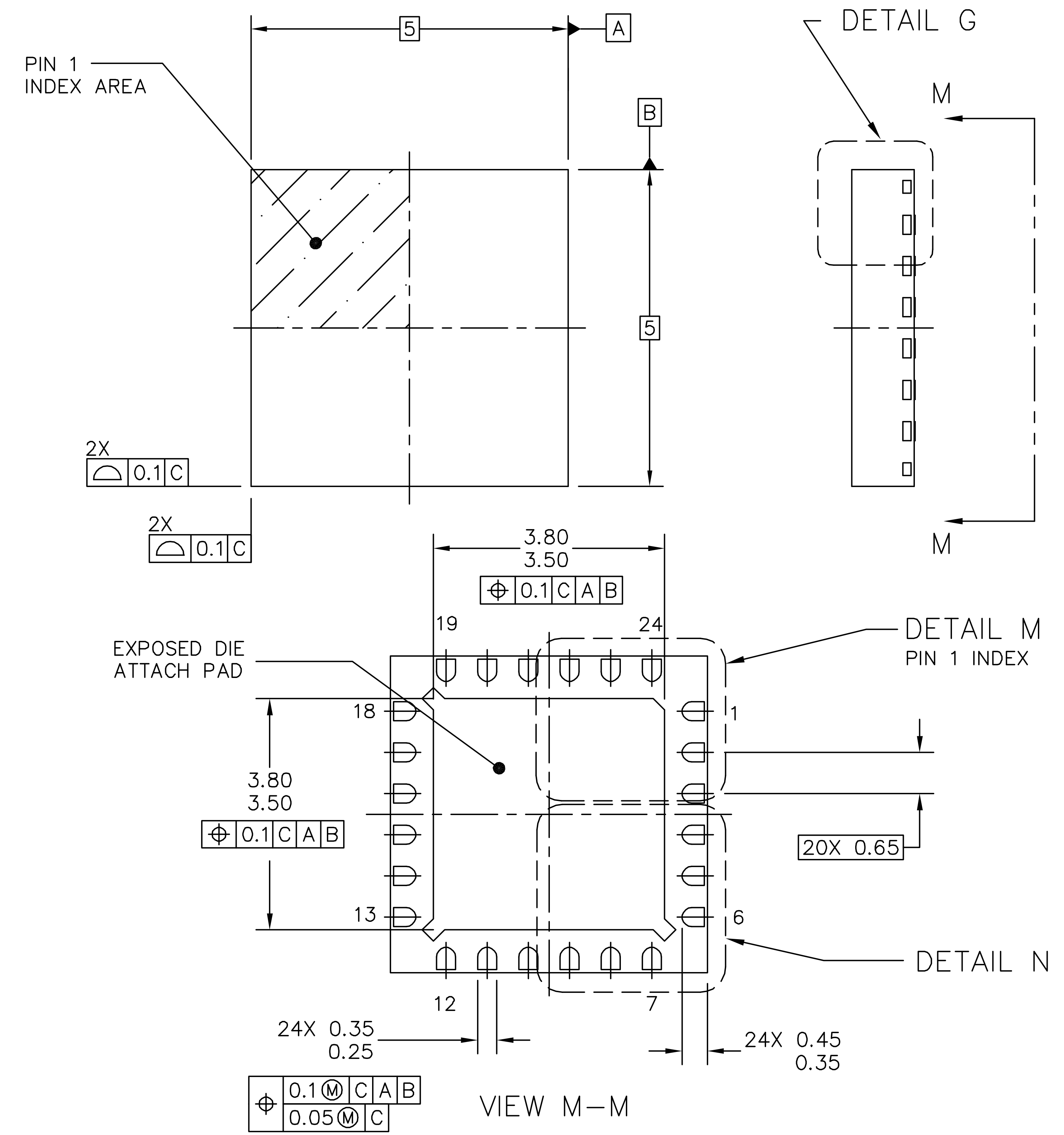
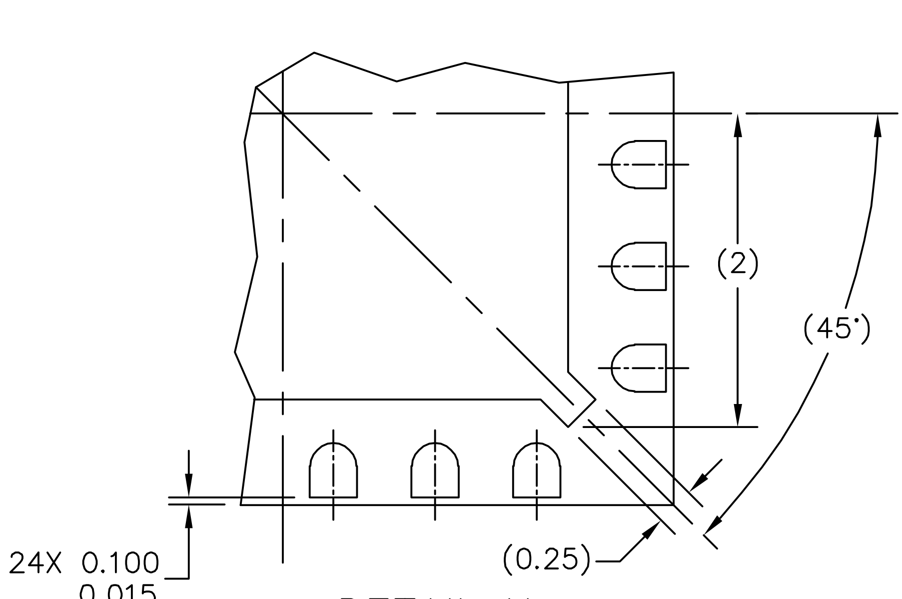
		PAGE: 1982
	DO NOT SCALE THIS DRAWING	REV: 0

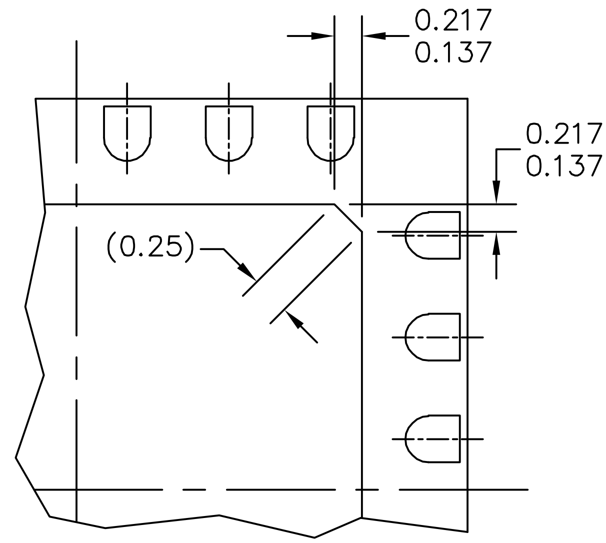


TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.65 PITCH (5 X 5 X 1)	CASE NUMBER: 1982–01	
	STANDARD: JEDEC–MO–220 VHHC–1	
	PACKAGE CODE: 6238	SHEET: 1 OF 4



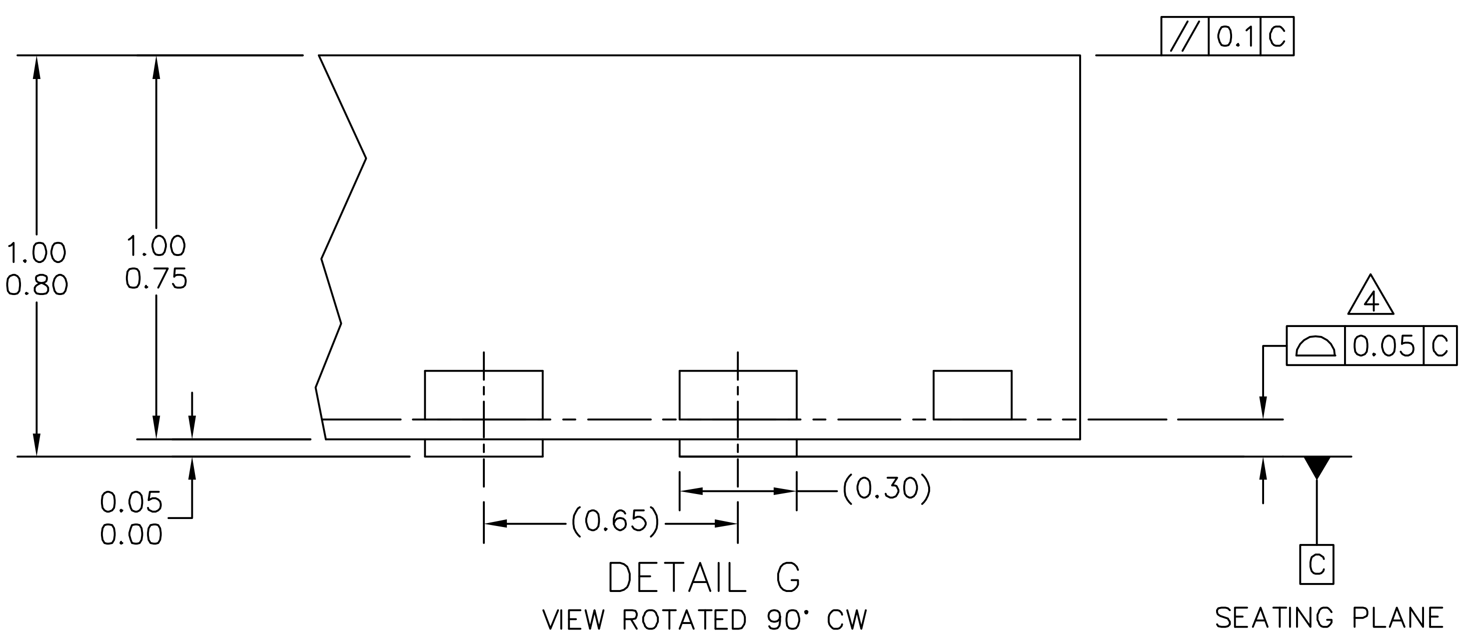
DETAIL N

PREFERRED CORNER CONFIGURATION



DETAIL M

PREFERED PIN 1 BACKSIDE IDENTIFIER

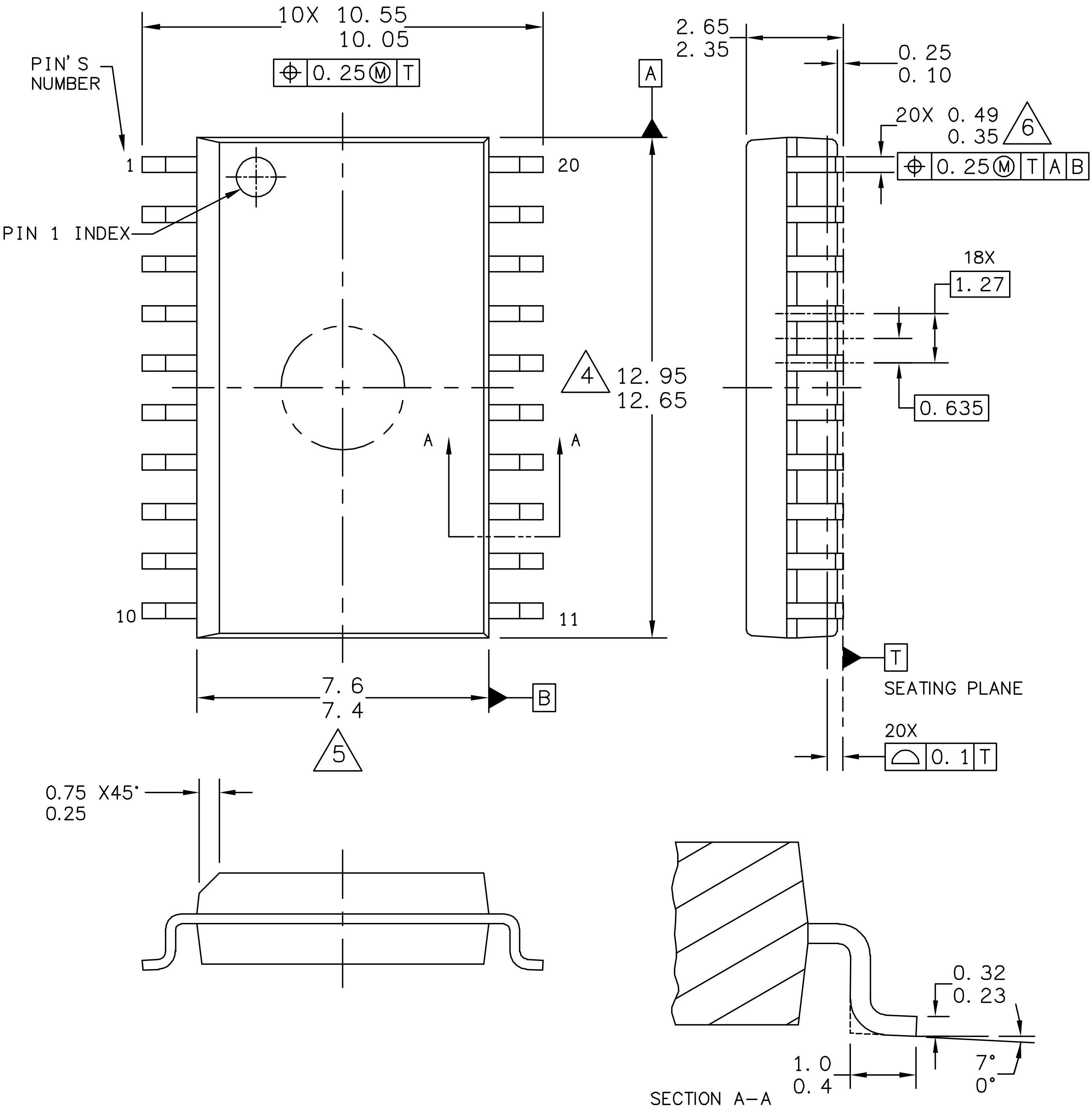


DETAIL G

VIEW ROTATED 90° CW

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	