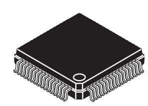
Freescale Semiconductor
Data Sheet: Technical Data

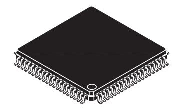
An Energy-Efficient Solution from Freescale

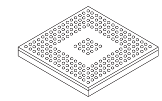
Document Number: MC9S08MM128
Rev. 3, 10/2010

MC9S08MM128 series

Covers: MC9S08MM128, and MC9S08MM64, MC9S08MM32, and MC9S08MM32A


64-LQFP 10mm x 10mm


80-LQFP 12mm x 12mm


81-MapBGA 10mm x10mr

8-Bit HCS08 Central Processor Unit (CPU)

- Up to 48-MHz CPU above 2.4 V, 40 MHz CPU above 2.1 V, and 20 MHz CPU above 1.8 V across temperature of -40°C to 105°C
- HCS08 instruction set with added BGND instruction
- Support for up to 33 interrupt/reset sources

On-Chip Memory

- 128 K Dual Array Flash read/program/erase over full operating voltage and temperature
- 12 KB Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and Flash

Power-Saving Modes

- Two ultra-low power stop modes. Peripheral clock enable register can disable clocks to unused modules to reduce currents
- Time of Day (TOD) — Ultra-low power 1/4 sec counter with up to 64s timeout.
- Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to the TOD. 6 usec typical wake up time from stop3 mode

Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator dedicated for TOD operation.
- Oscillator (XOSC2) — for high frequency crystal input for MCG reference to be used for system clock and USB operations.
- Multipurpose Clock Generator (MCG) — PLL and FLL; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 48 MHz.

System Protection

- Watchdog computer operating properly (COP) reset Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points; separate low-voltage warning with optional interrupt; selectable trip points
- Illegal opcode and illegal address detection with reset
- Flash block protection for each array to prevent accidental write/erasure
- Hardware CRC to support fast cyclic redundancy checks

Development Support

- Single-wire background debug interface
- Real-time debug with 6 hardware breakpoints (4 PC, 1 address and 1 data) Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- On-chip in-circuit emulator (ICE) debug module containing 3 comparators and 9 trigger modes

Peripherals

- **CMT**— Carrier Modulator timer for remote control communications. Carrier generator, modulator and driver for dedicated infrared out. Can be used as an output compare timer.
- **IIC**— Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 11-bit addressing
- **PRACMP** — Analog comparator with selectable interrupt; compare option to programmable internal reference voltage; operation in stop3
- **SCI** — Two serial communications interfaces with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; High current drive on Tx on SCI1 and SCI2; wake-up from stop3 on Rx edge
- **SPI1**— Serial peripheral interface (SPI) with 64-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI2**— Serial peripheral interface with full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **TPM** — Two 4-channel Timer/PWM Module; Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator
- **USB** — Supports USB in full-speed device configuration. On-chip transceiver and 3.3V regulator help save system cost, fully compliant with USB Specification 2.0. Allows control, bulk, interrupt and isochronous transfers. Not available on MC9S08MM32A devices.
- **ADC16** — 16-bit Successive approximation ADC with up to 4 dedicated differential channels and 8 single-ended channels; range compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V, Configurable hardware trigger for 8 Channel select and result registers
- **PDB** — Programmable delay block with 16-bit counter and modulus and prescale to set reference clock to bus divided by 1 to bus divided by 2048; 8 trigger outputs for ADC16 module provides periodic coordination of ADC sampling sequence with sequence completion interrupt; Back-to-Back mode and Timed mode
- **DAC** — 12-bit resolution; 16-word data buffers with configurable watermark.
- **OPAMP** — Two flexible operational amplifiers configurable for general operations; Low offset and temperature drift.
- **TRIAMP** — Two trans-impedance amplifiers dedicated for converting current inputs into voltages.

Input/Output

- Up to 47 GPIOs and 2 output-only pin and 1 input-only pin.
- Voltage Reference output (VREFO).
- Dedicated infrared output pin (IRO) with high current sink capability.
- Up to 16 KBI pins with selectable polarity.

Package Options

- 81-MBGA 10x10 mm
- 80-LQFP 12x12 mm
- 64-LQFP 10x10 mm

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08MM128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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1 Devices in the MC9S08MM128 series

The following table summarizes the feature set available in the MC9S08MM128 series of MCUs.

Table 1. MC9S08MM128 series Features by MCU and Package

Feature	MC9S08MM128			MC9S08MM64	MC9S08MM32	MC9S08MM32A
Pin quantity	81	80	64	64	64	64
FLASH size (bytes)	131072			65535	32768	32768
RAM size (bytes)	12K			12K	4K	2K
Programmable Analog Comparator (PRACMP)	yes			yes	yes	yes
Debug Module (DBG)	yes			yes	yes	yes
Multipurpose Clock Generator (MCG)	yes			yes	yes	yes
Inter-Integrated Communication (IIC)	yes			yes	yes	yes
Interrupt Request Pin (IRQ)	yes			yes	yes	yes
Keyboard Interrupt (KBI)	16	16	6	6	6	6
Port I/O[1]	47	46	33	33	33	33
Dedicated Analog Input Pins	12			12	12	12
Power and Ground Pins	8			8	8	8
Time Of Day (TOD)	yes			yes	yes	yes
Serial Communications (SCI1)	yes			yes	yes	yes
Serial Communications (SCI2)	yes			yes	yes	yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes	yes	yes
Serial Peripheral Interface 2 (SPI2)	yes			yes	yes	yes
Carrier Modulator Timer pin (IRO)	yes			yes	yes	yes
TPM input clock pin (TPMCLK)	yes			yes	yes	yes
TPM1 channels	4			4	4	4
TPM2 channels	4	4	2	2	2	2
XOSC1	yes			yes	yes	yes
XOSC2	yes			yes	yes	yes
USB	yes			yes	yes	no
Programmable Delay Block (PDB)	yes			yes	yes	yes
SAR ADC differential channels[2]	4	4	3	3	3	3
SAR ADC single-ended channels	8	8	6	6	6	6
DAC ouput pin (DACO)	yes			yes	yes	yes
Voltage reference output pin (VREFO)	yes			yes	yes	yes
General Purpose OPAMP (OPAMP)	yes			yes	yes	yes
Trans-Impedance Amplifier (TRIAMP)	yes			yes	yes	yes

[1] Port I/O count does not include two (2) output-only and one (1) input-only pins.
[2] Each differential channel is comprised of 2 pin inputs.

A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC16)	1
General Purpose Operational Amplifier (OPAMP)	1
Trans-Impedance Operational Amplifier (TRIAMP)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)[1]	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

[1] USB Module not available on MC9S08MM32A devices.

The block diagram in Figure 1 shows the structure of the MC9S08MM128 series MCU.

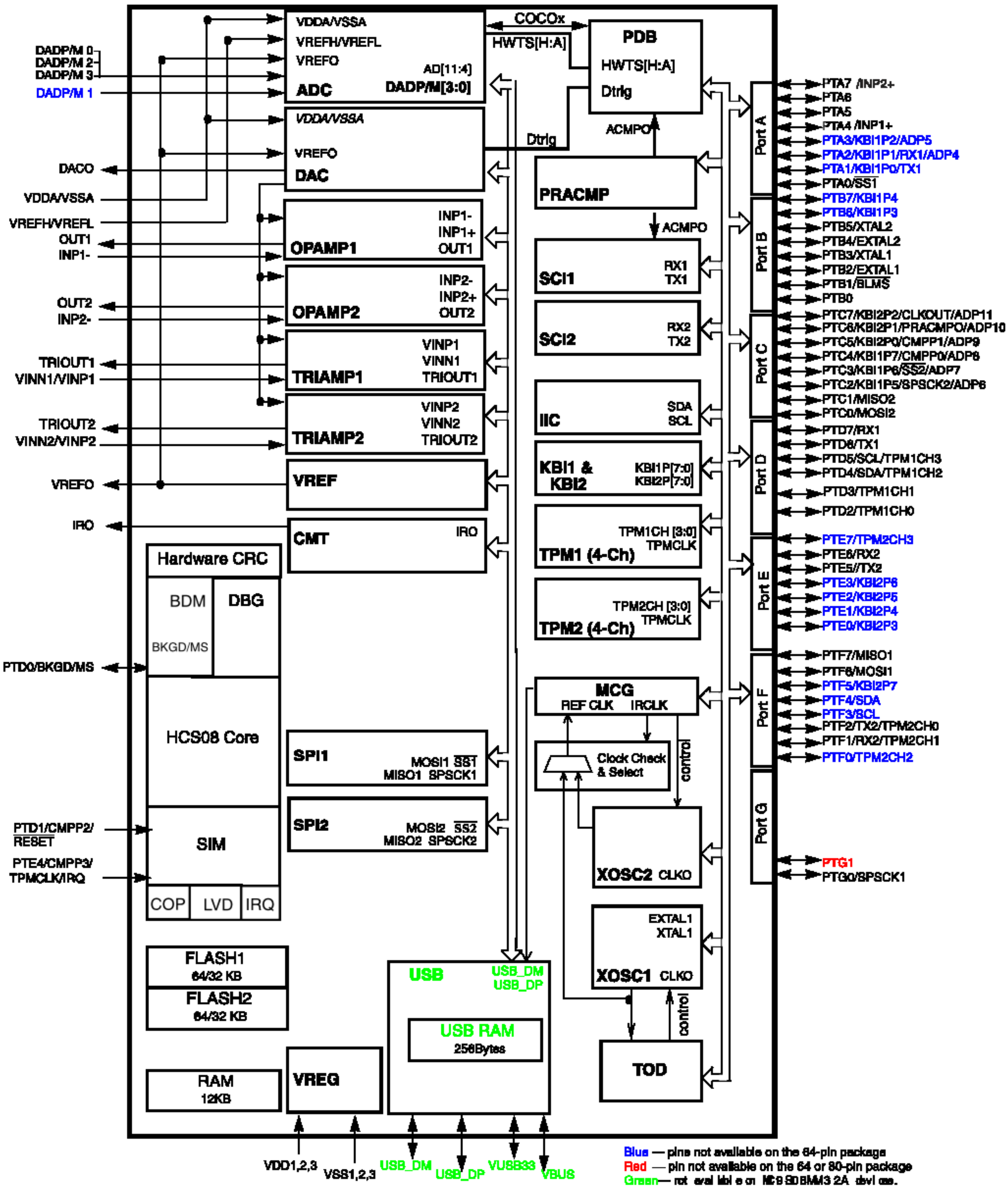


Figure 1. MC9S08MM128 series Block Diagram

1.1 Pin Assignments

This section shows the pin assignments for the MC9S08MM128 series devices.

1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration. The first illustrates the pinout configuration for MC9S08MM128, MC9S08MM64, and MC9S08MM32 devices.

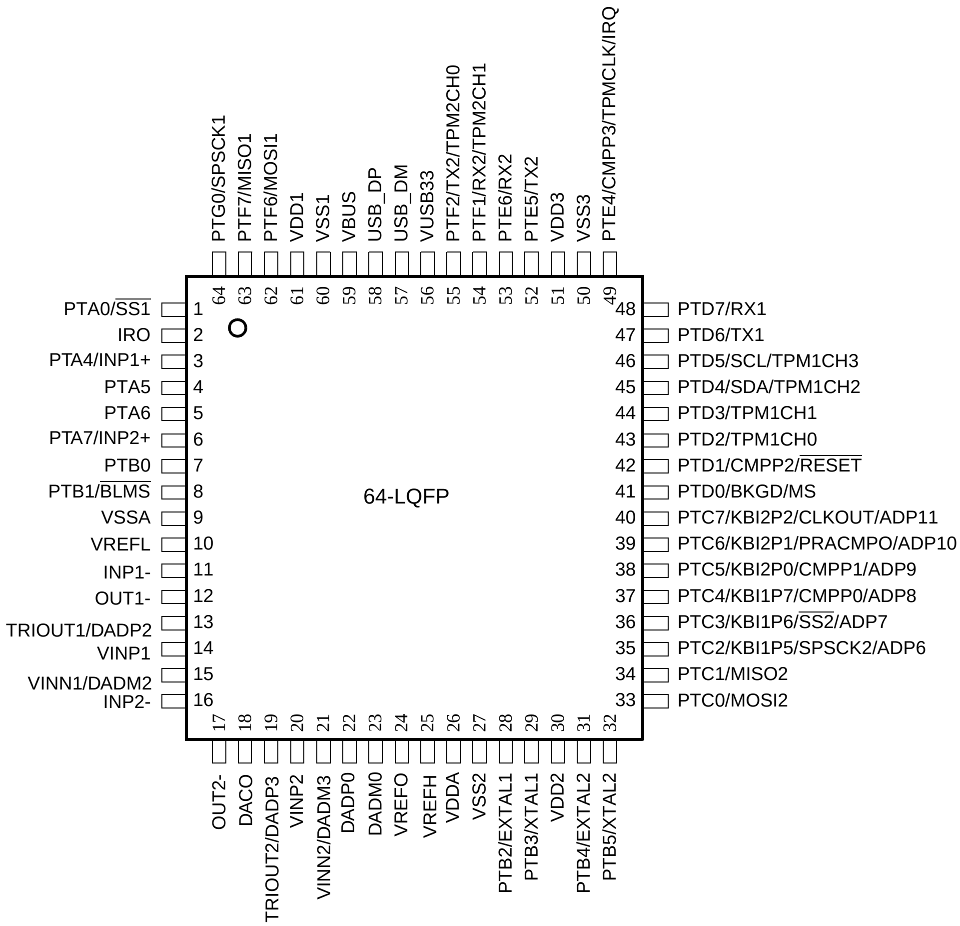


Figure 2. 64-Pin LQFP for MC9S08MM128, MC9S08MM64, and MC9S08MM32 devices

For MC9S08MM32A devices, pins 56, 57, 58, and 59 are no connects (NC) as illustrated in the following figure.

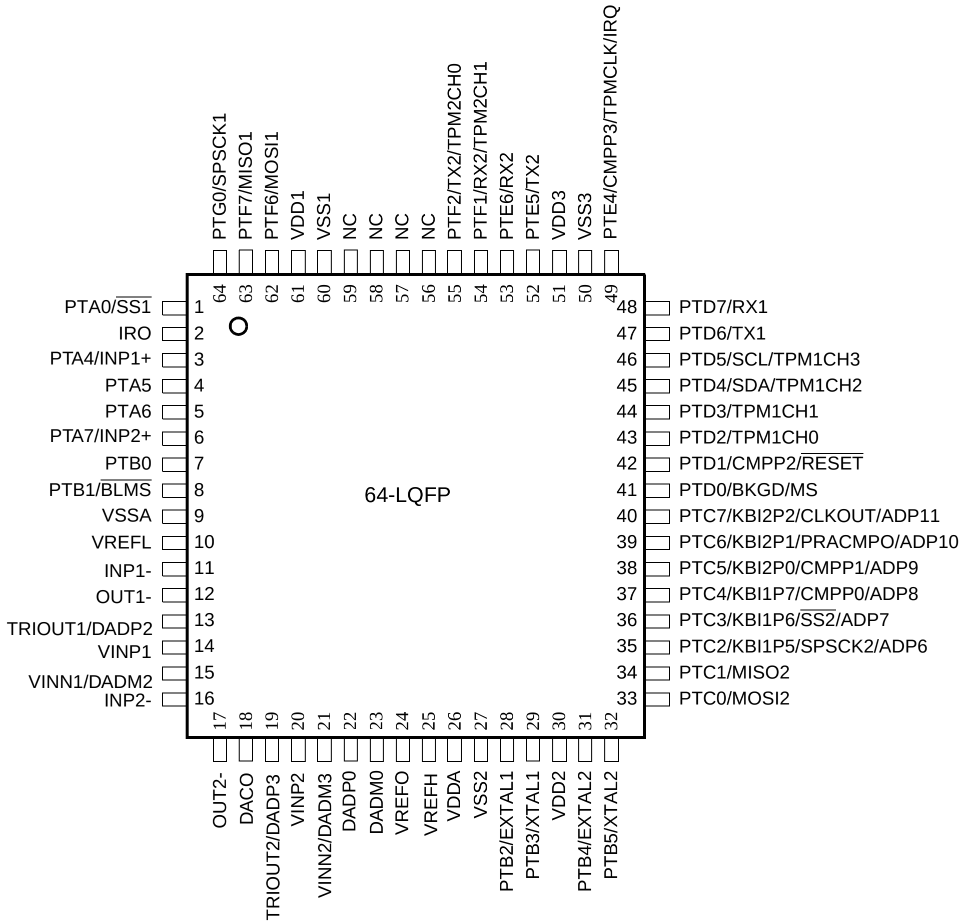


Figure 3. 64-Pin LQFP for MC9S08MM32A devices

1.1.2 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

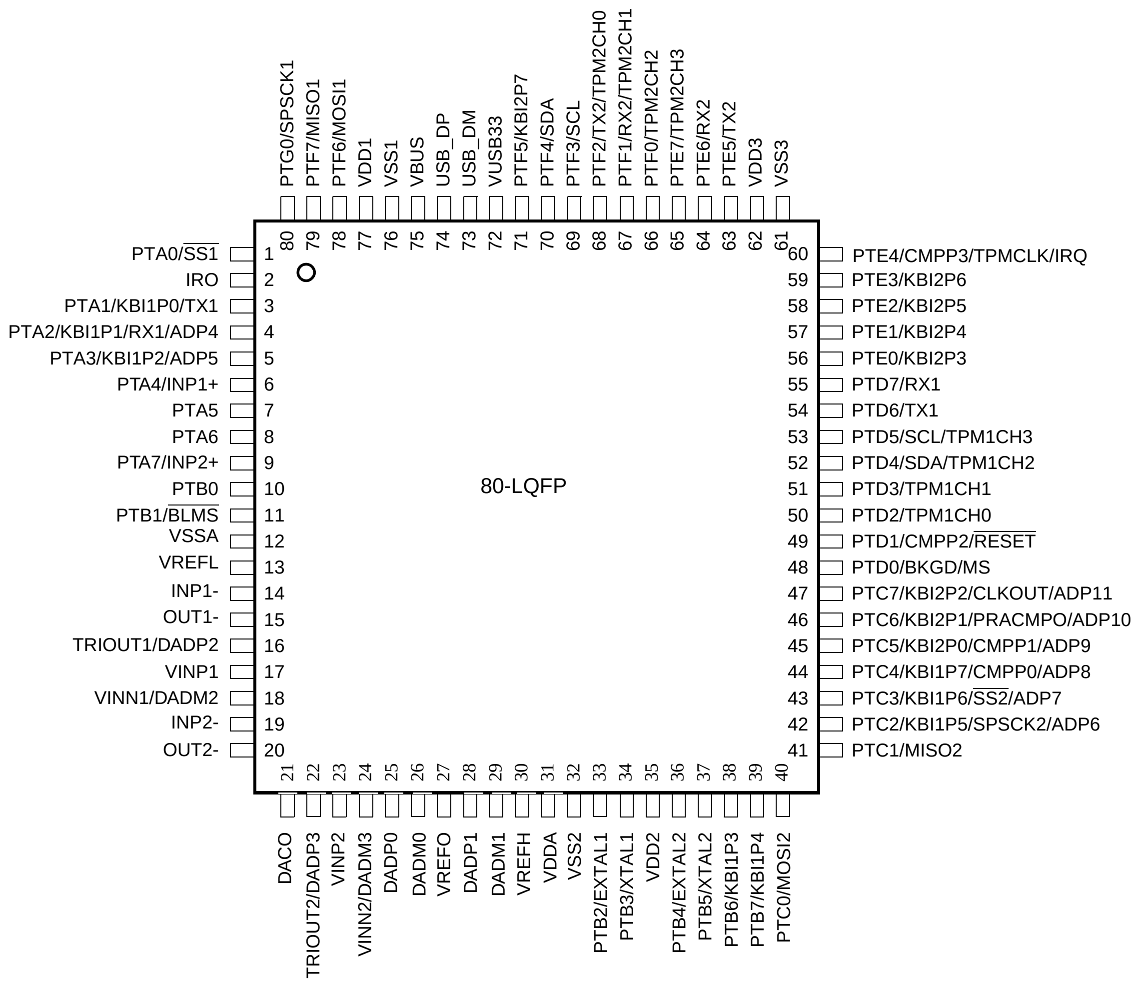


Figure 4. 80-Pin LQFP

1.1.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1
D	INP1-	PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0
E	OUT1	VINN1	OUT2	VDD2	VDD3	VDD1	PTD2	PTD3	PTD6
F	VINP1	TRIOUT1	INP2-	VSS2	VSS3	VSS1	PTB7	PTC7	PTD4
G	DADP0	DACO	TRIOUT2	VINN2	VREFO	PTB6	PTC0	PTC1	PTC2
H	DADM0	DADM1	DADP1	VINP2	PTC3	PTC4	PTD0	PTC5	PTC6
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5

Figure 5. 81-Pin MAPBGA

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{\text{SS1}}$	—	—	PTA0/$\overline{\text{SS1}}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	INP1+	—	—	PTA4/INP1+
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	INP2+	—	—	PTA7/INP2+
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{\text{BLMS}}$	—	—	PTB1/$\overline{\text{BLMS}}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	INP1-	—	—	—	INP1-
E1	15	12	OUT1	—	—	—	OUT1
F2	16	13	DADP2	TRIOUT1	—	—	DADP2/TRIOUT1
F1	17	14	VINP1	—	—	—	VINP1
E2	18	15	DADM2	VINN1	—	—	DADM2/VINN1
F3	19	16	INP2-	—	—	—	INP2-
E3	20	17	OUT2	—	—	—	OUT2
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	TRIOUT2	—	—	DADP3/TRIOUT2
H4	23	20	VINP2	—	—	—	VINP2
G4	24	21	DADM3	VINN2	—	—	DADM3/VINN2
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
J3	30	25	VREFH	—	—	—	VREFH
J4	31	26	VDDA	—	—	—	VDDA
F4	32	27	VSS2	—	—	—	VSS2
J5	33	28	PTB2	EXTAL1	—	—	PTB2/EXTAL1
J6	34	29	PTB3	XTAL1	—	—	PTB3/XTAL1
E4	35	30	VDD2	—	—	—	VDD2
J8	36	31	PTB4	EXTAL2	—	—	PTB4/EXTAL2
J9	37	32	PTB5	XTAL2	—	—	PTB5/XTAL2
G6	38	—	PTB6	KBI1P3	—	—	PTB6/KBI1P3
F7	39	—	PTB7	KBI1P4	—	—	PTB7/KBI1P4
G7	40	33	PTC0	MOSI2	—	—	PTC0/MOSI2
G8	41	34	PTC1	MISO2	—	—	PTC1/MISO2
G9	42	35	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
H5	43	36	PTC3	KBI1P6	$\overline{\text{SS2}}$	ADP7	PTC3/KBI1P6/$\overline{\text{SS2}}$/ADP7
H6	44	37	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
H8	45	38	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
H9	46	39	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	47	40	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
H7	48	41	PTD0	BKGD	MS	—	PTD0/BKGD/MS
J7	49	42	PTD1	CMPP2	$\overline{\text{RESET}}$	—	PTD1/CMPP2/$\overline{\text{RESET}}$
E7	50	43	PTD2	TPM1CH0	—	—	PTD2TPM1CH0
E8	51	44	PTD3	TPM1CH1	—	—	PTD3/TPM1CH1
F9	52	45	PTD4	SDA	TPM1CH2	—	PTD4/SDA/TPM1CH2
D7	53	46	PTD5	SCL	TPM1CH3	—	PTD5/SCL/TPM1CH3
E9	54	47	PTD6	TX1	—	—	PTD6/TX1
D8	55	48	PTD7	RX1	—	—	PTD7/RX1
D9	56	—	PTE0	KBI2P3	—	—	PTE0/KBI2P3
C9	57	—	PTE1	KBI2P4	—	—	PTE1/KBI2P4
C8	58	—	PTE2	KBI2P5	—	—	PTE2/KBI2P5
B9	59	—	PTE3	KBI2P6	—	—	PTE3/KBI2P6
A9	60	49	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33[1]	—	—	—	VUSB33
B4	73	57	USB_DM[2]	—	—	—	USB_DM
A4	74	58	USB_DP[3]	—	—	—	USB_DP
A5	75	59	VBUS[4]	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

[1] NC on MC9S08MM32A devices.
[2] NC on MC9S08MM32A devices.
[3] NC on MC9S08MM32A devices.
[4] NC on MC9S08MM32A devices.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08MM128/64/32/32A microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating		Value	Unit
1	T_A	Operating temperature range (packaged):			°C
			MC9S08MM128	–40 to 105	
			MC9S08MM64	–40 to 105	
			MC9S08MM32	–40 to 105	
			MC9S08MM32A	–40 to 105	
2	T_{JMAX}	Maximum junction temperature		135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s			°C/W
			81-pin MBGA	77	
			80-pin LQFP	55	
			64-pin LQFP	68	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p			°C/W
			81-pin MBGA	47	
			80-pin LQFP	40	
			64-pin LQFP	49	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
1	V_{DD}	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600\ \mu A$	$V_{DD} - 0.5$	—	—	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current	Max total I_{OH} for all ports					
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage	All I/O pins, low-drive strength					
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600\ \mu A$	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current Max total I_{OL} for all ports	—	—	—	100	mA	D
6	V_{IH}	Input high voltage	all digital inputs					
			all digital inputs, $V_{DD} > 2.7$ V	$0.70 \times V_{DD}$	—	—	V	P
			all digital inputs, $2.7\ V > V_{DD} \geq 1.8$ V	$0.85 \times V_{DD}$	—	—	V	P

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic		Condition	Min	Typ[1]	Max	Unit	C
7	V_{IL}	Input low voltage	all digital inputs						
				all digital inputs, $V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
				all digital inputs, $2.7 > V_{DD} \geq 1.8$ V	—	—	0.30 x V_{DD}	V	P
8	V_{hys}	Input hysteresis	all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current	all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.5	µA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3]	all digital input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	0.003	0.5	µA	P
11	R_{PU}	Pull-up resistors		—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]		—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7]	Single pin limit						
				$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
			Total MCU limit, includes sum of all stressed pins						
				$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins		—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage		—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]		—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time		—	10	—	—	µs	D
18	V_{LVDH}[9]	Low-voltage detection threshold — high range	V_{DD} falling						
				—	2.11	2.16	2.22	V	P
			V_{DD} rising						
				—	2.16	2.23	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9]	V_{DD} falling						
				—	1.80	1.84	1.88	V	P
			V_{DD} rising						
				—	1.88	1.93	1.96	V	P

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic		Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVWH}	Low-voltage warning threshold — high range[9]	V_{DD} falling	—	2.36	2.46	2.56	V	P
			V_{DD} rising	—	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9]	V_{DD} falling	—	2.11	2.16	2.22	V	P
			V_{DD} rising	—	2.16	2.23	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]		—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]		—	1.15	1.17	1.18	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to V_{DD} or V_{SS} and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

8 Maximum is highest voltage that POR is guaranteed.

9 Run at 1 MHz bus frequency

10 Low voltage detection and warning limits measured at 1 MHz bus frequency.

11 Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter		Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current	FEI mode; all modules ON[2]							
				24 MHz	3	20	24	mA	–40 to 25	P
				24 MHz	3	20	24	mA	105	P
				20 MHz	3	18	—	mA	–40 to 105	T
				8 MHz	3	8	—	mA	–40 to 105	T
				1 MHz	3	1.8	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current	FEI mode; all modules OFF[3]							
				24 MHz	3	12.3	14.1	mA	–40 to 105	C
				20 MHz	3	10.5	—	mA	–40 to 105	T
				8 MHz	3	4.8	—	mA	–40 to 105	T
				1 MHz	3	1.3	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current	LPS=0; all modules OFF[3]							
				16 kHz FBILP	3	153	222	µA	–40 to 105	T
				16 kHz FBELP	3	143	200	µA	–40 to 105	T
4	RI_{DD}	Run supply current	LPS=1, all modules OFF[3]							
				16 kHz FBELP	3	20	26	µA	0 to 70	T
				16 kHz FBELP	3	20	70	µA	–40 to 105	T

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current	FEI mode, all modules OFF[3]						
			24 MHz	3	6.7	—	mA	–40 to 105	C
			20 MHz	3	5.6	—	mA	–40 to 105	T
			8 MHz	3	2.4	—	mA	–40 to 105	T
			1 MHz	3	1	—	mA	–40 to 105	T
6	$LPWI_{DD}$	Low-Power Wait mode supply current							
			16 KHz	3	10	40	µA	–40 to 105	T
7	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.39	0.8	µA	–40 to 25	P
			N/A	3	2.4	4.5	µA	70	C
			N/A	3	7	11	µA	85	C
			N/A	3	16	22	µA	105	P
			N/A	2	0.2	0.45	µA	–40 to 25	C
			N/A	2	2	3.8	µA	70	C
			N/A	2	8	12	µA	85	C
			N/A	2	10	20	µA	105	C

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter		Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
8	$S3I_{DD}$	Stop3 mode supply current[4]	No clocks active							
				N/A	3	0.55	0.9	µA	–40 to 25	P
				N/A	3	5.5	8.9	µA	70	C
				N/A	3	14	18	µA	85	C
				N/A	3	37	42	µA	105	P
				N/A	2	0.35	0.5	µA	–40 to 25	C
				N/A	2	3.8	6.8	µA	70	C
				N/A	2	14	20	µA	85	C
				N/A	2	25	46	µA	105	C

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

3 OFF = System Clock Gating Control registers turn off system clock to the corresponding modules.

4 All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw.
NOTE: I/O pins are configured to output low, input-only pins are configured to pullup enabled. IRO pin connects to ground. TRIAMP*x*, OPAMP*x*, DACO, and VREFO pins are at reset state and unconnected.

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			–40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
3	IREFSTEN[1]	—	—	73	80	92	125	µA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	PRACMP[1]	Not using the bandgap (BGBE = 0)	30	35	40	55	75	µA	T
6	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	190	195	210	220	260	µA	T

Table 11. Typical Stop Mode Adders (Continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			–40	25	70	85	105		
7	DAC[1]	High-Power mode; no load on DACO	369	377	377	390	410	µA	T
		Low-Power mode	50	51	51	52	60	µA	T
8	OPAMP[1]	High-Power mode	453	538	538	540	540	µA	T
		Low-Power mode	56	67	67	68	70	µA	T
9	TRIAMP[1]	High-Power mode	430	432	433	438	478	µA	T
		Low-Power mode	52	52	52	55	60	µA	T

[1] Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	80	µA	D
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	D
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	D
6	Analog input offset voltage	VAIO	—	5	40	mV	D
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	D
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	D
10	Programmable reference generator inputs	V_{In2} (V_{DD25})	1.8	—	2.75	V	D
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	0.75	1	1.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V	P

2.8 12-Bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	µA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	µA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C\text{-}C}LP$	—	—	5	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode (3 V at Room Temperature)	$Ts_{C\text{-}C}HP$	—	1	—	µs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0) (3 V at Room Temperature)	$V_{dacoutl}$	—	—	100	mV	T	

Table 14. DAC 12-Bit Operating Behaviors (Continued)

#	Characteristic	Symbol	Min	Typ	Max	Unit	C	Notes
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}-100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	± 8	LSB	T	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	—	± 1	LSB	T	
12	Offset error	E_O	—	±0.4	± 3	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV
13	Gain error, $V_{REFH} = V_{ext} = V_{DD}$	E_G	—	±0.1	± 0.5	%FSR	T	Calculated by a best fit curve from V_{SS} + 100mV to V_{REFH} –100mV
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	—	dB	T	
15	Temperature drift of offset voltage (DAC set to 0x0800)	T_{co}	—	—	2	mV	T	See Typical Drift figure that follows.
16	Offset aging coefficient	A_c	—	—	8	µV/yr	T	

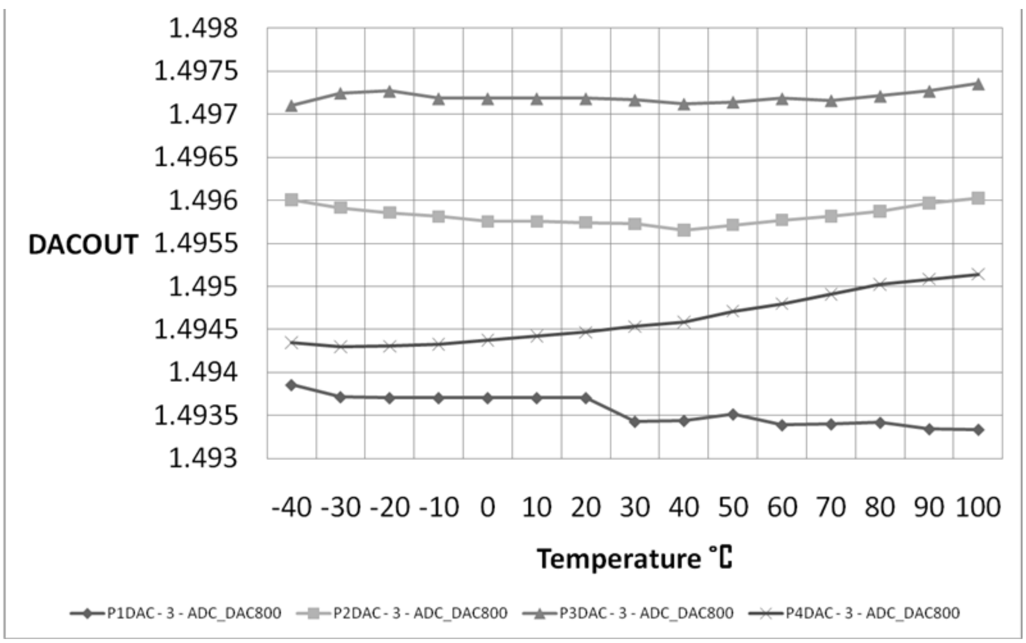


Figure 6. Offset at Half Scale vs Temperature

2.9 ADC Characteristics

Table 15. 16-Bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
1	V_{DDA}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV_{DDA}		Delta to V_{DD} (V_{DD}–V_{DDA})[2]	–100	0	+100	mV	D	
3	ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	–100	0	+100	mV	D	
4	V_{REFH}	Ref Voltage High		1.15	V_{DDA}	V_{DDA}	V	D	
5	V_{REFL}	Ref Voltage Low		V_{SSA}	V_{SSA}	V_{SSA}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance	16-bit modes 8/10/12-bit modes	—	8 4	10 5	pF	T	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	T	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
		16-bit mode	$f_{ADCK} > 8$ MHz	—	—	0.5	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	1	kΩ	T	
			$f_{ADCK} < 4$ MHz	—	—	2	kΩ	T	
		13/12-bit mode	$f_{ADCK} > 8$ MHz	—	—	1	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	2	kΩ	T	
			$f_{ADCK} < 4$ MHz	—	—	5	kΩ	T	
		11/10-bit mode	$f_{ADCK} > 8$ MHz	—	—	2	kΩ	T	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	T	
			$f_{ADCK} < 4$ MHz	—	—	10	kΩ	T	
		9/8-bit mode	$f_{ADCK} > 8$ MHz	—	—	5	kΩ	T	
			$f_{ADCK} < 8$ MHz	—	—	10	kΩ	T	

Table 15. 16-Bit ADC Operating Conditions (Continued)

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
10	f_{ADCK}	ADC Conversion Clock Frequency							
		ADLPC=0, ADHSC=1		1.0	—	8.0	MHz	D	
		ADLPC=0, ADHSC=0		1.0	—	5.0	MHz	D	
		ADLPC=1, ADHSC=0		1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

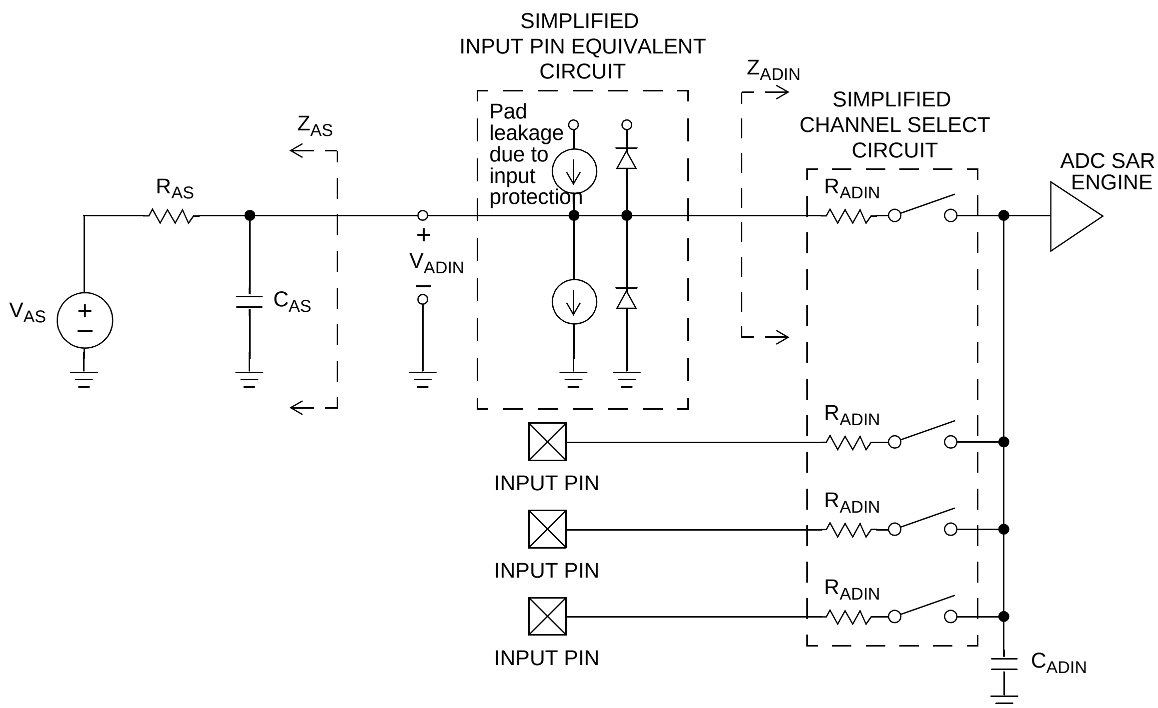


Figure 7. ADC Input Impedance Equivalency Diagram

Table 16. 16-Bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, > 1.8, $V_{REFL} = V_{SSA} \leq$ 8 MHz, –40 to 85 °C)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	µA	T	ADLSMP =0 ADCO=1
		ADLPC=0, ADHSC=0		—	470	—			
		ADLPC=0, ADHSC=1		—	610	—			
2	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	µA	T	
3	ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	C	$t_{ADACK} = 1/f_{ADACK}$
		ADLPC=0, ADHSC=0		—	5.2	—			
		ADLPC=0, ADHSC=1		—	6.2	—			
4	Sample Time	See Reference Manual for sample times							
5	Conversion Time	See Reference Manual for conversion times							
6	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+48/ –40 +56/ –28	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±3.0 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
7	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	+5/–3 +5/–3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 16. 16-Bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDA}, > 1.8, V_{REFL} = V_{SSA} ≤ 8 MHz, –40 to 85 °C) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
8	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±16.0 ±20.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.5 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
9	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+32/ –24 +24/ –16	LSB[2]	T	V_{ADIN} = V_{SSA}
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.5 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
10	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+10/0 +14/0	+42/–2 +46/–2	LSB[2]	T	V_{ADIN} = V_{DDA}
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±3.5 ±3.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
11	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
12	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 12.8 12.7 12.6 12.5 11.9	 14.2 13.8 13.6 13.3 12.5	 — — — — —	Bits	C	F_{in} = F_{sample}/100
13	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		

Table 16. 16-Bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDA}, > 1.8, V_{REFL} = V_{SSA} ≤ 8 MHz, –40 to 85 °C) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
14	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–91.5	–74.3	dB	C	F_{in} = F_{sample}/100
		16-bit single-ended mode Avg=32		—	–85.5	—		D	
15	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	75.0	92.2	—	dB	C	F_{in} = F_{sample}/100
		16-bit single-ended mode Avg=32		—	86.2	—		D	
16	Input Leakage Error	all modes	E_{IL}	I_{In} * R_{AS}			mV	D	I_{In} = leakage current (refer to DC characteristics)
17	Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
		25°C – 125°C		—	1.769	—			
18	Temp Sensor Voltage	25°C	V_{TEMP25}	—	718.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} – V_{REFL})/2^N$

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq$ 4 MHz, ADHSC = 1)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
1	Total Unadjusted Error	16-bit differential mode 16-bit single-ended mode	TUE	— —	±16 ±20	+24/ –24 +32/–20	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
		13-bit differential mode 12-bit single-ended mode		— —	±1.5 ±1.75	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.0 ±1.25		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
2	Differential Non-Linearity	16-bit differential mode 16-bit single-ended mode	DNL	— —	±2.5 ±2.5	±3 ±3	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±1 ±1		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
3	Integral Non-Linearity	16-bit differential mode 16-bit single-ended mode	INL	— —	±6.0 ±10.0	±12.0 ±16.0	LSB[2]	T	
		13-bit differential mode 12-bit single-ended mode		— —	±1.0 ±1.0	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	
4	Zero-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{ZS}	— —	±4.0 ±4.0	+16/0 +16/-8	LSB[2]	T	$V_{ADIN} = V_{SSA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.0		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	

Table 17. 16-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDA}$, ≥ 2.7 V, $V_{REFL} = V_{SSA}$, $f_{ADACK} \leq 4$ MHz, ADHSC = 1) (Continued)

#	Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
5	Full-Scale Error	16-bit differential mode 16-bit single-ended mode	E_{FS}	— —	+8/0 +12/0	+24/0 +24/0	LSB[2]	T	$V_{ADIN} = V_{DDA}$
		13-bit differential mode 12-bit single-ended mode		— —	±0.7 ±0.7	±2.0 ±2.5		T	
		11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
		9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
6	Quantization Error	16-bit modes	E_Q	—	–1 to 0	—	LSB[2]	D	
		≤13-bit modes		—	—	±0.5			
7	Effective Number of Bits	16-bit differential mode Avg=32 Avg=16 Avg=8 Avg=4 Avg=1	ENOB	 14.3 13.8 13.4 13.1 12.4	 14.5 14.0 13.7 13.4 12.6	 — — — — —	Bits	C	$F_{in} = F_{sample}/100$
8	Signal to Noise plus Distortion	See ENOB	SINAD	$SINAD = 6.02 \cdot ENOB + 1.76$			dB		
9	Total Harmonic Distortion	16-bit differential mode Avg=32	THD	—	–95.8	–90.4	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
10	Spurious Free Dynamic Range	16-bit differential mode Avg=32	SFDR	91.0	96.5	—	dB	C	$F_{in} = F_{sample}/100$
		16-bit single-ended mode Avg=32		—	—	—		D	
11	Input Leakage Error	all modes	E_{IL}	$I_{In} * R_{AS}$			mV	D	I_{In} = leakage current (refer to DC characteristics)

1 All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}$

2 Typical values assume V_{DDA} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = $(V_{REFH} – V_{REFL})/2^N$

2.10 MCG and External Oscillator (XOSC) Characteristics

Table 18. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0 V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625		C
3	DCO output frequency range — trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40		C
		High range[1] (DRS=10)		40	—	60		C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4		C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	±1.0	± 2	$\%f_{dco}$	P
		over fixed voltage and temp range of 0 – 70 °C		—	± 0.5	± 1		C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1		D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625ns [5]	Long term	$f_{pll\_jitter\_625ns}$	—	0.566[4]	—	$\%f_{pll}$	D
11	Lock frequency tolerance	Entry[6]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[7]	D_{unl}	± 4.47	—	± 5.97		D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})		D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

1 This should not exceed the maximum CPU frequency for this device which is 48 MHz.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[3] This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

[4] Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

[5] 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

[6] Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

[7] Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz	D
		• High range (RANGE = 1), • FEE or FBE mode [2]	$f_{hi\text{-}fll}$	1	—	5	MHz	D
		• High range (RANGE = 1), • PEE or PBE mode [3]	$f_{hi\text{-}pll}$	1	—	16	MHz	D
		• High range (RANGE = 1), • High gain (HGO = 1), • BLPE mode	$f_{hi\text{-}hgo}$	1	—	16	MHz	D
		• High range (RANGE = 1), • Low power (HGO = 0), • BLPE mode	$f_{hi\text{-}lp}$	1	—	8	MHz	D
2	Load capacitors		C_1 C_2	See crystal or resonator manufacturer's recommendation.				D
3	Feedback resistor	• Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ	D
		• High range (1 MHz to 16 MHz)	—	—	1	—	MΩ	D
4	Series resistor — Low range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)		—	100	—		D
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ	D
		• High Gain (HGO = 1)						D
		≥ 8 MHz		—	0	0		D
		4 MHz		—	0	10		D
		1 MHz		—	0	20		D

Table 19. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit	C
6	Crystal start-up time [4]	• Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	ms	D
		• Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—		D
		• High range, low gain (RANGE = 1, HGO = 0)[5]	$t_{CSTH-LP}$	—	5	—		D
		• High range, high gain (RANGE = 1, HGO = 1)[5]	$t_{CSTH-HGO}$	—	15	—		D

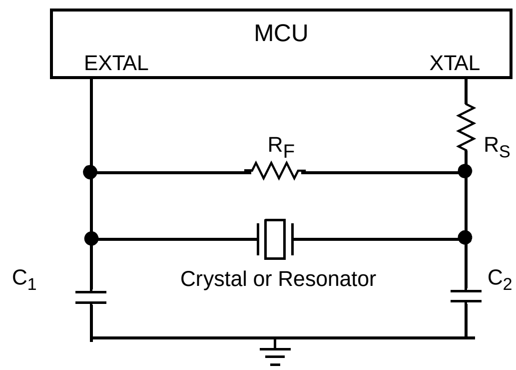
1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout porcedures must be followed to achieve specifications.

5 4 MHz crystal.



2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 20. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		700	1000	1300	P	μs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

Table 20. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive						ns
			Slew rate control disabled (PTxSE = 0)	—	11	—	D	
			Slew rate control enabled (PTxSE = 1)	—	35	—	D	
			Slew rate control disabled (PTxSE = 0)	—	40	—	D	
			Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

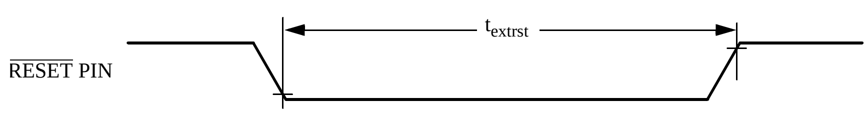


Figure 8. Reset Timing

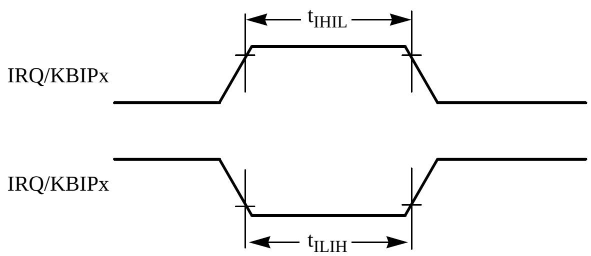


Figure 9. IRQ/KBIPx Timing

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

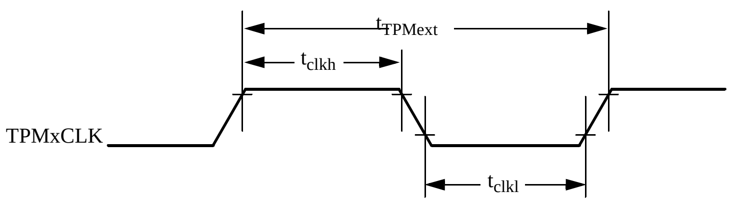


Figure 10. Timer External Clock

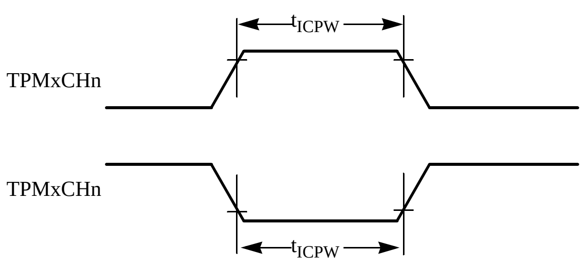


Figure 11. Timer Input Capture Pulse

2.12 SPI Characteristics

Table 22 and Figure 12 through Figure 15 describe the timing requirements for the SPI system.

Table 22. SPI Timing

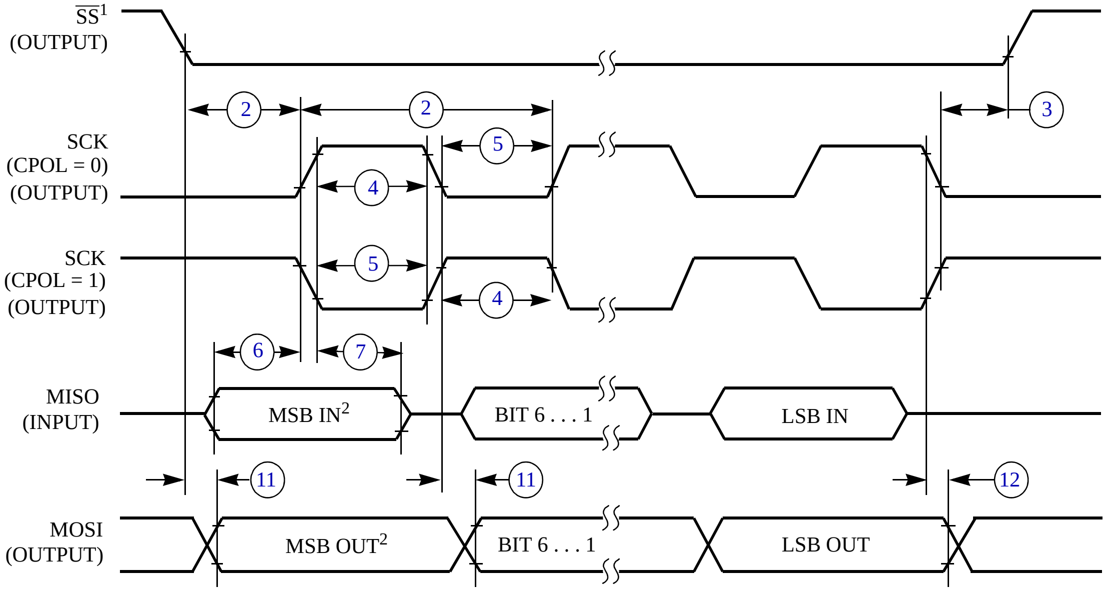
No.[1]	Characteristic[2]	Symbol	Min	Max	Unit	C
1	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz Hz	D
2	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns	D
6	Data setup time (inputs) Master Slave	t_{SU} t_{SU}	15 15	— —	ns ns	D
7	Data hold time (inputs) Master Slave	t_{HI} t_{HI}	0 25	— —	ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns	D
11	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns	D
12	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns	D
13	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns	D

[1] Numbers in this column identify elements in Figure 12 through Figure 15.

[2] All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

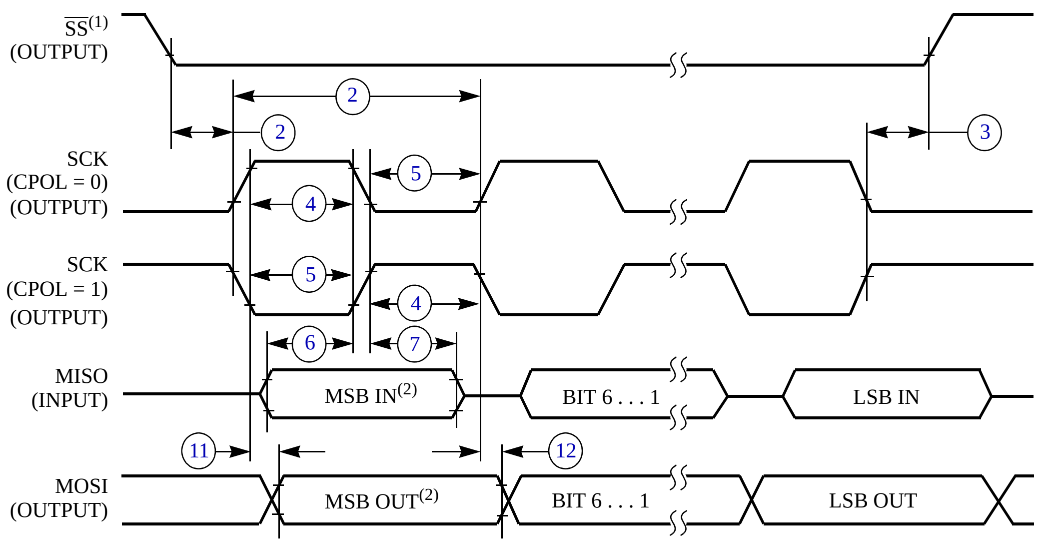
[3] Time to data active from high-impedance state.

[4] Hold time to high-impedance state.



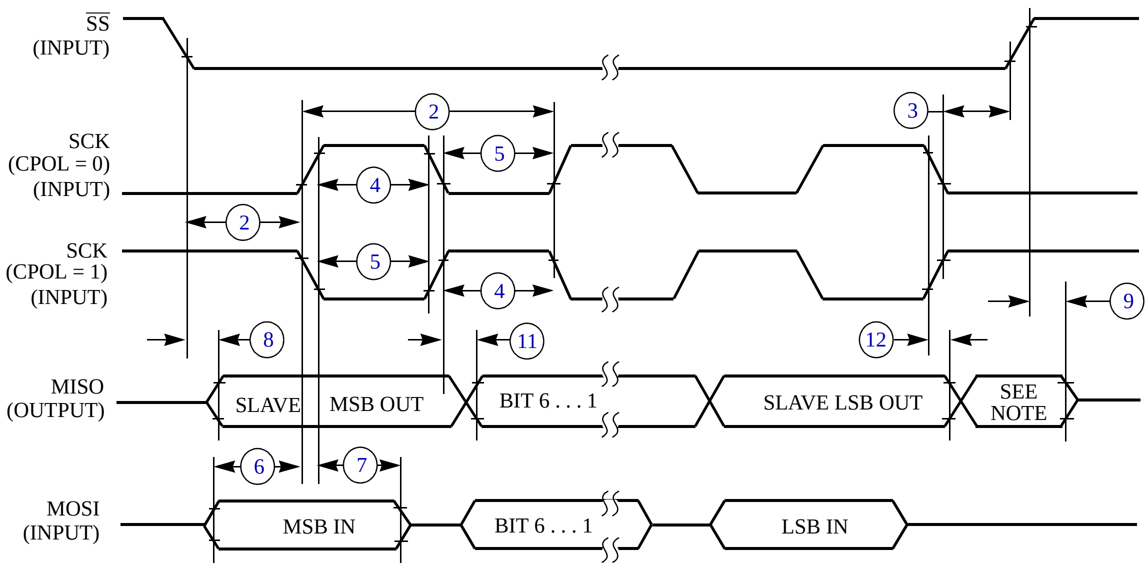
NOTES:
1. SS output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

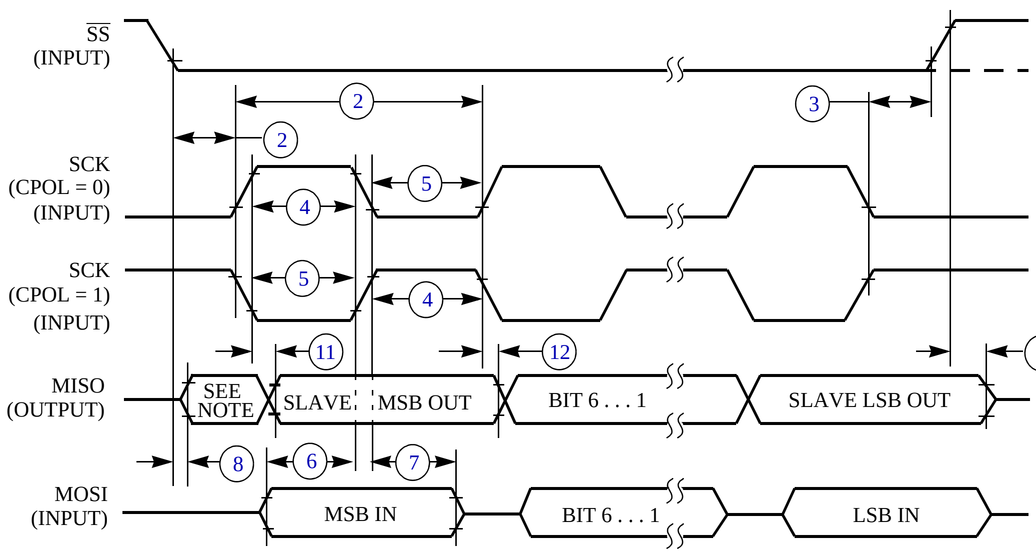
Figure 13. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 14. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 15. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MC9S08MM128RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase –40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs	D
5	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}	P
7	Page erase time[2]	t_{Page}		4000		t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

2.15 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V at 25°C.	Vout	1.140	1.160	V	P
6	Temperature Drift (Vmin – Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	µV/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation V_{DD} < 2.3 V, Delta V_{DDA} = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection)	DC	70	—	dB	C

[1] See typical chart that follows (Figure 16).

[2] Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging µV/year. V_{refo} data recorded per month.

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim (Temperature range from 0° C to 50° C)	V_{out}	1.149	1.152	mV	T	
2	Temperature Drift (V_{min} – V_{max} Temperature range from 0° C to 50° C)	T_{drift}	—	3	mV[1]	T	

[1] See typical chart that follows (Figure 16).

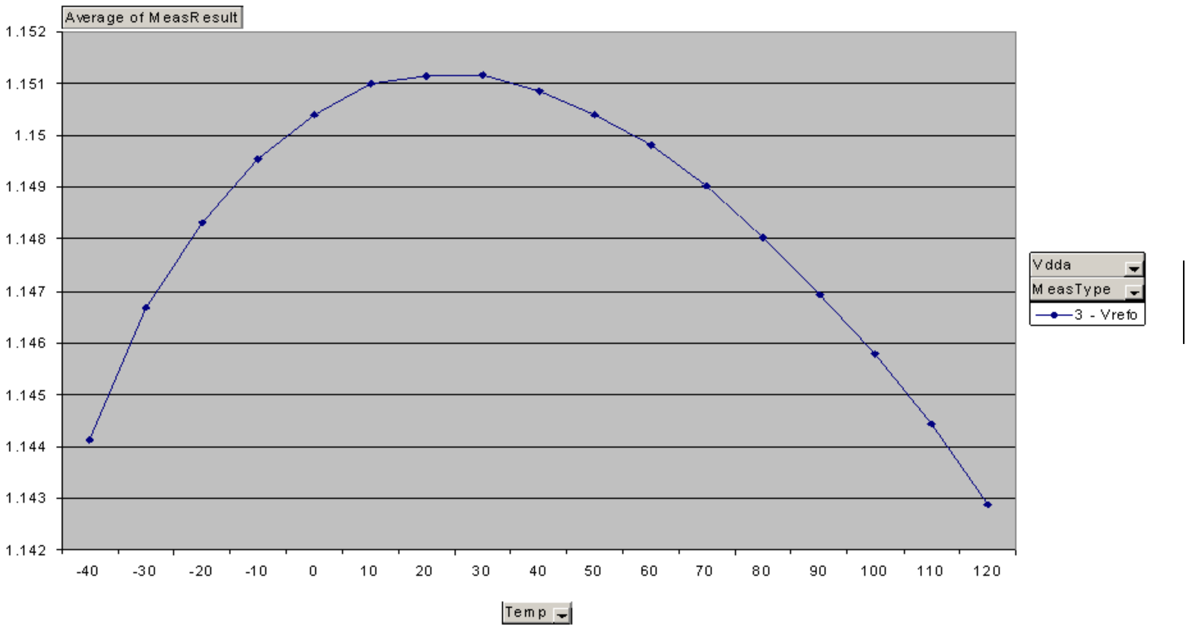


Figure 16. Typical VREF Output vs. Temperature

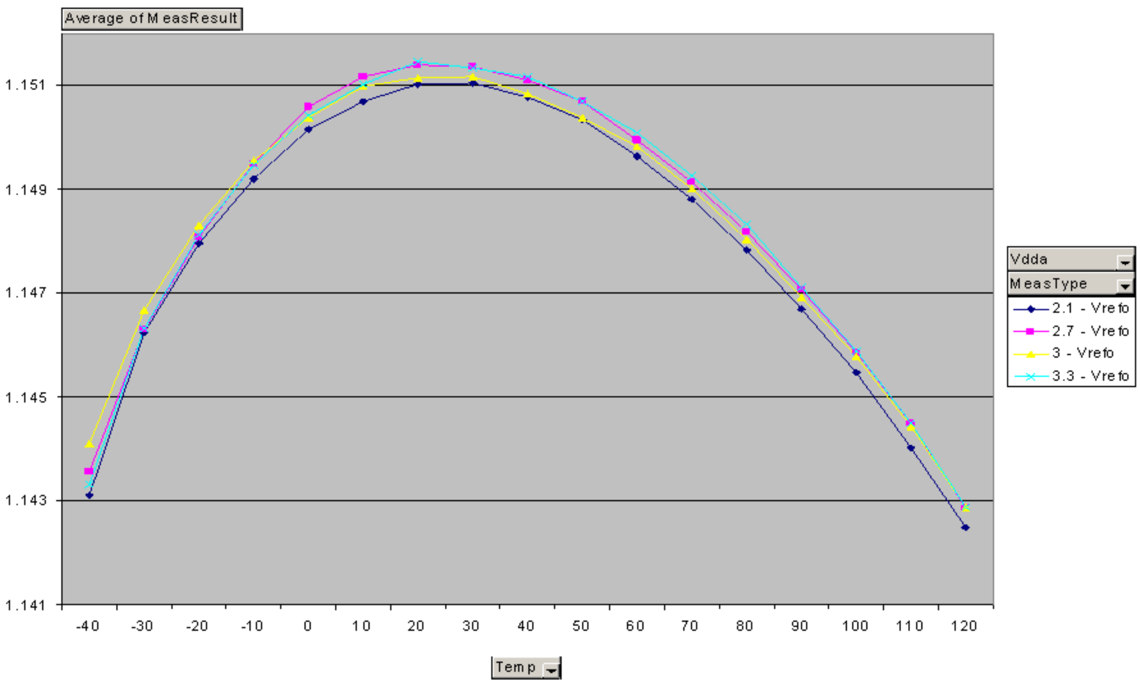


Figure 17. Typical VREF Output vs. V_{DD}

2.16 TRIAMP Electrical Parameters

Table 27. TRIAMP Characteristics 1.8–3.6 V, –40°C~105°C

#	Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0) Low-power mode	I_{SUPPLY}	—	52	60	µA	T
3	Supply Current (I_{OUT}=0mA, CL=0) High-speed mode	I_{SUPPLY}	—	432	480	µA	T
4	Input Offset Voltage	V_{OS}	—	± 1	± 5	mV	T
5	Input Offset Voltage Temperature Drift	α_{VOS}	—	600	—	µV	T
6	Input Offset Current	I_{OS}	—	±120	500	pA	T
7	Input Bias Current (0 ~ 50°C)	I_{BIAS}	—	< 350	< ±500	pA	T
8	Input Bias Current (–40 ~ 105°C)	I_{BIAS}	—	3	6.55	nA	T
9	Input Common Mode Voltage Low	V_{CML}	0	—	—	V	T
10	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}–1.4	V	T
11	Input Resistance	R_{IN}	500	—	—	MΩ	T
12	Input Capacitances	C_{IN}	—	—	5	pF	D
13	AC Input Impedance (f_{IN}=100kHz)	$\|X_{IN}\|$	—	1	—	MΩ	D
14	Input Common Mode Rejection Ratio	CMRR	60	70	—	dB	T
15	Power Supply Rejection Ration	PSRR	60	70	—	dB	T
16	Slew Rate (ΔV_{IN}=100mV) Low-power mode	SR	—	0.1	—	V/µs	T
17	Slew Rate (ΔV_{IN}=100mV) High-speed mode	SR	—	1	—	V/µs	T
18	Unity Gain Bandwidth (Low-power mode) 50pF	GBW	0.15	0.25	—	MHz	T
19	Unity Gain Bandwidth (High-speed mode) 50pF	GBW	—	1.6	—	MHz	T
20	DC Open Loop Voltage Gain	A_V	—	80	—	dB	T
21	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
22	Output Impedance AC Open Loop (@100 kHz Low-power mode)	R_{OUT}	—	1.4	—	kΩ	D
23	Output Impedance AC Open Loop (@100 kHz High-speed mode)	R_{OUT}	—	184	—	Ω	D
24	Output Voltage Range	triout	0.15	—	V_{DD} – 0.15	V	T
25	Output Drive Capability	I_{OUT}	—	± 1.0	—	mA	T
26	Gain Margin	GM	20	—	—	dB	D
27	Phase Margin	PM	45	55	—	deg	T
28	Input Voltage Noise Density	f= 1 kHz	—	160	—	nV/√Hz	T

[1] All parameters are measured at 3.0 V, CL= 47 pF across temperature –40 to + 105 °C unless specified.

[2] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2.17 OPAMP Electrical Parameters

Table 28. OPAMP Characteristics 1.8–3.6 V

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
1	Operating Voltage	V_{DD}	1.8	—	3.6	V	C
2	Supply Current (I_{OUT}=0mA, CL=0 Low-Power mode)	I_{SUPPLY}	—	67	80	µA	T
3	Supply Current (I_{OUT}=0mA, CL=0 High-Speed mode)	I_{SUPPLY}	—	538	550	µA	T
4	Input Offset Voltage	V_{OS}	—	±2	±6	mV	T
5	Input Offset Voltage Temperature Coefficient	α_{VOS}	—	10	—	µV/C	T
6	Input Offset Current (–40°C to 105°C)	I_{OS}	—	±2.5	±250	nA	T
7	Input Offset Current (–40°C to 50°C)	I_{OS}	—	—	45	nA	T
8	Positive Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	0.8	3.5	nA	T
9	Positive Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	±2	nA	T
10	Negative Input Bias Current (–40°C to 105°C)	I_{BIAS}	—	2.5	250	nA	T
11	Negative Input Bias Current (–40°C to 50°C)	I_{BIAS}	—	—	45	nA	T
12	Input Common Mode Voltage Low	V_{CML}	0.1	—	—	V	T
13	Input Common Mode Voltage High	V_{CMH}	—	—	V_{DD}	V	T
14	Input Resistance	R_{IN}	—	500	—	MΩ	T
15	Input Capacitances	C_{IN}	—	—	10	pF	D
16	AC Input Impedance (f_{IN}=100kHz Negative Channel)	$\lvert X_{IN} \rvert$	—	52	—	kΩ	D
17	AC Input Impedance (f_{IN}=100kHz Positive Channel)	$\lvert X_{IN} \rvert$	—	132	—	kΩ	D
18	Input Common Mode Rejection Ratio	CMRR	55	65	—	dB	T
19	Power Supply Rejection Ratio	PSRR	60	65	—	dB	T
20	Slew Rate (ΔV_{IN}=100mV Low-Power mode)	SR	0.1	—	—	V/µs	T
21	Slew Rate (ΔV_{IN}=100mV High-Speed mode)	SR	1	—	—	V/µs	T
22	Unity Gain Bandwidth (Low-Power mode)	GBW	0.2	—	—	MHz	T
23	Unity Gain Bandwidth (High-Speed mode)	GBW	1	—	—	MHz	T
24	DC Open Loop Voltage Gain	A_V	80	90	—	dB	T
25	Load Capacitance Driving Capability	CL(max)	—	—	100	pF	T
26	Output Impedance AC Open Loop (@100 kHz Low-Power mode)	R_{OUT}	—	4k	—	Ω	D
27	Output Impedance AC Open Loop (@100 kHz High-Speed mode)	R_{OUT}	—	220	—	Ω	D
28	Output Voltage Range	V_{OUT}	0.15	—	V_{DD}–0.1 5	V	T
29	Output Drive Capability	I_{OUT}	±0.5	±1.0	—	mA	T
30	Gain Margin	GM	20	—	—	dB	D
31	Phase Margin	PM	45	55	—	deg	T

Table 28. OPAMP Characteristics 1.8–3.6 V (Continued)

#	Characteristics[1]	Symbol	Min	Typ[2]	Max	Unit	C
32	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	4	—	uS	T
33	GPAMP startup time (Low-Power mode) (Tolerance < 1%, Vin = 0.5 Vp–p, CL = 25 pF, RL = 100k)	$T_{startup}$	—	1	—	uS	T
34	Input Voltage Noise Density	f=1 kHz	—	250	—	nV/√Hz	T

1 All parameters are measured at 3.3 V, CL =4 7 pF across temperature –40 to + 105°C unless specified.
2 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

3 Ordering Information

This appendix contains ordering information for the device numbering system. MC9S08MM128 and MC9S08MM64 devices.

3.1 Device Numbering System

Example of the device numbering system:

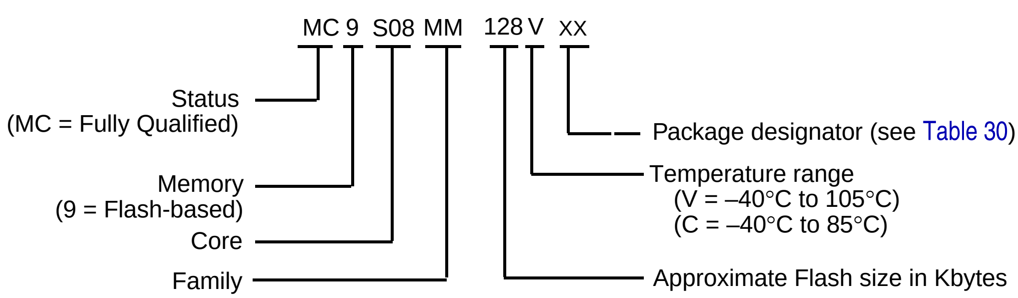


Table 29. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08MM128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08MM64	65,536	12,288	64 LQFP
MC9S08MM32	32768	4096	64 LQFP
MC9S08MM32A	32768	2048	64 LQFP

1 See Table 2 for a complete description of modules included on each device.
2 See Table 30 for package information.

3.2 Package Information

Table 30. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F-02	98ASS23234W
80	Low Quad Flat Package	LQFP	LK	917-01	98ASS23174W
81	MAPBGA Package	Map PBGA	MB	1662-01	98ASA10670D

3.3 Mechanical Drawings

Table 30 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08MM128 series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 30, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 30) in the “Enter Keyword” search box at the top of the page.

4 Revision History

Table 31. Revision History

Rev	Date	Description of Changes
0	06/2009	Initial release of the Data Sheet.
1	07/2009	Updated MCG and XOSC Average internal reference frequency.
2	01/2010	Revised to include MC9S08MM32 and MC9S08MM32A devices.Updated electrical characteristic data.
3	10/2010	Updated with the latest characteristic data. Added several figures. Added the ADCTypical Operation table.