

Thyristor Module

$$V_{RRM} = 2 \times 1600 \text{ V}$$

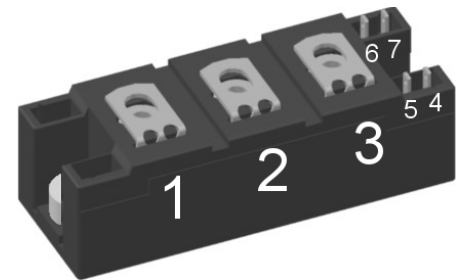
$$I_{TAV} = 181 \text{ A}$$

$$V_T = 1.03 \text{ V}$$

Phase leg

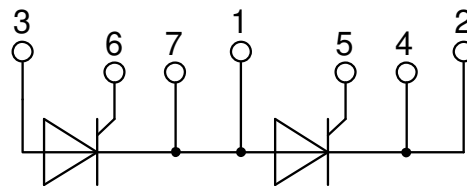
Part number

MCC162-16io1B



Backside: isolated

 E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al₂O₃-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: Y4

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

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Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			1600	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1600 V$	$T_{VJ} = 25^{\circ}C$		300	μA
		$V_{R/D} = 1600 V$	$T_{VJ} = 125^{\circ}C$		10	mA
V_T	forward voltage drop	$I_T = 150 A$	$T_{VJ} = 25^{\circ}C$		1.09	V
		$I_T = 300 A$			1.25	V
		$I_T = 150 A$	$T_{VJ} = 125^{\circ}C$		1.03	V
		$I_T = 300 A$			1.25	V
I_{TAV}	average forward current	$T_C = 85^{\circ}C$	$T_{VJ} = 125^{\circ}C$		181	A
$I_{T(RMS)}$	RMS forward current	180° sine			300	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 125^{\circ}C$		0.88	V
r_T	slope resistance				1.15	m Ω
R_{thJC}	thermal resistance junction to case				0.155	K/W
R_{thCH}	thermal resistance case to heatsink			0.07		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		645	W
I_{TSM}	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		6.00	kA
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		6.48	kA
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}C$		5.10	kA
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		5.51	kA
I^2t	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}C$		180.0	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		174.7	kA ² s
		$t = 10 \text{ ms}; (50 \text{ Hz}), \text{ sine}$	$T_{VJ} = 125^{\circ}C$		130.1	kA ² s
		$t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{ sine}$	$V_R = 0 V$		126.3	kA ² s
C_J	junction capacitance	$V_R = 400 V \quad f = 1 \text{ MHz}$	$T_{VJ} = 25^{\circ}C$		273	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 125^{\circ}C$		120	W
		$t_p = 500 \mu s$			60	W
P_{GAV}	average gate power dissipation				8	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^{\circ}C; f = 50 \text{ Hz}$	repetitive, $I_T = 540 A$		150	A/ μs
		$t_p = 200 \mu s; di_G/dt = 0.5 A/\mu s;$	non-repet., $I_T = 180 A$		500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		1000	V/ μs
		$R_{GK} = \infty; \text{method 1 (linear voltage rise)}$				
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		2.5	V
			$T_{VJ} = -40^{\circ}C$		2.6	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		150	mA
			$T_{VJ} = -40^{\circ}C$		200	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^{\circ}C$		0.2	V
I_{GD}	gate non-trigger current				10	mA
I_L	latching current	$t_p = 30 \mu s$	$T_{VJ} = 25^{\circ}C$		300	mA
		$I_G = 0.5 A; di_G/dt = 0.5 A/\mu s$				
I_H	holding current	$V_D = 6 V \quad R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		200	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0.5 A; di_G/dt = 0.5 A/\mu s$				
t_q	turn-off time	$V_R = 100 V; I_T = 300 A; V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 100^{\circ}C$		150	μs
		$di/dt = 10 A/\mu s \quad dv/dt = 20 V/\mu s \quad t_p = 200 \mu s$				



Package Y4				Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit	
I_{RMS}	RMS current	per terminal			300	A	
T_{VJ}	virtual junction temperature		-40		125	°C	
T_{op}	operation temperature		-40		100	°C	
T_{stg}	storage temperature		-40		125	°C	
Weight					150	g	
M_D	mounting torque		2.25		2.75	Nm	
M_T	terminal torque		4.5		5.5	Nm	
$d_{Spp/App}$	creepage distance on surface striking distance through air	terminal to terminal	14.0	10.0		mm	
$d_{Spb/Apb}$		terminal to backside	16.0	16.0		mm	
V_{ISOL}	isolation voltage	t = 1 second			3600	V	
		t = 1 minute	50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA		3000	V	



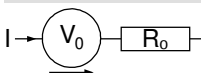
Data Matrix: part no. (1-19), DC + PI (20-25), lot.no.# (26-31), blank (32), serial no.# (33-36)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCC162-16io1B	MCC162-16io1B	Box	6	507588

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 125$ °C



Thyristor

$V_{0 \max}$	threshold voltage	0.88	V
$R_{0 \max}$	slope resistance *	0.8	mΩ



Outlines Y4



Dim.	MIN [mm]	MAX [mm]	MIN [inch]	MAX [inch]
a	30.0	30.6	1.181	1.205
b	typ. 0.25		typ. 0.010	
c	64.0	65.0	2.520	2.559
d	typ. 6.4		typ. 0.250	
e	4.9	5.1	0.193	0.201
f	28.6	29.2	1.126	1.150
g	7.3	7.7	0.287	0.303
h	93.5	94.5	3.681	3.720
i	79.5	80.5	3.130	3.169
j	4.8	5.2	0.189	0.205
k	33.4	34.0	1.315	1.339
l	16.7	17.3	0.657	0.681
m	22.7	23.3	0.894	0.917
n	22.7	23.3	0.894	0.917
o	14.0	15.0	0.551	0.591
p	typ. 10.5		typ. 0.413	
q	22.8	23.3	0.898	0.917
r	1.8	2.4	0.071	0.041

Optional accessories for modules

Keyed gate/cathode twin plugs with wire length = 350 mm, gate = white, cathode = red

Type ZY 180L (L = Left for pin pair 4/5)

Type ZY 180R (R = Right for pin pair 6/7) } UL 758, style 3751



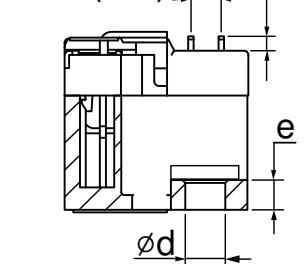
A (3:1)



C-C (1:1)



B-B (1:1)



Thyristor



Fig. 1 Surge overload current I_{TSM} , I_{FSM} : Crest value, t: duration



Fig. 2 I^2t versus time (1-10 ms)

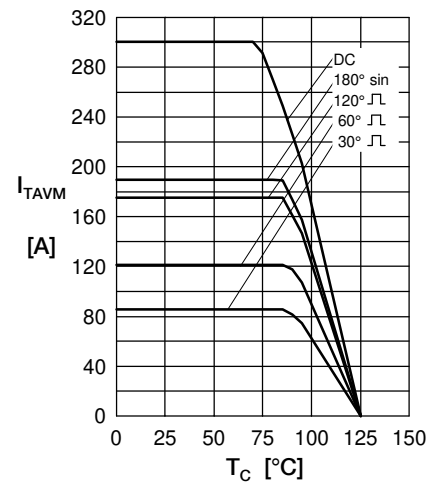


Fig. 3 Max. forward current at case temperature



Fig. 4 Power dissipation vs. on-state current & ambient temperature (per thyristor or diode)



Fig. 5 Gate trigger characteristics



Fig. 6 Three phase rectifier bridge: Power dissipation versus direct output current and ambient temperature



Fig. 7 Gate trigger delay time