MCDP6150
DisplayPort 1.4a
Link Training Tunable PHY Retimer

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- DisplayPort 1.4a Link Training Tunable PHY Retimer (LTTPR) to support
  - 4/2/1-Lane DP1.4a (RBR/HBR/HBR2/HBR3)
- Power Supply Voltages
  - 1.8 V for I/O, 1.2 V for Core
- DP1.4a Compliant Retimer
  - Data rate 1.62 Gbps / 2.7 Gbps / 5.4 Gbps / 8.1 Gbps
  - Transparent mode with proprietary link training architecture
  - Non-transparent mode support as specified in DP1.4a standard
  - AUX_CH transaction snooping
  - DP1.4a Compliant Retimer DPCD registers
  - 8b/10b coding
  - Pattern generator and Error Checker
  - Down-spreading of link clock
  - Error detection
  - Adjustable TXEQ during the link training through AUX_CH
  - Adaptive equalizer with CTLE and DFE
  - DFE + CTLE for HBR3 to compensate -27dB insertion loss @4.05GHz
  - CTLE for HBR2 / HBR / RBR
  - Support of custom PHY configuration through TWI
- Real time Eye Opening Monitor (EOM)
- TWI (Two Wire Interface) slave to configure the integrated lane mapping and operation mode
  - Compatible with I2C master
  - Support up to 4 unique TWI device ID
- Low Power Operation
  - 460 mW for 4-lane HBR3 in typical condition
  - < 10mW in D3 mode
  - < 1mW in low power mode
- ESD Specification
  - 2kV HBM, ±500V CDM
- Package
  - 46 Ex-VQFN (6.5 mm x 4.5 mm)

Applications

- Desktop PC / Notebook / Tablet
- Active cable
- Virtual Reality / Augmented Reality head mount display
- DP1.4a monitor (8K monitor / Gaming monitor)
- Video card / converter
- Video router / switch
- 4K / 8K UHD camera
- Video conferencing
- Digital signage
- Interactive display

Figure 1. MCDP6150 System Block Diagram in DPTX device

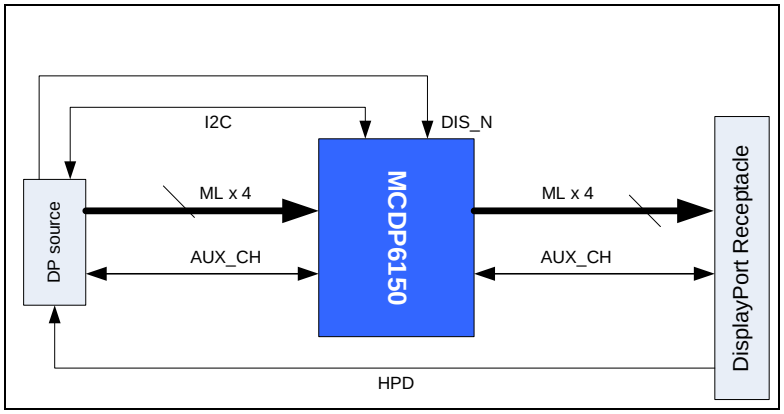


Figure 2. MCDP6150 System Block Diagram in DPRX device

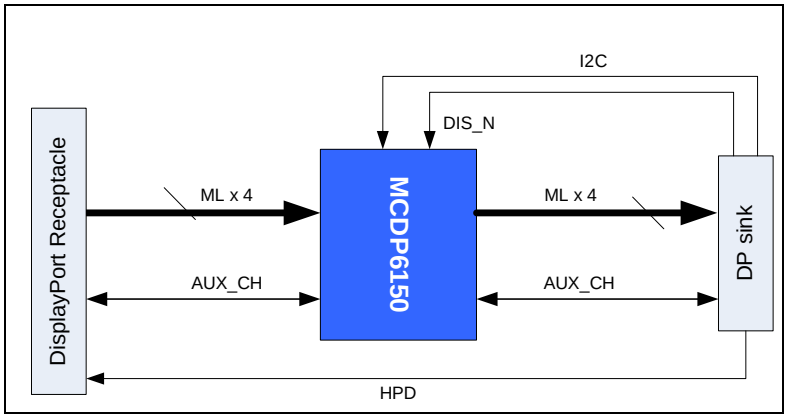
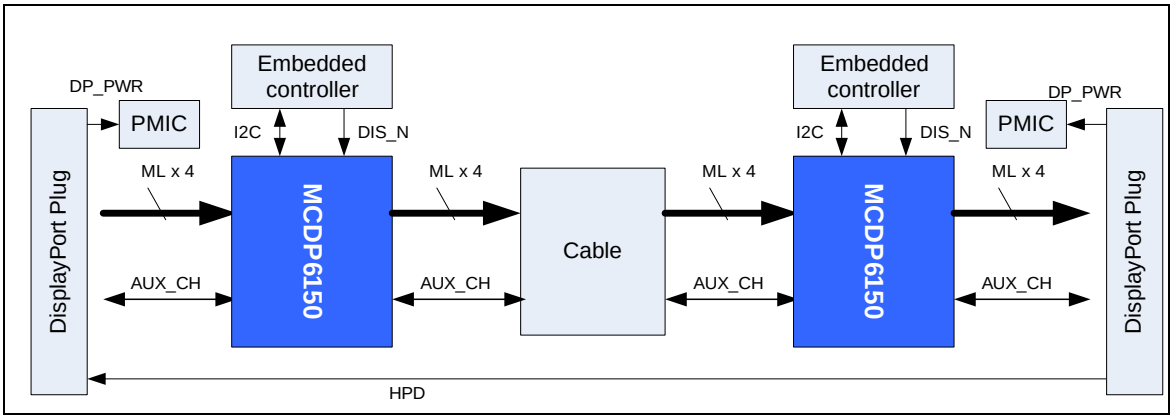


Figure 3. MCDP6150 System Block Diagram in DP active cable



1. Description

The MCDP6150 is a low power DisplayPort1.4a retimer targeted for high-end audio video applications. The MCDP6150 supports 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps data rates. The following use cases are supported.

Table 1. DP1.4a Repeater Mode

	Mode	AUX_CH Function
LT tunable PHY Repeater	Non-transparent mode	Sample, Manipulate, and Forward to snoop or respond as defined in DP1.4a standard.
	Transparent mode	Sample and Forward to snoop

The DP1.4a repeater implements AUX_CH snooping function of DPCD addresses defined in the standard as well as the LT-tunable PHY Repeater DPCD registers. The DP1.4a repeater can support up to a 0.5% down-spread link rate. The transmitter employs TXEQ, which adjusts its pre-emphasis level according to either the AUX_CH transaction during the link training or the Two Wire Interface (TWI). The receiver employs a fully adaptive Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE). The transmitter parameters to support the amplitude level and the pre-emphasis level defined in DP 1.4a standard are provided in default. The transmitter configuration can be also customized to extend the media length such as PCB trace and the cable.

The MCDP6150 operates at two power supplies; 1.8 V and 1.2 V.

The power consumption with the two supply voltages is:

1. 460 mW with an active 4 lane retimer (DP 4 lanes HBR3) in typical condition
2. < 10mW in D3 power mode

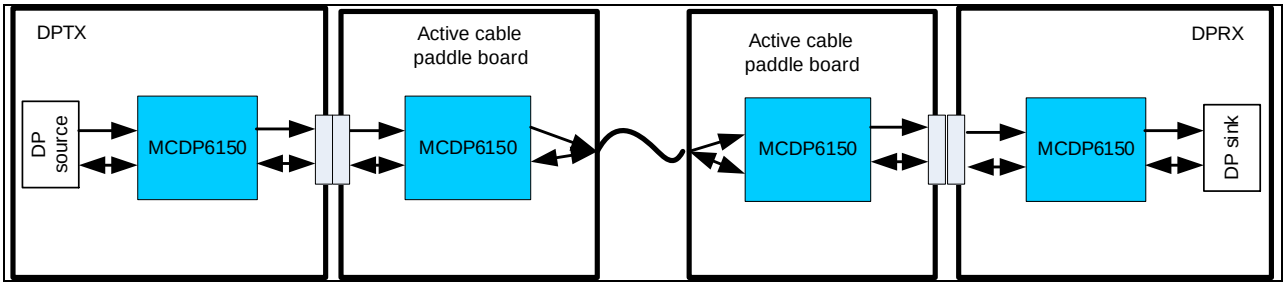
The MCDP6150 is offered in a 46-pin, 6.5 mm x 4.5 mm Ex-VQFN package.

2. Application Overview

The target applications of MCDP6150 are high-end DPTX systems, DPRX systems and a DisplayPort 1.4a active cable.

The MCDP6150 resides next to the DisplayPort™ source (CPU/GPU) device (DPTX device) or the DisplayPort sink (scaler, SoC) device (DPRX device). In addition, the MCDP6150 is implemented in the DisplayPort active cable paddle board. High speed serial interface tracks are typical microstrip lines with controlled impedance of 100 ohm. The MCDP6150 communicates with DPTX and/or DPRX devices through either TWI or AUX_CH. When the DisplayPort link is discovered by the DPTX via HPD signal, the link training is initiated by the DPTX device through the AUX_CH.

Figure 4. MCDP6150 Use Case



3. Functional Description

This section describes the following operations of the MCDP6150:

1. System block diagram
2. MCDP6150 block diagram
3. Receiver PHY
4. Transmitter PHY
5. Upstream Facing Port (UFP) interface
6. Downstream Facing Port (DFP) interface
7. AUX_CH interface
8. IC operation
9. Power consumption
10. Power supply
11. System interface

3.1. System Block Diagram

Figure 5. MCDP6150 DPTX System Block Diagram

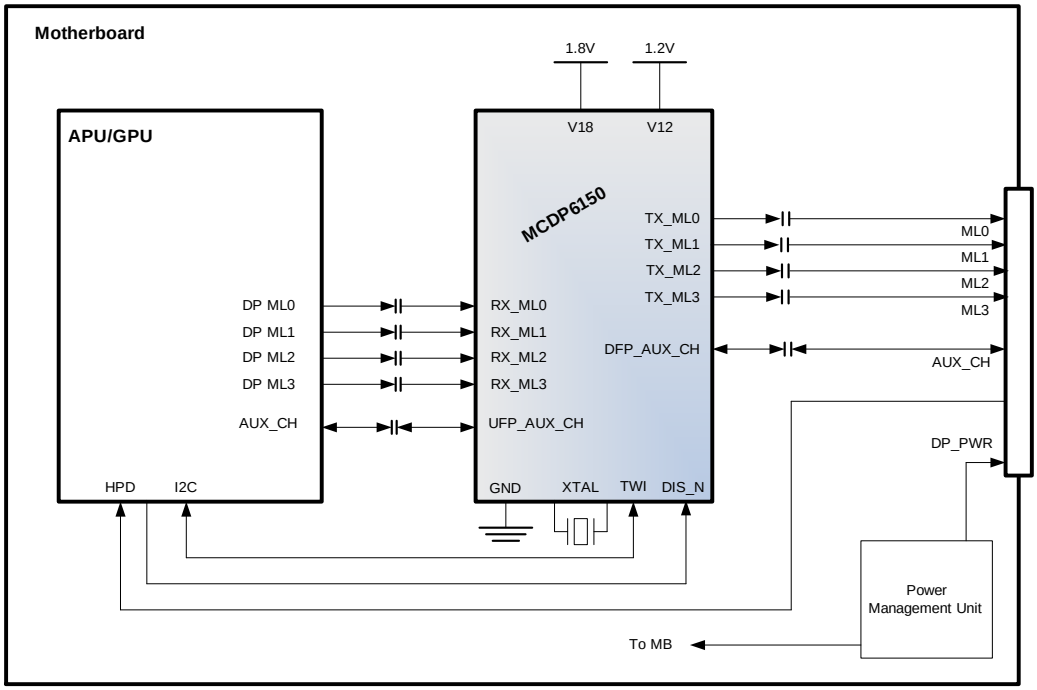
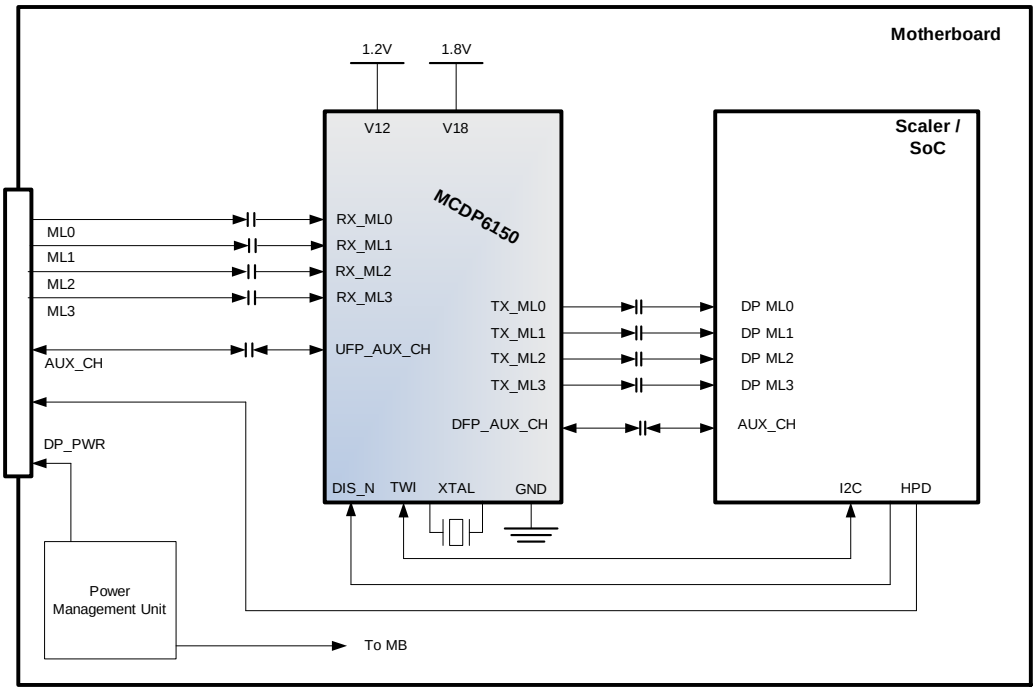
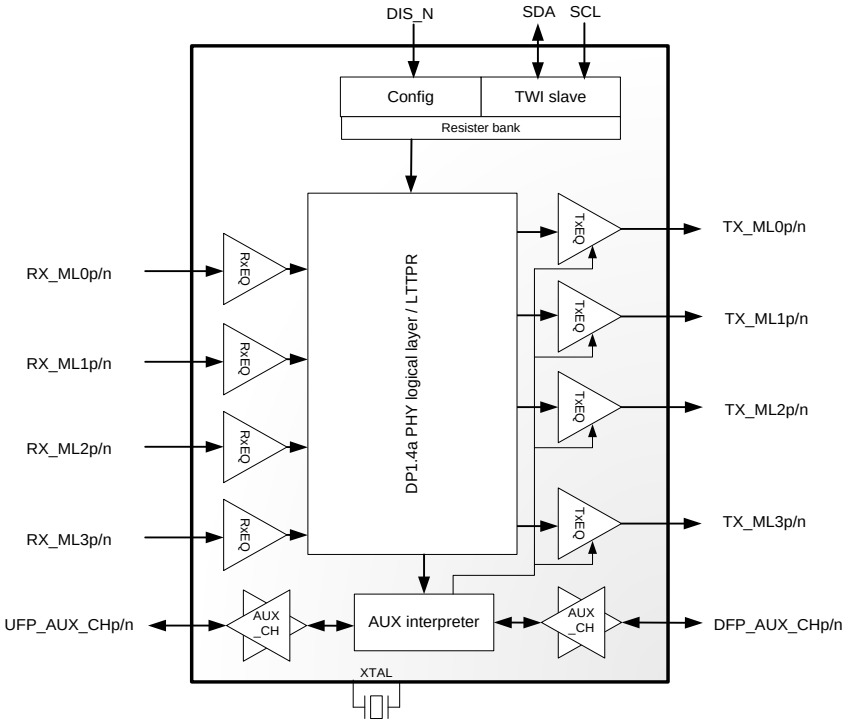


Figure 6. MCDP6150 DPRX System Block Diagram



3.2. MCDP6150 Block Diagram

Figure 7. MCDP6150 Block Diagram



The figure above shows a block diagram of the MCDP6150. The MCDP6150 includes the following blocks. The details of each block are described in the following sections:

1. Receiver PHY
2. Transmitter PHY
3. UFP interface
4. DFP interface
5. AUX_CH
6. TWI
7. Crystal Interface for reference clock

3.3. Receiver PHY

The receiver PHY of the MCDP6150 employs CTLE and DFE with adaptive equalization logic, CDR block, a serial to parallel conversion block, and an eye-opening monitor (EOM) block. The termination register of the receiver is calibrated to a differential of 100 ohm by default. Depending on the impedance of PCB track, the termination can be programmed to 80 ohm.

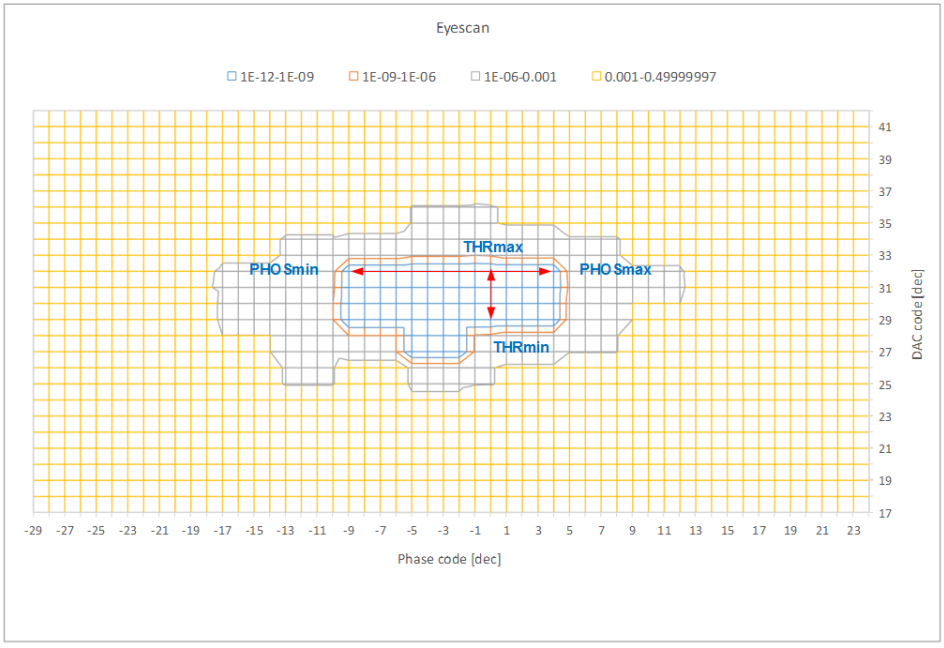
CTLE's degeneration resistance is tunable for up to 40 steps, which corresponds to 0 dB to 14 dB peaking at 4.05 GHz (in a typical case). The CTLE capacitance is fixed by default.

Both the CTLE degeneration resistance and each DFE TAP value are automatically adapted to channel characteristics during the link training.

The MCDP6150 supports the real time eye-opening monitor (EOM) in the background. EOM can use two different methods:

- FSM based observation of four sampling points which detects a lower BER than the configured threshold
- Scans all sampling points by software implementation

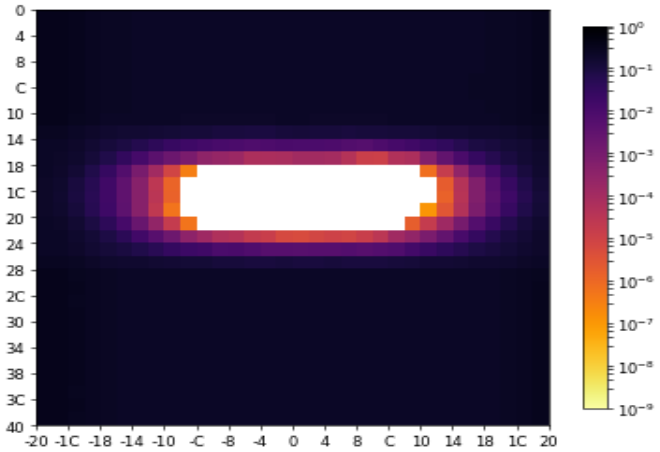
Figure 8. FSM Based Eye Scan Concept



The figure above shows a concept of the FSM based EOM method. THRmax and THRmin indicate the vertical range to operate in less than 1E-9 BER. PHOSmin and PHOSmax indicate the horizontal range to operate in less than 1E-9 BER.

Scanning full range is also possible by software. The figure below is an example of a software based EOM.

Figure 9. Example Output of Software Based Eye Scan



3.4. Transmitter PHY

The MCDP6150 transmitter supports up to 1000 mVpp diff swing without emphasis. The MCDP6150 supports up to 9 dB pre-emphasis when the voltage swing level is set to 0. The MCDP6150 uses pre-programmed parameter sets to be compliant with DP 1.4a standards. The table below shows a combination of the voltage swing levels and the pre-emphasis level which the MCDP6150 supports.

Table 2. DP transmitter configuration

Voltage Swing Level	Pre-emphasis Level			
	0	**1**	**2**	**3**
0	Support	Support	Support	Support
1	Support	Support	Support	Not Support
2	Support	Support	Not Support	Not Support
3	Support	Not Support	Not Support	Not Support

The MCDP6150 transmitter uses the clock from a phase interpolator. The phase interpolator generates a modulated clock to support SSC (Spread Spectrum Clocking). The table below shows the origin of the SSC generator in the MCDP6150. Since the MCDP6150 operates as a BLR (Bit Level Retimer), which does not support an elasticity buffer to compensate for the clock offset, the transmitter clock has to be synchronized with the receiver clock through the low pass filter.

Table 3. SSC source

SSC Source	SSC Profile
Recovered Clock	Depend on DPTX SSC profile

3.5. UFP Interface

The MCDP6150 receives audio-video streams (DisplayPort) from a source device via the DisplayPort link (DP Link). The UFP interface comprises four main link receivers and an AUX CH, which become ready for the operation upon the power-up. Both the receiver and AUX_CH shall be AC-coupled.

The MCDP6150 provides the receiver status monitor registers through the TWI in the transparent mode. Those registers can be accessed by reading the repeater DPCD field through AUX_CH when the MCDP6150 is in the non-transparent mode.

The MCDP6150 receiver includes an adaptive equalizer so that the receiving signal is properly equalized during the channel equalization phase. The adaptation is enabled when the TRAINING_PATTERN_SELECT of DPCD ‘h00102 in transparent mode, or the corresponding repeater DPCD field in non-transparent mode, is TPS2, TPS3, or TPS4.

3.6. DFP Interface

The MCDP6150 DFP interface consists of four main link transmitters and AUX_CH interface, which become ready for the operation upon the power-up. Both the transmitter and AUX_CH shall be AC-coupled.

The MCDP6150 adjusts its main link transmitter amplitude level and pre-emphasis level according to the DPCD transaction of ‘h00103 – ‘h00106, ‘h00206 and ‘h00207 in the transparent mode or equivalent PHY repeater DPCD address in the non-transparent mode. The transmitter can be also configured via TWI.

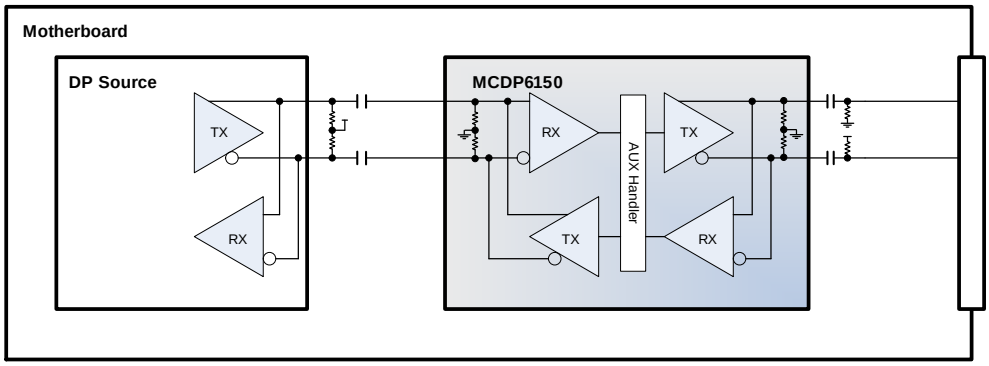
3.7. AUX_CH Interface

The DisplayPort Aux channel is a half-duplex bidirectional, AC-coupled, doubly-terminated differential pair. It is capable of transmitting and receiving bits at 1 Mbps. The AUX channel is used for link management and device control and handles the following functions:

1. Link training
2. Exchanging DPCD

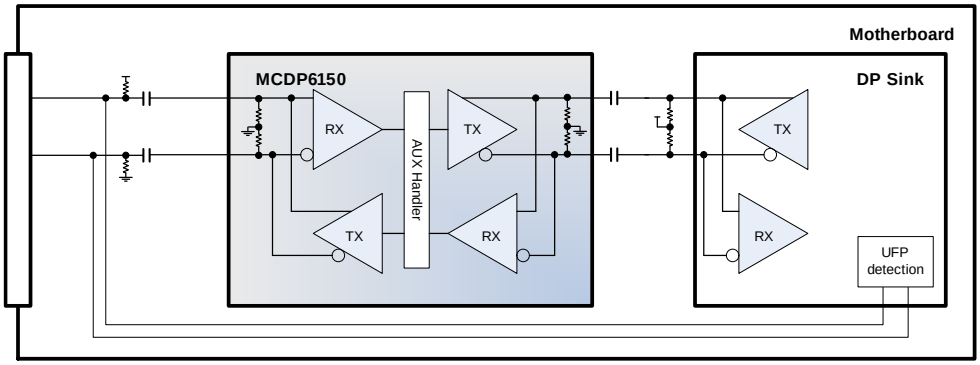
The MCDP6150 is compliant with DPCD Rev. 1.4.

Figure 10. AUX_CH topology in DPTX system



Note: The termination resistors next to the DP source may not be required when DP source integrates these resistors.

Figure 11. AUX_CH topology in DPRX system



Note: The termination resistors next to the DP sink may not be required when DP sink integrates these resistors.

The MCDP6150 monitors DPCD ‘h00100 – ‘h00101 to decide the bit rate and the lane configuration.

The MCDP6150’s DP receiver status can be obtained through DPCD. The snooped information can be also read through the TWI.

3.7.1. AUX_CH latency mode

The MCDP6150 provides two AUX_CH latency modes, low latency mode and normal latency mode. The summary of the differences between two modes are described in Table 4. AUX_CH latency mode can be preconfigured by the bootstrap as described in section 3.8.1. It can be also configured through 0x350 register configuration.

Table 4. AUX_CH latency mode

mode	AUX_CH UI tolerance	AUX_CH propagation delay
Low latency	0.5UI -10%/+5%	15-us for round trip
Normal latency	0.5UI +/-20%	100-us for round trip

Table 5. 0x350 register definition

0x350	DP_RT_CONFIG	RW
POD: 0x0000000F		
BIT	**BIT NAME**	**FUNCTION**
3:0	DP_RXEQ_CONT	DP Rx EQ adaptation option for [0] RBR, [1] HBR, [2] HBR2, [3] HBR3 0: Rx EQ adaptation during TPS2-4 (Default) 1: Rx EQ adaptation during TPS2-4 and the beginning of Video stream
4	RTMR_DP_AUX_CONFIG	0: Low latency mode (Default) 1: Normal latency mode
6:5	Reserved	Reserved
7	DPRX_RST_CONFIG	0: initialize DPRX upon DPCD 100h and 600h write acknowledgement (Default) 1: disable DPRX initialization based on DPCD 100h and 600h
8	Reserved	Reserved
9	RETIMER_CONFIG_RW9	Bootstrap override enable for RTMR_DP_AUX_CONFIG[0]
31:10	Reserved	Reserved

When the MCDP6150 is embedded in DPRX system operating in the transparent mode of LTTPR, the AUX_CH propagation delay needs to be as part of the AUX_CH response time from the DPRX device. (e.g.

in normal latency mode, 50 µs is already added when the DPRX device received the AUX_CH request from DPTX and another 50 µs is added when the DPTX detects DPRX response. Therefore AUX_CH response should be prepared within 200 µs by DPRX. Otherwise, DPRX should respond with AUX_DEFER by 200 µs timer timeout.)

When the MCDP6150 is embedded in DPTX system operating in the transparent mode of LTTPR, it is recommended to configure the MCDP6150 to the normal latency mode and configure the AUX_CH response timeout timer to 500 µs instead of 400 µs.

When the MCDP6150 is cascaded in the active cable, it is recommended to configure the MCDP6150 at the DPRX side to the normal latency mode and the other to the low latency mode.

3.8. IC Operation

3.8.1. Bootstrap

Table 6. MCDP6150 Bootstrap for start-up mode

DIS_N	Description
0	MCDP6150 enters low power mode upon the power-up. TWI shall be connected to an I2C master for the device configuration.
1	DisplayPort 1.4a LTTPR is enabled after the power-up.

Table 7. MCDP6150 Bootstrap for AUX_CH latency mode

TWISLV1	Description
0	Low latency mode
1	Normal latency mode

When the DIS_N is pulled down to GND during the power-up, the external pin control is enabled. To change the control mode to TWI control mode, the following bits should be set to 1:

- OPMODE_CONF.DIS_N_BS_OVR

Table 8. Operation mode configuration register

0x504	OPMODE_CONF	RW
Chip configuration		
BIT	BIT NAME	FUNCTION
2:0	Reserved	Reserved
3	DIS_N_OVR_EN	DIS_N_OVR_EN, 0: GPIO setting, 1: TWI setting
5:4	Reserved	Reserved
6	DIS_N	0: Configure MCDP6150 to Low power mode 1: Enable DisplayPort 1.4a retimer
7	Reserved	Reserved
8	IC_SOFT_RST	0: Normal operation 1: Reset whole IC
9	Reserved	Reserved
10	DP_SOFT_RST	0: Normal operation 1: Reset DP data path
11	DP_AUX_SOFT_RST	0: Normal operation 1: Reset DP AUX_CH logic
13:12	Reserved	Reserved
14	DIS_N_BS_OVR	Bootstrap override enable for DIS_N
15	Reserved	Reserved
16	DP_LT_AMP_PRE_CHK_DIS	0: Enable EQ adaptation result check to request different voltage swing or pre-emphasis level 1: Disable EQ adaptation result check during DP link training
17	DP_LT_SYMB_ERR_CHK_DIS	0: Enable symbol error count check to request different voltage swing or pre-emphasis level 1: Disable symbol error count check during DP link training
31:18	Reserved	Reserved

3.8.2. IC Top-Level State Machine

The figure below shows the state machine to control the MCDP6150. This state machine changes the MCDP6150 operation mode based on the configuration registers or pins. The MCDP6150 provides two options to trigger the state change as explained in Section 0 and Section 3.8.4.

Note: DIS_N is recommended to be high upon the power-up of the MCDP6150. Otherwise, a couple of register accesses may be required to configure the MCDP6150.

Figure 12. MCDP6150 Operation Mode State Machine

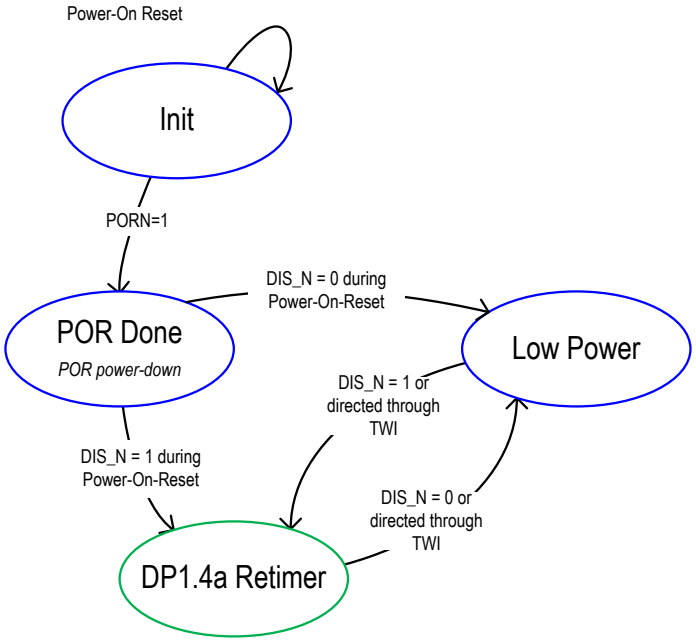


Table 9. MCDP6150 Operating Mode

DIS_N	Description
0	Low power mode
1	Normal operation

3.8.3. TWI Programmable Mode

The MCDP6150 operation mode shall be controlled through DIS_N pin in default. TWI register access is required to enable the operation mode change through TWI.

3.8.4. Stand-Alone Mode

The MCDP6150 operation mode shall be controlled through DIS_N pin in default. The default state after the power-on is the normal operation when DIS_N pin is high upon the power-on. The MCDP6150 changes its state according to the DIS_N pin's level.

Note: DIS_N are designed to operate under 1.8 V in nominal case. Connecting this I/O with 3.3 V output buffer would cause damage.

Note: MCDP6150 must be connected to a controller through TWI for IC configuration. The exceptional use case must be reviewed.

3.8.5. Low Power Mode

The MCDP6150 enters into the low power mode when DIS_N is set to low. Upon the power-up, DIS_N should be high for proper operation. Only DIS_N pin, the TWI slave and the register banks in always power-on domain are enabled in the low power mode. The MCDP6150 can be programmed through the TWI for any required changes in the configuration of low power mode. When the operating mode changes from the normal operation mode to the low power mode, the MCDP6150 goes through the reset cycle except for the register bank in always power-on domain.

The receiver termination is not present in the low power mode; for example, the high impedance can be seen by the UFP transmitter.

3.8.6. DisplayPort Retimer Operation

The MCDP6150 operates as the DisplayPort LT-tunable PHY repeater at the DisplayPort bit rate of RBR, HBR, HBR2 and HBR3 when the DIS_N is set to high. The default is transparent mode as defined in DisplayPort1.4a standard. The MCDP6150 can be set to non-transparent mode by writing AAh to F0003h of the DPCD address. Non-transparent mode is allowed only when the DPCD revision is DPCD Rev. 1.4 or higher.

The HPD signal is not routed to the MCDP6150. The MCDP6150 transitions to the DP sink detected state when DIS_N is set to high. The MCDP6150 supports DPCD version 1.4.

Transparent Mode

The transparent mode is the default operating mode of the MCDP6150.

The MCDP6150 starts charging the AC coupling capacitors on the transmission lines of the main links and AUX_CH as soon as DIS_N is set to high.

The MCDP6150 snoops some link configuration registers. However, the MCDP6150 manipulates the received ADJUST_REQUEST_LANEx message from the sink device according to its receiver link training status. When the MCDP6150 receiver is trained while the sink device receiver is still not trained, the MCDP6150 manipulates the received ADJUST_REQUEST_LANEx message so that the source device does not change the transmitter parameter. When the receiver of the MCDP6150 is not trained when it receives the adjusted request, the MCDP6150 manipulates the received ADJUST_REQUEST_LANEx based on its preprogrammed adjust request sequence.

The MCDP6150 manipulates TRAINING_LANEx_SET from the source device to be consistent with its manipulation of ADJUST_REQUEST_LANEx.

The MCDP6150 changes its transmitter configuration based on the ADJUST_REQUEST_LANEx field, which determines the DPTX' voltage swing level and pre-emphasis magnitude.

Non-Transparent Mode

The MCDP6150 operates as defined in the section of the LT-tunable PHY repeater of DisplayPort1.4a.

3.9. Power Supply

The MCDP6150 operates at 1.8V and 1.2V supplies.

Note: There is no relationship between 1.8 V ramp-up timing and 1.2 V ramp-up timing. 1.2 V can be supplied earlier than 1.8 V. Each power supply ramp-up time shall be between 200-us and 10-ms.

3.10. Power Consumption

Table 10. Power Consumption (Preliminary estimation in typical conditions)

IC Operation Mode	State	Power Consumption (mW)
Low Power Mode	Low Power Mode	0.85
DisplayPort 4 lane DP_BR (HBR3)	D0 power state	460
DisplayPort 4 lane DP_BR (HBR3)	D3 power state	10

3.11. System Interface

3.11.1. TWI

The TWI slave, which is compatible with I2C, is intended for an external host controller to configure the MCDP6150 registers for certain use cases. TWI is accessible in any operating mode.

Note: SDA and SCL shall be pulled up to 3.3 V.

TWISLV0 and TWISLV1 are designed to operate under 1.8V in nominal case. Connecting these I/O with a 3.3 V output buffer would cause damage.

TWI Device ID

The TWI of the MCDP6150 operates as the slave. Four device IDs can be supported. Each device's ID is determined by the TWISLV0 and TWISLV1 pins as shown in the table below. The TWISLV0/1 pull-up/down status is detected by the MCDP6150 during the power-up sequence.

Table 11. TWI Device ID Configuration

TWISLV1	TWISLV0	Slave ID
Pulled down to Ground	Pulled down to Ground	0x14
Pulled down to Ground	Pulled up to 1.8V	0x15
Pulled up to 1.8V	Pulled down to Ground	0x16
Pulled up to 1.8V	Pulled up to 1.8V	0x17

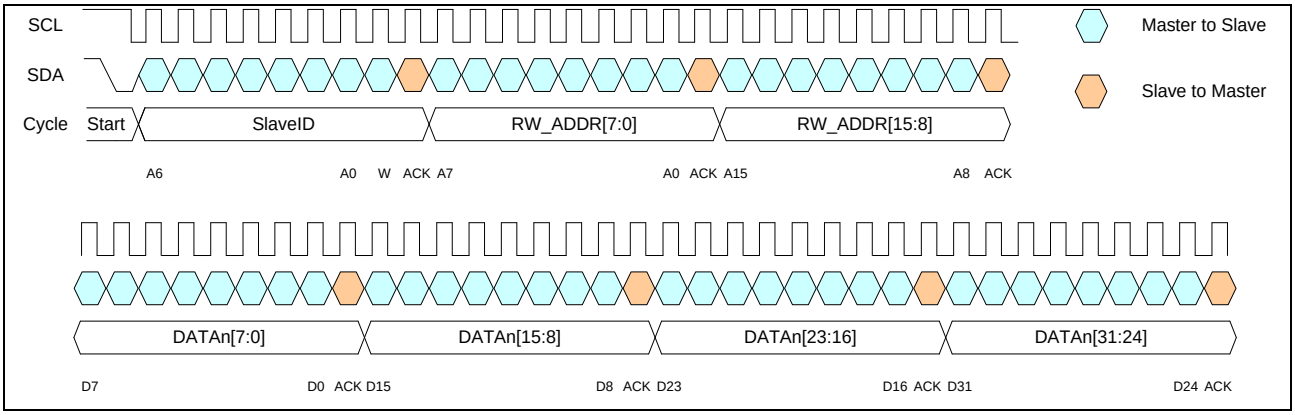
TWI Read / Write Access

The TWI access to the MCDP6150 is 32-bit write or read. All register accesses are on 32-bit word boundaries. Address auto-increment is also allowed on 32-bit word boundary. Stop / Repeated start can be used to change the base address to a new address definition.

The figure below shows typical write access:

1. Master sends Slave ID with write access.
2. Master sends lower byte of 16-bit register address.
3. Master sends higher bytes of 16-bit register address.
4. Master sends data bytes to be written in order of lower byte to higher byte.

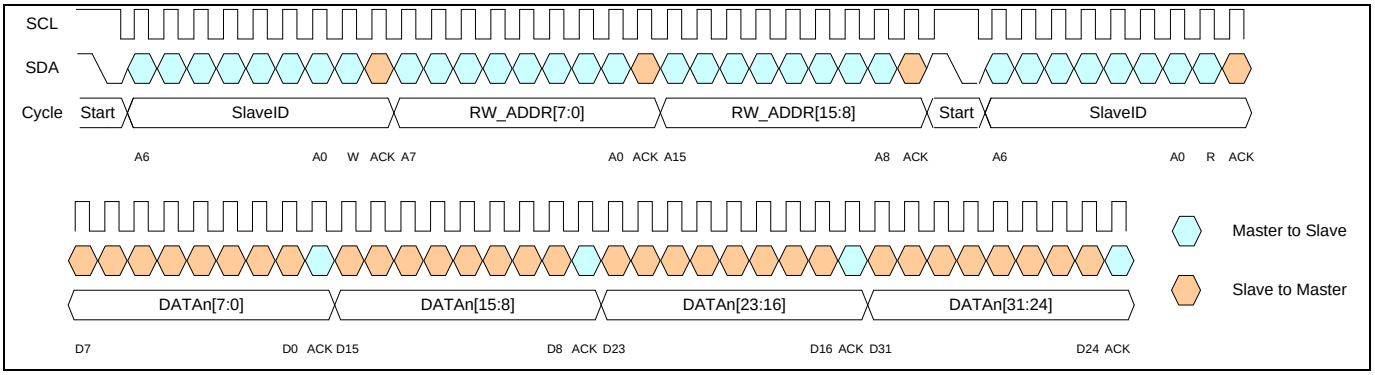
Figure 13. Write Access



The figure below shows typical read access:

1. Master sends Slave ID with write access.
2. Master sends lower byte of 16-bit register address.
3. Master sends higher bytes of 16-bit register address.
4. Master sends re-start with read access.
5. Slave responds with data bytes.

Figure 14. Read Access

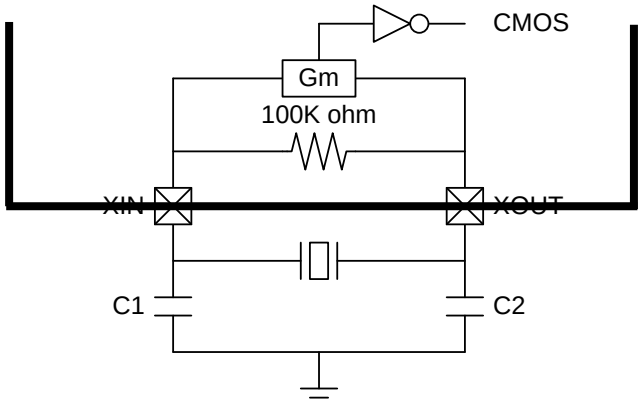


3.11.2. XTAL Buffer Operation

When a crystal resonator is connected between the XIN pin and XOUT pin with the appropriate-sized loading capacitors C1 and C2, the internal oscillator becomes active. A 25 MHz crystal oscillation is required to meet the frequency requirements.

Note: The size of C1 and C2 is determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the device and the printed circuit board traces. The loading capacitors are terminated to the ground.

Figure 15. Internal Oscillator with an External Crystal



Recommendation for the crystal is shown in the table below.

Table 12. Recommended Crystal Specifications

Parameters	Specifications
Frequency	25.000 MHz
Operation mode	Fundamental
Operating temperature	-10ºC to +85ºC
Frequency tolerance @25ºC	+/- 50 ppm max
Equivalent series resistance	< 50Ω

Suggested load capacitance value is 10pF ~ 12pF.

3.11.3. Reference Clock Input

The MCDP6150 can also use the reference clock input. XIN can be the reference clock input buffer. When the reference clock is used, XOUT has to be floated. Setting bit 30 of RETIMER_CONFIG3 register (address 0x30C) enables the single-ended reference clock input buffer.

Table 13. Recommended Reference Clock Input Characteristics

Parameters	Specifications
Frequency	25.000 MHz
Frequency tolerance @25ºC	+/- 50 ppm max
Maximum Input Voltage	1.8 V

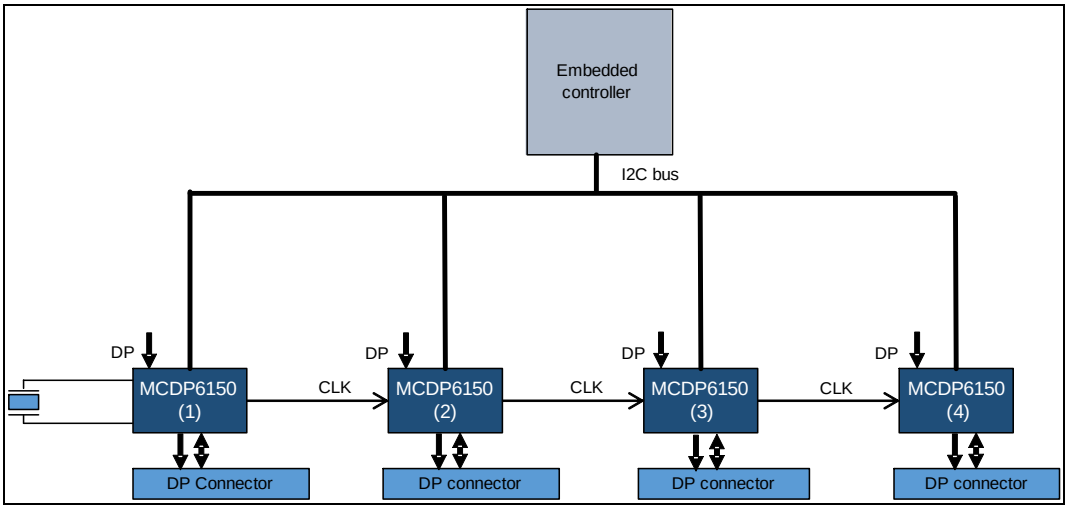
3.11.4. Reference Clock Output

The MCDP6150 supports cascading the reference clock for the system which implements multiple MCDP6150 closely. The reference clock output can be enabled or disabled through the TWI register. The MCDP6150 does not require the reference clock in low-power mode. The MCDP6150 requires the reference clock when DisplayPort channels are active.

Table 14. Reference Clock Output Characteristics

Parameters	Specifications
Frequency	25.000 MHz
Frequency tolerance @25ºC	+/- 50 ppm max
Maximum output Voltage	0.9 V
Load capacitance	< 5 pF

Figure 16. Cascading Reference Clock Across Multiple MCDP6150 in DPTX system



Note: To enable the reference clock cascading, MCDP6150 should be configured sequentially from MCDP6150 (1) in Figure 16, followed by MCDP6150 (2).

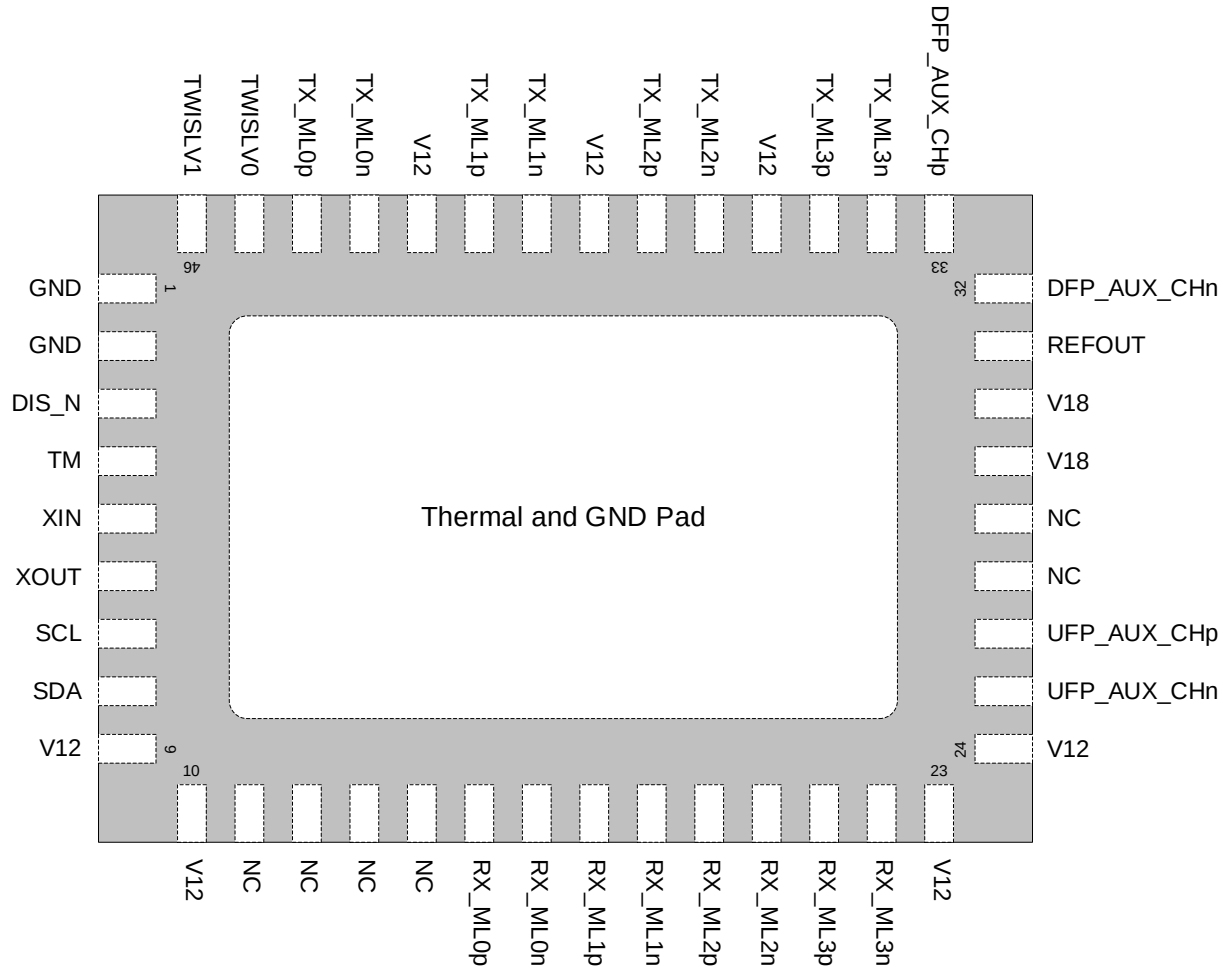
Bit 30 and 31 shall be programmed to cascade the reference clock. Bit 30 is to use the single-end reference clock instead of XTAL. Bit 31 is to output the single-end clock. Until the reference clock is available, the MCDP6150 operates with internal ring oscillator.

Table 15. Reference Clock Configuration Register Definition

0x30C	IC_RT_CONFIG	RW
Reference clock configuration		
BIT	**BIT NAME**	**FUNCTION**
29:0	Reserved	Reserved
30	XTAL_REF_MODE	0: Normal operation (crystal driven mode) (Default) 1: Single-end reference clock receiver mode
31	REFOUT_EN	REFOUT enable. Active high. 0: Disable REFOUT (Default) 1: Enable REFOUT

4. Pin Description

Figure 17. MCDP6150 Ex-VQFN46 Pin Assignment (Top-View)



Note: The pin assignment in Figure 17 is applicable when DIS_N is pulled up to high during the power-up.

I/O Legend:

I = Input; O = Output; P = Power, G = Ground; IO = Bi-direction

Table 16. Pin Description

Pin#	Name	I/O	Description
1	GND	G	Ground
2	GND	G	Ground
3	DIS_N	I	Active low disable pin 0: MCDP6150 in low power mode 1: MCDP6150 in normal operation DIS_N shall be 1 upon power-up
4	TM	I	Test Mode pin. Internally pulled-down to GND.
5	XIN		XTAL nodes. XIN: When the oscillator clock is used as reference, connect to the clock XOUT: When the oscillator clock is used as reference, float this pin.
6	XOUT		
7	SCL	I	TWI clock line. External pull-up required for TWI operation. Leave NC when not used.
8	SDA	IO	TWI data line. External pull-up required for TWI operation. Leave NC when not used.
9	V12	P	1.2 V power supply.
10	V12	P	1.2 V power supply.
11	NC	-	Not Connect
12	NC	-	Not Connect
13	NC	-	Not Connect
14	NC	-	Not Connect

Pin#	Name	I/O	Description
15	RX_ML0p	I	DisplayPort receiver main link Lane 0 positive analog input
16	RX_ML0n	I	DisplayPort receiver main link Lane 0 negative analog input
17	RX_ML1p	I	DisplayPort receiver main link Lane 1 positive analog input
18	RX_ML1n	I	DisplayPort receiver main link Lane 1 negative analog input
19	RX_ML2p	I	DisplayPort receiver main link Lane 2 positive analog input
20	RX_ML2n	I	DisplayPort receiver main link Lane 2 negative analog input
21	RX_ML3p	I	DisplayPort receiver main link Lane 3 positive analog input
22	RX_ML3n	I	DisplayPort receiver main link Lane 3 negative analog input
23	V12	P	1.2 V power supply.
24	V12	P	1.2 V power supply.
25	UFP_AUX_CHn	IO	DisplayPort receiver auxiliary channel negative analog input/output.
26	UFP_AUX_CHp	IO	DisplayPort receiver auxiliary channel positive analog input/output.
27	NC	-	Not Connect
28	NC	-	Not Connect
29	V18	P	1.8 V power supply
30	V18	P	1.8 V power supply
31	REFOUT	O	Reference clock output
32	DFP_AUX_CHn	IO	DisplayPort receiver auxiliary channel negative analog input/output.
33	DFP_AUX_CHp	IO	DisplayPort receiver auxiliary channel positive analog input/output.
34	TX_ML3n	O	DisplayPort transmitter main link Lane 3 negative analog output

Pin#	Name	I/O	Description
35	TX_ML3p	O	DisplayPort transmitter main link Lane 3 positive analog output
36	V12	P	1.2 V power supply.
37	TX_ML2n	O	DisplayPort transmitter main link Lane 2 negative analog output
38	TX_ML2p	O	DisplayPort transmitter main link Lane 2 positive analog output
39	V12	P	1.2 V power supply.
40	TX_ML1n	O	DisplayPort transmitter main link Lane 1 negative analog output
41	TX_ML1p	O	DisplayPort transmitter main link Lane 1 positive analog output
42	V12	P	1.2 V power supply.
43	TX_ML0n	O	DisplayPort transmitter main link Lane 0 negative analog output
44	TX_ML0p	O	DisplayPort transmitter main link Lane 0 positive analog output
45	TWISLV0	I	Bit 0 of TWI device ID. Internally pulled-down to GND.
46	TWISLV1	I	Bit 1 of TWI device ID. Internally pulled-down to GND.
TGP	GND	G	Thermal and GND Pad. Connect to Ground for electrical and thermal usage.

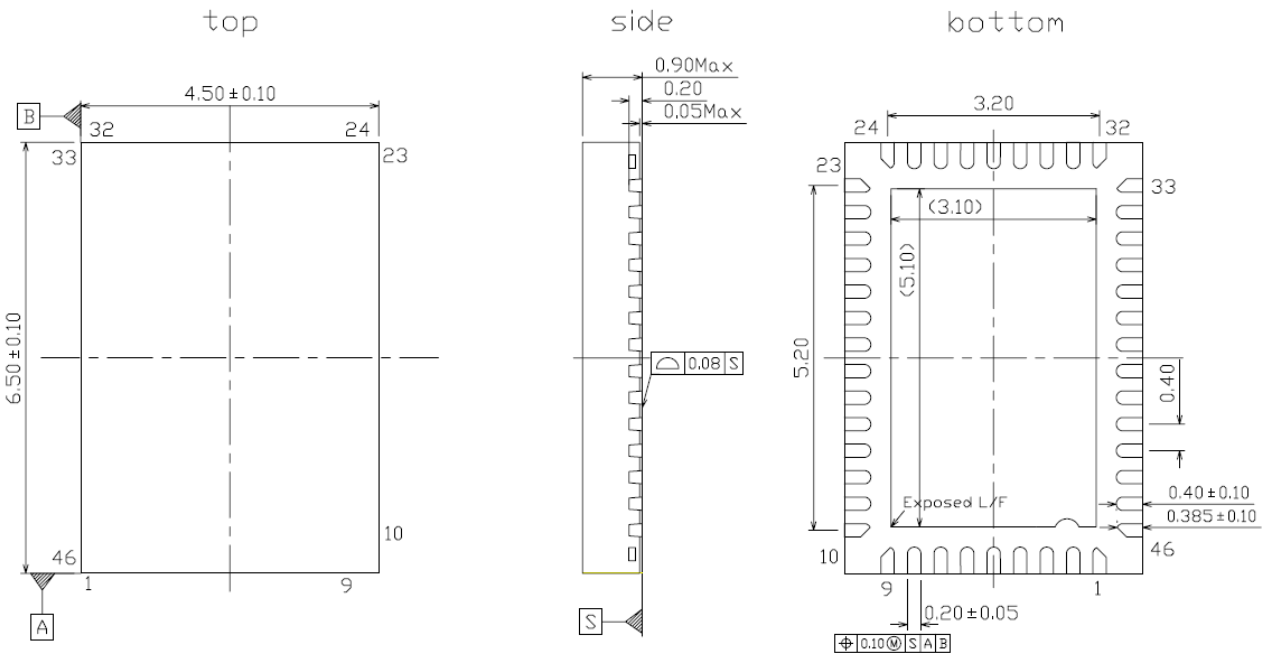
5. Package Specification

Package type:

Ex-VQFN46 (6.5 x 4.5, 46 pins, 0.40 mm pitch)

5.1. Package Drawing and Dimensions

Figure 18. MCDP6150 Ex-VQFN46 Package Outline Drawing (unit: mm)



6. Marking Field Template and Descriptors

The MCDP6150 marking template on Ex-VQFN46 is shown below.

Figure 19. MCDP6150 Ex-VQFN46 Marking Template

Table 17. Field Descriptors

Field	Description	Marking
DOT	Pin1 indicator	DOT
Line 1	Company logo	KT LOGO
Line 2	Part Number + IC revision	MCDP6150RR
Line 3	TNNNNN: Fab Lot Number	“Variant”
Line 4	YYWW: Assembly Date Code (Work Year & Work Week) V: Assembly Vendor Code XXX: Serial Number	“Variant”

7. Electrical Specifications

7.1. Absolute Maximum Ratings

Table 18. Absolute Maximum Ratings[1]

(T_A = 25^{O}C unless otherwise stated)

Symbol	Description	Value	Units
$V_{DD\_1.8V}$	VDD1.8V to GND	-0.3 to 2.5	V
$V_{DD\_1.2V}$	VDD1.2V to GND	-0.3 to 1.5	V
V_{RF_IN}	USB, SSTX, DP, Mln, RX1, RX2 to GND	-0.3 to 1.4	V
V_{RF_OUT}	USB, SSRX, TX1, TX2 to GND	-0.3 to 1.4	V
T_J	Junction Operating Temperature Range	-0 to 125	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

7.2. ESD and Latch-up Ratings

Table 19. ESD and Latch-up Ratings[2]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JESD22-A114 ESD HBM (all pins)	±2.0	kV
V_{ESD_CDM}	JEDEC JESD22-C101 ESD CDM (all pins)	±500	V
I_{LU}	JEDEC JESD78	±100	mA

7.3. Thermal Capabilities

Table 20. Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	36.6	°C/W
Θ_{JC}	Thermal Resistance – Junction to Case	19.5	°C/W
φ_{JT}	Thermal Resistance – Junction to Package Top	0.3	°C/W
φ_{JB}	Thermal Resistance – Junction to PCB	10.3	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD and Latch-up Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
3. .Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a four-layer JEDEC PCB board, no heat spreader, and no air flow.

7.4. Recommended Operating Conditions

Table 21. Recommended Operating Conditions

Description	Range
1.2V Supply Voltage	1.14V to 1.26V
1.8V Supply Voltage	1.65V to 1.95V
Ambient Operating Temperature Range	0°C to 70°C
Junction Operating Temperature Range	0°C to 125°C

7.5. Electrical Characteristics

7.5.1. DC Characteristics

Table 22. DC Characteristics

Specifications	Symbol	Unit	Min	Typ	Max	Comments
Supply Current in 4-Lane active mode (DisplayPort HBR3 4 lane)						
VDD 1.8 V	I_{d18}	mA		10	13	
VDD 1.2 V	I_{d12}	mA		370	532	
Supply Current in low power mode (DIS_N = 0)						
VDD 1.8 V	I_{s18}	µA		70		
VDD 1.2 V	I_{s12}	µA		600		
Open drain IO (SCL, SDA)						
Input voltage	Vpad	V	3	3.3	3.6	
Input high voltage	Vihod	V	2.4			
Input low voltage	Vilod	V			0.35	
Output low Current	Iol	mA	5.3	8.7	10.7	At Vol = 0.4V
Schmitt trigger pins (TWISLV0/1)						
Positive Going Threshold Voltage	V_{t+}	V	0.4 V_{18}		0.7 V_{18}	V_{OUT} >= V_{OH}(min)
Negative Going Threshold Voltage	V_{t-}	V	0.3 V_{18}		0.6 V_{18}	V_{OUT} <= V_{OL}(max)
Hysteresis Voltage	V_h	V	0.1 V_{18}		0.5 V_{18}	V_{t+} - V_{t-}
Input low current	I_{ILst}	µA			10	
Input high current	I_{IHst}	µA			10	

DIS_N						
Input low voltage	V_{IL}	V	-0.3		0.3 V_{18}	
Input high voltage	V_{IH}	V	0.65 V_{18}		V_{18}+0.3	
Input low current	I_{IL}	µA			10	
Input high current	I_{IH}	µA			10	

7.5.2. DisplayPort transmitter

AC characteristics parameters are guaranteed by the silicon characterization across operating condition unless otherwise specified. Not all parameters are tested in the production test.

Table 23. DisplayPort transmitter characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Comments
DisplayPort Main-Link transmitter system parameters (Type-C interface in DP mode)						
Differential output voltage range	$V_{TX\_DIF\_PP\_RANGE}$	V			1.05	
Termination control range	$R_{TX\_TERM\_RANGE}$	ohm	80		120	
Frequency for high bit rate 3	f_{HBR3}	Gbps		8.1		
Frequency for high bit rate 2	f_{HBR2}	Gbps		5.4		
Frequency for high bit rate	f_{HBR}	Gbps		2.7		
Frequency for reduced bit rate	f_{RBR}	Gbps		1.62		
Link clock down-spreading amplitude	SSC_{DPTX_AMP}	%	0		0.5	
Link clock down-spreading frequency	SSC_{DPTX_FREQ}	kHz	30		33	
AC coupling capacitor	C_{TX_DP}	nF	75		265	
HBR3/HBR2 transmitter TP2 parameters						
Ratio of Voltage Swing (VSL[1]/VSL[0])	$R_{VSL\_1\_0\_HBR3\_2}$	dB	1.6		4.5	Calculated using measured value of 1st harmonic of FFT at TX_EOL[0]
Ratio of Voltage Swing (VSL[2]/VSL[0])	$R_{VSL\_2\_0\_HBR3\_2}$	dB	3.2		7.0	
Ratio of Voltage Swing (VSL[3]/VSL[0])	$R_{VSL\_3\_0\_HBR3\_2}$	dB	4.8		10.5	
Ratio of Voltage Swing (VSL[2]/VSL[1])	$R_{VSL\_2\_1\_HBR3\_2}$	dB	1.1			
Ratio of Voltage Swing (VSL[3]/VSL[2])	$R_{VSL\_3\_2\_HBR3\_2}$	dB	1.1			
Delta of TX Pre-emphasis TX_EQL[1]/TX_EQL[0]	$\Delta_{EQL\_1\_0\_HBR3\_2}$	dB	1.3		4.0	Calculated using

Parameter	Symbol	Unit	Min	Typ	Max	Comments
Delta of TX Pre-emphasis TX_EQL[2]/TX_EQL[0]	$\Delta_{EQL\_2\_0\_HBR3\_2}$	dB	2.4		6.0	measured value of 1st and 5th harmonics of FFT
Delta of TX Pre-emphasis TX_EQL[3]/TX_EQL[0]	$\Delta_{EQL\_3\_0\_HBR3\_2}$	dB	3.5		8.0	
Delta of TX Pre-emphasis TX_EQL[2]/TX_EQL[1]	$\Delta_{EQL\_2\_1\_HBR3\_2}$	dB	0.7			
Delta of TX Pre-emphasis TX_EQL[3]/TX_EQL[2]	$\Delta_{EQL\_3\_2\_HBR3\_2}$	dB	0.7			
HBR/RBR transmitter TP2 parameters						
Ratio of Output Voltage Level 1/Level 0	$R_{VSL\_1\_0\_HBR\_RBR}$	dB	0.8		6.0	Measured on non-transition bits at Pre-emphasis Level 0 setting.
Ratio of Output Voltage Level 2/Level 1	$R_{VSL\_2\_1\_HBR\_RBR}$	dB	0.1		5.1	
Ratio of Output Voltage Level 3/Level 2	$R_{VSL\_3\_2\_HBR\_RBR}$	dB	0.8		6.0	
Maximum Pre-emphasis when disabled	$R_{EQ\_DISABLE}$	dB			0.25	
Delta of Pre-emphasis Level 1 vs. Level 0	$\Delta_{EQL\_1\_0\_HBR\_RBR}$	dB	2			
Delta of Pre-emphasis Level 2 vs. Level 1	$\Delta_{EQL\_2\_1\_HBR\_RBR}$	dB	1.6			
Delta of Pre-emphasis Level 3 vs. Level 2	$\Delta_{EQL\_3\_2\_HBR\_RBR}$	dB	1.6			
HBR3 transmitter TP3_CTLE parameters						
Total jitter	$T_{TX\_TJ\_TPS4\_HBR3}$	mUI			470	Measured at BER 10^{-6} with TPS4
Non-ISI jitter	$J_{TX\_NonISI\_TPS4\_HBR3}$	mUI			230	Measured at BER 10^{-6} with TPS4
Eye height	V_{HEIGHT_HBR3}	mV	65			
HBR2 transmitter TP3_EQ parameters						
Total jitter	$T_{TX\_TJ\_CP2520\_HBR2}$	mUI			620	Measured at BER 10^{-9} with CP2520
Random Jitter	RJ_HBR2	mUI			230	
Eye height	V_{HEIGHT_HBR2}	mV	90			

7.5.3. DisplayPort receiver

AC characteristics parameters are guaranteed by the silicon characterization across operating condition unless otherwise specified. Not all parameters are tested in the production test.

Table 24. DisplayPort receiver characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Comments
DisplayPort Main-Link receiver system parameters						
Termination control range	$R_{TX\_TERM\_RANGE}$	ohm	80		120	
Frequency for high bit rate 3	f_{HBR3}	Gbps		8.1		
Frequency for high bit rate 2	f_{HBR2}	Gbps		5.4		
Frequency for high bit rate	f_{HBR}	Gbps		2.7		
Frequency for reduced bit rate	f_{RBR}	Gbps		1.62		
Link clock down-spreading amplitude	SSC_{DPTX_AMP}	%	0		0.5	
Link clock down-spreading frequency	SSC_{DPTX_FREQ}	kHz	30		33	
HBR3 DisplayPort Main-Link Receiver TP3_EQ parameters						
Minimum Receiver Eye width	$T_{HBR3\_EYE\_TPS3EQ}$	mUI	380			Measured at 10^{-6} BER
RX differential peak-to-peak Eye voltage	$V_{RX\_DIF\_PP\_MIN\_HBR3}$	mV	40			
Random Jitter	$T_{RX\_RJ\_TPS4\_HBR3}$	mUI			123	
Minimum Receiver Non-ISI jitter	$T_{RX\_NON\_ISI\_HBR3}$	mUI			380	
HBR2 DisplayPort Main-Link Receiver TP3_EQ parameters						
Minimum Receiver Eye width	$T_{HBR2\_EYE\_TPS3EQ}$	mUI	380			Measured at 10^{-9} BER
RX differential peak-to-peak Eye voltage	$V_{RX\_DIF\_PP\_MIN\_HBR2}$	mV	70			
HBR DisplayPort Main-Link Receiver TP3_EQ parameters						
Minimum Receiver Eye width	$T_{HBR\_EYE\_TPS3EQ}$	mUI	509			Measured at 10^{-9} BER
RX differential peak-to-peak Eye voltage	$V_{RX\_DIF\_PP\_MIN\_HBR}$	mV	150			
RBR DisplayPort Main-Link Receiver TP3 parameters						
Minimum Receiver Eye width	$T_{HBR\_EYE\_TPS3EQ}$	mUI	250			Measured at 10^{-9} BER
RX differential peak-to-peak Eye voltage	$V_{RX\_DIF\_PP\_MIN\_HBR}$	mV	46			

7.5.4. DisplayPort AUX_CH

AC characteristics parameters are guaranteed by the silicon characterization across operating condition unless otherwise specified. Not all parameters are tested in the production test.

Parameter	Symbol	Unit	Min	Typ	Max	Comments
Manchester transaction unit interval	UI_{AUX_MAN}	µs	0.4		0.6	
Number of pre-charge pulses	$N_{PRE\_CHARGE\_PULSE}$		10		16	
AUX CH bus park time	$T_{AUX\_BUS\_PARK}$	ns	10			
AUX peak-to-peak voltage at transmitter	$V_{AUX\_DIFFp-p\_TX}$	V	0.29	0.40	1.38	
AUX peak-to-peak voltage at receiver	$V_{AUX\_DIFFp\_p\_RX}$	V	0.27		1.36	
AUX CH termination	R_{AUX_TERM}	ohm		100		
AUX_DC common mode voltage	$V_{AUX\_TURN\_CM}$	V	0		3.6	
AUX turn-around common mode voltage	$V_{AUX\_TURN\_CM}$	V			0.3	
AC coupling capacitor	C_{AUX}	nF	75		200	

7.5.5. TWI Timing

Table 25. TWI Timing

Symbol	Parameter	Min	Max	Unit
FSCL	SCL Clock Frequency	400	1000	KHz
tSP	Pulse width of spikes that must be suppressed by the input filter		50	ns
tLOW	LOW period of the SCL clock	0.5	-	µs
tHIGH	HIGH period of the SCL clock	0.26	-	µs
thd: DAT	Data hold time	0	-	µs
tSU :DAT	Data se t-up time	50	-	µs
tR	Rise time of both SDA and SCL signals	-	120	µs
tF	Fall time of both SDA and SCL signals	20x (VDD /5.5)	120	µs
tBUF	Bus free time between a STOP and START condition	0.5	-	µs
CB	Capacitance load for each bus line	-	550	pF
tVD: DAT	Data valid time	-	0.45	µs
tVD: ACK	Data valid acknowledge time	-	0.45	µs