MCDP9000

USB Type-C Port Controller

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- V_{BUS} monitor
  - 10-bit measurement interface
  - 4V to 21.5V (± margin) with 25mV resolution
  - Accuracy of ±2% or ±50mV in above voltage region
- Active low Alert# as status change indicator
- V_{BUS} discharge control
  - Integrated 5V V_{BUS} discharge path
  - Control signal for > 5V V_{BUS} discharge path
- V_{BUS} load control
  - External FET control signal
- V_{BUS} voltage control
  - Variable resistance interface connected to feedback voltage of buck regulators
- USB Billboard device class support
  - USB 2.0 FS (Full-Speed) support
  - Flexibility to configure the bit field of billboard device class attributes
- Reference Clock
  - Operate with internal ring oscillator when USB billboard device is not used
  - Internal 48MHz reference clock for USB 2.0 FS PHY
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  - V_{BUS} reporting disable
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    - V_{BUS} monitoring
    - V_{BUS} auto discharge
  - Fault status reporting disable
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  - Power Supply
    - 5V ±10%
  - I/O voltage for I^2C and GPIOs
    - From 1.8V to 3.6V
  - CC / V_{CONN} / USB 2.0 D+/-
    - 5V tolerant
- ESD Specification
  - 2kV HBM
- Package
  - 24 pin QFN (4 mm x 4 mm)

Applications

- Desktop PC / Notebook / Tablet / Smartphone motherboard / Docking Station / USB Type-C AV accessory

1. Description

The MCDP9000 is a USB Type-C Port Controller (TCPC) primarily targeted for USB type-C alternate mode and / or Power Delivery (PD) provider/consumer/dual-role devices such as mobile phones, tablets, notebooks, dongles, docking stations etc., which implement USB PD communication stack based on TCPM / TCPC topology. The MCDP9000 implements Type-C CC logic, USB PD BMC PHY for CC communication, V_{CONN} switch, V_{BUS} voltage monitor, V_{BUS} voltage control logic, 5V V_{BUS} discharge path, high voltage V_{BUS} discharge control, I^2C slave to interface with EC (Embedded Controller) or CPU running device / policy management stack of PD, USB 2.0 full speed (FS) PHY and device controller to support billboard device.

2. Application Overview

Figure 1 shows a typical use case of the MCDP9000 together with a MCDP6000 in the notebook. This diagram shows a use case where a notebook supports both PD source to charge mobile devices such as smartphones and tablets and PD sink for its operation and battery charging. As the PD source for the mobile devices, 5V / 3A should cover most of the use cases while a higher power profile is required as the sink. To support higher power profiles, the MCDP9000 needs external components to handle higher voltage V_{BUS} line.

Figure 1. Typical use case of MCDP9000 together with MCDP6000 in Notebook

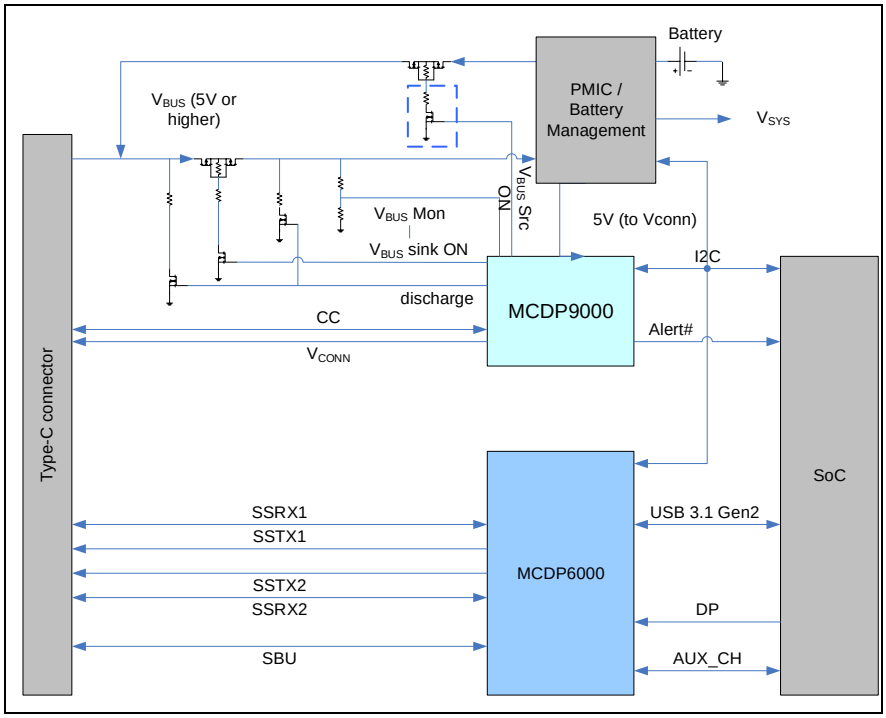


Figure 2 shows a typical use case of the MCDP9000 together with the MCDP6000 and the MCDP5xxx in a docking station. Type-C plug interface will be plugged into a notebook while USB Type-C pluggable device or cable will be plugged into the receptacle interface. In this use case, the MCDP9000 facing the plug interface will support “Provider” as PD source, which supports higher power profile than 15W. The receptacle receives the power from another PD source in this diagram. It is also possible that the Type-C receptacle interface supports “Provider” feature for battery charging of mobile devices. When the MCDP9000 is used with the MCDP5xxx, it will operate as TCPM interfacing with the MCDP9000 through I2C and Alert#. Since a typical docking station supports USB functionality, the MCDP9000’s billboard device class feature is defeatured for docking station type applications.

Figure 2. Typical use case of MCDP9000 together with MCDP5xxx and MCDP6000 in Docking Station

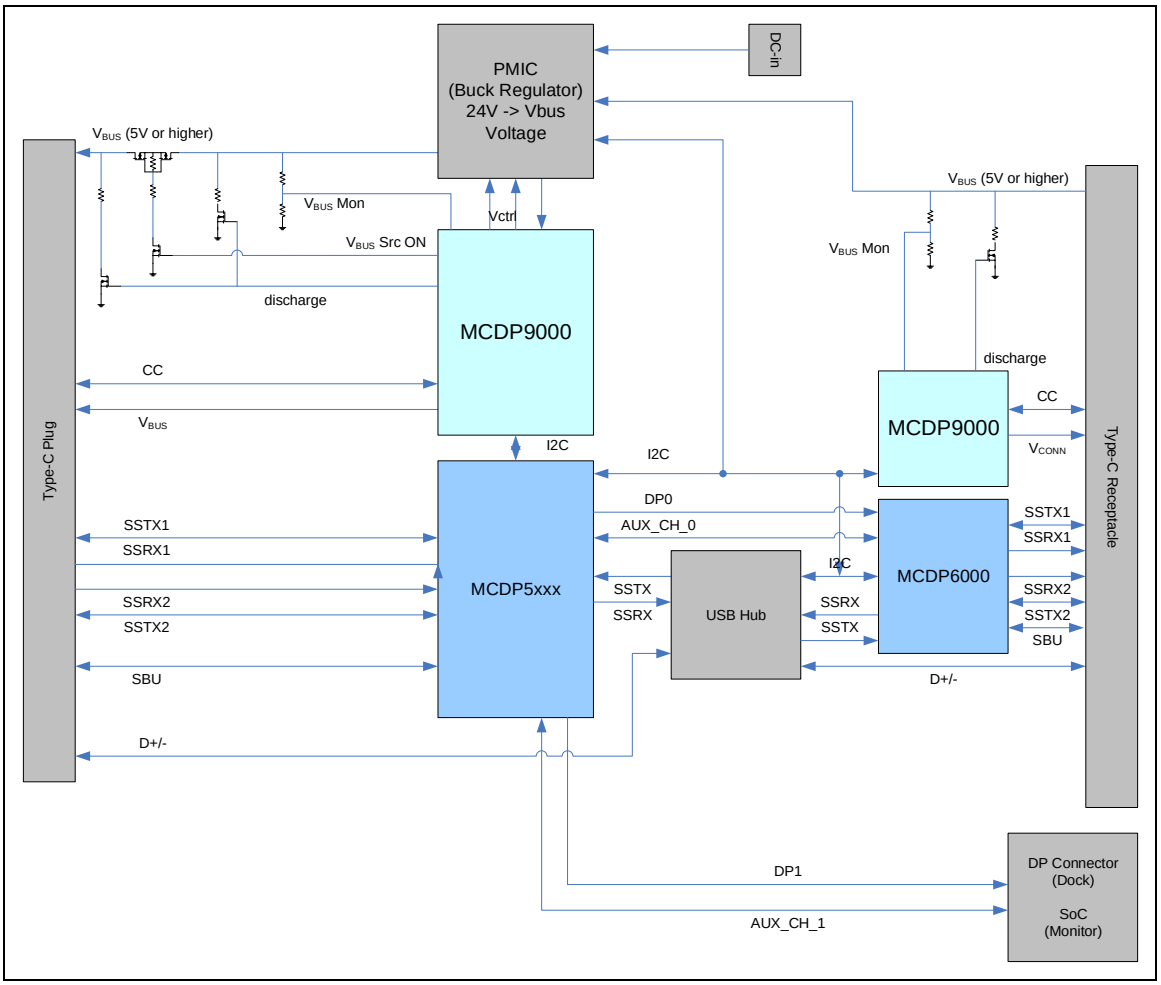
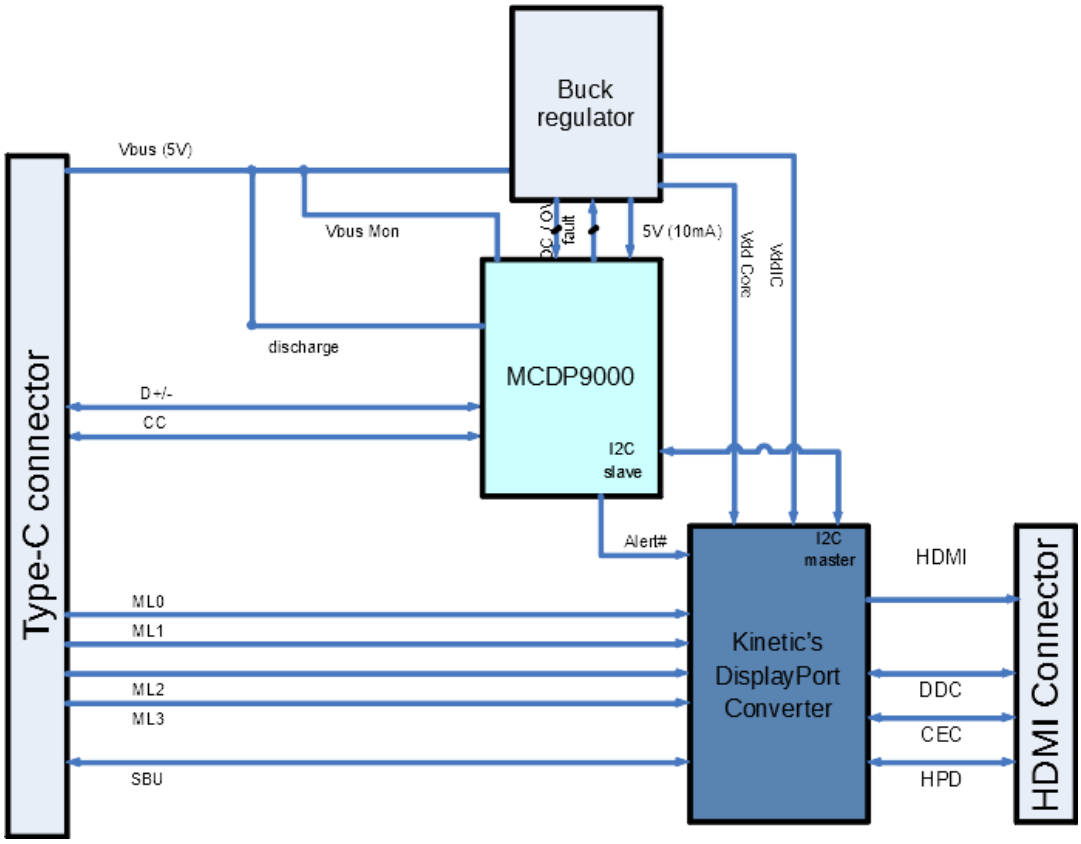


Figure 3 shows a typical use case of the MCDP9000 with a Kinetics’ DisplayPort converter product in an AV adapter. The AV adapter is going to use V_{BUS} line for its own power supply. 5V / 3A power profile should suffice for this application. Therefore, minimum BOM will be required in this use case. Because this

application does not support a separate USB function, the billboard device class in the MCDP9000 is used. A 48MHz reference clock is required to use USB 2.0 PHY and controller IP.

Figure 3. Typical use case of the MCDP9000 together with Kinetic IC in A/V accessory



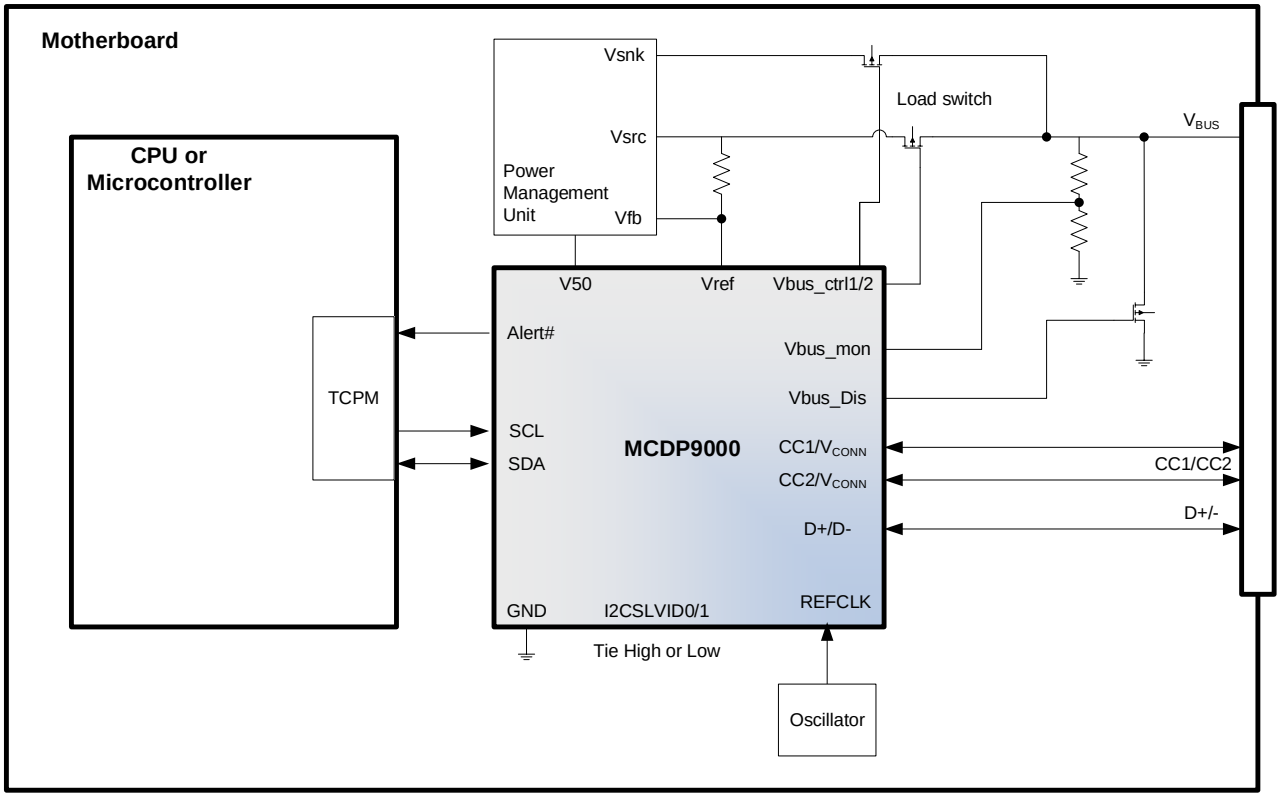
3. Functional Description

This section describes the following operations of the MCDP9000:

1. System block diagram
2. MCDP9000 block diagram
3. USB Type-C Interface (CC / V_{CONN})
4. V_{BUS} Interface
5. PMIC (Power Management IC) Interface
6. USB 2.0 FS PHY Interface
7. System interface

3.1. System Block Diagram

Figure 4. MCDP9000 System Block Diagram



3.2. MCDP9000 Block Diagram

Figure 5. MCDP9000 Block Diagram

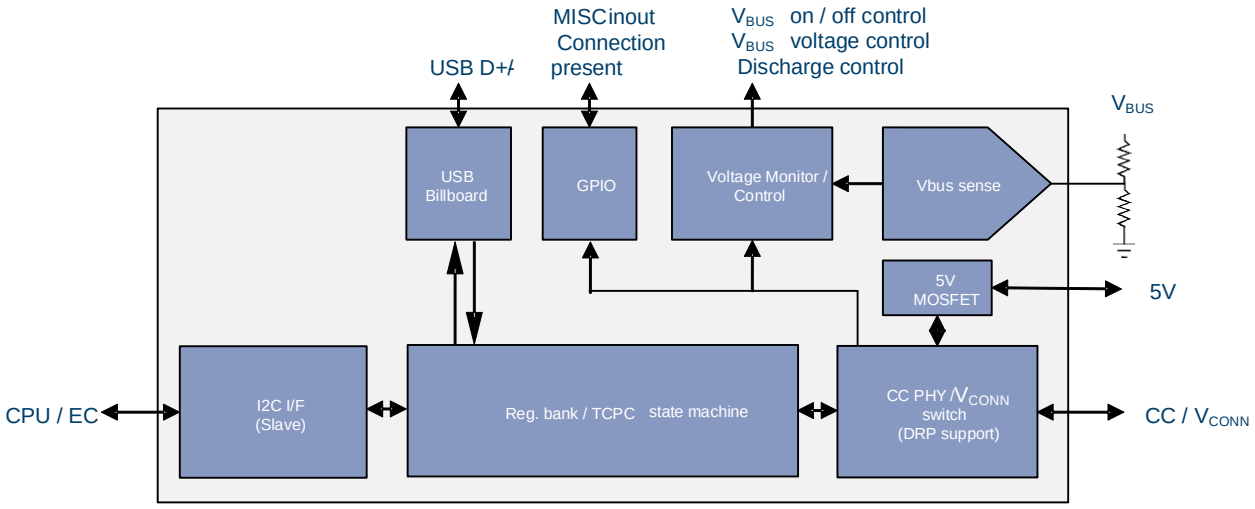


Figure 5 shows a block diagram of the MCDP9000. The MCDP9000 includes the following blocks. The details of each block are described in the following sections:

1. USB Type-C CC/V_{CONN} interface
2. V_{BUS} Monitor
3. V_{BUS} control
4. Billboard device
5. I2C slave interface
6. Reference clock interface

3.3. USB Type-C CC / V_{CONN} source Interface

CC1 and CC2 (CC) pins are used for the cable detection, plug orientation detection, PD communication and advertisement of the device capability of USB role direction and PD current rating. One of CCs is remapped to V_{CONN} pin of the plug to provide a power over it.

The MCDP9000 supports following use cases. The termination resistance on both CC1 and CC2 are programmable through the I^2C according to the use case.

Table 1. Supported PD Roles

Power Delivery Role	Source Advertisement	Rp or Rd	To 3.3V ±5% (Rp) To GND (Rd)	MCDP9000 Support
Source	Default USB Power	Rp	36k ohm ±20%	Yes
Source	1.5A @ 5V	Rp	12k ohm ±5%	Yes
Source	3A @ 5V	Rp	4.7k ohm ±5%	Yes
Sink	N/A	Rd	5.1k ohm ±10%	Yes
Self-powered sink	N/A	Rd	> 126k ohm	Yes
DRP (Dual-Role Power)	All possible source	Both	All of above	Yes

Upon the detection of the cable, the MCDP9000 detects the plug orientation. One of CC pins will be reassigned as V_{CONN} pin according to the advertisement at the plug connector. When the MCDP9000 operates in PD source system, it starts sourcing V_{CONN}. The MCDP9000 limits the maximum current drawn by the sink device. V_{CONN} function capability is described in Table 2.

Table 2. V_{CONN} Source Capability

V_{CONN} Support Capability	Voltage	Power	Current rating	V_{CONN} current limit (OCP: Over-current Protection)	V_{CONN} supply detection
Source	3.0V – 5.5V	1.5W	1.5W / Voltage	Yes	Yes

V_{CONN} OCP alarm is triggered when the V_{CONN} current exceeds 350mA debounced over the range of 100ms to 500ms. If the V_{CONN} current exceeds 650mA, the short protection circuit is activated. The short circuit detection is immediate as soon as the MCDP9000 detects more than 650mA current.

3.4. V_{CONN} sink Interface

$V_{CONNSNK}$ pin should be connected to CC2 pin when the MCDP9000 is used in the USB Type-C accessory which source the power from V_{CONN}. $V_{CONNSNK}$ is used to expose Ra connected to the ground to request V_{CONN} supply from the V_{CONN} source.

3.5. V_{BUS} Monitor

The MCDP9000 integrates a 10-bit ADC (Analog to Digital Converter) to monitor V_{BUS} voltage. The MCDP9000 provides the monitored voltage through TCPC register. V_{BUS} monitor covers the range from 4V to 21.5V with 25mV resolution.

The V_{BUS} monitor pin should not be exposed to more than 5.5V to prevent it from any potential damage. The V_{BUS} voltage is expected to be divided by at least 4 by implementing a resistive voltage divider if the V_{BUS} can exceed 5.5V. It is possible to directly connect V_{BUS} line to the V_{BUS} monitor pin in a system of which the maximum V_{BUS} voltage doesn't exceed 5.5V.

The ADC value is compared with some threshold values to trigger Alert# for OVP (Over Voltage Protection). These values are configured to TCPC registers through I^2C.

3.6. V_{BUS} Control

V_{BUS} load is controlled by TCPC according to the detected role or direction from TCPM. The MCDP9000 implements following features to control the V_{BUS} load;

- Load switch control
- Discharge control
- V_{BUS} voltage control (This usage depends on a control scheme of PMIC)

3.6.1. Load switch control

When the MCDP9000 is used for DRP or source capable ports, one or two load switches are required to control the V_{BUS} line.

3.6.2. Discharge control

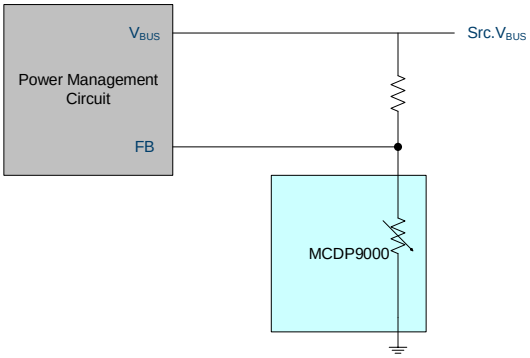
The MCDP9000 implements both V_{BUS} discharge path for 5V V_{BUS} line and discharge control for more than 5V V_{BUS} line. The V_{BUS} line, which limits the capability to source or sink only 5V, can be directly connected to the MCDP9000. Upon the cable unplug detection or direction from TCPM, the MCDP9000 turn-on the build-in switch on the discharge path.

The discharge from the V_{BUS} line, which has the capability to source or sink higher than 5V, is performed through a discharge path outside of the MCDP9000. The MCDP9000 provides the control signal to drive an external FET on the discharge path.

3.6.3. V_{BUS} Voltage control

The MCDP9000 integrates a variable resistor to control the feedback reference voltage for a buck regulator. The resistor value outside of the MCDP9000 is decided by the requirement of FB voltage from PMIC. This pin should be maintained below 5V. When the V_{BUS} voltage has to transit from 20V to 5V upon an error direction or request from TCPM, the internal resistor value has to be increased. It is possible that the higher voltage than 5V can be seen on the feedback voltage node during the transition. To avoid the MCDP9000 to be exposed to the voltage higher than 5V, the internal resistance is gradually changed to meet the V_{BUS} settle time requirement.

Figure 6. MCDP9000 V_{BUS} Voltage Control Concept



3.7. Billboard Device

3.7.1. USB 2.0 Transceiver (FS Only Support)

The MCDP9000 supports FS (Full Speed: 12Mbps) only. No external reference clock is required as precise 48MHz clock is generated internally.

3.7.2. USB Billboard Device Class

The Billboard device exposes the following descriptors structure to the USB host:

- Device Descriptor
- Configuration Descriptor
  - Interface Descriptor
- BOS Descriptor
  - Container ID Descriptor
  - Billboard Descriptor
  - Alternate Mode #1 Descriptor
  - Alternate Mode #2 Descriptor
- String Descriptor (language list)
- String Descriptor (Manufacturer)
- String Descriptor (Product)
- String Descriptor (Serial Number)
- String Descriptor (Support URL)
- String Descriptor (Alternate Mode #1)
- String Descriptor (Alternate Mode #2)

The number of alternate mode support can be selected from 1 or 2. The maximum number of languages to be supported is two. Configurable fields in the billboard device class can be accessed through I^2C register access.

3.8. I²C Interface

The I²C slave interface is intended for an external host controller to configure the MCDP9000 registers for certain use cases. I²C is accessible in any operating mode.

3.8.1. I²C Device ID

The I²C interface of the MCDP9000 operates as the slave.

Table 3. I²C Device ID Configuration

Slave ID
0x53

3.8.2. I²C Interface Timing

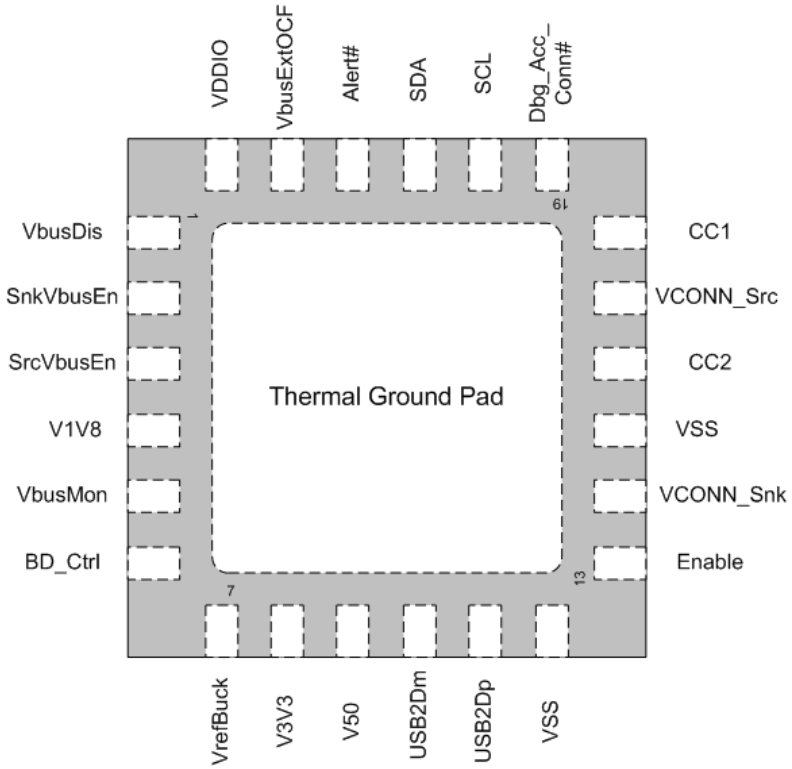
Table 4. I²C Interface timing

Symbol	Parameter	Min	Max	Unit
F_{SCL}	SCL Clock Frequency	400	1000	KHz
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		50[2]	ns
t_{LOW}	LOW period of the SCL clock	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	0.26	-	µs
$t_{hd: DAT}$	Data hold time	0	-	µs
$t_{SU :DAT}$	Data se t-up time	50	-	ns
t_R	Rise time of both SDA and SCL signals	-	120	ns
t_F	Fall time of both SDA and SCL signals	20x (VDD /5.5)[1]	120	ns
t_{BUF}	Bus free time between a STOP and START condition	0.5	-	µs
C_B	Capacitance load for each bus line [3]	-	550	pF
$t_{VD: DAT}$[4]	Data valid time	-	0.45	µs
$t_{VD: ACK}$ [5]	Data valid acknowledge time	-	0.45	µs
t_{I2C_SBR} (1000KHZ)	Time for I²C SINGLE BYTER EAD	-	50	µs
t_{I2C_SBW} (1000KHZ)	Time for I²C SINGLE BYTE WRITE	-	40	µs
T_{I2C_MBR} (1000KHZ)	Time for I²C Multi BYTE READ	-	50 + 12/byte[7]	µs
T_{I2C_MBW} (1000KHZ)	Time for I²C Multi BYTE WRITE		40+12/byte [7]	µs
t_{I2C_SBR} (400KHZ)[6]	Time for I²C SINGLE BYTE READ	-	110	µs
t_{I2C_SBW} (400KHZ)[6]	Time for I²C SINGLE BYTE WRITE	-	85	µs
t_{I2C_MBR} (400KHZ)[6]	Time for I²C Multi BYTE READ	-	100+35/byte[7]	µs
t_{I2C_MBW} (400KHZ)[6]	Time for I²C Multi BYTE WRITE		85+30/byte [7]	µs

1. Necessary to be backwards compatible with Fast-mode.
2. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
3. The maximum capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.
4. Time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. Time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
6. The TCPC should only run at 400KHz Fscl when the TCPM is servicing only one TCPC.
7. The TCPM may disable clock stretching by setting TCPC_CONTROL.I2CclockStretchingControl to 00b. The TCPC is not allowed to Nak I2C transfers no matter which clock stretching setting is chosen by the TCPM, unless the TCPM has put it to sleep using COMMAND.I2Cidle or the TCPM writes to a register/bit that is not implemented/reserved.

4. Pin Description

Figure 7. MCDP9000 Pin Assignment (Top-View)



I/O Legend:

I = Input; O = Output; P = Power, G = Ground; IO = Bi-direction

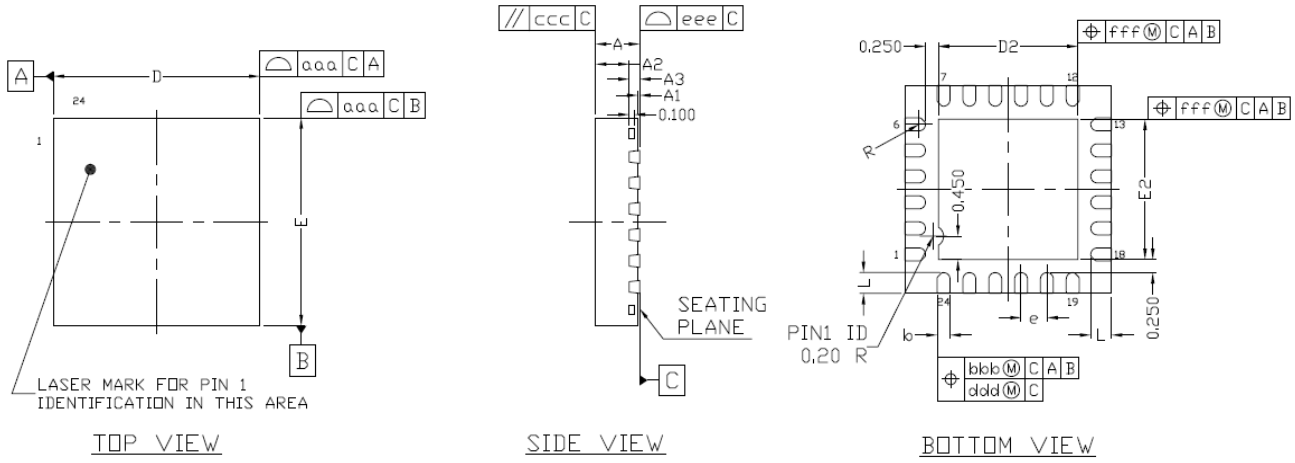
Table 5. Pin Description

Pin	Assignment	I/O	Description
1	VbusDis	Output	V_{BUS} discharge (either 5V discharge or HV discharge control)
2	SnkVbusEn	Output	V_{BUS} sink path enable
3	SrcVbusEn	Output	V_{BUS} source path enable
4	V1V8	Power	Core Power Supply Capacitor
5	VbusMon	Input	V_{BUS} monitor pin
6	BD_Ctrl	Output	V_{BUS} Bleed Discharge enable
7	VrefBuck	Input	FB voltage for a buck regulator
8	V3V3	Power	Analog Power Supply Capacitor
9	V50	Power	5V power supply
10	USB2Dm	Inout	USB 2.0 D- pin
11	USB2Dp	In/Out	USB 2.0 D+ pin
12	VSS	Ground	Ground
13	Enable	Input	Enable pin
14	VCONN_Snk	Input	Ra termination
15	VSS	Ground	Ground
16	CC2	Inout	CC2 pin of USB Type-C
17	VCONN_Src	Power	V_{CONN} as provider
18	CC1	Inout	CC1 pin of USB Type-C
19	Dbg_Acc_Conn#	Output	Debug Accessory Indicator
20	SCL	Input	I^2C SCL (clock)
21	SDA	In/Out	I^2C SDA (data)
22	Alert#	Output	Alert# for interrupt signal to TCPM
23	VbusExtOCF	Input	V_{BUS} Over-Current Indicator
24	VDDIO	Power	IO Power Supply
NA	Thermal Ground Pad	Ground	Solder the exposed pad to the ground.

5. Package Specification

5.1. Package Drawing and Dimensions

Figure 8 MCDP9000 Package Outline Drawing (unit: mm)



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.900	---	---	0.035
A1	0.000	---	0.050	0.000	---	0.002
A2	---	0.650	0.700	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.180	0.250	0.300	0.007	0.010	0.012
D	4 BSC			0.157 BSC		
D2	2.600	2.700	2.800	0.102	0.106	0.110
E	4 BSC			0.157 BSC		
E2	2.600	2.700	2.800	0.102	0.106	0.110
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.500 BSC			0.020 BSC		
R	0.090	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.150			0.006		
bbb	0.100			0.004		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

6. Marking Field Template and Descriptors

Figure 9. MCDP9000 Marking Template

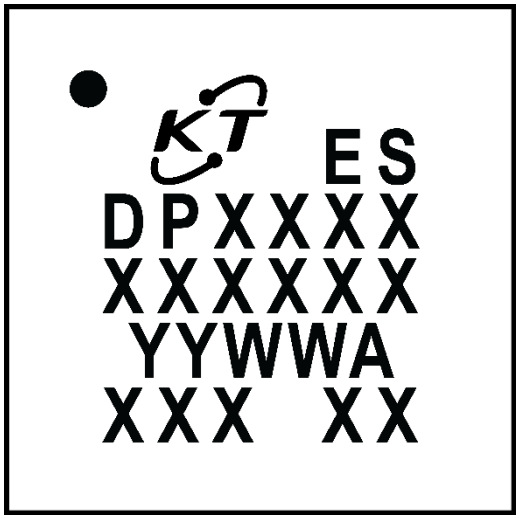


Table 6. Field Descriptors

Line	Description	Marking
1	Pin 1 Dot	Dot
2	Logo	Logo
2	ES = Engineering Sample (Optional Marking)	ES
3	Part Number (without MC)	DP9000
4	Last 6 Digits from Mother Lot Number	XXXXXX
5	YYWW = Date Code, A = Kinetic Assigned	YYWWA
6	XXX = Running Number, XX = Wafer Revision	XXX XX

7. Electrical Specifications

7.1. Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Specifications	Unit	Min	Typ	Max	Comments
1.8 V supply voltage	V	-0.3	-	2.5	
3.3 V supply voltage	V	-0.3	-	4.6	
5 V supply voltage	V	-0.5	-	6.0	
V_{CONN} supply voltage	V	-0.5	-	6.0	
ESD Rating	V		±2000		HBM
ESD Rating	V		±500		CDM
Storage temperature	°C	-55	-	125	

7.2. Recommended Operating Conditions

Table 8. Device Operating Conditions

Parameter	Description	Units	Min	Typ	Max	Note
V50	Device Power Supply	V	3.0[1]	5	5.5	
VCONN	Operating Voltage – VCONN	V	4.85		5.5	
	eFuse Programming voltage	V	5.5	6	6.5	
V1V8	Core power supply voltage	V	1.62	1.8	1.98	
V3V3	Analog power supply voltage	V	3.135	3.3	3.465	
VDDIO	Digital IO power supply voltage	V	1.62		3.6	
TA	Ambient Temperature Range	°C	-10		85	
TJ	Junction Temperature Range	°C	-40		125	Design Temperature Range
V1V8 COUT	Output Capacitor for 1V8	nF		100		
V3V3 COUT	Output Capacitor for 3V3	µF		10		
CIN	V50 Input Capacitor	µF		2.2		
V1V8 Load Current	Output Current	mA	4			
VCC UVL	Under Voltage Lockout	V	2.5		2.7	UVLO Threshold
		mV	150			UVLO Hysteresis
ICONN	Operation Current	mA	0		300	
ICONN_OCP	VCONN over current capability	mA	350		560	Debounced over t_{OCP}
tOCP	Over current detection time	ms	100		500	
ICONN_SCP	VCONN short circuit current capability	mA	650		950	
tSCP	Short Circuit detection time	µs	0		1.5	
ICC	Current Consumption Not including the Type-C PullUp (Rp) current.	µA		80		Port Sleep and DRP looking for connection, I2C in idle mode
		mA		0.8		Port Active, PD in Receiver mode and VBUS monitoring disabled
		mA		0.95		Port Active, PD in Receiver mode
		mA		2.5		Port Active, PD in Transmit Mode
		mA		9		Port Active, PD in Transmit Mode, USB Billboard is active
		µA			5	From VCC: Port Disabled
I2C Freq	I2C Frequency	MHz	0.1		1	Support for Standard Mode, Fast Mode and Fast Mode+

1. Minimum VDD is 3.0V for functional mode only in case of VCONN sink device. All the electrical parameters are defined for a minimum VDD of 4.5V

7.3. CC Pull-up Resistance (Rp)

Table 9. CC Pull-up Resistance Characteristics

Description	Units	Min	Typ	Max	Note
Reference VDD	V	3.135	3.3	3.465	
Default USB Power - res	kΩ	28.8	36	43.2	
1.5A@5V - res	kΩ	11.4	12	12.6	
3.0A@5V - res	kΩ	4.465	4.7	4.935	
High-Z pull up	MΩ	1.0			

7.4. Pull-down Resistance (Rd)

Table 10. CC Pull-down Resistance Characteristics

Description	Units	Min	Typ	Max	Note
Pull-down Resistance after trimming	kΩ	4.59	5.1	5.61	
High-Z pull down	MΩ	1			
Dead Battery voltage clamp, RP@default	V	0.25		1.375	
Dead Battery voltage clamp, RP@1.5A	V	0.45		1.375	
Dead Battery voltage clamp, RP@3A	V	0.85		2.2	

7.5. Powered Cable Termination Resistance (Ra)

Table 11. Powered Cable Pull-down Resistance Characteristics

Description	Units	Min	Typ	Max	Note
Pull-down Resistance	Ω	800		1200	

7.6. V_{BUS} Monitor

Table 12. V_{BUS} Monitor Characteristics

Description	Units	Min	Typ	Max	Note
Number of conversion bit	bit		10		
Conversion duration	µs			80	
Measurement time	ms			2.56	Data average over 32 conversion
VBUS voltage measurement value - LSB	mV		25		
VBUS voltage measurement accuracy	%	-2		+2	VBUS>2.5V
VBUS voltage measurement accuracy	mV	-50		50	VBUS≤2.5V
VFS	V		2.56		External Resistor Ratio of 10
ADC measurement accuracy1	%	-1		+1	0.25V<VIN≤VFS
	LSB	-1		+1	0.125<VIN≤0.25V
	LSB	-1.5		+1.5	0≤VIN≤0.125V
DNL	LSB	-1		+1	

7.7. V_{BUS} Detection Comparator

Table 13. V_{BUS} Detection Comparator Characteristics

Description	Units	Min	Max	Note
VBUS_comp input	V	0	2.15	Max VBUS functional voltage is 21.5V
Comparator - Offset @0.375V Threshold voltage	mV		10	
Comparator - Rise propagation delay @ 150mV overdrive	µs		100	
Comparator - Fall propagation delay @ 150mV overdrive	µs		100	

7.8. V_{CONN} Switch

Table 14. V_{CONN} Switch Characteristics

Description	Units	Min	Max	Note
VCONN Input Supply	V	4.85	5.5	
VCONN Output Power Capabilities	W	1.5		
VCONN Output Voltage on CCx	V	4.75	5.5	For active cables
VCONN Output Voltage on CCx	V	3.0	5.5	For VCONN powered accessory
VCONN Switch Ron	mΩ		240	
IOCP threshold	mA	350	560	
tOCP	ms	100	500	Debounce detection time
ISCP threshold	mA	650	950	
tSCP	µs	0		Debounce detection time without filtering
In-rush peak current	mA		500	The maximum VCONN load cap is 10µF.

7.9. Resistive DAC (Buck Feedback)

Table 15. Resistive DAC Characteristics

Description	Units	Min	Max	Note
Maximum voltage on the Resistor	V		5.5	
Number of bits of the DAC	N		7	
Resistor min value [code 0]	Ω	518	800	
Resistor max value [code 127]	Ω	16313	24450	
Resistor Step	Ω	116	190.1	

7.10. USB PD Transmitter

Table 16. USB PD Transmitter Characteristics

Description	Units	Min	Typ	Max	Note
Bit rate	kbps	270	300	330	
Maximum difference between the bit-rate	%			0.25	
Fast Role Swap request transmit driver resistance	ohm			5	
Time to cease driving the line after the end of the last bit of the Frame	µs			23	
Time to cease driving the line after the final high-to-low transition	µs	1			
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble	µs	25			
Fast Role Swap request transmit duration	µs	60		120	
Time before the start of the first bit of the Preamble	µs	-1		1	
Vswing (TX Hi level – TX Lo level) – Peak	V	1.05		1.2	
Transmitter Rise Time	ns	300		600	
Transmitter Fall Time	ns	300		600	
Transmitter output impedance	ohm	33		75	

7.11. USB PD Receiver

Table 17. USB PD Receiver Characteristics

Description	Units	Min	Typ	Max	Note
Bit rate	kbps	270	300	330	
CC receiver capacitance	pF	200		600	
Bit error rate			10E-6		S/N = 25dB
Transitions for signal detect		3		3.6	
Fast Role Swap request detection time	µs	30		50	
RX bandwidth limiting filter	ns	100			
Time window for detecting no-idle	µs	12		20	
Fast Role Swap request voltage detection threshold	mV	490	520	550	
Noise immunity when BMC is active	mV			165	Peak-to-peak noise from V_{BUS}, USB2 and SBU line after the Rx bandwidth limiting filter with the time constant has been applied.
Noise immunity when BMC is idle	mV			300	Peak-to-peak noise from V_{BUS}, USB2 and SBU line after the Rx bandwidth limiting filter with the time constant has been applied.
Input Impedance	MΩ	1			
Filter – High Pass Frequency @-3dB	kHz	30			
Filter – Low Pass Frequency @-3dB	MHz			1.59	

7.12. USB 2.0 Transceiver (Full-Speed Mode Only)

Table 18. USB 2.0 FS Transceiver Characteristics

Description	Units	Min	Typ	Max	Note
VDI - Differential Input Sensitivity	mV	200			|ViDP-ViDM|
VCM - Differential Common Mode Voltage	V	0.8		2.5	Includes VDI range
VIL - LOW-level input voltage	V			0.8	
VIH - HIGH-level input voltage	V	2			
V_{HYS} - hysteresis voltage	V	0.4		0.7	
VOL - LOW-level output voltage	V			0.3	
VOH - HIGH-level output voltage	V	2.8		3.6	
Rpu - Idle - Pull up resistance	Ω	900		1575	
Rpu - Active - Pull up resistance	Ω	1425		3090	
ILZ - off-state leakage current	µA	-1		1	
Cin - input capacitance	pF			10	pin to GND (150pF max)
ZDRV - driver output impedance	Ω	28	36	44	driver output impedance
ZINP - input impedance	MΩ	1			
TFR, TFF - Rise time, Fall time of DP and DM lines	ns	4		20	For low-speed: CL=50-150pF and RL=15K only on DM. For full-speed:CL=50pF
TFRFM - differential rise time/fall time matching (TFR/TFF)	%	90		111.1	
VCRS - output signal crossover	V	1.3		2	
TPLH, TPHL - Driver propagation	ns			20	
TPHZ, TPLZ - Driver disable delay	ns			20	
TPZH, TPZL - Driver enable delay	ns			20	